

Product Summary

BV _{DSS}	R _{DSON} Max	I _D Max T _A = +25°C
60V	25mΩ @ V _{GS} = 10V	6.5A
	34mΩ @ V _{GS} = 4.5V	5.2A

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance (R_{DSON}) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

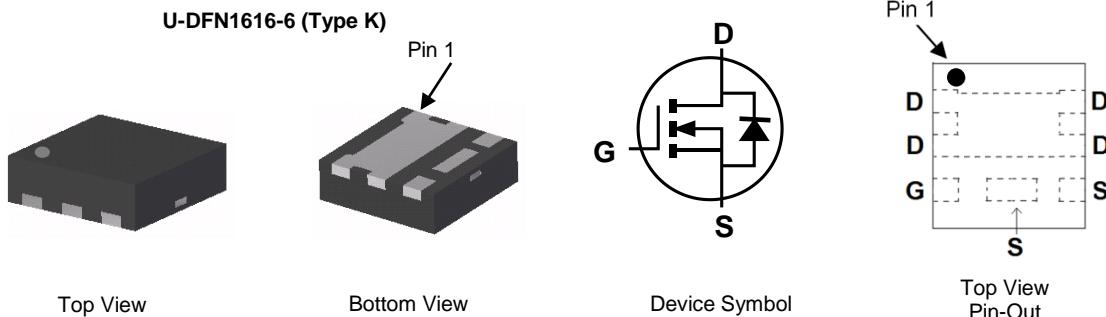
- Power Management Functions
- Load Switch

Features and Benefits

- 0.6mm Profile—Ideal for Low Profile Applications
- Low On-Resistance
- PCB Footprint of 2.56mm²
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.
<https://www.diodes.com/quality/product-definitions/>

Mechanical Data

- Case: U-DFN1616-6
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Lead Free Plating (NiPdAu Finish over Copper Leadframe). Solderable per MIL-STD-202, Method 208^(e4)
- Weight: 0.003 grams (Approximate)



Ordering Information (Note 4)

Part Number	Case	Packaging
DMT6030LFCL-7	U-DFN1616-6 (Type K)	3,000/Tape & Reel

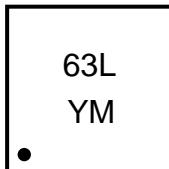
Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

Site 1:

U-DFN1616-6 (Type K)



63L = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: H = 2020)
 M = Month (ex: 9 = September)

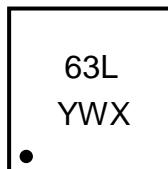
Date Code Key

Year	2017	...	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	E	...	H	I	J	K	L	M	N	O	P	R

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Site 2:

U-DFN1616-6 (Type K)



63L = Product Type Marking Code
 YWX = Date Code Marking
 Y = Year (ex: 0 = 2020)
 W = Week (ex: a = Week 27; z Represents Week 52 and 53)
 X = Internal Code (ex: U = Monday)

Date Code Key

Year	2017	...	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	7	...	0	1	2	3	4	5	6	7	8	9

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	I_D	6.5	A
		$T_A = +70^\circ\text{C}$		5.2	
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)			I_{DM}	30	A
Maximum Body Diode Continuous Current (Note 6)			I_S	1.7	A
Pulsed Body Diode Forward Current (10 μs Pulse, Duty Cycle = 1%)			I_{SM}	30	A

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	0.78	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	160	$^\circ\text{C}/\text{W}$
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	1.58	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	79	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	16.7	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	1	—	2.5	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	19	25	$\text{m}\Omega$	$V_{GS} = 10\text{V}, I_D = 6.5\text{A}$
		—	25	34		$V_{GS} = 4.5\text{V}, I_D = 4\text{A}$
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	639	—	pF	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{oss}	—	166	—		
Reverse Transfer Capacitance	C_{rss}	—	13.1	—		
Gate Resistance	R_g	—	1.4	—		
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	9.1	—	nC	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	4.5	—		
Gate-Source Charge	Q_{gs}	—	1.2	—		
Gate-Drain Charge	Q_{gd}	—	2.0	—		
Turn-On Delay Time	$t_{D(ON)}$	—	2.6	—	ns	$V_{GS} = 10\text{V}, V_{DD} = 30\text{V}, R_g = 6\Omega, I_D = 10\text{A}$
Turn-On Rise Time	t_R	—	2.2	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	10.7	—		
Turn-Off Fall Time	t_F	—	3.4	—		
Body Diode Reverse Recovery Time	t_{RR}	—	26.5	—	ns	$I_F = 10\text{A}, dI/dt = 100\text{A}/\mu\text{s}$
Body Diode Reverse Recovery Charge	Q_{RR}	—	12.3	—		

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

7. Short duration pulse test used to minimize self-heating effect.

8. Guaranteed by design. Not subject to product testing.

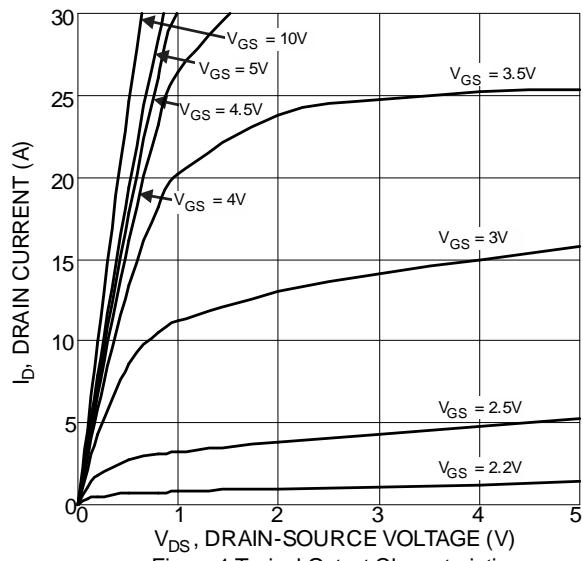


Figure 1 Typical Output Characteristic

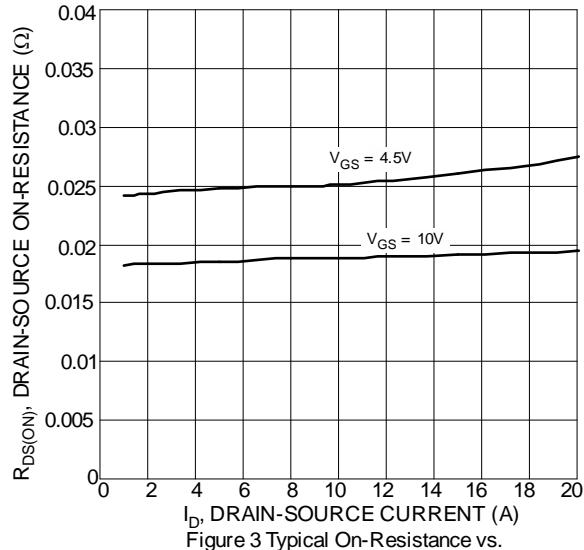


Figure 3 Typical On-Resistance vs.
Drain Current and Gate Voltage

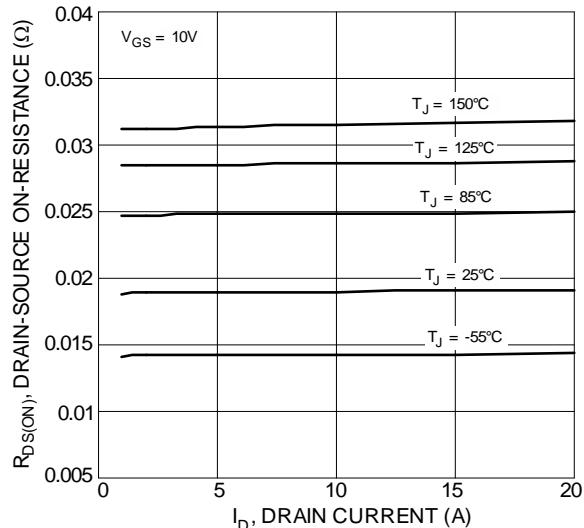


Figure 5 Typical On-Resistance vs.
Drain Current and Temperature

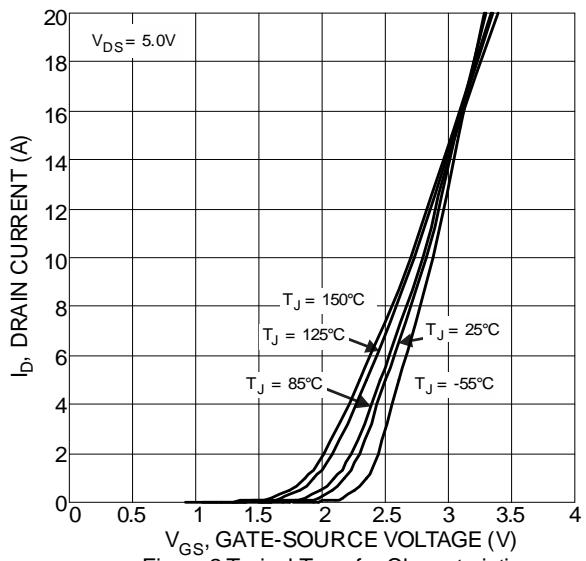


Figure 2 Typical Transfer Characteristics

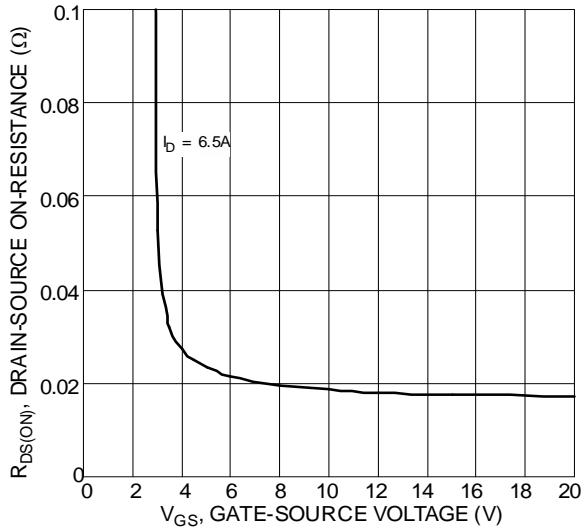


Figure 4 Typical Drain-Source On-Resistance
vs. Gate-Source Voltage

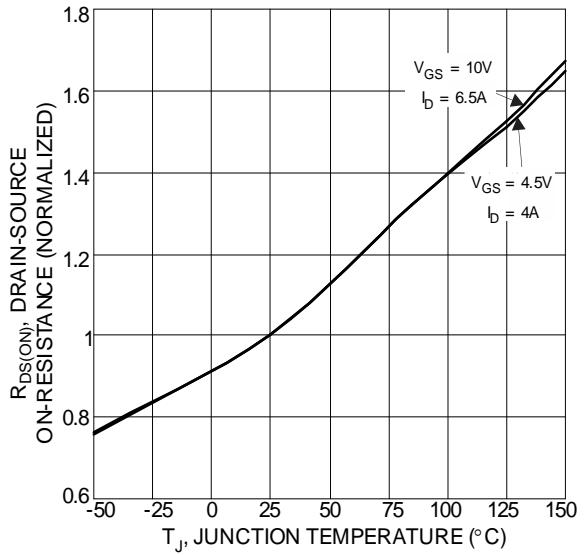


Figure 6 On-Resistance Variation with Temperature

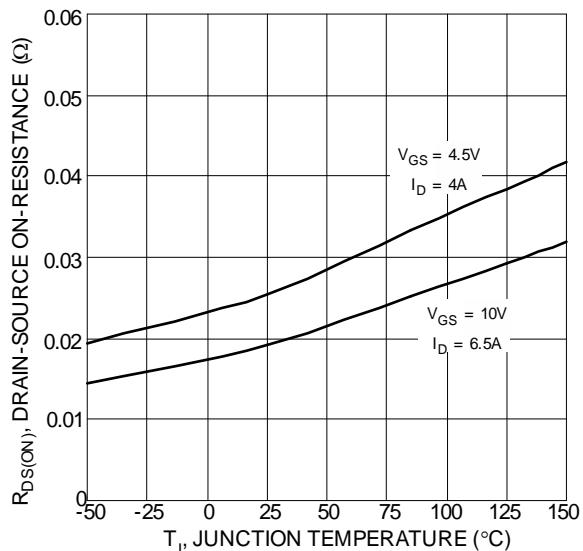


Figure 7 On-Resistance Variation with Temperature

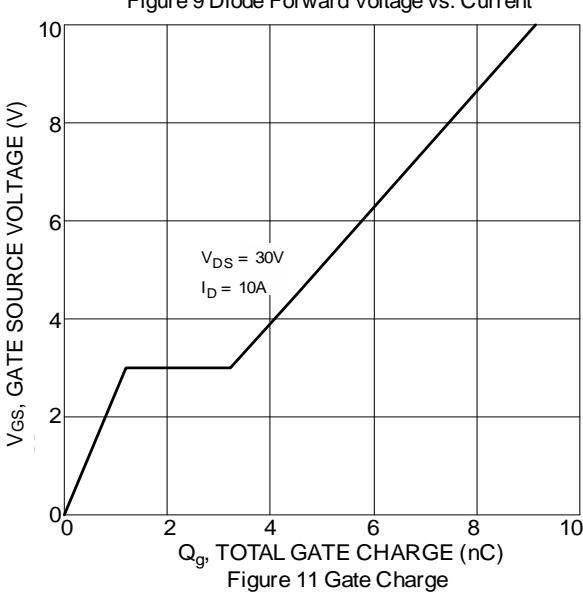
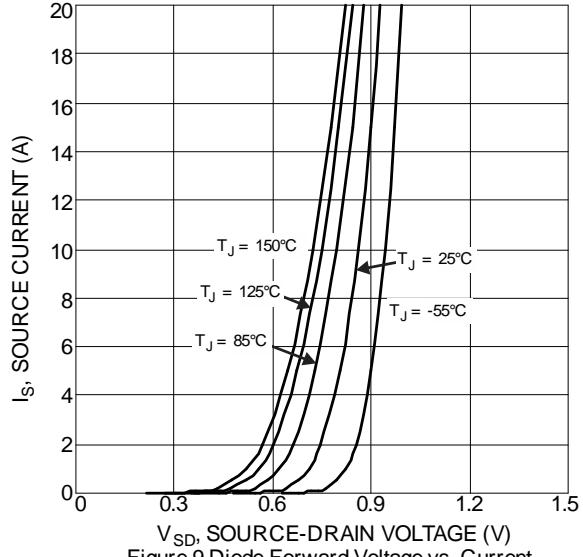


Figure 11 Gate Charge

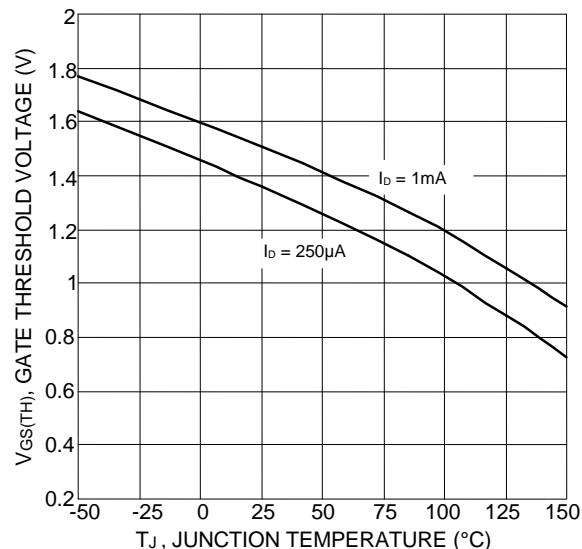


Figure 8 Gate Threshold Variation vs. Junction Temperature

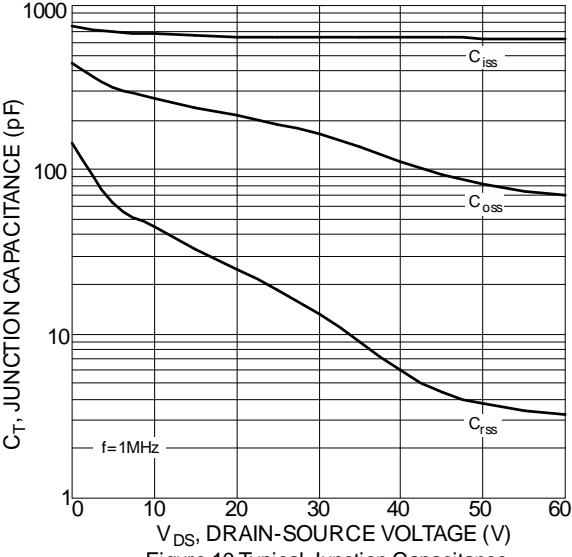


Figure 10 Typical Junction Capacitance

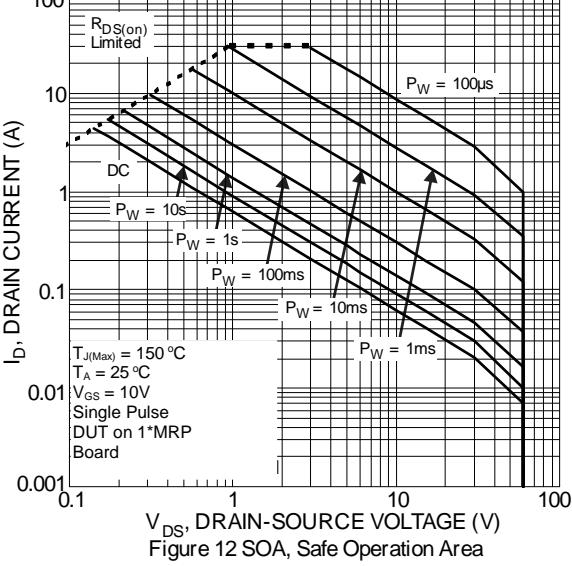


Figure 12 SOA, Safe Operation Area

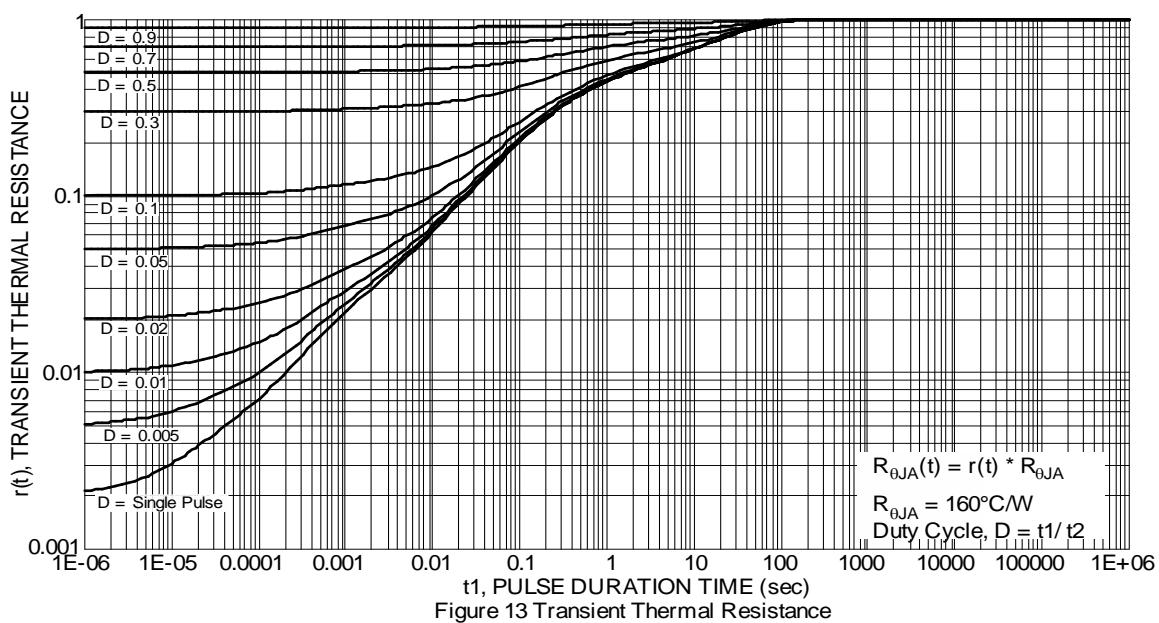
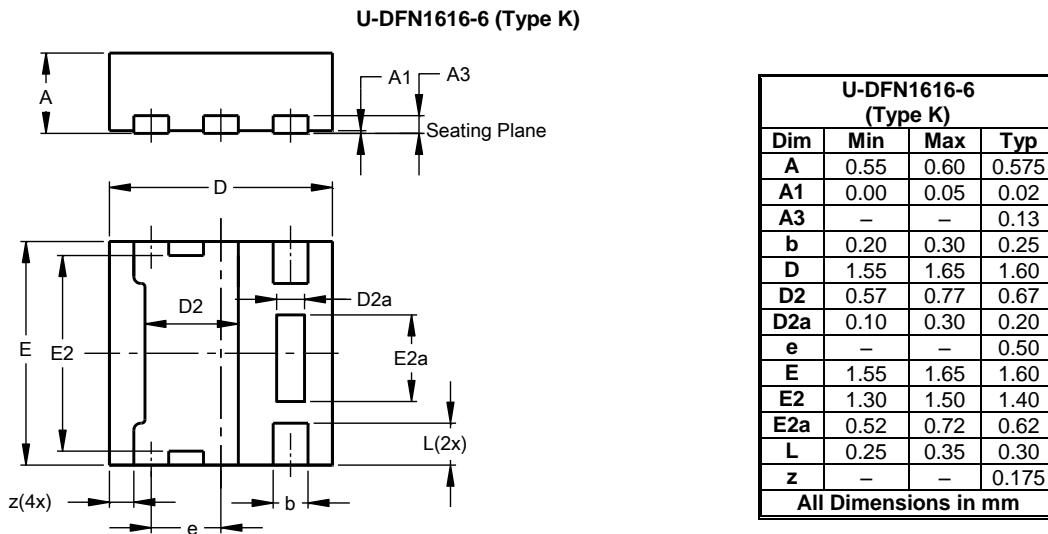


Figure 13 Transient Thermal Resistance

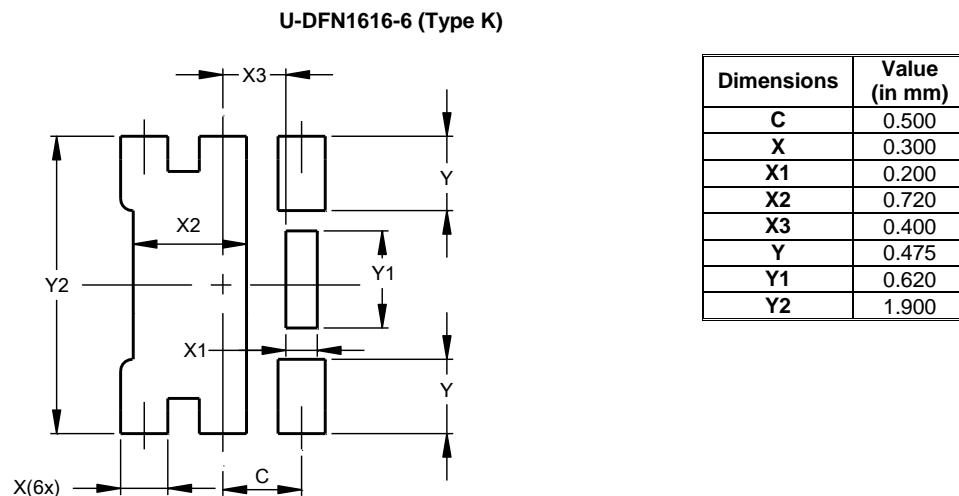
Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



Suggested Pad Layout

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