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April 2014

FQD17P06 / FQU17P06

P-Channel QFET® MOSFET

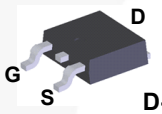
-60 V, -12 A, 135 mΩ

Description

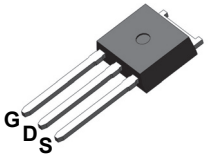
This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

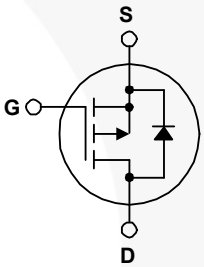
- -12 A, -60 V, $R_{DS(on)}$ = 135 mΩ (Max.) @ V_{GS} = -10 V, I_D = -6 A
- Low Gate Charge (Typ. 21 nC)
- Low Crss (Typ. 80 pF)
- 100% Avalanche Tested



D-PAK



I-PAK



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted.

Symbol	Parameter			FQD17P06 / FQU17P06	Unit
V_{DSS}	Drain-Source Voltage			-60	V
I_D	Drain Current	- Continuous (T_C = 25°C)		-12	A
		- Continuous (T_C = 100°C)		-7.6	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	-48	A
V_{GSS}	Gate-Source Voltage			± 25	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	300	mJ
I_{AR}	Avalanche Current		(Note 1)	-12	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	-7.0	V/ns
P_D	Power Dissipation (T_A = 25°C) *			2.5	W
	Power Dissipation (T_C = 25°C)			44	W
		- Derate above 25°C		0.35	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds.			300	°C

Thermal Characteristics

Symbol	Parameter	FQD17P06 / FQU17P06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.85	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (*1 in² Pad of 2-oz Copper), Max.	50	

* When mounted on the minimum pad size recommended (PCB Mount)

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Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD17P06TM	FQD17P06	DPAK	Tape and Reel	330 mm	16 mm	2500 units
FQU17P06TU	FQU17P06	IPAK	Tube	N/A	N/A	70 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-60	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C	--	-0.06	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -60 V, V_{GS} = 0 V	--	--	-1	μA
		V_{DS} = -48 V, T_C = 125°C	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = -25 V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = 25 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -6.0 A	--	0.11	0.135	Ω
g_{FS}	Forward Transconductance	V_{DS} = -30 V, I_D = -6.0 A	--	8.7	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	--	690	900	pF
C_{oss}	Output Capacitance		--	325	420	pF
C_{rss}	Reverse Transfer Capacitance		--	80	105	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -30 V, I_D = -8.5 A, R_G = 25 Ω (Note 4)	--	13	35	ns
t_r	Turn-On Rise Time		--	100	210	ns
$t_{d(off)}$	Turn-Off Delay Time		--	22	55	ns
t_f	Turn-Off Fall Time		--	60	130	ns
Q_g	Total Gate Charge	V_{DS} = -48 V, I_D = -17 A, V_{GS} = -10 V (Note 4)	--	21	27	nC
Q_{gs}	Gate-Source Charge		--	4.2	--	nC
Q_{gd}	Gate-Drain Charge		--	10	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-12	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-48	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -12 A	--	--	-4.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -17 A, dI_F / dt = 100 A/μs	--	92	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.32	--	μC

NOTES:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 2.4 mH, I_{AS} = -12 A, V_{DD} = -25 V, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq$ -17 A, di/dt ≤ 300 A/μs, $V_{DD} \leq BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

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Typical Performance Characteristics

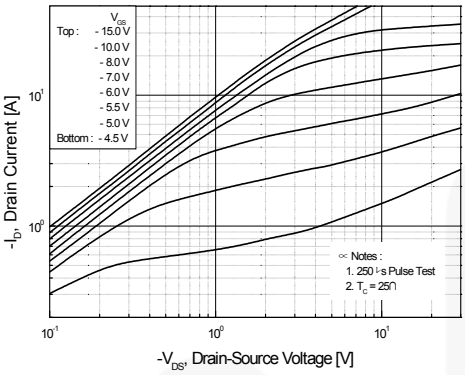

Figure 1. On-Region Characteristics

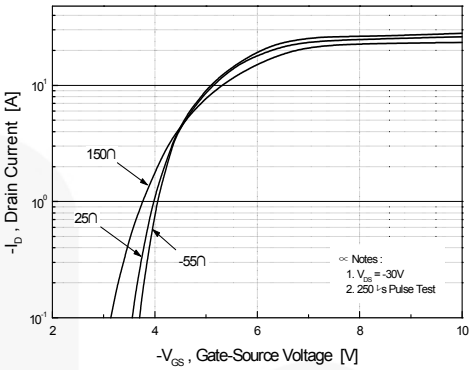

Figure 2. Transfer Characteristics

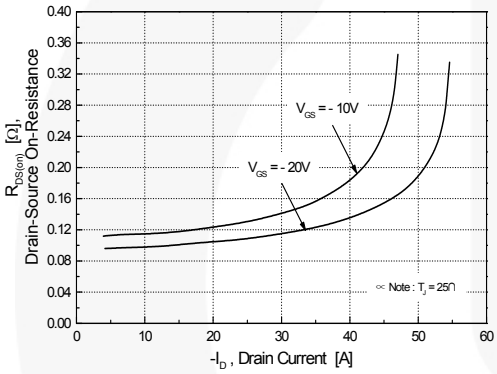

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

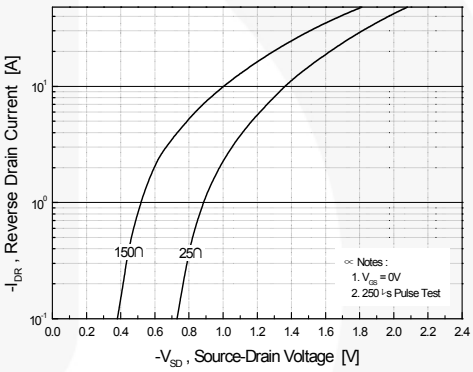

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

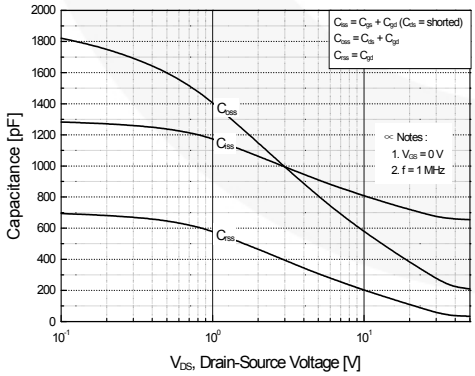

Figure 5. Capacitance Characteristics

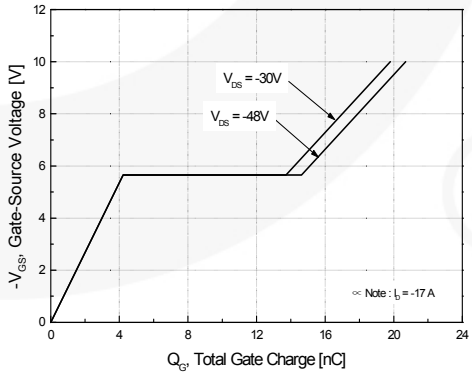

Figure 6. Gate Charge Characteristics

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Typical Performance Characteristics (Continued)

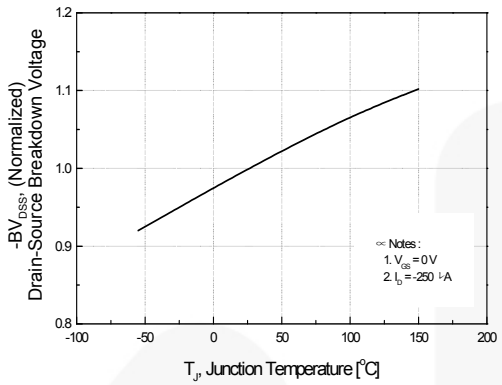

Figure 7. Breakdown Voltage Variation vs. Temperature

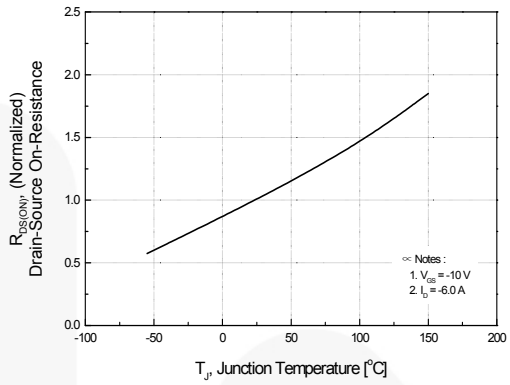

Figure 8. On-Resistance Variation vs. Temperature

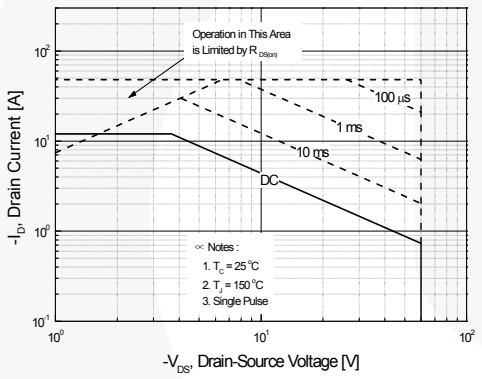

Figure 9. Maximum Safe Operating Area

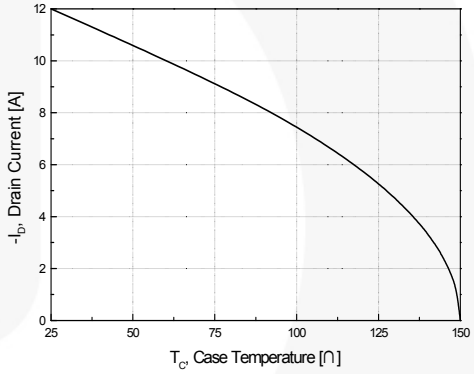

Figure 10. Maximum Drain Current vs. Case Temperature

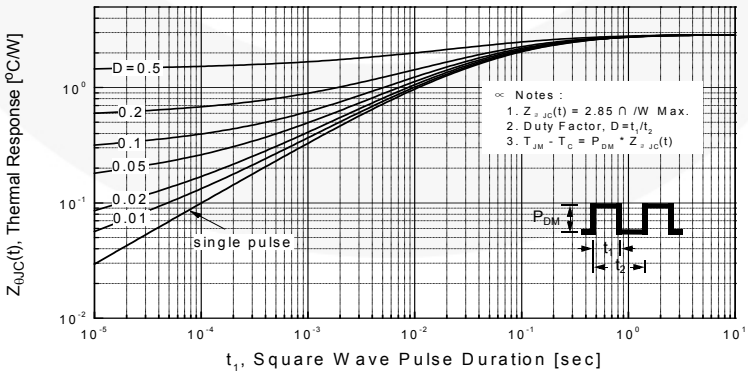

Figure 11. Transient Thermal Response Curve

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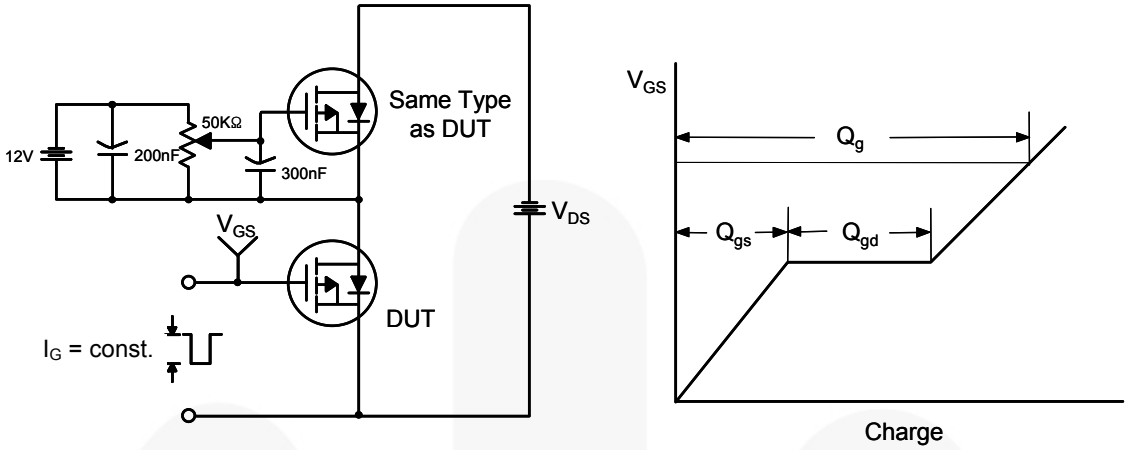

Figure 12. Gate Charge Test Circuit & Waveform

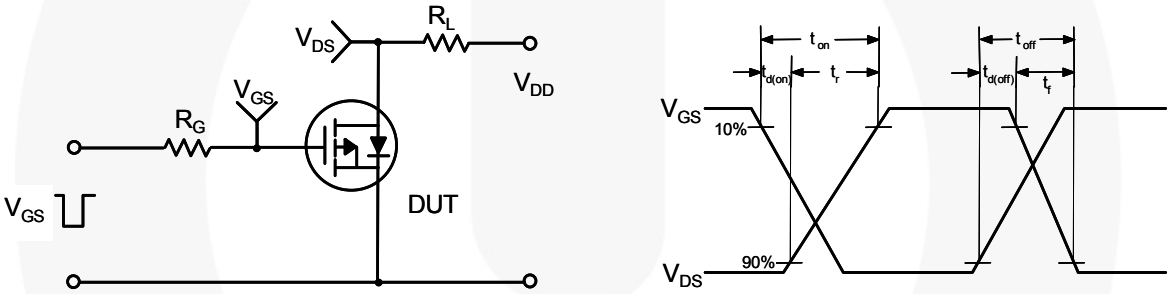

Figure 13. Resistive Switching Test Circuit & Waveforms

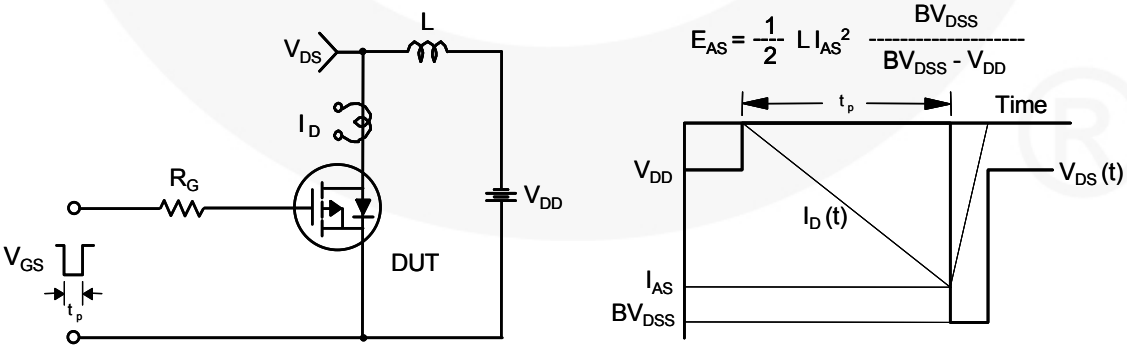

Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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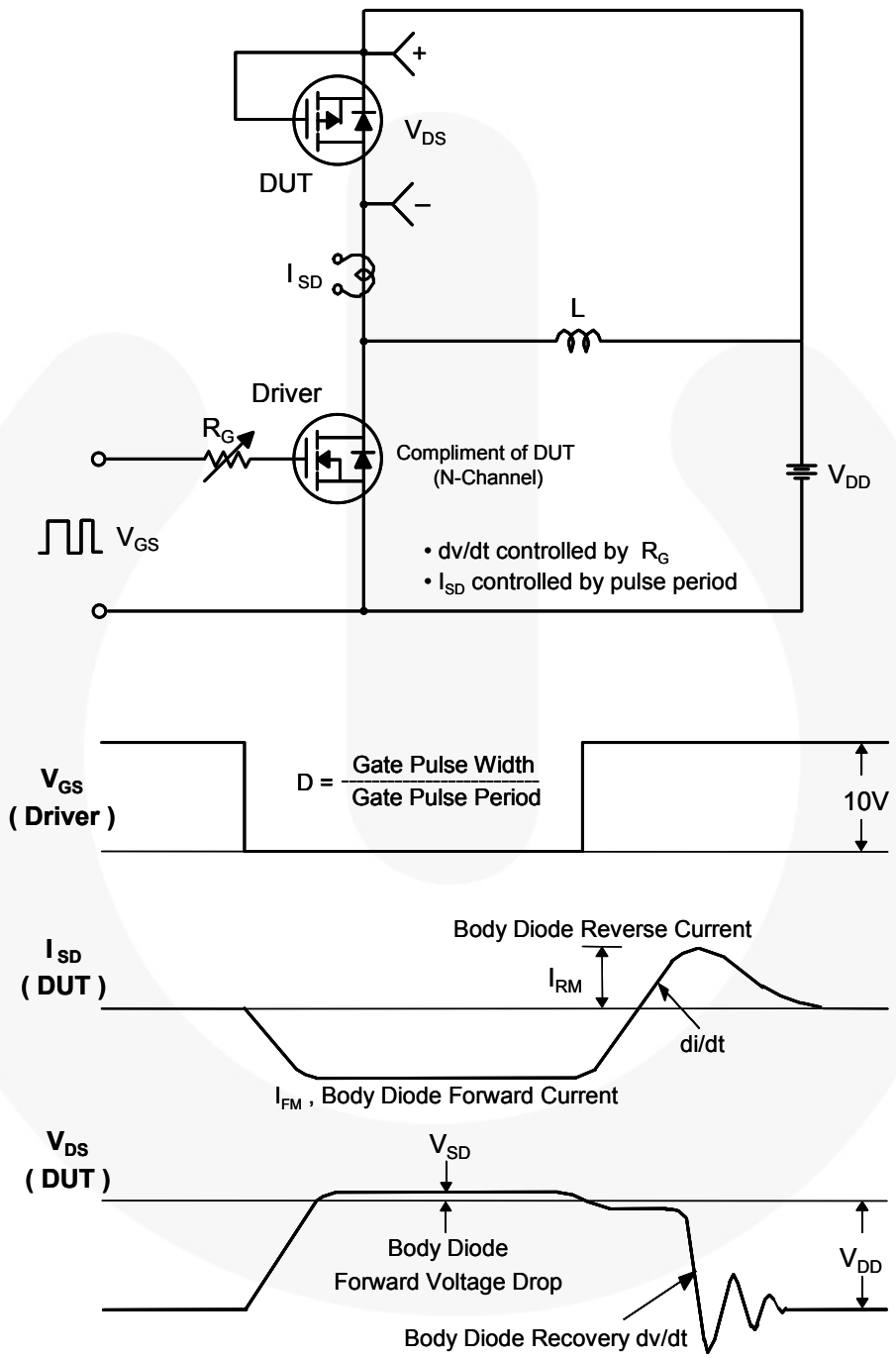

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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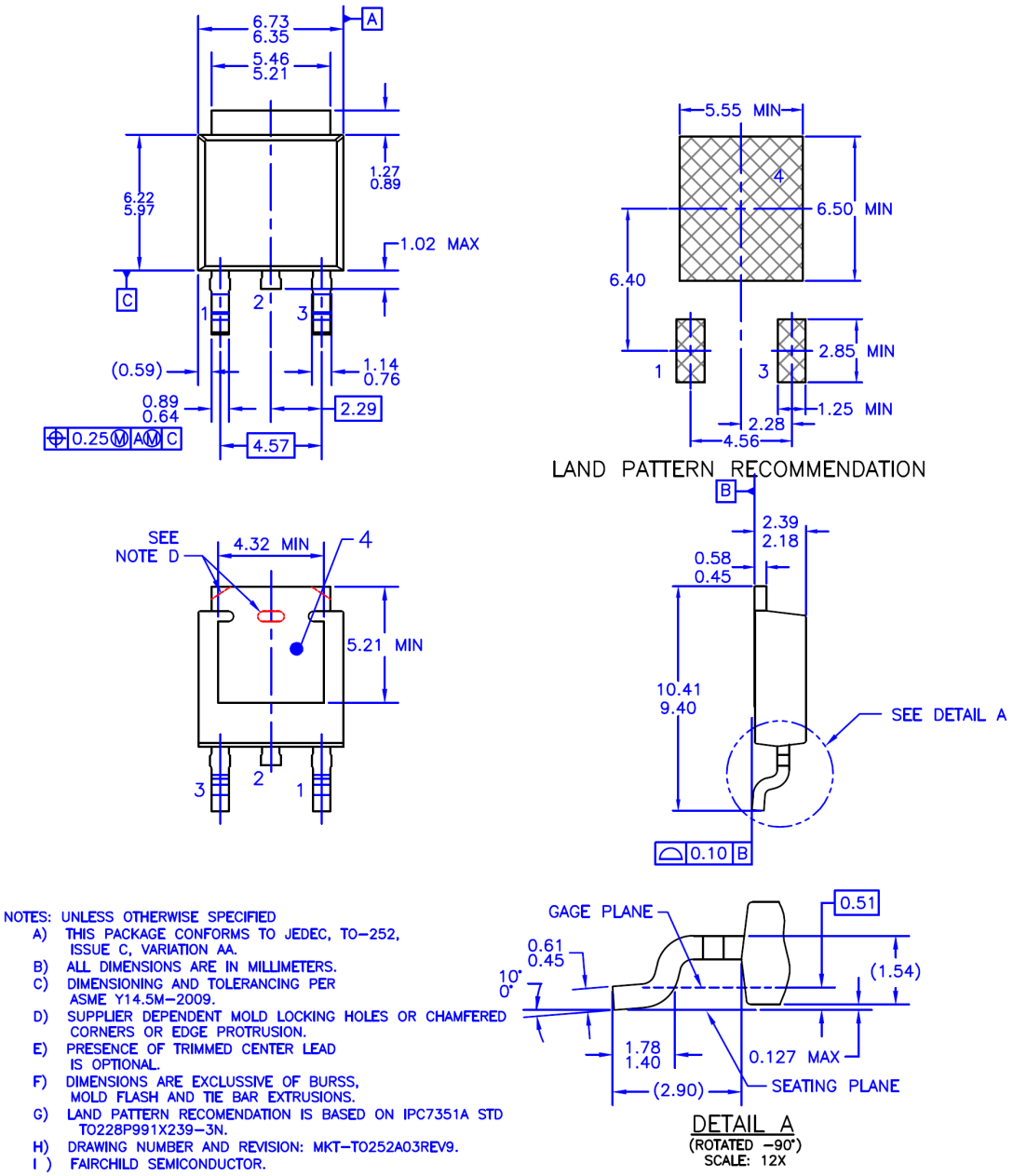

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- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
- F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239−3N.
- H) DRAWING NUMBER AND REVISION: MKT−TO252A03REV9.
- I) FAIRCHILD SEMICONDUCTOR.

Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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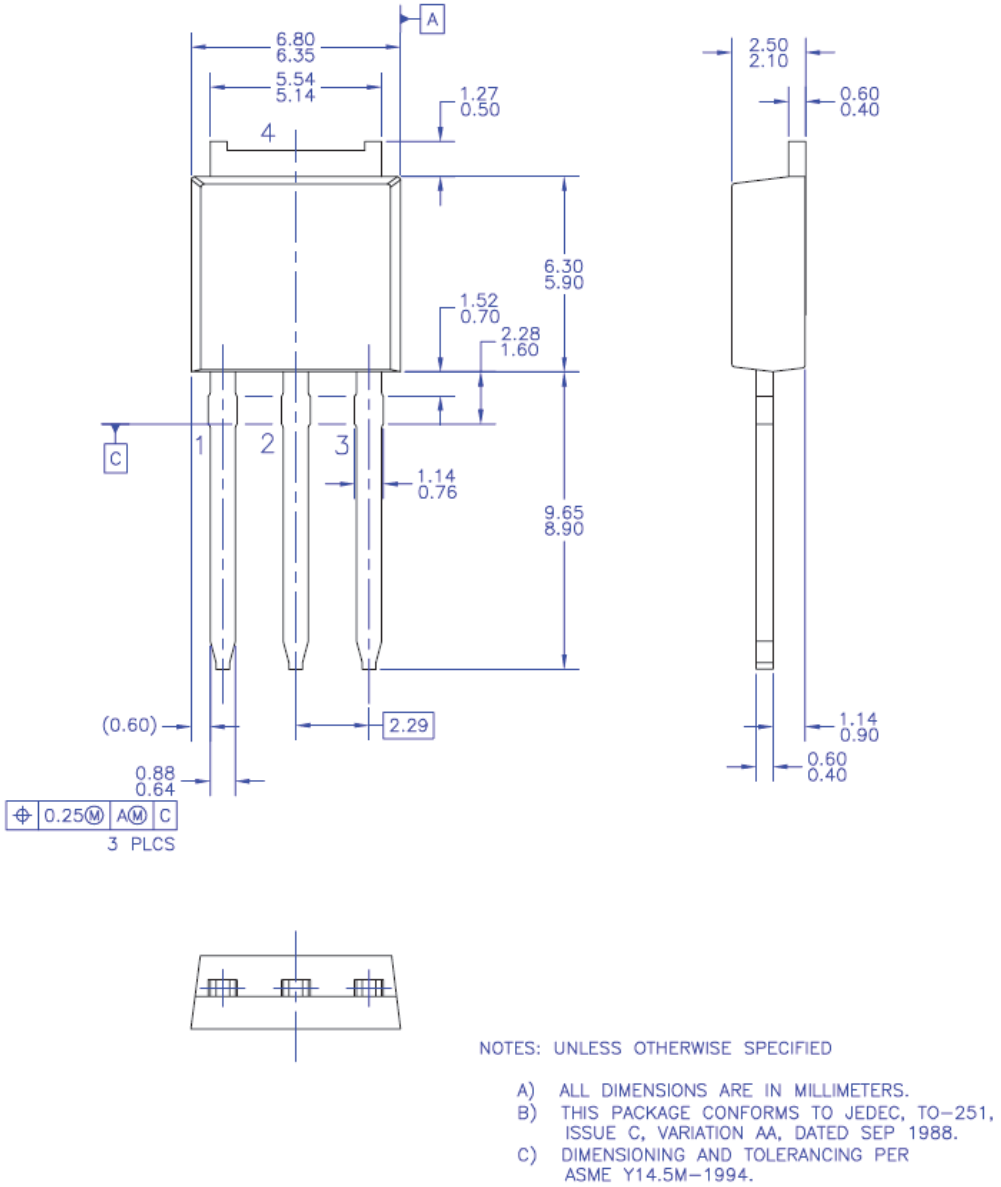

Figure 17. TO251 (I-PAK), Molded, 3-Lead

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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