

# 74LVT244A-Q100; 74LVTH244A-Q100

3.3 V octal buffer/line driver; 3-state

Rev. 3 — 8 July 2024

Product data sheet

## 1. General description

The 74LVT244A-Q100; 74LVTH244A-Q100 is a high-performance BiCMOS product designed for V<sub>CC</sub> operation at 3.3 V.

This device is an octal buffer that is ideal for driving bus lines. The device features two output enables (1 $\overline{OE}$ , 2 $\overline{OE}$ ), each controlling four of the 3-state outputs.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
  - Specified from -40 °C to +85 °C
- Octal bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- Wide supply voltage range from 2.7 V to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- Direct interface with TTL levels
- BiCMOS high speed and output drive
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- DHVQFN package with Side-Wettable Flanks enabling Automated Optical Inspection (AOI) of solder joints

## 3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
<a href="#">74LVT244AD-Q100</a> <a href="#">74LVTH244AD-Q100</a>	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm		<a href="#">SOT163-1</a>
<a href="#">74LVT244APW-Q100</a> <a href="#">74LVTH244APW-Q100</a>	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm		<a href="#">SOT360-1</a>

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Type number	Package			
	Temperature range	Name	Description	Version
74LVT244ABQ-Q100	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74LVTH244ABQ-Q100				

## 4. Functional diagram

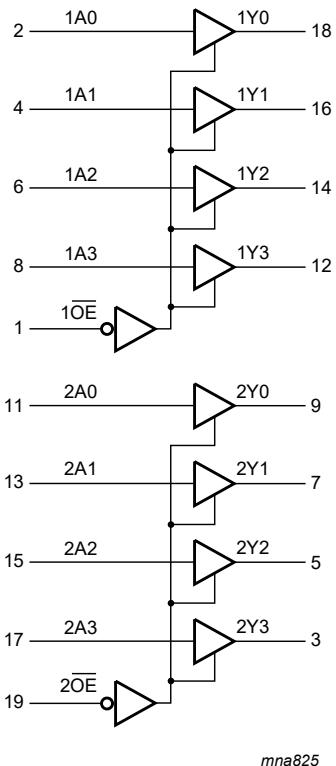


Fig. 1. Logic symbol

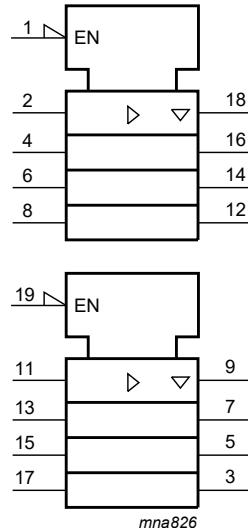
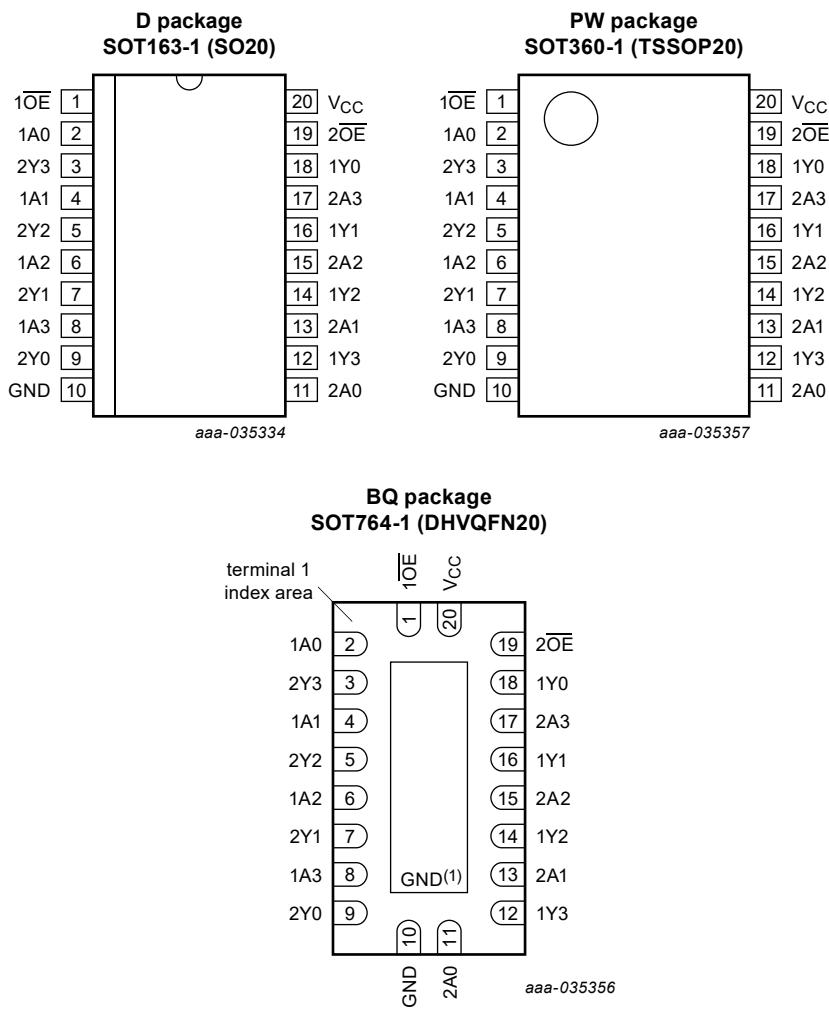


Fig. 2. IEC logic symbol

## 5. Pinning information

### 5.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$ , $\overline{OE}$	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
$V_{CC}$	20	supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

Control	Input	Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage		[1] -0.5	+7.0	V
V <sub>O</sub>	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature		[2] -	150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 to +85 °C	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		2.7	-	3.6	V
V <sub>I</sub>	input voltage		0	-	5.5	V
I <sub>OH</sub>	HIGH-level output current		-32	-	-	mA
I <sub>OL</sub>	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f <sub>i</sub> ≥ 1 kHz	-	-	64	mA
T <sub>amb</sub>	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 2.7 V; I <sub>IK</sub> = -18 mA	-1.2	-0.9	-	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 2.7 V to 3.6 V; I <sub>OH</sub> = -100 µA	V <sub>CC</sub> - 0.2	V <sub>CC</sub> - 0.1	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V; I <sub>OH</sub> = -8 mA	2.4	2.5	-	V
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -32 mA	2.0	2.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 100 µA	-	0.1	0.2	V
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 24 mA	-	0.3	0.5	V
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA	-	0.25	0.4	V
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 32 mA	-	0.3	0.5	V
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 64 mA	-	0.4	0.55	V
I <sub>I</sub>	input leakage current	all input pins				
		V <sub>CC</sub> = 0 V or 3.6 V; V <sub>I</sub> = 5.5 V	-	0.1	10	µA
		control pins				
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	±0.1	±1	µA
		data pins	[2]			
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub>		0.1	1	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 0 V to 4.5 V	-	1	±100	µA
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 3 V; V <sub>I</sub> = 0.8 V	75	150	-	µA
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 3 V; V <sub>I</sub> = 2.0 V	-	-150	-75	µA
I <sub>BHLO</sub>	bus hold LOW overdrive current	nAn input; V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0 V to 3.6 V	[3]	500	-	µA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	nAn input; V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0 V to 3.6 V		-	-	-500 µA
I <sub>EX</sub>	external current	nYn output in HIGH-state when V <sub>O</sub> > V <sub>CC</sub> ; V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 3.0 V	-	60	125	µA
I <sub>O(pu/pd)</sub>	power-up/power-down output current	V <sub>CC</sub> ≤ 1.2 V; V <sub>O</sub> = 0.5 V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; nOE = don't care	[4]	-	±1	±100 µA
I <sub>OZ</sub>	OFF-state output current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		V <sub>O</sub> = 3.0 V		-	1	5 µA
		V <sub>O</sub> = 0.5 V		-5	-1	- µA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A				
		output HIGH	-	0.13	0.19	mA
		output LOW	-	3	12	mA
		outputs disabled	[5]	-	0.13	0.19 mA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; one input at V <sub>CC</sub> - 0.6 V and other inputs at V <sub>CC</sub> or GND		-	0.1	0.2 mA

Symbol	Parameter	Conditions	$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			Unit
			Min	Typ[1]	Max	
$C_I$	input capacitance	$V_I = 0 \text{ V}$ or $3.0 \text{ V}$	-	4	-	pF
$C_O$	output capacitance	outputs disabled; $V_O = 0 \text{ V}$ or $3.0 \text{ V}$	-	8	-	pF

[1] All typical values are measured at  $T_{amb} = 25^{\circ}\text{C}$ .  
 [2] Unused pins at  $V_{CC}$  or GND.  
 [3] This is the bus hold overdrive current required to force the input to the opposite logic state.  
 [4] This parameter is valid for any  $V_{CC}$  between  $0 \text{ V}$  and  $1.2 \text{ V}$  with a transition time of up to  $10 \text{ ms}$ .  
 From  $V_{CC} = 1.2 \text{ V}$  to  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  a transition time of  $100 \text{ }\mu\text{s}$  is permitted. This parameter is valid for  $T_{amb} = 25^{\circ}\text{C}$  only.  
 [5]  $I_{CC}$  is measured with outputs pulled to  $V_{CC}$  or GND.  
 [6] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

## 10. Dynamic characteristics

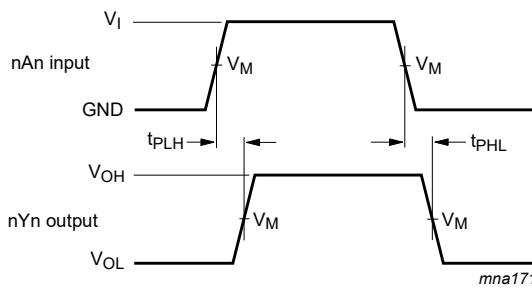
**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Fig. 5](#).

Symbol	Parameter	Conditions	$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			Unit
			Min	Typ[1]	Max	
$t_{PLH}$	LOW to HIGH propagation delay	$nAn$ to $nYn$ ; see <a href="#">Fig. 3</a>				
		$V_{CC} = 2.7 \text{ V}$	-	-	5.0	ns
		$V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}$	1	2.5	4.1	ns
$t_{PHL}$	HIGH to LOW propagation delay	$nAn$ to $nYn$ ; see <a href="#">Fig. 3</a>				
		$V_{CC} = 2.7 \text{ V}$	-	-	5.1	ns
		$V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}$	1	2.6	4.1	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	$n\overline{OE}$ to $nYn$ ; see <a href="#">Fig. 4</a>				
		$V_{CC} = 2.7 \text{ V}$	-	-	6.3	ns
		$V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}$	1	3.2	5.2	ns
$t_{PZL}$	OFF-state to LOW propagation delay	$n\overline{OE}$ to $nYn$ ; see <a href="#">Fig. 4</a>				
		$V_{CC} = 2.7 \text{ V}$	-	-	6.7	ns
		$V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}$	1.1	3.1	5.2	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	$n\overline{OE}$ to $nYn$ ; see <a href="#">Fig. 4</a>				
		$V_{CC} = 2.7 \text{ V}$	-	-	6.3	ns
		$V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}$	1.9	3.3	5.6	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	$n\overline{OE}$ to $nYn$ ; see <a href="#">Fig. 4</a>				
		$V_{CC} = 2.7 \text{ V}$	-	-	5.6	ns
		$V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}$	1.8	3.3	5.1	ns

[1] All typical values are at  $V_{CC} = 3.3 \text{ V}$  and  $T_{amb} = 25^{\circ}\text{C}$ .

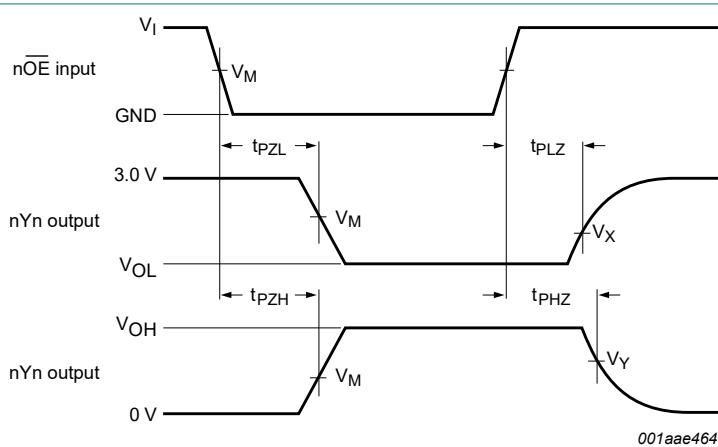
### 10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 3. Input (nAn) to output (nYn) propagation delays**



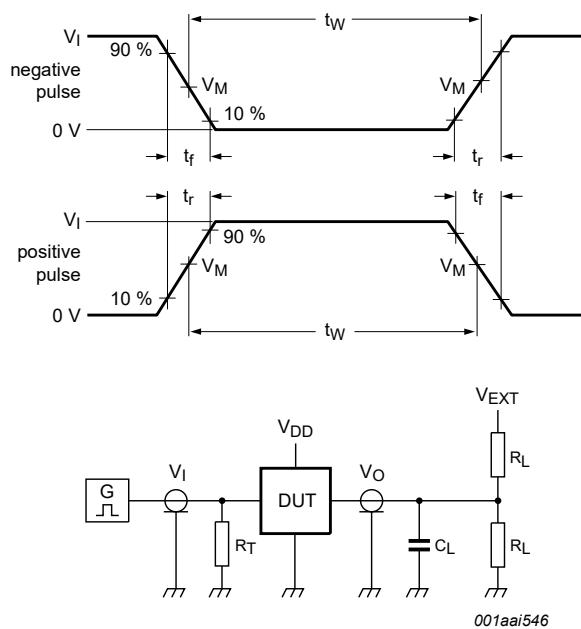
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 4. 3-state output enable and disable times**

**Table 8. Measurement points**

Input	Output		
$V_M$	$V_M$	$V_X$	$V_Y$
1.5 V	1.5 V	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V



Test data is given in [Table 9](#).

Definitions test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$V_{EXT}$  = Test voltage for switching times.

**Fig. 5. Test circuit for measuring switching times**

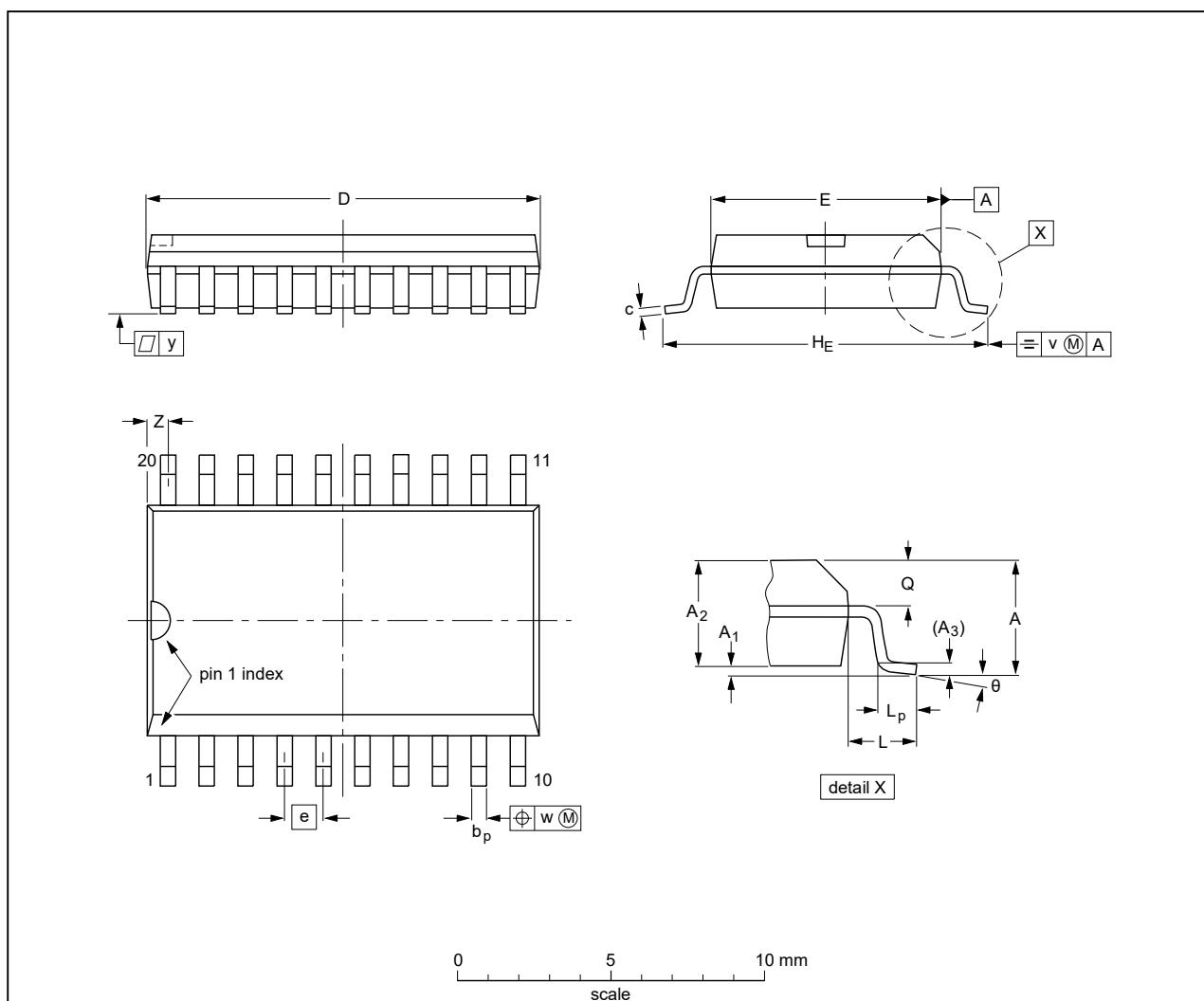
**Table 9. Test data**

Input				Load		$V_{EXT}$		
$V_I$	$f_I$	$t_W$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
2.7 V	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$	GND	6 V	open

## 11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.3	2.45	0.25	0.49	0.32	13.0	7.6	1.27	10.65	1.4	1.1	1.1	0.25	0.25	0.1	0.9	8°
inches	0.1	0.012	0.096	0.01	0.019	0.013	12.6	7.4		10.00	0.4	1.0	0.4	0.016	0.039	0.004	0.035	0°

### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Fig. 6. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

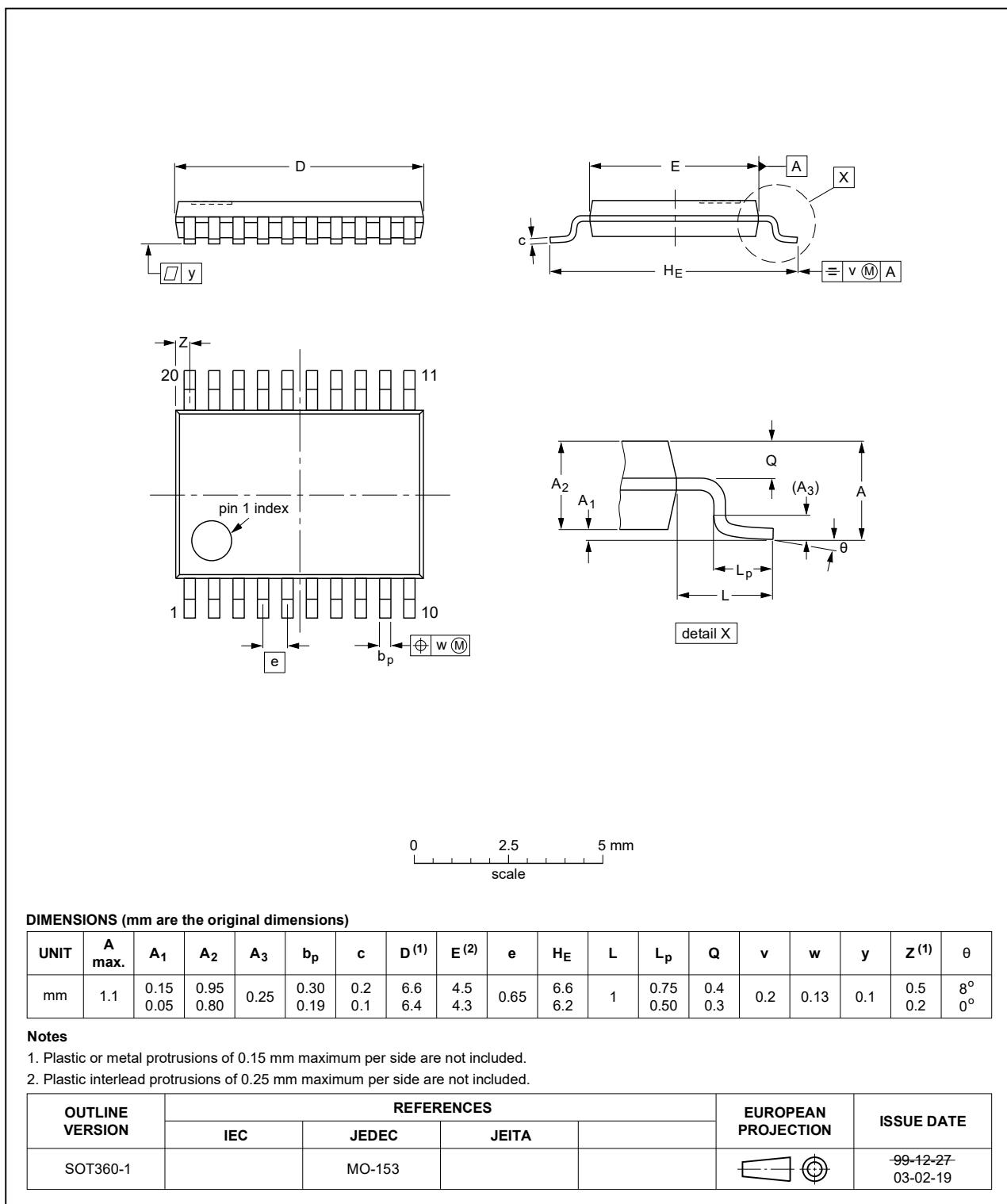


Fig. 7. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

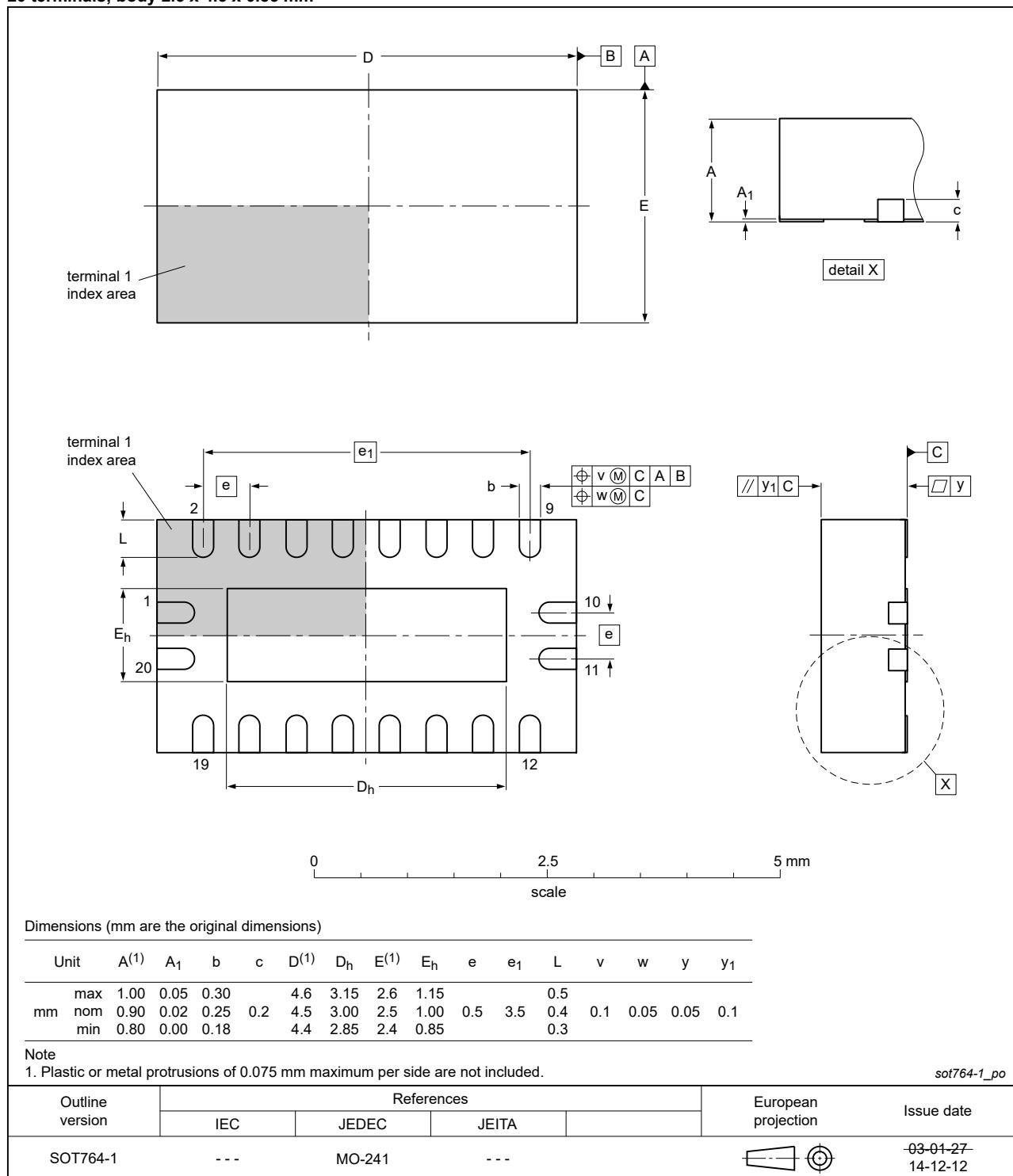


Fig. 8. Package outline SOT764-1 (DHVQFN20)

## 12. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

## 13. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH244A_Q100 v.3	20240708	Product data sheet	-	74LVT_LVTH244A_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74LVT_LVTH244A_Q100 v.2	20200824	Product data sheet	-	74LVT_LVTH244A_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 2</a> updated.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li> <li><a href="#">Table 6</a>: conditions for bushold overdrive current corrected.</li> <li>Package outline drawing <a href="#">Fig. 8</a> (DHVQFN20) updated.</li> </ul>			
74LVT_LVTH244A_Q100 v.1	20130422	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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