Silicon SPDT Switch, Non-Reflective, 9 kHz to 44 GHz

Preliminary Technical Data

ADRF5027

FEATURES

- Ultrawideband frequency range: 9 kHz to 44 GHz
- Non-reflective design
- Low insertion loss:
  - 1.1 dB at 18 GHz
  - 2.2 dB at 40 GHz
- High isolation:
  - TBD dB at 18 GHz
  - TBD dB at 40 GHz
- High input linearity:
  - 1 dB compression (P1dB): TBD dBm
  - Third order intercept (IP3): TBD dBm
- High power handling:
  - 24 dBm through path
  - 24 dBm terminated path
- All-off function
- No low frequency spurious
- RF Settling time (0.1dB final RF Out): TBD
- 20-lead, 3 mm × 3 mm land grid array package
- Pin compatible with ADRF5026, fast switching version

APPLICATIONS

- Industrial Scanners
- Test and instrumentation
- Cellular infrastructure - mmWave 5G
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

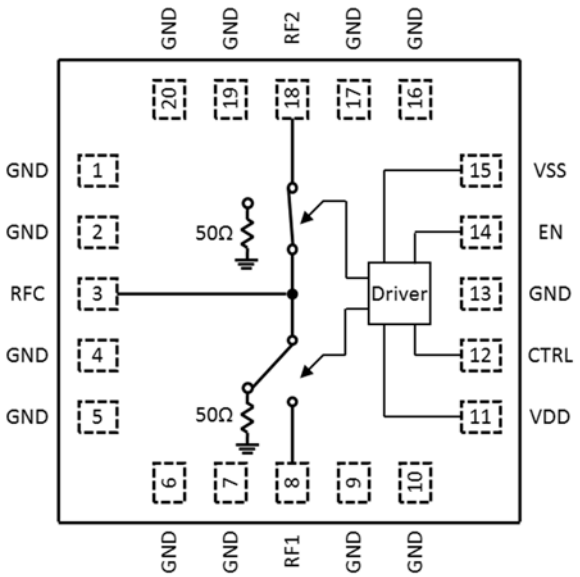

Figure 1.

GENERAL DESCRIPTION

The ADRF5027 is a single-pole, double-throw (SPDT) silicon switch operating from 9 kHz to 44 GHz.

This switch offers low insertion loss of 2.2 dB at 40 GHz, and high isolation of TBD dB at 40 GHz. This switch also features an all-off function, where both the RF ports are in isolation state. The ADRF5027 is non-reflective design; both the RF ports are internally terminated to 50 Ω.

The ADRF5027 draws a low current of 2uA on the positive supply of +3.3V and -100uA on the negative supply of -3.3V. This switch also provides CMOS/LVTTL logic-compatible control.

The ADRF5027 is pin compatible with the ADRF5026, the fast switching version, which operates from 100 MHz to 44 GHz.

For ultrawideband surface mount technology (SMT), impedance matching on the RF transmission lines can improve insertion loss and return loss performance at high frequencies. Refer to **Error! Reference source not found.**, **Error! Reference source not found.**, and Applications Information for more details.

The ADRF5027 comes in a 3 mm by 3 mm, 20-loead land grid array (LGA) package.

Rev. PrE Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = -3.3 V, V_{CTRL} = 0 or V_{DD} V, V_{EN} = 0 or V_{DD} V, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.009		44,000	MHz
INSERTION LOSS	IL	With impedance match, See Figure 23				
Between RFC and RF1/RF2		9 kHz to 18 GHz		1.1		dB
		18 GHz to 26 GHz		1.5		dB
		26 GHz to 35 GHz		1.9		dB
		35 GHz to 40 GHz		2.2		dB
		40 GHz to 44 GHz		3.4		dB
		Without impedance match, See Figure 24				
		9 kHz to 18 GHz		TBD		dB
		18 GHz to 26 GHz		TBD		dB
		26 GHz to 35 GHz		TBD		dB
		35 GHz to 40 GHz		TBD		dB
		40 GHz to 44 GHz		TBD		dB
RETURN LOSS		With impedance match, See Figure 23				
RFC and RF1/RF2 (On)		9 kHz to 18 GHz		25		dB
		18 GHz to 26 GHz		14		dB
		26 GHz to 35 GHz		10		dB
		35 GHz to 40 GHz		10		dB
		40 GHz to 44 GHz		8		dB
		Without impedance match, See Figure 24				
		9 kHz to 18 GHz		TBD		dB
		18 GHz to 26 GHz		TBD		dB
		26 GHz to 35 GHz		TBD		dB
		35 GHz to 40 GHz		TBD		dB
		40 GHz to 44 GHz		TBD		dB
RF1/RF2 (Off)		With impedance match, See Figure 23				
		9 kHz to 18 GHz		28		dB
		18 GHz to 26 GHz		28		dB
		26 GHz to 35 GHz		17		dB
		35 GHz to 40 GHz		13		dB
		40 GHz to 44 GHz		9		dB
		Without impedance match, See Figure 24				
		9 kHz to 18 GHz		TBD		dB
		18 GHz to 26 GHz		TBD		dB
		26 GHz to 35 GHz		TBD		dB
		35 GHz to 40 GHz		TBD		dB
		40 GHz to 44 GHz		TBD		dB
ISOLATION						
Between RFC and RF1/RF2		9 kHz to 18 GHz		53		dB
		18 GHz to 26 GHz		48		dB
		26 GHz to 35 GHz		48		dB
		35 GHz to 40 GHz		48		dB
		40 GHz to 44 GHz		43		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
ISOLATION						
Between RF1 and RF2		9 kHz to 18 GHz		58		dB
		18 GHz to 26 GHz		53		dB
		26 GHz to 35 GHz		53		dB
		35 GHz to 40 GHz		55		dB
		40 GHz to 44 GHz		50		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		1.0		µs
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		1.1		µs
Settling Time						
0.1 dB Settling Time		50% V_{CTL} to 0.1 dB of final RF output		6.2		µs
0.01 dB Settling Time		50% V_{CTL} to 0.01 dB of final RF output		TBD		µs
INPUT LINEARITY						
1 dB Compression	P1dB			TBD		dBm
Third-Order Intercept	IP3	Two-tone input power = 14 dBm each tone, Δf = 1 MHz		TBD		dBm
SUPPLY CURRENT		V_{DD}, V_{SS} pins				
Positive Supply Current	I_{DD}			2		V
Negative Supply Current	I_{SS}			100		V
DIGITAL CONTROL INPUTS		CTRL, EN pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low and High Current	I_{INL}, I_{INH}			TBD		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	
Negative	V_{SS}		-3.45		-3.15	
Digital Control Voltage	V_{CTRL}, V_{EN}		0		V_{DD}	
RF Input Power	P_{IN}	f = 1 MHz to 40 GHz, T_{CASE} = 85°C				
Insertion Loss Path		RF signal is applied to RFC or through connected RF1/RF2			24	dBm
Isolation Path		RF signal is applied to terminated RF1/RF2			24	dBm
Hot Switching		RF signal is present at RFC while switching between RF1 and RF2			TBD	dBm
Case Temperature	T_{CASE}		−55		+105	°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.3 V
Digital Control Input Voltage	-0.3 V to V_{DD} + 0.3 V
RF Input Power (1 MHz to 44 GHz, T_{CASE} = 85°C)	
Through Path	26 dBm
Termination Path	25 dBm
Hot Switching	TBD
Temperature	
Junction, T_J	135°C
Storage	−65°C to +150°C
Reflow	260°C
Junction to Case Thermal Resistance, θ_{JC}	
Through Path	TBD
ESD Sensitivity	
Human Body Model (HBM)	TBD
Charged Device Model (CDM)	TBD

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

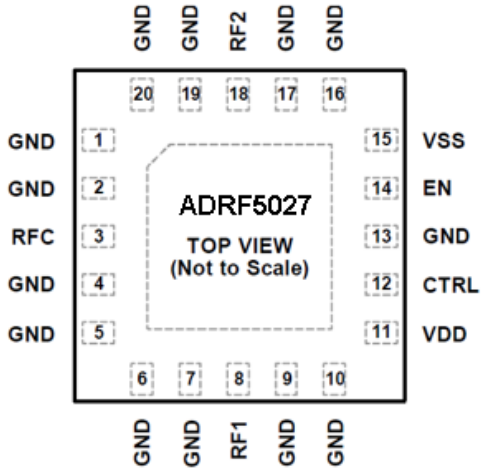

Figure 2. Pin Configuration (Top View)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 7, 9, 10, 13, 16, 17, 19, 20	GND	Ground. These pins must be connected to the RF/dc ground of the printed circuit board (PCB).
3	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
8	RF1	RF1 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
11	VDD	Positive Supply Voltage Pin.
12	CTRL	Control Input Pin. See Table
14	EN	Enable Input Pin. See Table
15	VSS	Negative Supply Voltage Pin.
18	RF2	RF2 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the printed circuit board (PCB).

INTERFACE SCHEMATICS

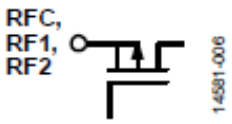

Figure 3. RFC, RF1, RF2 Interface Schematic

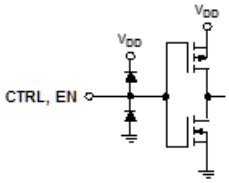

Figure 4. CTRL, EN Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = -3.3 V, V_{CTRL} = 0 or V_{DD} V, V_{EN} = 0 or V_{DD} V, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Insertion loss and return loss are measured on the probe matrix board using G-S-G probes close to the RF pins. However, signal coupling between the probes limits the isolation performance of ADRF5027; isolation is measured on the evaluation board. See Applications Information section for details on evaluation and probe matrix boards.

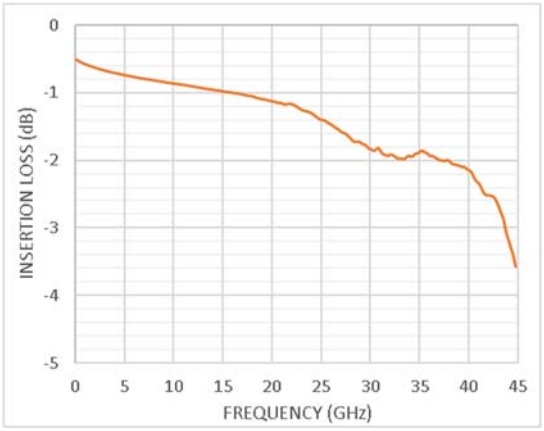

Figure 5. Insertion Loss vs. Frequency, With impedance match

Figure 8. Insertion Loss vs. Frequency, Without impedance match

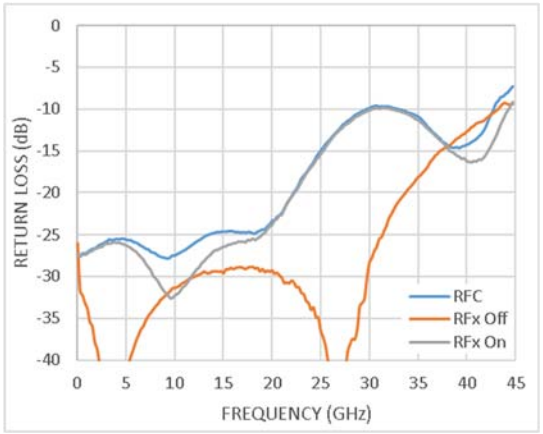

Figure 6. Return Loss vs. Frequency, With impedance match

Figure 9. Return Loss vs. Frequency, Without impedance match

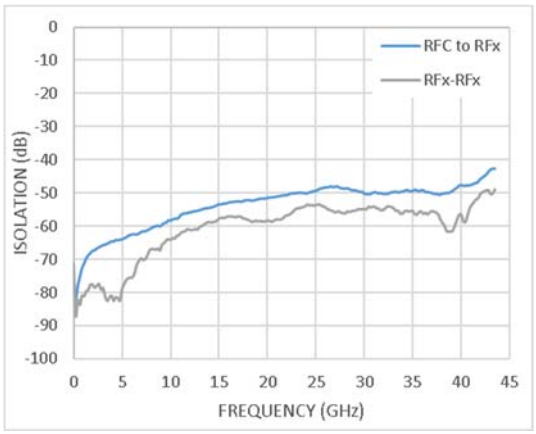

Figure 7. Isolation vs. Frequency, With impedance match

Figure 10. Isolation vs. Frequency, Without impedance match

INPUT POWER COMPRESSIONS AND THIRD ORDER INTERCEPT

V_{DD} = 3.3 V, V_{SS} = -3.3 V, V_{CTRL} = 0 or V_{DD} V, V_{EN} = 0 or V_{DD} V, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

All of the large signal performance parameters were measured on the evaluation board.

Figure 11. Input 0.1 dB Power Compression vs. Frequency, over Temperature

Figure 14. Input 0.1 dB Power Compression vs. Frequency, over Temperature (Low Frequency Detail)

Figure 12. Input 1 dB Power Compression vs. Frequency, over Temperature

Figure 15. Input 1 dB Power Compression vs. Frequency, over Temperature (Low Frequency Detail)

Figure 13. Input IP3 vs. Frequency, over Temperature

Figure 16. Input IP3 vs. Frequency, over Temperature (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5027 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

All of the RF ports (RFC, RF1 and RF2) are dc-coupled to 0V, and dc blocking capacitors are not required on the RF paths if the RF potential is equal to 0 V.

The RF ports are internally matched to 50 Ω; therefore, external matching networks are not required. However, impedance matching on the RF transmission lines may be used to improve insertion loss and return loss performance at high frequencies.

The ADRF5027 integrates a driver to perform logic function internally and provide the user with the advantage of a simplified control interface. The driver features two digital control input pins, CTRL and EN. When the EN pin is logic low, the logic level applied to the CTRL pin determines which RF port is in insertion loss state and in isolation state.

ADRF5027 supports all-off function. When the EN pin is logic high, both RF1 to RFC path and RF2 to RFC path are in isolation state regardless of logic state of CTRL. RF1 and RF2 ports are terminated to internal 50 Ω resistors and RFC becomes open reflective.

See Table 4 for control voltage truth table.

The ADRF5027 design is bidirectional with equal power handling capability; an RF input signal (P_{IN}) can be applied to the RFC port or the RF1/RF2 ports. The isolation path provides high loss between the unselected RF port and the insertion loss path.

The ideal power-up sequence is as follows:

1. Power up GND.
2. Power up VDD and VSS. The relative order is not important.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. Powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures.
4. Apply an RF input signal.

Table 4. Control Voltage Truth Table

Digital Control Input		RF Paths	
EN	**CTRL**	**RF1 to RFC**	**RF2 to RFC**
Low	Low	Isolation	Insertion Loss
Low	High	Insertion Loss	Isolation
High	Low	Isolation	Isolation
High	High	Isolation	Isolation

APPLICATIONS INFORMATION

EVALUATION BOARD

Figure 17 and Figure 18 show the top and cross-sectional views of the evaluation board, which uses 4-layer construction with a copper thickness of 0.5 oz (0.7 mil) and dielectric materials between each copper layer.

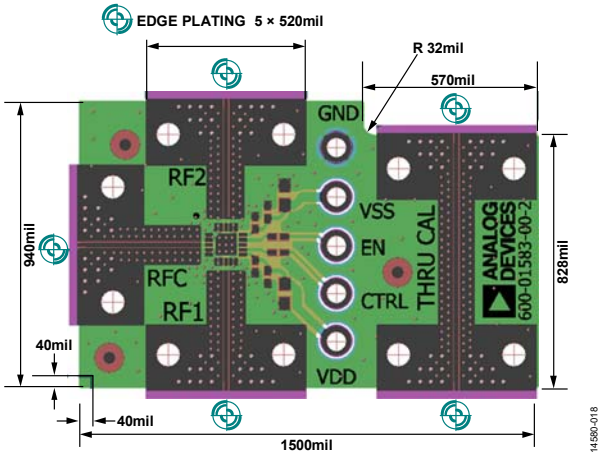

Figure 17. Evaluation Board Layout (Top View)

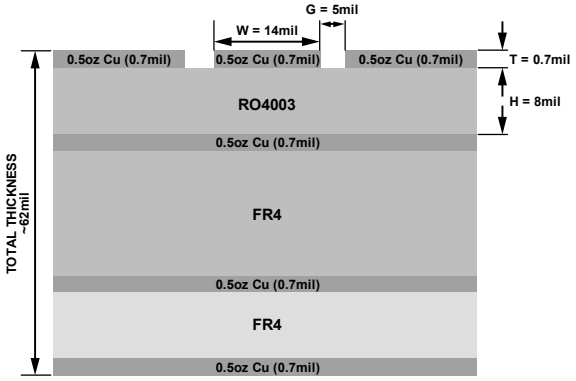

Figure 18. Evaluation Board (Cross Sectional View)

All RF and dc traces are routed on the top copper layer whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. Top dielectric material is 8 mil Rogers RO4003, offering good high frequency performance. The middle and bottom dielectric materials are FR-4 type materials to achieve an overall board thickness of 62 mil.

The RF transmission lines were designed using a coplanar waveguide (CPWG) model with a width of 14 mil and ground spacing of 5 mil to have a characteristic impedance of 50 Ω. For good RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

Two power supply ports are connected to the VDD and VSS test points, TP5 and TP2, and the ground reference is connected to the GND test point, TP1. On each supply trace, a 100 pF bypass capacitor is used, and unpopulated components positions are available for applying extra bypass capacitors.

Two control ports are connected to the EN and CTRL test points, TP3 and TP4. On each control trace, a resistor position is available to improve the isolation between the RF and control signals. The RF ports are connected to the RFC, RF1, and RF2 connectors (J1, J2, and J3) that are end launch 2.4 mm RF connectors. A through transmission line that connects unpopulated RF connectors (J7 and J8) is also available to measure the loss of the PCB. Figure 12 and Table 5 are the evaluation board schematic and bill of materials, respectively.

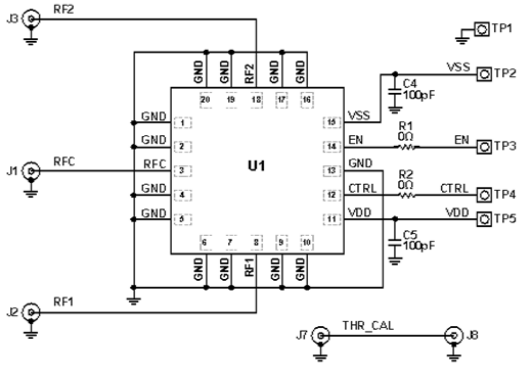

Figure 19. Evaluation Board Schematic

Table 5. Bill of Materials, Evaluation Board Components

Component	Description
J1-J3, J7-8	End launch connectors, 2.4 mm
TP1 to TP5	Through hole mount test points
C4, C5	100 pF capacitors, 0402 package
C2, C3	Unpopulated capacitors, 0402 package
C1, C6	Unpopulated capacitors, 0603 package
R1, R2	0 Ω resistors, 0402 package
U1	ADRF5027 SPDT switch

The "Thru Cal" is used to remove the board losses from the evaluation board measurements to determine the true part performance. Figure 20 shows the typical board loss for this evaluation board at room temperature, the embedded insertion loss, and the deembedded insertion loss for ADRF5027.

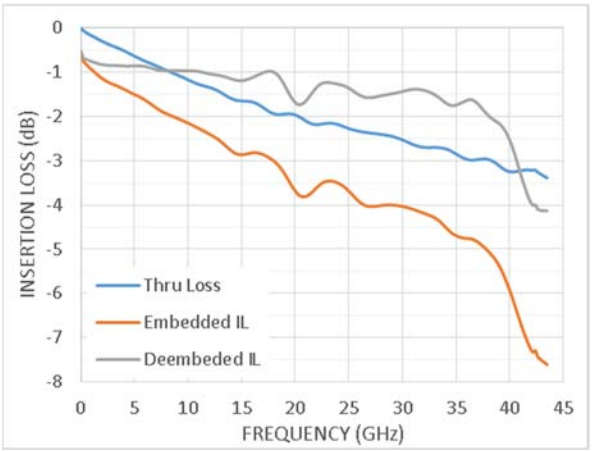

Figure 20. Insertion Loss vs. Frequency

PROBE MATRIX BOARD

The probe matrix board is a 4-layer board. This board also uses a 8 mil Rogers RO4003 dielectric. The outer copper layers are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil). The RF transmission lines were designed using a CPWG model with a width of 14 mil and ground spacing of 7 mil to have a characteristic impedance of 50 Ω.

Figure 21 and Figure 22 show the top and cross-sectional views of the probe matrix board. Measurements are made using ground-signal-ground (G-S-G) probes at close proximity to the RF pins. Probing reduces the reflections caused by mismatch arising from connectors, cables, and board layout, resulting in a more accurate measurement of insertion loss and return loss. However, signal coupling between the RF probes limit the isolation measurement. The evaluation board is used for making isolation measurements.

RF traces for a through-reflect-line (TRL) calibration are designed on the board itself. Board loss is compensated for by using a nonzero line length at calibration. The actual board duplicates the same layout in matrix form to assemble multiple devices at once. Insertion loss and return loss measurements are made on this board. Isolation measurements are made on the evaluation board.

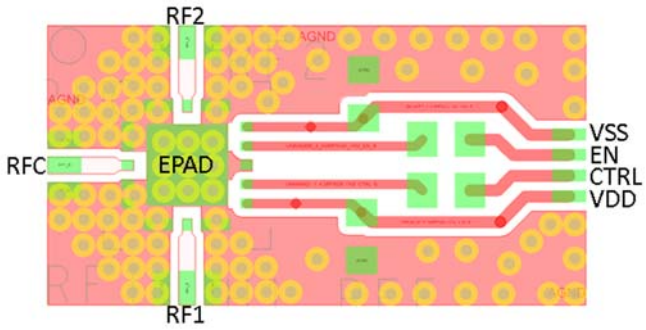

Figure 21. Probe Board Layout (Top View)

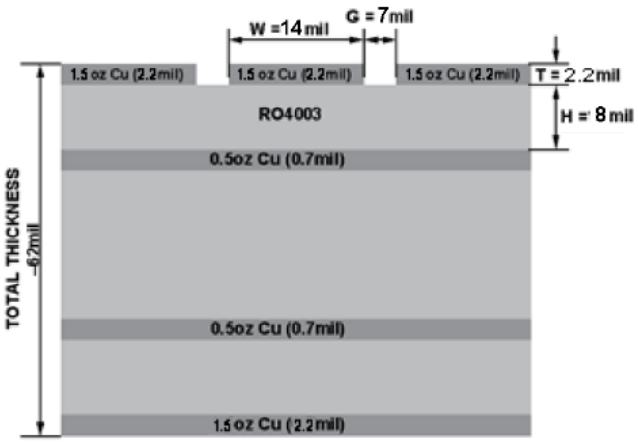

Figure 22. Probe Matrix Board (Cross Sectional View)

Impedance match for Ultrawideband Frequencies

The footprint and landing pattern is critical to performance. Insertion loss and return loss performance at high frequencies can be improved by implementing impedance matching on the RF transmission lines. Figure 24 and Figure 23 highlight the difference in the transmission lines at the RF ports.

The dimensions of the 50 Ω lines are 14 mil trace width and 7 mil gap. To implement this impedance match, the pad length was extended by 8 mil

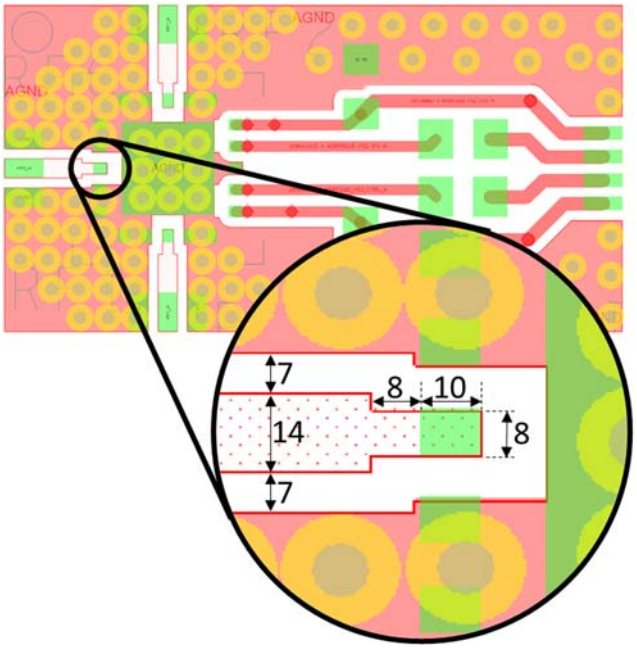

Figure 23. With impedance match circuit

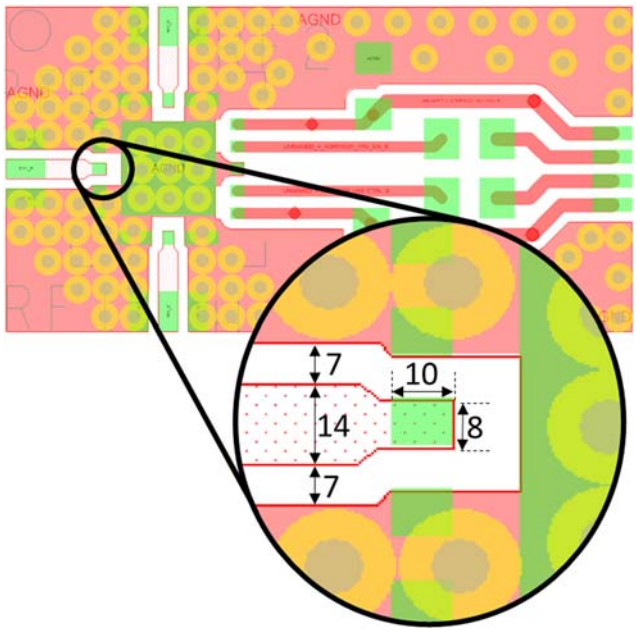

Figure 24. Without impedance match circuit

Narrowband Impedance Matching – mmWave 5G Frequencies

Narrowband impedance matching on the RF transmission lines can be used to improve return loss and insertion loss for a targeted frequency range. The impedance matched circuit highlighted below achieves flat insertion loss response of 2.3 dB between 32 GHz to 43 GHz. Figure 25 shows the trace dimensions of the RF ports. The dimensions of the 50 Ω lines are 14 mil trace width and 7 mil gap. To implement this impedance matched circuit, an 8 mil trace with a width of 5 mils was inserted between the pin pad and the 50 Ω trace.

Table 6 and Figure 26, Figure 27, and Figure 28 show the measured performance of ADRF5027 on this circuit on a probe matrix board.

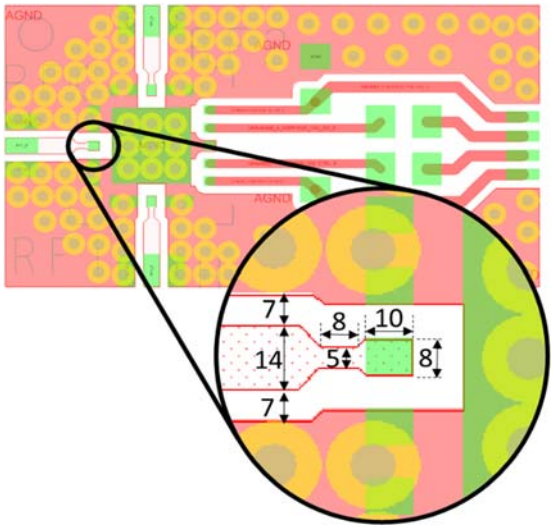

Figure 25. Impedance Matched Circuit

Table 6. Impedance Matched Parameters

Parameter	Test Condition	Typ	Unit
INSERTION LOSS	See Figure 25		
Between RFC and RF1/RF2	9 kHz to 18 GHz	1.1	dB
	18 GHz to 26 GHz	1.6	dB
	26 GHz to 35 GHz	2.3	dB
	35 GHz to 40 GHz	2.3	dB
	40 GHz to 44 GHz	3.0	dB
RETURN LOSS	See Figure 25		
RFC and RF1/RF2 (On)	9 kHz to 18 GHz	22	dB
	18 GHz to 26 GHz	13	dB
	26 GHz to 35 GHz	7	dB
	35 GHz to 40 GHz	7	dB
	40 GHz to 44 GHz	14	dB
RF1/RF2 (Off)	See Figure 25		
	9 kHz to 18 GHz	25	dB
	18 GHz to 26 GHz	23	dB
	26 GHz to 35 GHz	15	dB
	35 GHz to 40 GHz	9	dB
	40 GHz to 44 GHz	7	dB

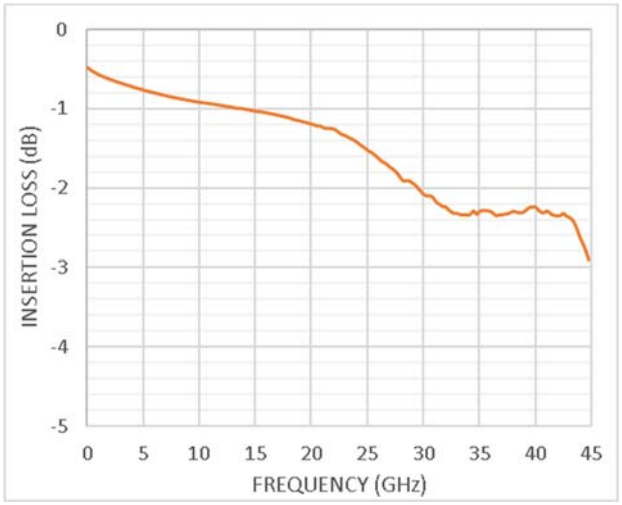

Figure 26. Insertion Loss vs. Frequency, With Impedance Matching

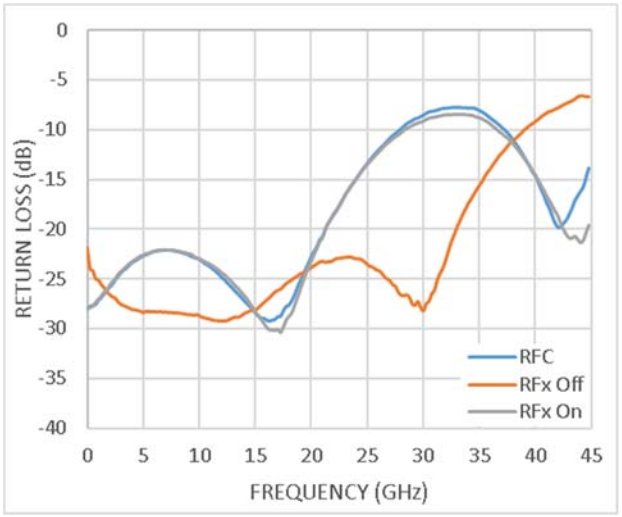

Figure 27. Return Loss vs. Frequency, With Impedance Matching

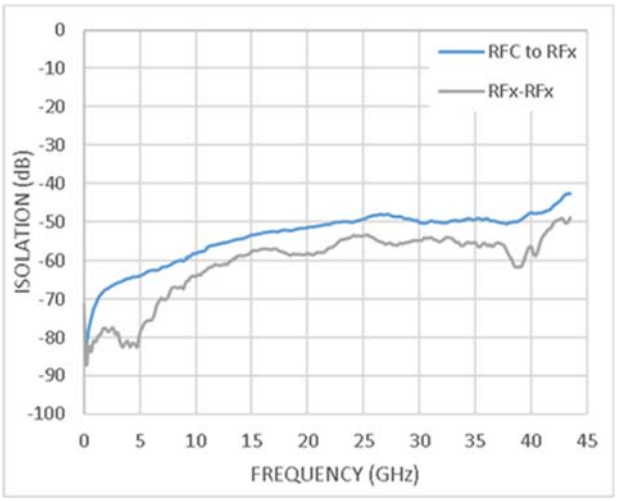

Figure 28. Isolation vs. Frequency, With Impedance Matching

OUTLINE DIMENSIONS

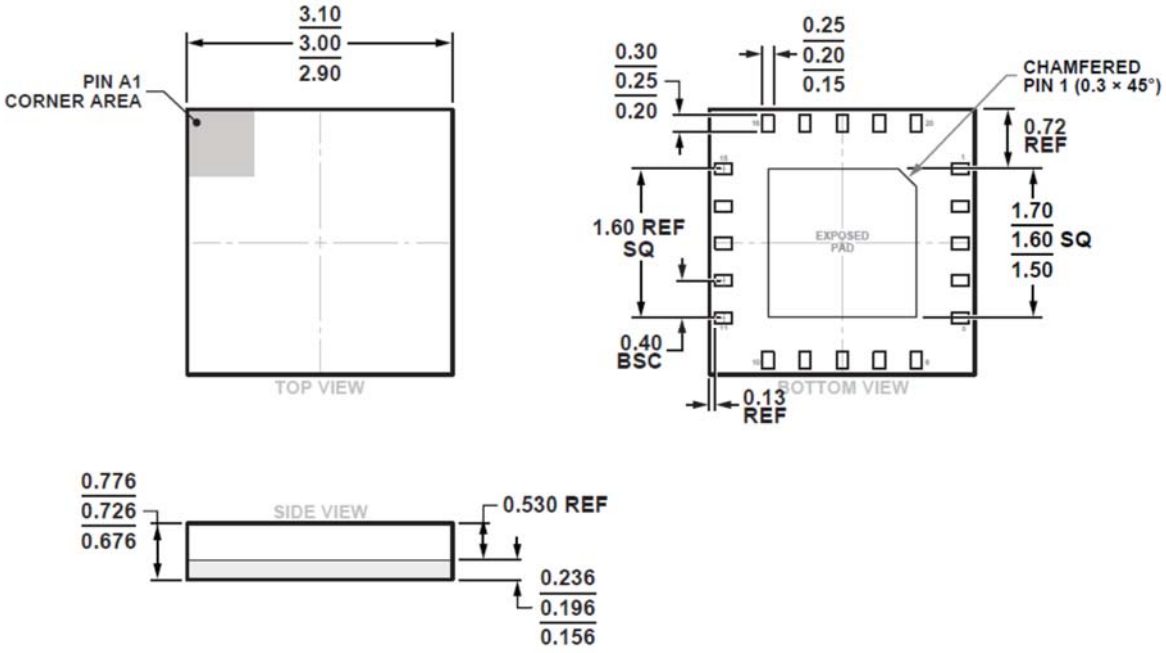

Figure 29. 20-Lead Land Grid Array [LGA]
3 mm × 3 mm Body and 0.72 mm Package Height
(CC-20-4)
Dimensions shown in millimeters

PR16768-0-3/18(PrE)