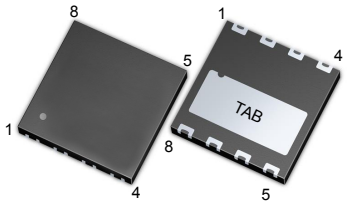
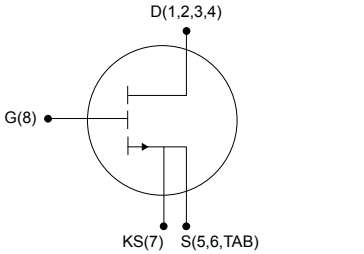
SGT080R70ILB

Datasheet

700 V, 60 mΩ typ., 29 A, e-mode PowerGaN transistor



PowerFLAT 8x8 HV for PowerGaN



G8D1234S56TABKS7

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Series
SGT080R70ILB	700 V	80 mΩ	29 A	G-HEMT

- Enhancement mode normally off transistor
- Very high switching speed
- High power management capability
- Extremely low capacitances
- Kelvin source pad for optimum gate driving
- Zero reverse recovery charge
- ESD safeguard

Applications

- Adapters for tablets, notebook and AIO
- USB type-C PD adapters and quick chargers
- AC-DC converters
- DC-DC converters

Description

The SGT080R70ILB is a 700 V, 29 A e-mode PowerGaN transistor combined with a well established packaging technology. The resulting G-HEMT device provides extremely low conduction losses, high current capability and ultra fast switching operation to enable high power density and unbeatable efficiency performances.

Product status link
SGT080R70ILB

Product summary	
Order code	SGT080R70ILB
Marking	080R70I
Package	PowerFLAT 8x8 HV for PowerGaN
Packing	Tape and reel

1 Electrical ratings

T_C = 25 °C unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	700(1)	V
	Drain-source voltage (transient, t_p < 200 µs)	800	
V_{GS}	Gate-source voltage	-6 to 7	V
I_D	Drain current (continuous) at T_C = 25 °C	29(2)	A
I_{DM}	Pulse drain current (t_p = 10 µs)	58	A
P_{TOT}	Total power dissipation at T_C = 25 °C	188(2)	W
ESD	Human body model, R = 1.5 kΩ, C = 100 pF	2	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Recommended continuous maximum bus voltage during switching operations should not exceed 450 V.*
2. *Limited by design.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.52	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	33.6(1)	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Drain-source leakage current	V_{GS} = 0 V, V_{DS} = 700 V		5	65	µA
		V_{GS} = 0 V, V_{DS} = 700 V, T_J = 150 °C		13	390(1)	
I_{GSS}	Gate-source leakage current	V_{DS} = 0 V, V_{GS} = 6 V		163		µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 30.7 mA	1.2	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 6 V, I_D = 8 A		60	80	mΩ
		V_{GS} = 6 V, I_D = 8 A, T_J = 150 °C		135		

1. *Specified by design, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 400 V, f = 100 kHz	-	225	-	pF
C_{oss}	Output capacitance		-	70	-	pF
C_{rss}	Reverse transfer capacitance		-	0.5	-	pF
$C_{o(er)}$(1)	Equivalent output capacitance energy related	V_{GS} = 0 V, V_{DS} = 0 to 400 V	-	105	-	pF
$C_{o(tr)}$(2)	Equivalent output capacitance time related		-	150	-	pF
R_g	Intrinsic gate resistance	f = 5 MHz, I_D = 0 A	-	3	-	Ω
V_{plat}	Gate plateau voltage	V_{DS} = 400 V, I_D = 8 A	-	2.2	-	V
Q_g	Total gate charge	V_{GS} = 0 to 6 V, V_{DS} = 400 V, I_D = 8 A	-	6.2	-	nC
Q_{gs}	Gate-source charge		-	0.5	-	nC
Q_{gd}	Gate-drain charge		-	2.2	-	nC
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V, V_{DS} = 400 V	-	0	-	nC
Q_{oss}	Output charge		-	60	-	nC

1. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to the stated value.*
2. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to the stated value.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DS} = 400 V, I_D = 16 A, V_{GS} = 6 V, $R_{G(on)}$ = 10 Ω, $R_{G(off)}$ = 2 Ω, L = 318 µH	-	3	-	ns
t_r	Rise time		-	4	-	ns
$t_{d(off)}$	Turn-off delay time		-	5	-	ns
t_f	Fall time		-	4	-	ns

Table 6. Reverse conduction

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Source-drain reverse voltage	V_{GS} = 0 V, I_{SD} = 8 A	-	2.3	-	V

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area (T_C = 25 °C)

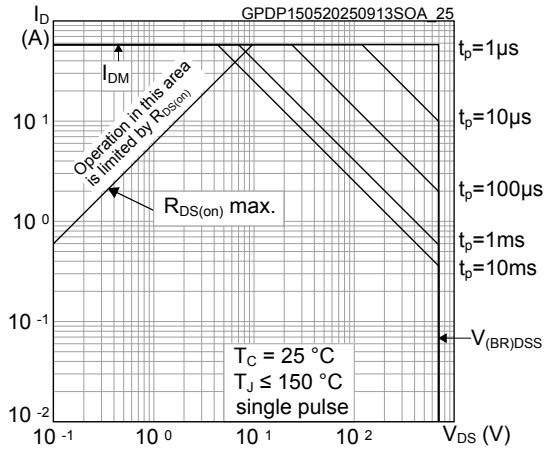


Figure 2. Safe operating area (T_C = 125 °C)

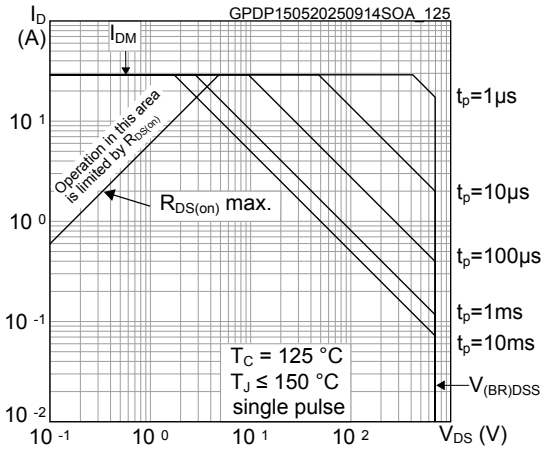


Figure 3. Maximum transient thermal impedance

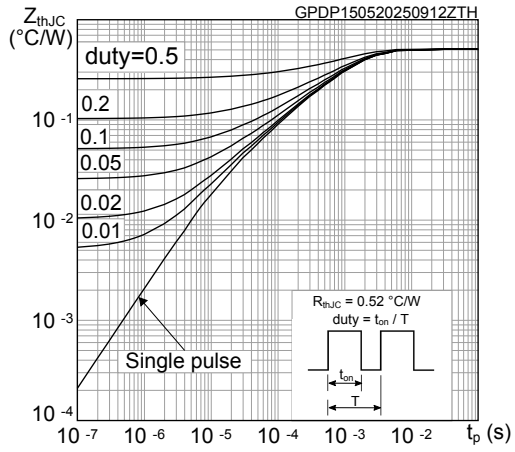


Figure 4. Total power dissipation

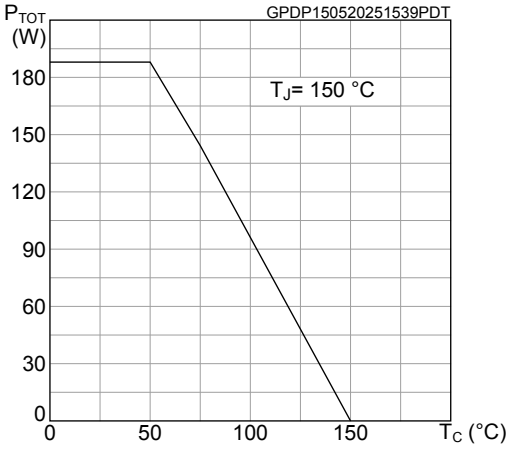


Figure 5. Typical output characteristics (T_J = 25 °C)

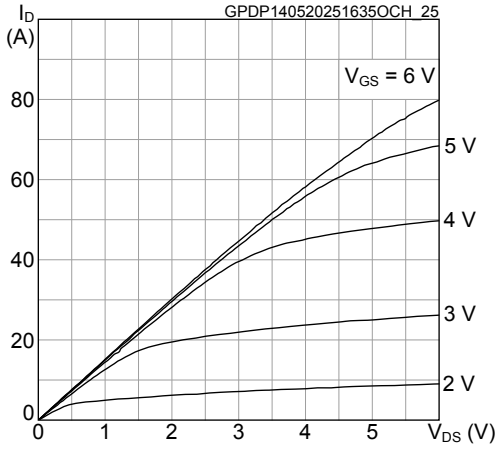


Figure 6. Typical output characteristics (T_J = 125 °C)

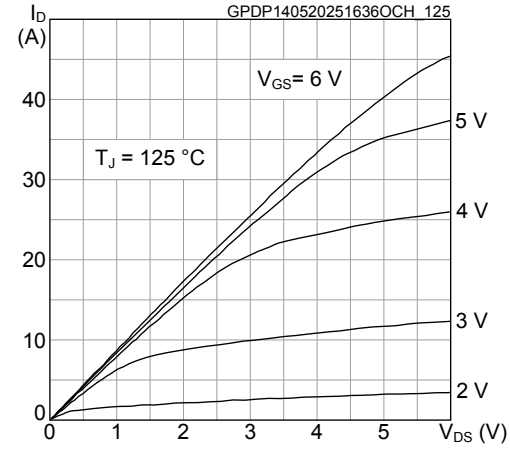


Figure 7. Typical transfer characteristics

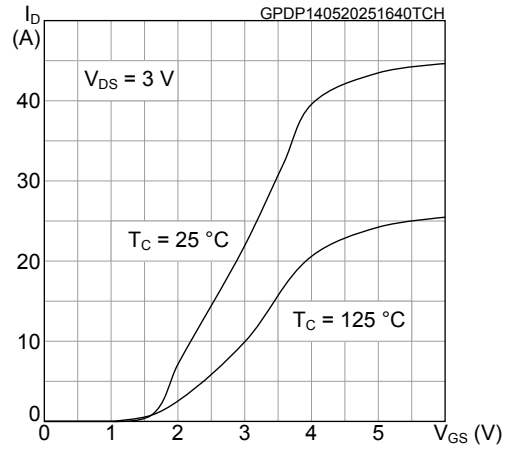


Figure 8. Normalized on-resistance vs temperature

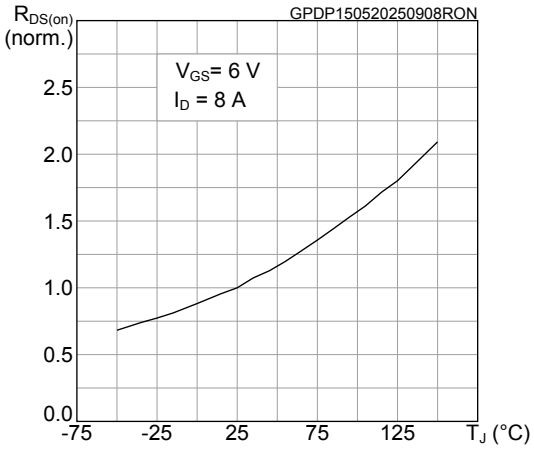


Figure 9. Typical drain-source on-resistance (T_J = 25 °C)

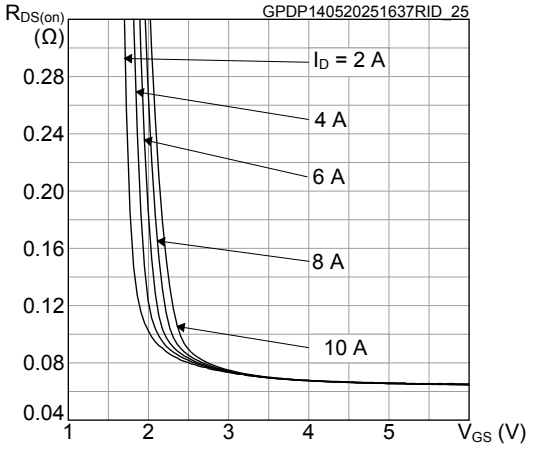


Figure 10. Typical drain-source on-resistance (T_J = 125 °C)

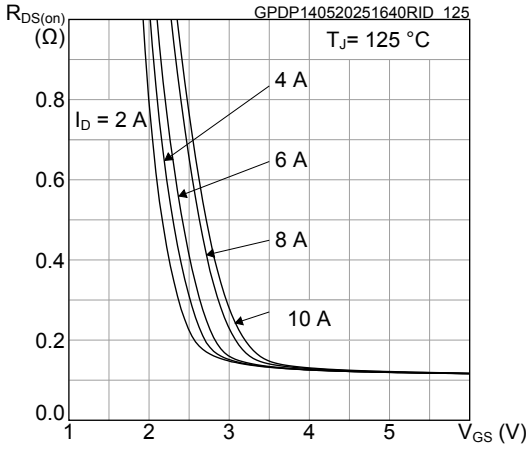


Figure 11. Typical gate charge characteristics

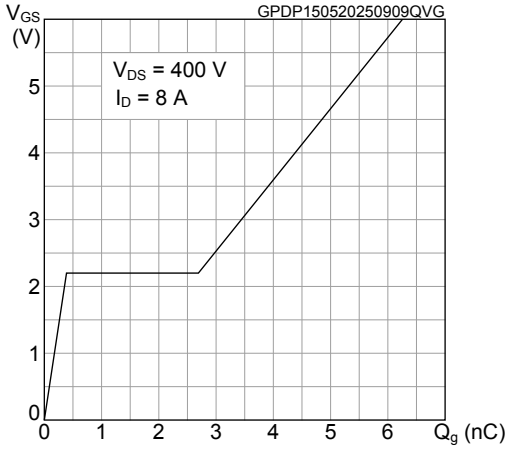


Figure 12. Typical capacitance characteristics

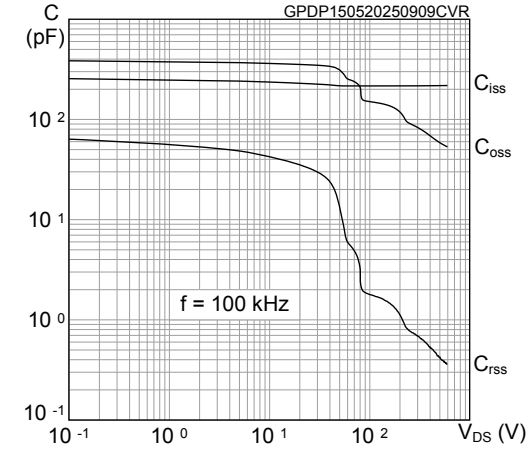


Figure 13. Typical output capacitance charge

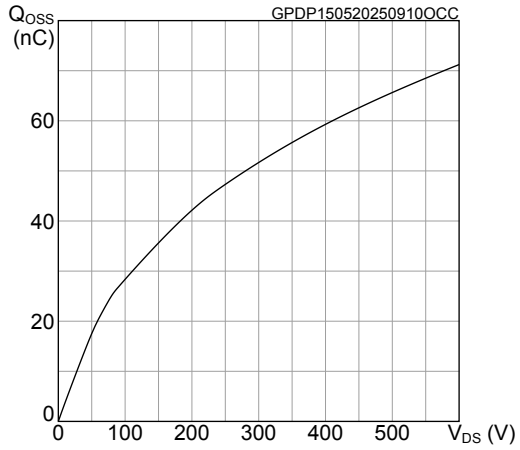


Figure 14. Typical output capacitance stored energy

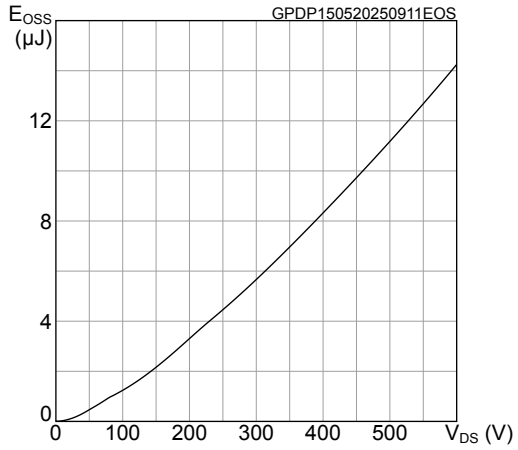


Figure 15. Typical diode reverse conduction characteristics (T_J = 25 °C)

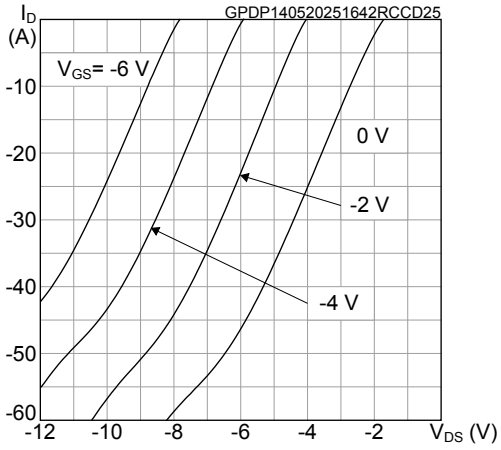


Figure 16. Typical diode reverse conduction characteristics (T_J = 125 °C)

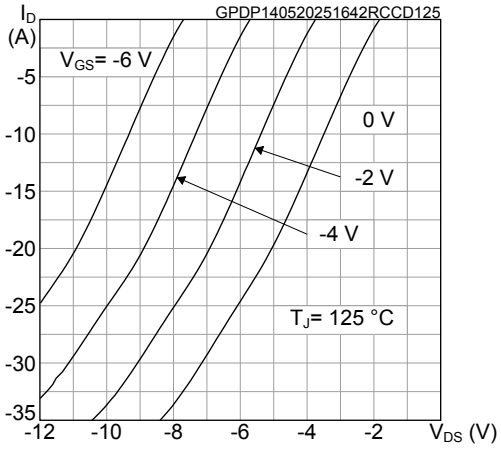


Figure 17. Typical reverse conduction characteristics (T_J = 25 °C)

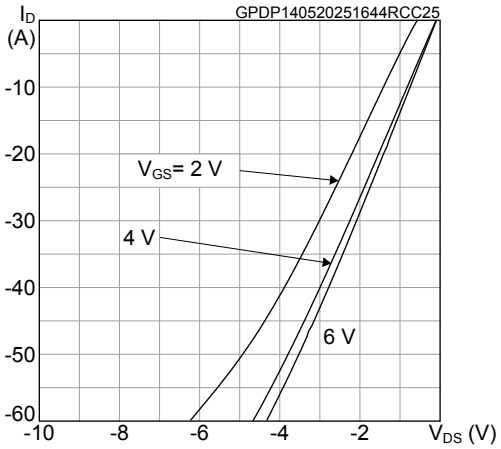


Figure 18. Typical reverse conduction characteristics (T_J = 125 °C)

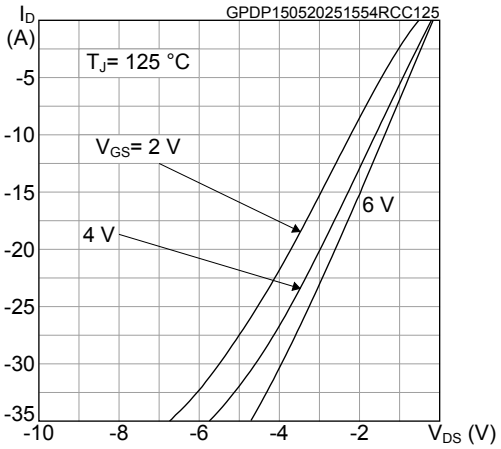
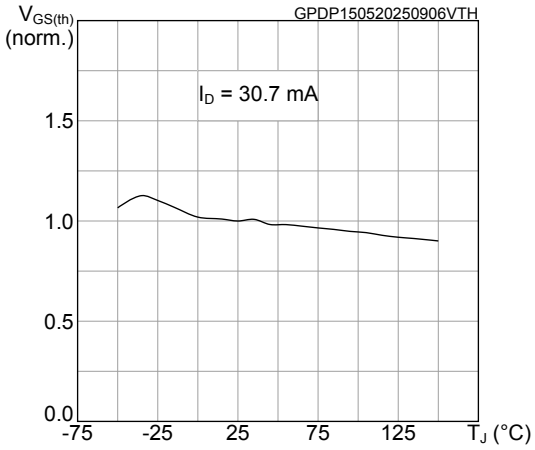


Figure 19. Normalized gate threshold vs temperature



3 Test circuits

Figure 20. Test circuit for inductive load switching times

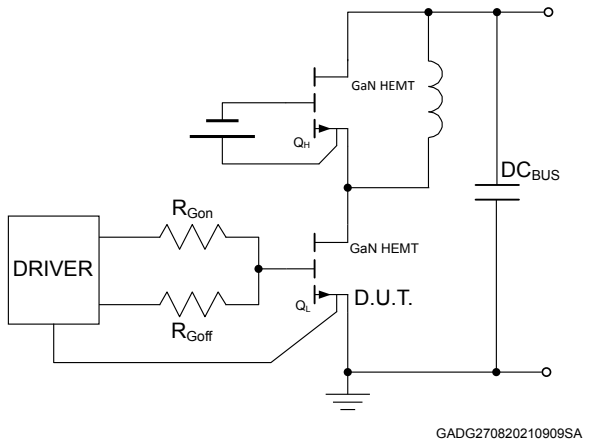
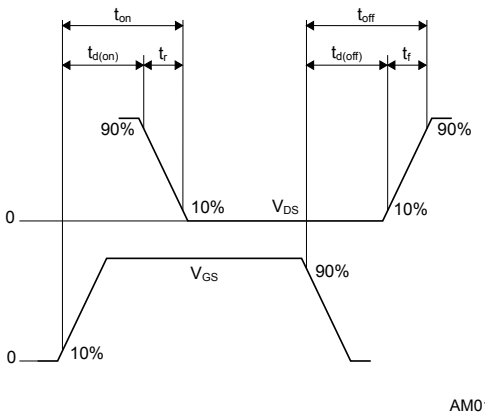


Figure 21. Switching time waveforms

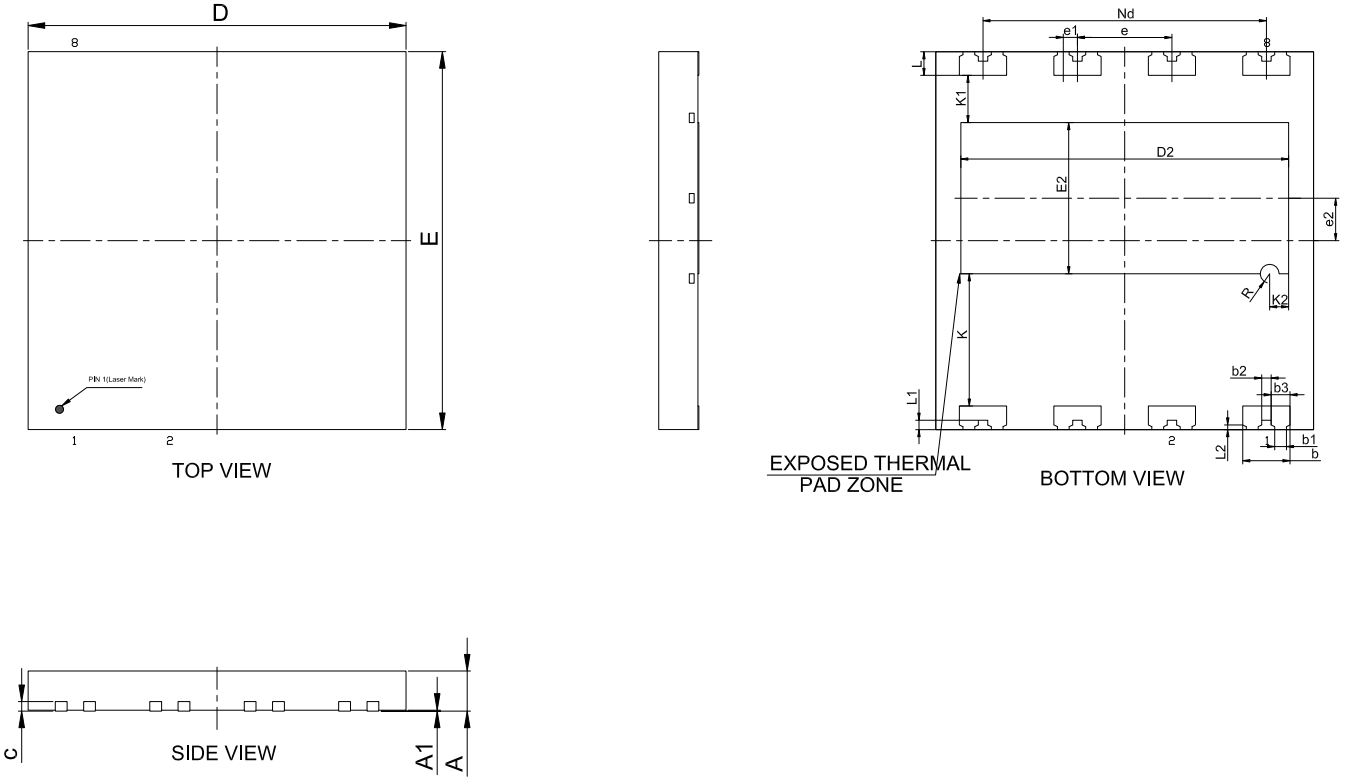


4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 8x8 HV for PowerGaN package information

Figure 22. PowerFLAT 8x8 HV for PowerGaN package outline

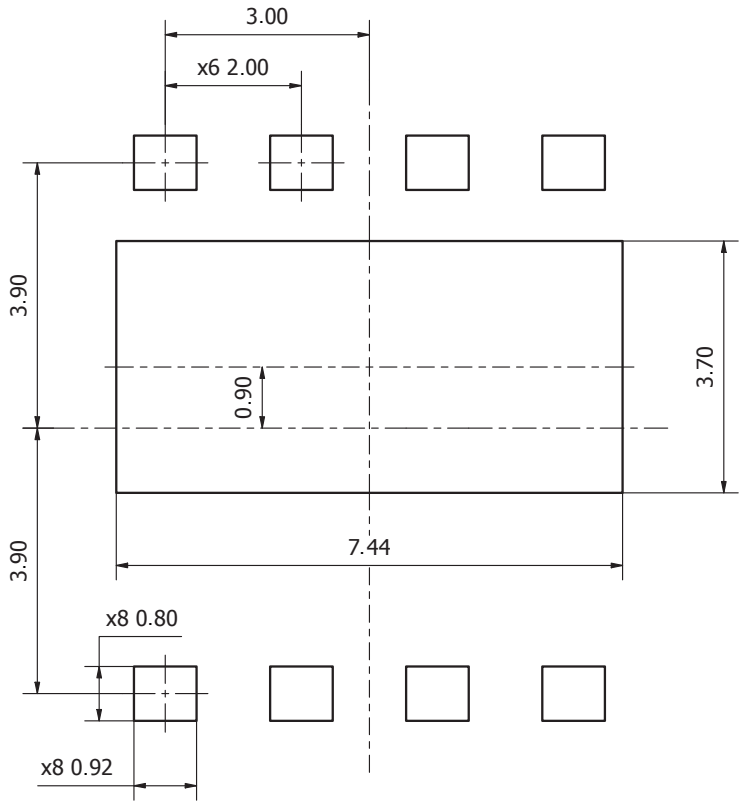


DM001104683_rev.2_PowerGaN

Table 7. **PowerFLAT 8x8 HV for PowerGaN mechanical data**

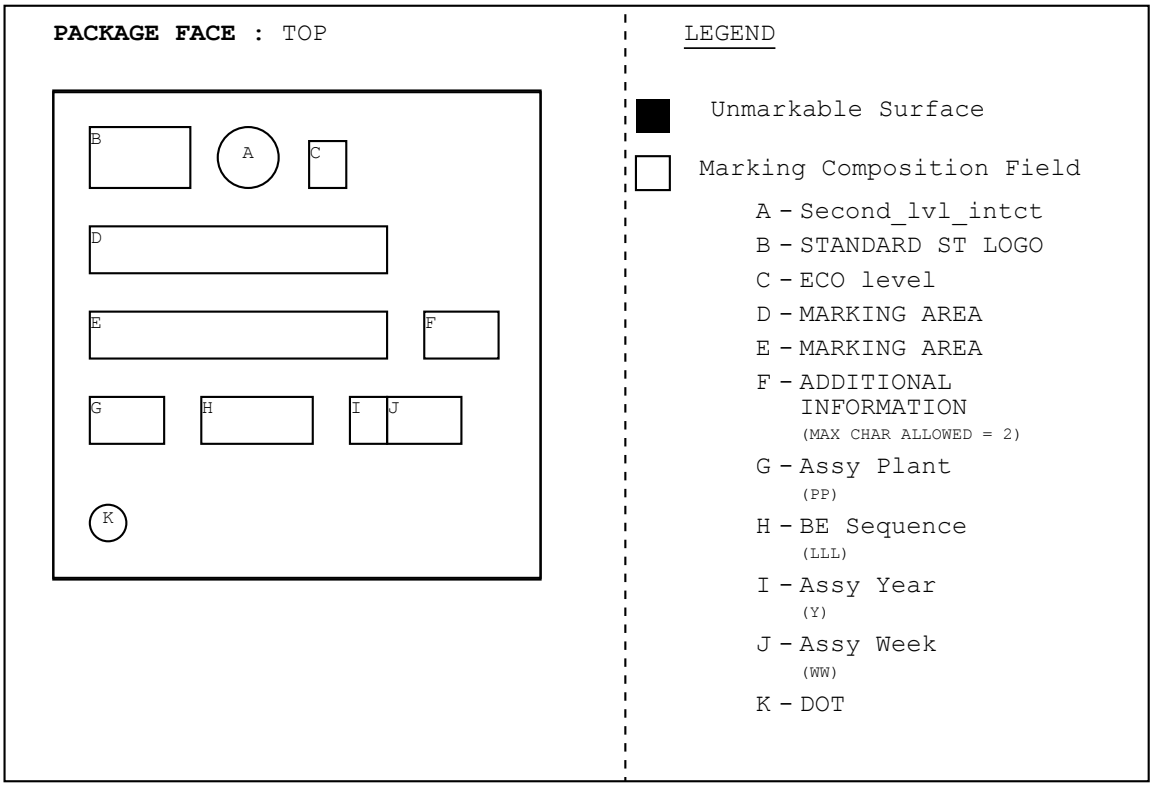
Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
b1		0.25 REF	
b2		0.20 REF	
b3	0.35	0.40	0.45
c		0.203 REF	
D	7.90	8.00	8.10
D2	6.84	6.94	7.04
Nd		6.00 BSC	
e		2.00 BSC	
e1		0.30 BSC	
e2		0.90 BSC	
E	7.90	8.00	8.10
E2	3.10	3.20	3.30
L	0.45	0.50	0.55
L1		0.20 REF	
L2		0.10 REF	
K		2.80 REF	
K1		1.00 REF	
K2		0.40 REF	
R		0.20 REF	

Figure 23. **PowerFLAT 8x8 HV for PowerGaN recommended footprint (dimensions are in mm)**



DM001104683_rev.2_PowerGaN_footprint

Figure 24. **Marking composition for PowerFLAT 8x8 HV for PowerGaN**



DM01133839_rev.1

Engineering samples

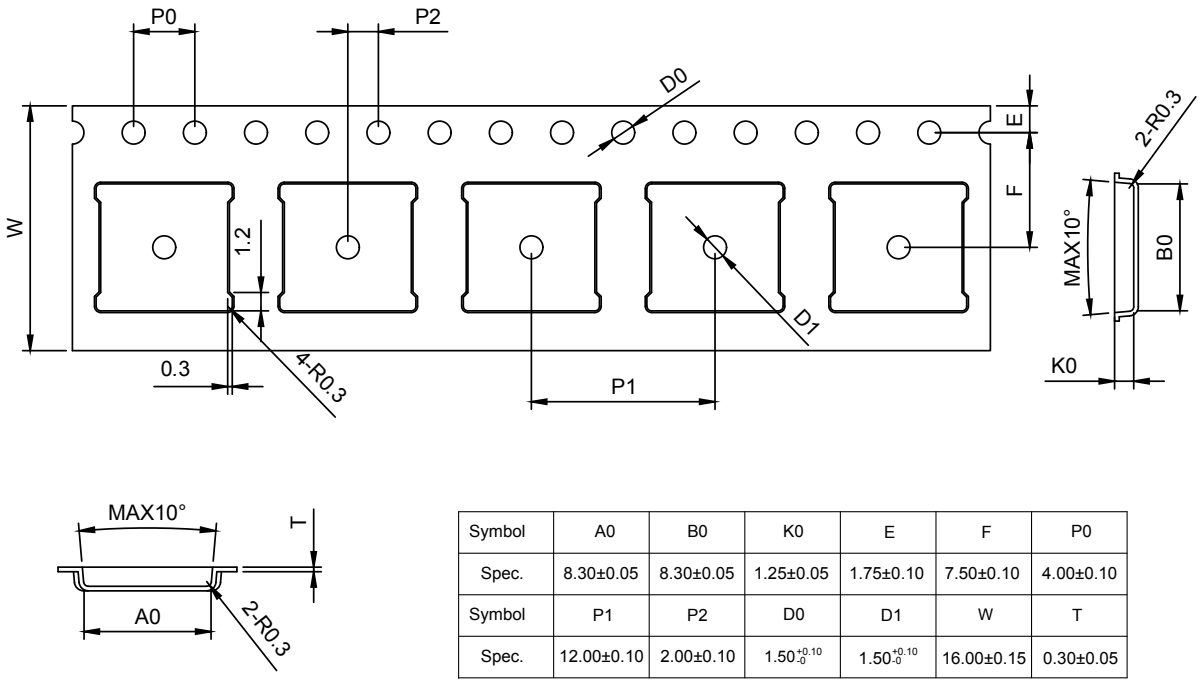
These samples are clearly identified by “ES” digits in the marking additional information field of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial samples

Fully qualified parts from ST standard production with no limitations of use or special identification marking.

4.2 PowerFLAT 8x8 HV for PowerGaN packing information

Figure 25. **PowerFLAT 8x8 HV for PowerGaN tape (dimensions are in mm)**



Symbol	A0	B0	K0	E	F	P0
Spec.	8.30±0.05	8.30±0.05	1.25±0.05	1.75±0.10	7.50±0.10	4.00±0.10
Symbol	P1	P2	D0	D1	W	T
Spec.	12.00±0.10	2.00±0.10	$1.50^{+0.10}_{-0}$	$1.50^{+0.10}_{-0}$	16.00±0.15	0.30±0.05

Tape_PowerFLAT 8x8 HV for PowerGaN

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
19-May-2025	1	First release.
29-May-2025	2	Updated Figure 5. Typical output characteristics (T_J = 25 °C).