# TLVx316-Q1
# 10-MHz, Rail-to-Rail Input/Output, Low-Voltage, 1.8-V CMOS Operational Amplifiers

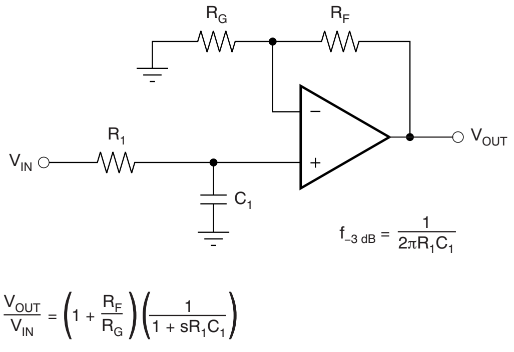
## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C5
- Unity-Gain Bandwidth: 10 MHz
- Low $I_Q$: 400 µA/ch
  - Excellent Power-to-Bandwidth Ratio
  - Stable $I_Q$ Over Temperature and Supply Range
- Wide Supply Range: 1.8 V to 5.5 V
- Low Noise: 12 nV/√Hz at 1 kHz
- Low Input Bias Current: ±10 pA
- Offset Voltage: ±0.75 mV
- Unity-Gain Stable
- Internal RFI and EMI Filter
- Number of Channels:
  - TLV316-Q1: 1
  - TLV2316-Q1: 2
  - TLV4316-Q1: 4
- Extended Temperature Range: –40°C to +125°C

## 2 Applications

- Automotive Applications:
  - ADAS
  - Body Electronics and Lighting
  - Current Sensing
  - Battery Management Systems

### Single-Pole, Low-Pass Filter



$$f_{-3\ dB} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

## 3 Description

The TLV316-Q1 (single), TLV2316-Q1 (dual), and TLV4316-Q1 (quad) devices comprise a family of general-purpose, low-power operational amplifiers. Features such as rail-to-rail input and output swings, low quiescent current (400 µA/ch typical) combined with a wide bandwidth of 10 MHz, and very-low noise (12 nV/√Hz at 1 kHz) make this family suitable for a circuits requiring a good speed and power ratio. The low input bias current supports operational amplifiers that are used in applications with megaohm source impedances. The low-input bias current of the TLVx316-Q1 yields a very-low current noise to make the family attractive for high impedance sensor interfaces.

The robust design of the TLVx316-Q1 provides ease-of-use to the circuit designer: a unity-gain stable, integrated RFI and EMI rejection filter, no phase reversal in overdrive condition, and high electrostatic discharge (ESD) protection (4-kV HBM).

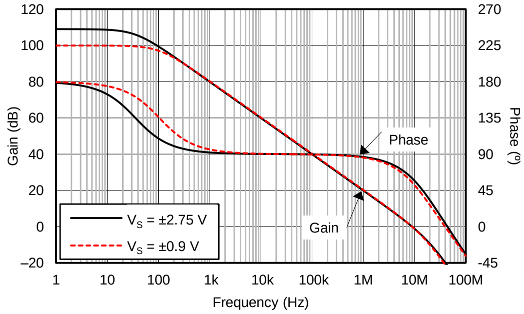
These devices are optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V). This latest addition of low-voltage CMOS operational amplifiers to the portfolio, in conjunction with the TLVx313-Q1 and TLVx314-Q1 series, offer a family of bandwidth, noise, and power options to meet the needs of a wide variety of applications.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLV316-Q1 | SOT-23 (5) | 1.60 mm × 2.90 mm |
| TLV2316-Q1 | VSSOP (8) | 3.00 mm × 3.00 mm |
| TLV4316-Q1 | TSSOP (14) | 4.40 mm × 5.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Low Supply Current (400 µA/Ch) for 10-MHz Bandwidth



# Table of Contents

## 4 Revision History

### Changes from Revision A (December 2016) to Revision B — Page

- Corrected typo; changed part numbers from TLV314, TLV2314, and TLV4314 to TLV316-Q1, TLV2316-Q1, and TLV4316-Q1 in *Features* section ... 1
- Changed values in the *Thermal Information: TLV4316-Q1* table to align with JEDEC standards. ... 8

### Changes from Original (November 2016) to Revision A — Page

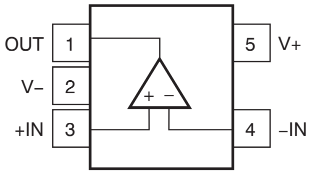
- Changed the CDM ESD Classification Level from C6 to C5 in the *Features* section ... 1
- Deleted the SC70 (5), SOIC (8), and SOIC (14) packages from the *Device Information* table ... 1
- Deleted the DCK (SC70) package from the TLV316-Q1 pinout diagram in the *Pin Configurations and Functions* section ... 4
- Deleted the DCK (SC70) pinout information from the *Pin Functions: TLV316-Q1* table in the *Pin Configurations and Functions* section ... 4
- Deleted D (SOIC) package from the TLV2316-Q1 pinout diagram in the *Pin Configurations and Functions* section ... 5
- Deleted the D (SOIC) package from TLV4316-Q1 pinout diagram in the *Pin Configurations and Functions* section ... 6
- Changed the *ESD Ratings* table from commercial to automotive specifications ... 7
- Changed the CDM ESD rating from ±1500 to ±750 in the *ESD Ratings* table ... 7
- Deleted the DCK (SC70) package from the *Thermal Information: TLV316-Q1* table in the *Specifications* section ... 8
- Changed the formatting of all *Thermal Information* table notes ... 8
- Deleted the D (SOIC) package from the *Thermal Information: TLV2316-Q1* table in the *Specifications* section ... 8
- Deleted the D (SOIC) package from the *Thermal Information: TLV4316-Q1* table in the *Specifications* section ... 8
- Deleted the static literature number in the SBOA128 application note reference in the *EMI Susceptibility and Input Filtering* section ... 16
- Deleted the static literature number in document reference in the *Layout Guidelines* section ... 19
- Changed the layout example image (Figure 41) in *Layout Example* section ... 19
- Deleted the static literature numbers from document references in *Related Documentation* section ... 20

# 5 Device Comparison Table

| DEVICE | NO. OF CHANNELS | PACKAGE-LEADS | | | | |
|---|---|---|---|---|---|---|
| | | DBV | DCK | D | DGK | PW |
| TLV316-Q1 | 1 | 5 | 5 | — | — | — |
| TLV2316-Q1 | 2 | — | — | 8 | 8 | — |
| TLV4316-Q1 | 4 | — | — | 14 | — | 14 |

# 6 Pin Configuration and Functions

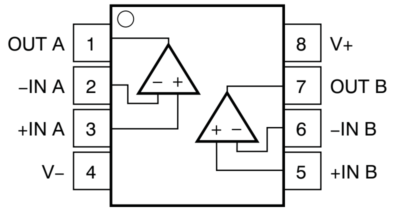
**TLV316-Q1 DBV Package**
**5-Pin SOT-23**
**Top View**



## Pin Functions: TLV316-Q1

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN | 4 | I | Inverting input |
| +IN | 3 | I | Noninverting input |
| OUT | 1 | O | Output |
| V– | 2 | — | Negative (lowest) supply or ground (for single-supply operation) |
| V+ | 5 | — | Positive (highest) supply |

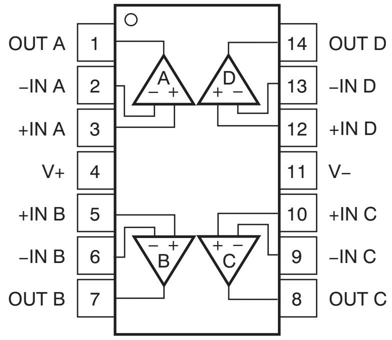
**TLV2316-Q1 DGK Package**
**8-Pin VSSOP**
**Top View**



## Pin Functions: TLV2316 -Q1

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN A | 2 | I | Inverting input, channel A |
| +IN A | 3 | I | Noninverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| +IN B | 5 | I | Noninverting input, channel B |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| V– | 4 | — | Negative (lowest) supply or ground (for single-supply operation) |
| V+ | 8 | — | Positive (highest) supply |

**TLV4316-Q1 PW Package**
**14-Pin TSSOP**
**Top View**



## Pin Functions: TLV4316-Q1

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN A | 2 | I | Inverting input, channel A |
| +IN A | 3 | I | Noninverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| +IN B | 5 | I | Noninverting input, channel B |
| –IN C | 9 | I | Inverting input, channel C |
| +IN C | 10 | I | Noninverting input, channel C |
| –IN D | 13 | I | Inverting input, channel D |
| +IN D | 12 | I | Noninverting input, channel D |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| OUT C | 8 | O | Output, channel C |
| OUT D | 14 | O | Output, channel D |
| V– | 11 | — | Negative (lowest) supply or ground (for single-supply operation) |
| V+ | 4 | — | Positive (highest) supply |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage | | | | 7 | V |
| Signal input pins | Voltage(2) | Common-mode | (V–) – 0.5 | (V+) + 0.5 | V |
| | | Differential | | (V+) – (V–) + 0.2 | |
| | Current(2) | | –10 | 10 | mA |
| Output short-circuit(3) | | | Continuous | | mA |
| Temperature | Specified, $T_A$ | | –40 | 125 | °C |
| | Junction, $T_J$ | | | 150 | |
| | Storage, $T_{stg}$ | | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±4000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_S$ | Supply voltage | 1.8 | | 5.5 | V |
| | Specified temperature range | –40 | | 125 | °C |

## 7.4 Thermal Information: TLV316-Q1

| THERMAL METRIC[1] | | TLV316-Q1<br>DBV (SOT-23)<br>5 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 221.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 144.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 26.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 49.0 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Thermal Information: TLV2316-Q1

| THERMAL METRIC[1] | | TLV2316-Q1<br>DGK (VSSOP)<br>8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 186.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 78.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 107.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 15.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 106.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.6 Thermal Information: TLV4316-Q1

| THERMAL METRIC[1] | | TLV4316-Q1<br>PW (TSSOP)<br>14 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 117.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 46.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 59.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 5.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 59 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.7 Electrical Characteristics

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted); $V_S$ (total supply voltage) = (V+) – (V–) = 1.8 V to 5.5 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | $V_S$ = 5 V | | ±0.75 | ±3 | mV |
| | | $V_S$ = 5 V, $T_A$ = –40°C to 125°C | | | ±4.5 | |
| $dV_{OS}/dT$ | Drift | $V_S$ = 5 V, $T_A$ = –40°C to 125°C | | ±2 | | µV/°C |
| PSRR | Power-supply rejection ratio | $V_S$ = 1.8 V – 5.5 V, $V_{CM}$ = (V–) | | ±30 | ±175 | µV/V |
| | Channel separation, dc | At dc | | 100 | | dB |
| **INPUT VOLTAGE RANGE** | | | | | | |
| $V_{CM}$ | Common-mode voltage range | $V_S$ = 5.5 V | (V–) – 0.2 | | (V+) + 0.2 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = 5.5 V, (V–) – 0.2 V < $V_{CM}$ < (V+) – 1.4 V, $T_A$ = –40°C to 125°C | 72 | 90 | | dB |
| | | $V_S$ = 5.5 V, $V_{CM}$ = –0.2 V to 5.7 V, $T_A$ = –40°C to 125°C | | 75 | | |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | | | ±10 | | pA |
| $I_{OS}$ | Input offset current | | | ±10 | | pA |
| **NOISE** | | | | | | |
| $E_n$ | Input voltage noise (peak-to-peak) | $V_S$ = 5 V, f = 0.1 Hz to 10 Hz | | 5 | | $\mu V_{PP}$ |
| $e_n$ | Input voltage noise density | $V_S$ = 5 V, f = 1 kHz | | 12 | | $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ |
| $i_n$ | Input current noise density | f = 1 kHz | | 1.3 | | $\mathrm{fA}/\sqrt{\mathrm{Hz}}$ |
| **INPUT IMPEDANCE** | | | | | | |
| $Z_{ID}$ | Differential | | | 2 \|\| 2 | | $10^{16}\Omega$ \|\| pF |
| $Z_{IC}$ | Common-mode | | | 2 \|\| 4 | | $10^{11}\Omega$ \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $V_S$ = 5.5 V, (V–) + 0.05 V < $V_O$ < (V+) – 0.05 V, $R_L$ = 10 kΩ | 100 | 104 | | dB |
| | | $V_S$ = 5.5 V, (V–) + 0.15 V < $V_O$ < (V+) – 0.15 V, $R_L$ = 2 kΩ | | 104 | | |
| **FREQUENCY RESPONSE** | | | | | | |
| GBP | Gain bandwidth product | $V_S$ = 5 V, G = 1 | | 10 | | MHz |
| $\varphi_m$ | Phase margin | $V_S$ = 5 V, G = 1 | | 60 | | Degrees |
| SR | Slew rate | $V_S$ = 5 V, G = 1 | | 6 | | V/µs |
| $t_S$ | Settling time | To 0.1%, $V_S$ = 5 V, 2-V step , G = 1, $C_L$ = 100 pF | | 1 | | µs |
| $t_{OR}$ | Overload recovery time | $V_S$ = 5 V, $V_{IN}$ × gain = $V_S$ | | 0.8 | | µs |
| THD + N | Total harmonic distortion + noise(1) | $V_S$ = 5 V, $V_O$ = 0.5 $V_{RMS}$, G = 1, f = 1 kHz | | 0.008% | | |
| **OUTPUT** | | | | | | |
| $V_O$ | Voltage output swing from supply rails | $V_S$ = 1.8 V to 5.5 V, $R_L$ = 10 kΩ | | | 35 | mV |
| | | $V_S$ = 1.8 to 5.5 V, $R_L$ = 2 kΩ | | | 125 | |
| $I_{SC}$ | Short-circuit current | $V_S$ = 5 V | | ±50 | | mA |
| $Z_O$ | Open-loop output impedance | $V_S$ = 5 V, f = 10 MHz | | 250 | | Ω |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Specified voltage range | | 1.8 | | 5.5 | V |
| $I_Q$ | Quiescent current per amplifier | $V_S$ = 5 V, $I_O$ = 0 mA, $T_A$ = –40°C to 125°C | | 400 | 575 | µA |
| **TEMPERATURE** | | | | | | |
| $T_A$ | Specified | | –40 | | 125 | °C |
| $T_{stg}$ | Storage | | –65 | | 150 | °C |

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

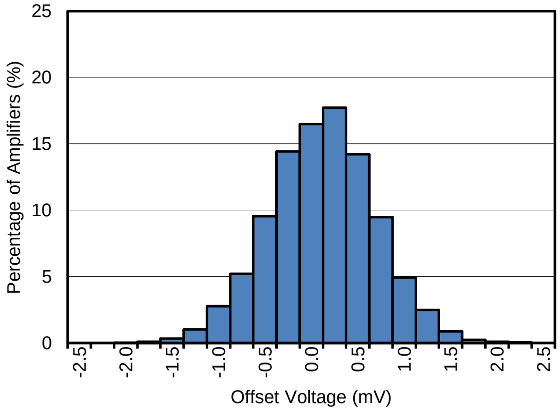
## 7.8 Typical Characteristics: Table of Graphs

### Table 1. Table of Graphs

| TITLE | FIGURE |
|---|---|
| Offset Voltage Production Distribution | Figure 1 |
| Offset Voltage vs Common-Mode Voltage | Figure 2 |
| Open- Loop Gain and Phase vs Frequency | Figure 3 |
| Input Bias and Offset Current vs Temperature | Figure 4 |
| Input Voltage Noise Spectral Density vs Frequency | Figure 5 |
| Quiescent Current vs Supply Voltage | Figure 6 |
| Small-Signal Overshoot vs Load Capacitance | Figure 7 |
| No Phase Reversal | Figure 8 |
| Small-Signal Step Response | Figure 9 |
| Large-Signal Step Response | Figure 10 |
| Short-Circuit Current vs Temperature | Figure 11 |
| Electromagnetic Interference Rejection Ratio Referred to Noninverting Input vs Frequency | Figure 12 |
| Channel Separation vs Frequency | Figure 13 |

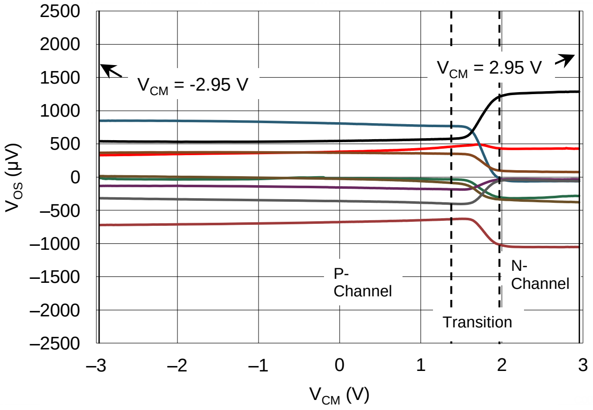
## 7.9 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = 5.5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2, (unless otherwise noted)



Distribution taken from 12551 amplifiers

**Figure 1. Offset Voltage Production Distribution**

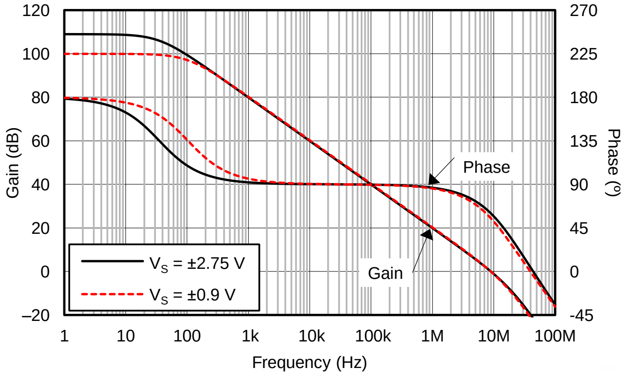


V+ = 2.75 V

V– = –2.75 V

9 typical units shown

**Figure 2. Offset Voltage vs Common-Mode Voltage**



$V_{CM}$ < (V+) – 1.4 V

**Figure 3. Open-Loop Gain and Phase vs Frequency**

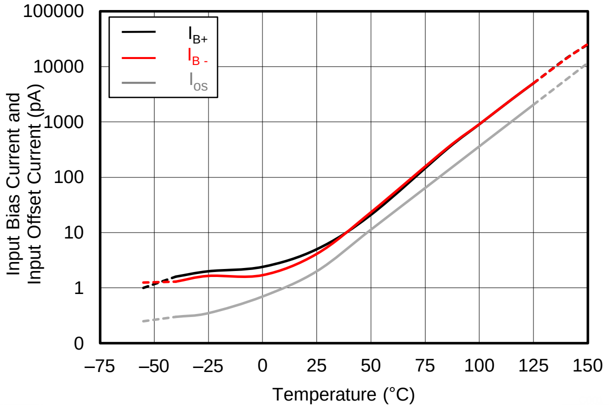


**Figure 4. Input Bias and Offset Current vs Temperature**

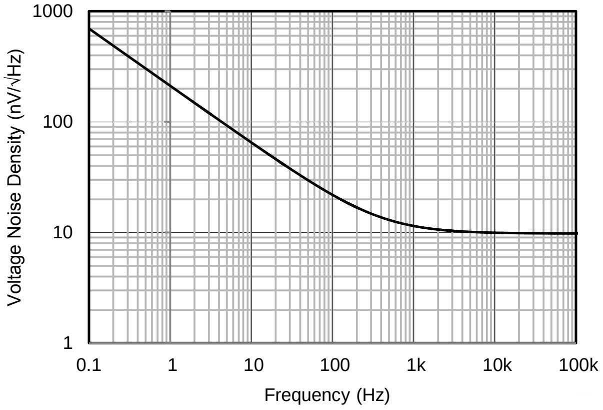


**Figure 5. Input Voltage Noise Spectral Density vs Frequency**

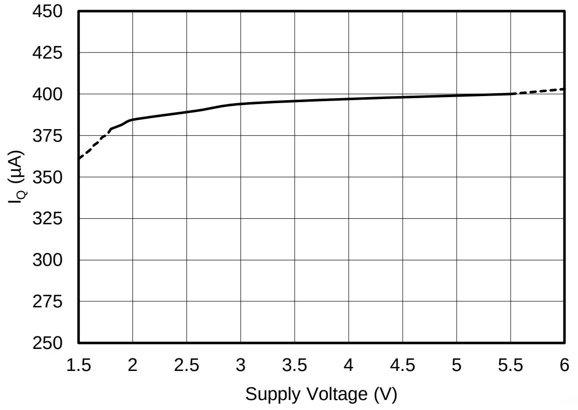
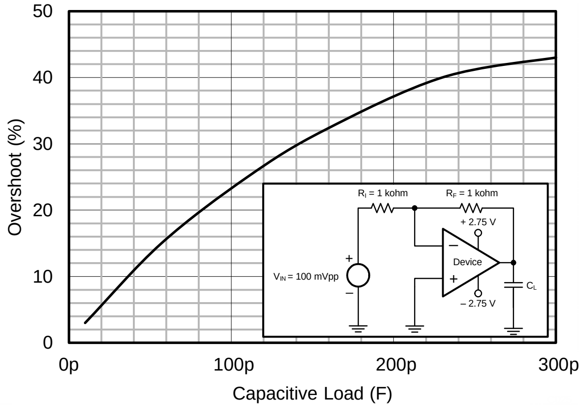


**Figure 6. Quiescent Current vs Supply Voltage**

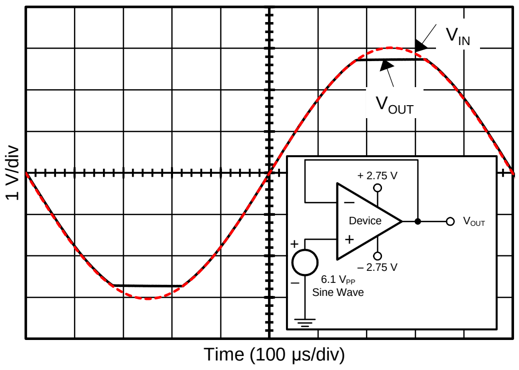
## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5.5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2, (unless otherwise noted)



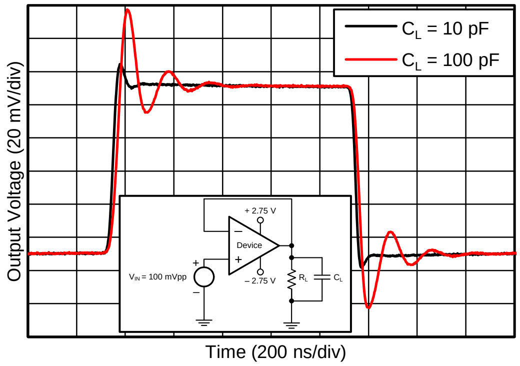
V+ = 2.75 V, V– = –2.75 V, G = –1 V/V

**Figure 7. Small-Signal Overshoot vs Load Capacitance**



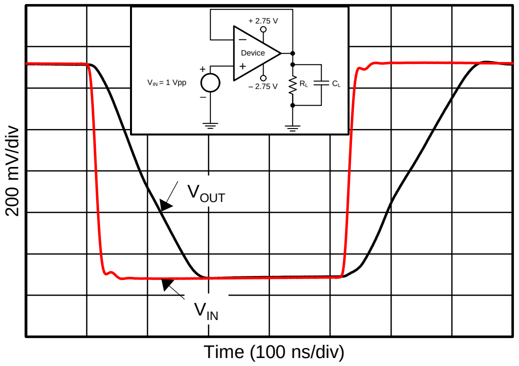
V+ = 2.75 V, V– = –2.75 V

**Figure 8. No Phase Reversal**



V+ = 2.75 V, V– = –2.75 V, G = 1 V/V

**Figure 9. Small-Signal Step Response**



V+ = 2.75 V, V– = –2.75 V, $C_L$ = 100 pF, G = 1 V/V

**Figure 10. Large-Signal Step Response**

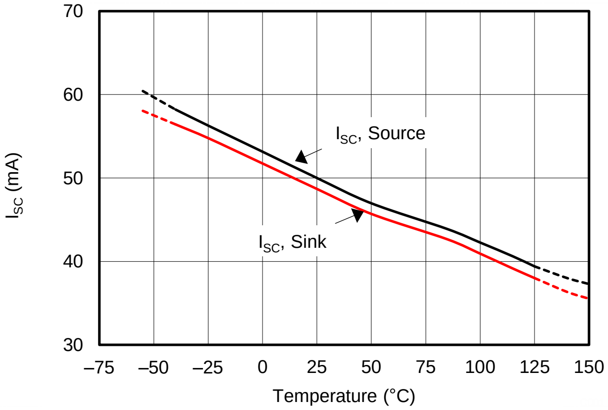
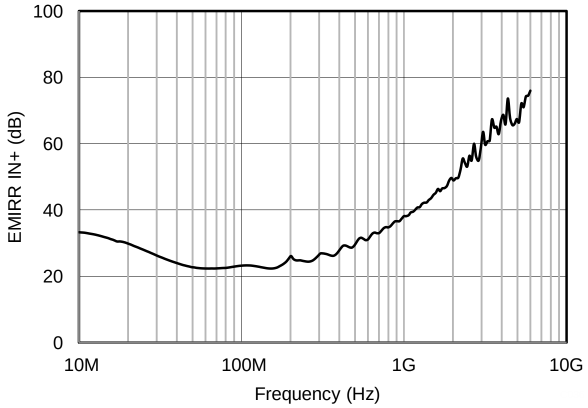


**Figure 11. Short-Circuit Current vs Temperature**



$P_{RF}$ = –10 dBm

**Figure 12. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input vs Frequency**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5.5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2, (unless otherwise noted)

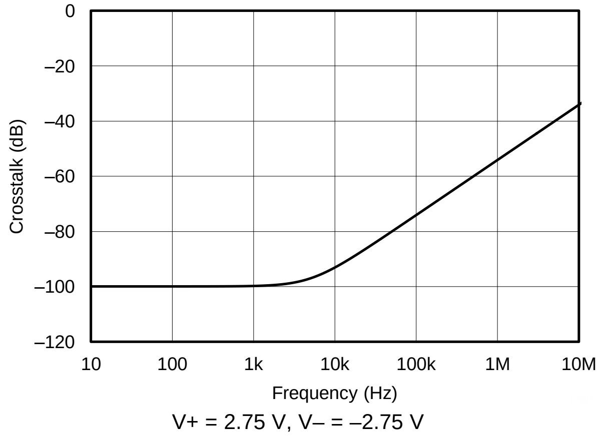


**Figure 13. Channel Separation vs Frequency**

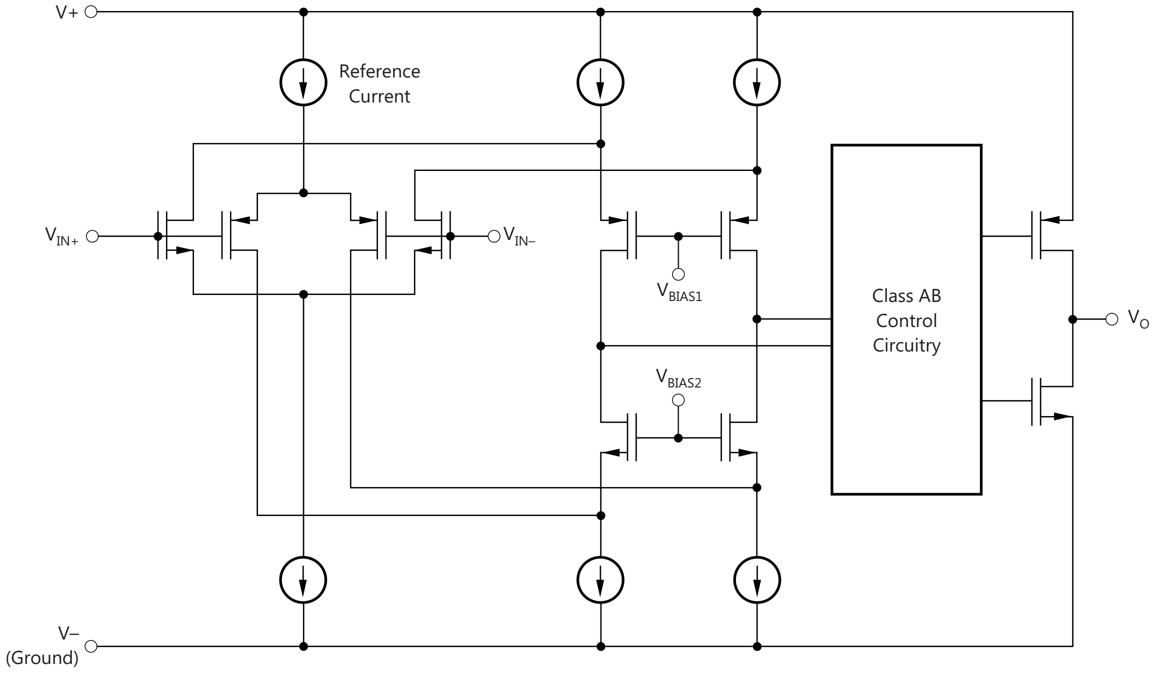
# 8 Detailed Description

## 8.1 Overview

The TLVx316-Q1 is a family of low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails and allows the TLVx316-Q1 to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them suitable for driving sampling analog-to-digital converters (ADCs).

The TLVx316-Q1 features 10-MHz bandwidth and 6-V/µs slew rate with only 400-µA supply current per channel, providing good ac performance at very-low-power consumption. DC applications are well served with a very-low input noise voltage of 12 nV/$\sqrt{\text{Hz}}$ at 1 kHz, low input bias current (5 pA), and an input offset voltage of 0.5 mV (typical).

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Operating Voltage

The TLVx316-Q1 operational amplifiers are fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the *Typical Characteristics* section.

### 8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLVx316-Q1 extends 200 mV beyond the supply rails for supply voltages greater than 2.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

### 8.3.3 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLVx316-Q1 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings typically to within 30 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; see .

### 8.3.4 Common-Mode Rejection Ratio (CMRR)

CMRR for the TLVx316-Q1 is specified in two ways so the best match for a given application can be selected. The *Electrical Characteristics* table provides the CMRR of the device in the common-mode range below the transition region [$V_{CM}$ < (V+) – 1.4 V]. This specification is the best indicator of device capability when the application requires using one of the differential input pairs. The CMRR over the entire common-mode range is specified at $V_{CM}$ = –0.2 V to 5.7 V for $V_S$ = 5.5 V. This last value includes the variations through the transition region.

### 8.3.5 Capacitive Load and Stability

The TLVx316-Q1 is designed for applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the TLVx316-Q1 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when the capacitive loading increases. For a conservative best practice, designing for 25% overshoot (40° phase margin) provides improved stability over process variations. The equivalent series resistance (ESR) of some very-large capacitors ($C_L$ capacitors with a value greater than 1 μF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains, as shown in Figure 7 (G = –1 V/V).

## Feature Description (continued)

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10-Ω to 20-Ω) in series with the output, as shown in Figure 14. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

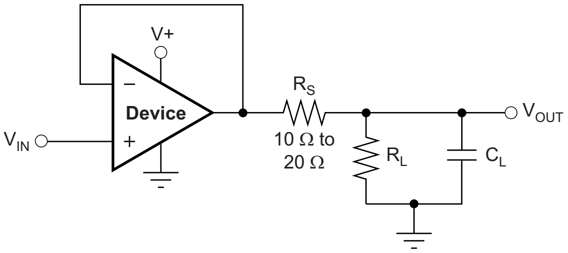


**Figure 14. Improving Capacitive Load Drive**

### 8.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset measured at the amplifier output can shift from the nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although EMI can affect all operational amplifier pin functions, the signal input pins are likely to be the most susceptible. The TLVx316-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. This filter provides both common-mode and differential-mode filtering. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

The immunity of an operational amplifier can be accurately measured and quantified over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows operational amplifiers to be directly compared by the EMI immunity. Figure 12 illustrates the results of this testing on the TLVx316-Q1. Detailed information can be found in *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

### 8.3.7 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLVx316-Q1 is approximately 300 ns.

## 8.4 Device Functional Modes

The TLVx316-Q1 family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

# 9 Application and Implementation

**NOTE**

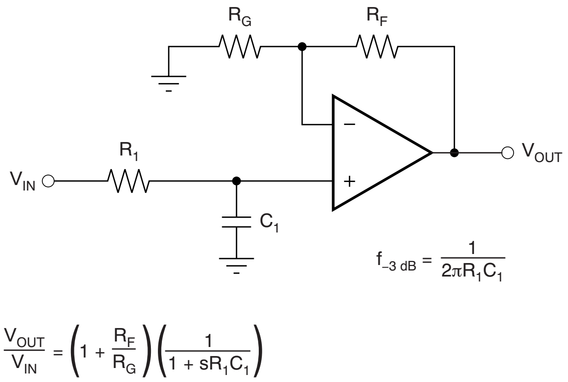
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TLV316-Q1, TLV2316-Q1, and TLV4316-Q1 devices are powered on when the supply is connected. The devices can operate as a single-supply operational amplifier or a dual-supply amplifier, depending on the application.

## 9.2 System Examples

When receiving low-level signals, the device often requires limiting the bandwidth of the incoming signals into the system. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting pin of the amplifier, as shown in Figure 15.

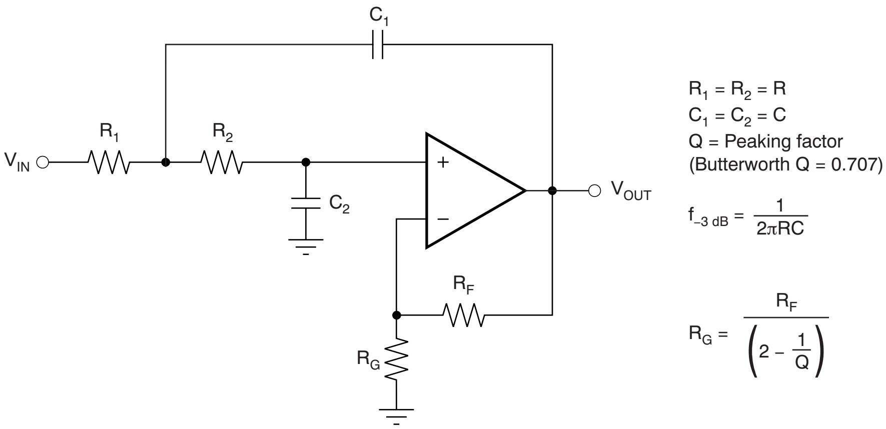


$$f_{-3\ dB} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

**Figure 15. Single-Pole, Low-Pass Filter**

If even more attenuation is needed, the device requires a multiple-pole filter. The Sallen-Key filter can be used for this task, as shown in Figure 16. For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in a phase shift of the amplifier.



$R_1 = R_2 = R$
$C_1 = C_2 = C$
Q = Peaking factor
(Butterworth Q = 0.707)

$$f_{-3\ dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

**Figure 16. Two-Pole, Low-Pass, Sallen-Key Filter**

# 10 Power Supply Recommendations

The TLVx316-Q1 family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

**CAUTION**

Supply voltages larger than 7 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

## 10.1 Input and ESD Protection

The TLVx316-Q1 incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as stated in the *Absolute Maximum Ratings* table. Figure 17 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

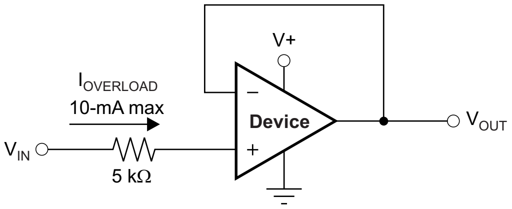


**Figure 17. Input Current Protection**

# 11 Layout

## 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping $R_F$ and $R_G$ close to the inverting input minimizes parasitic capacitance, as shown in Figure 18.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 11.2 Layout Example

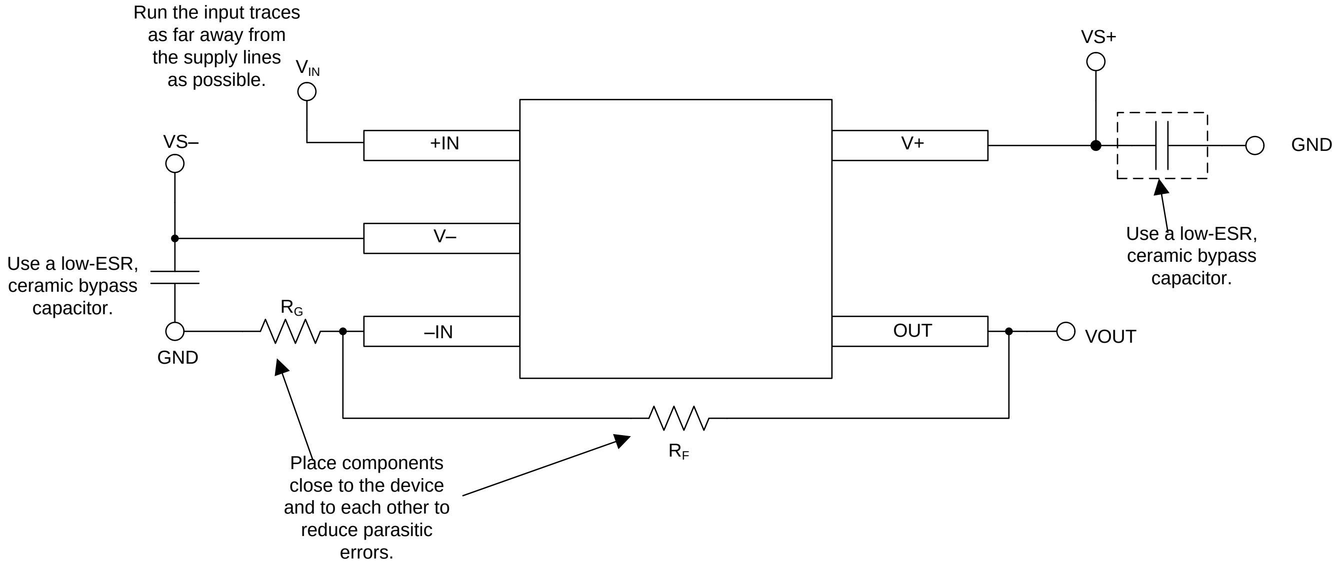


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**Figure 18. Operational Amplifier Board Layout for a Noninverting Configuration**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

*TLVx313 Low-Power, Rail-to-Rail In/Out, 500-μV Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems*

*TLVx314 3-MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier*

*EMI Rejection Ratio of Operational Amplifiers*

*QFN/SON PCB Attachment*

*Quad Flatpack No-Lead Logic Packages*

*Circuit Board Layout Techniques*

*Single-Ended Input to Differential Output Conversion Circuit Reference Design*

## 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TLV316-Q1 | Click here | Click here | Click here | Click here | Click here |
| TLV2316-Q1 | Click here | Click here | Click here | Click here | Click here |
| TLV4316-Q1 | Click here | Click here | Click here | Click here | Click here |

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.

### 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV2316QDGKRQ1 | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 16M6 |
| TLV2316QDGKTQ1 | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 16M6 |
| TLV316QDBVRQ1 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 16ND |
| TLV316QDBVTQ1 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 16ND |
| TLV4316QPWRQ1 | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | V4316Q1 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV2316-Q1, TLV316-Q1, TLV4316-Q1 :**

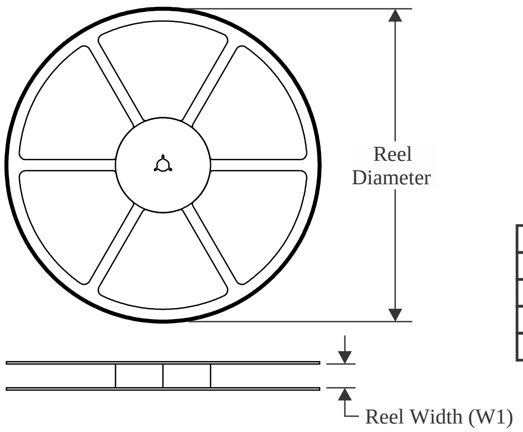
- Catalog : TLV2316, TLV316, TLV4316

NOTE: Qualified Version Definitions:

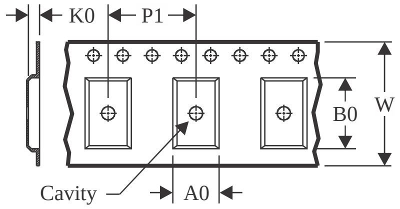
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

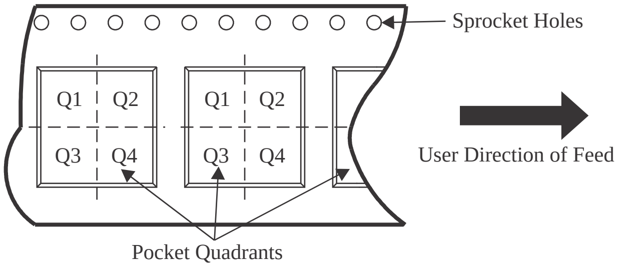


TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

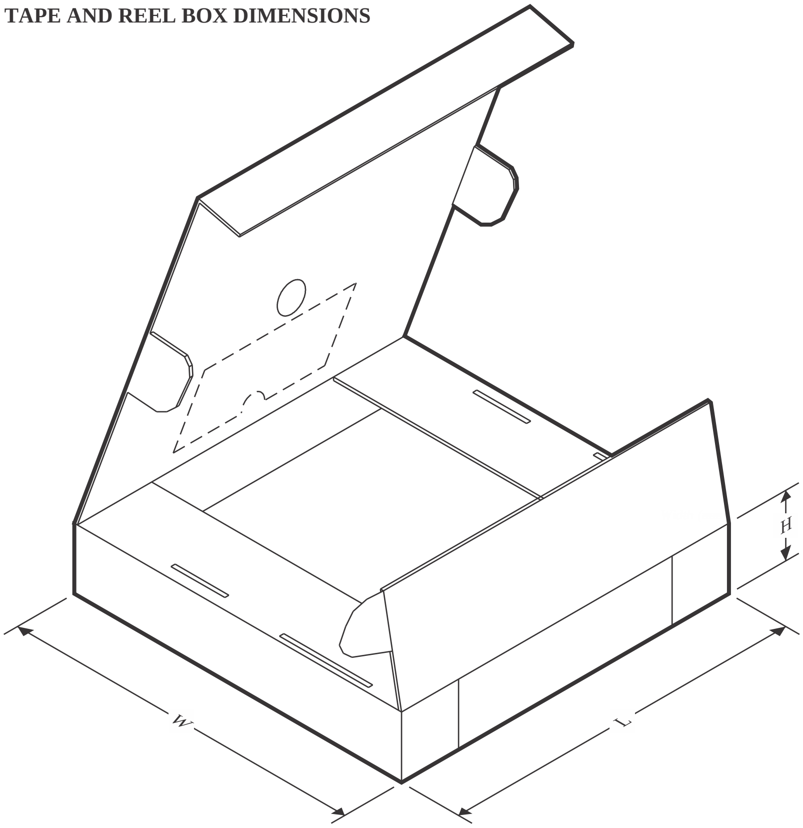
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2316QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2316QDGKTQ1 | VSSOP | DGK | 8 | 250 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV316QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV316QDBVTQ1 | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV4316QPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

### TAPE AND REEL BOX DIMENSIONS



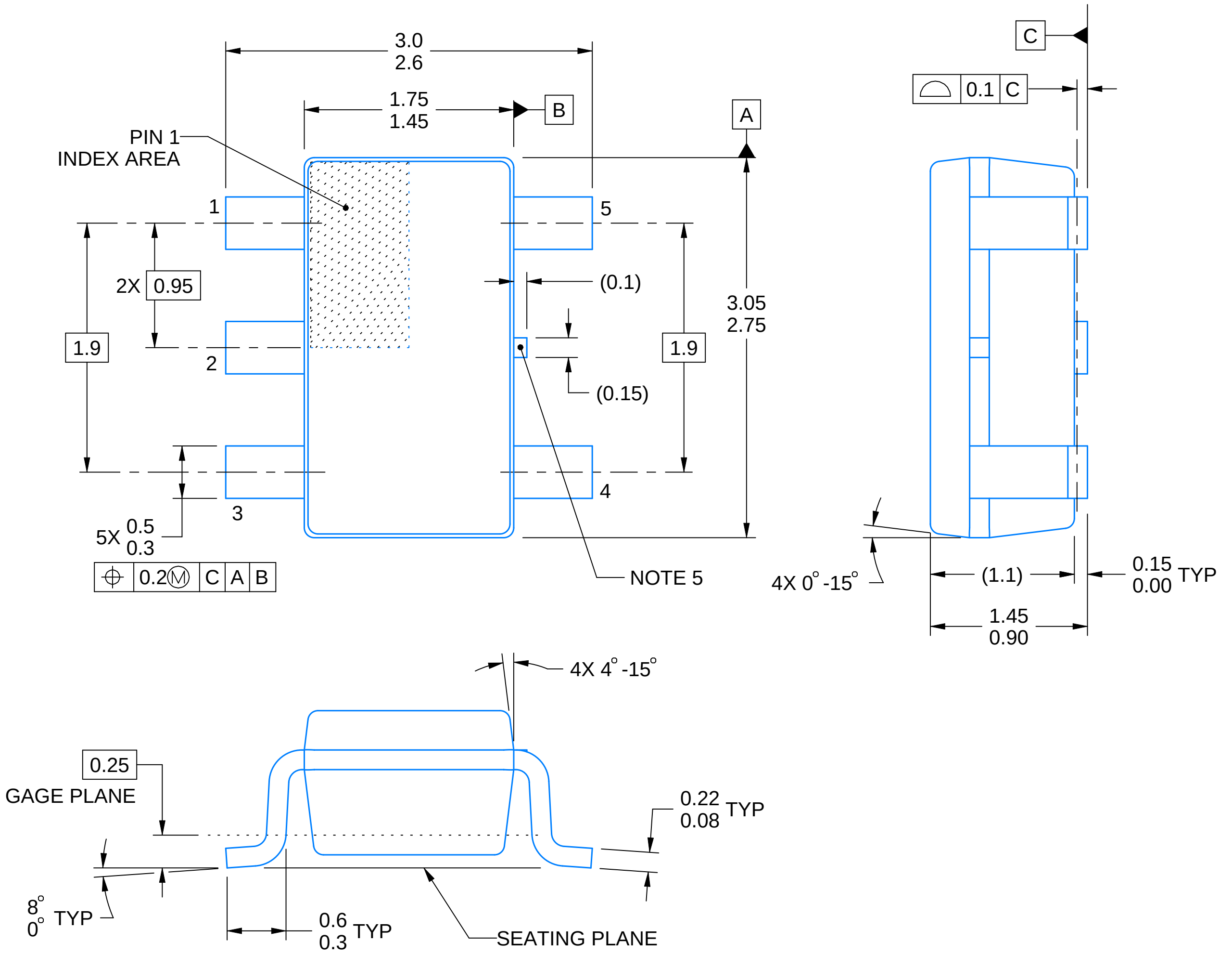
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV2316QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TLV2316QDGKTQ1 | VSSOP | DGK | 8 | 250 | 366.0 | 364.0 | 50.0 |
| TLV316QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV316QDBVTQ1 | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV4316QPWRQ1 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |

# PACKAGE OUTLINE

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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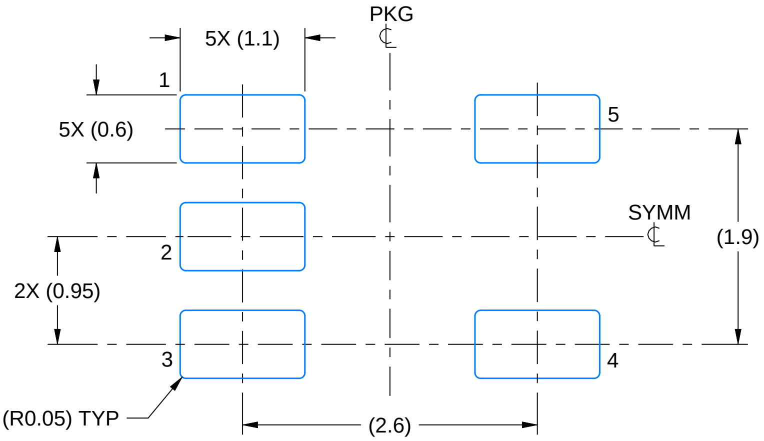
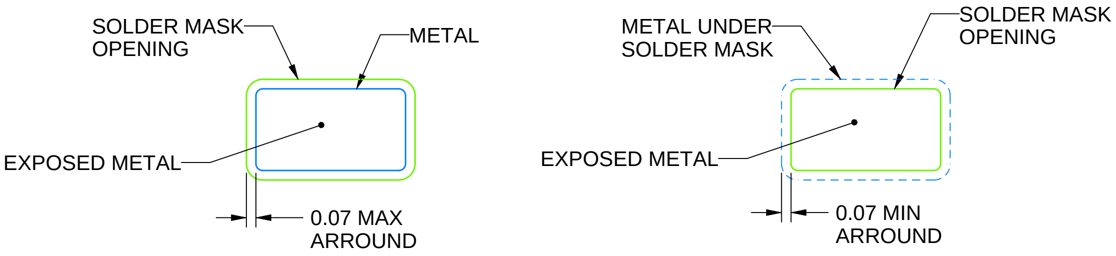
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



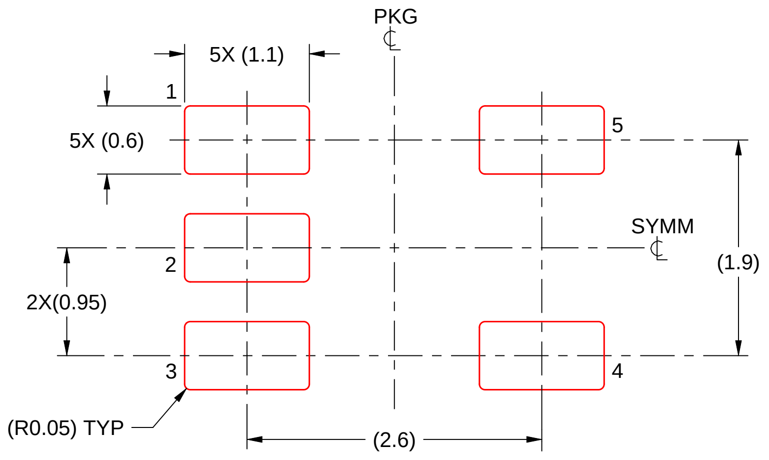
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

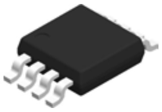


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

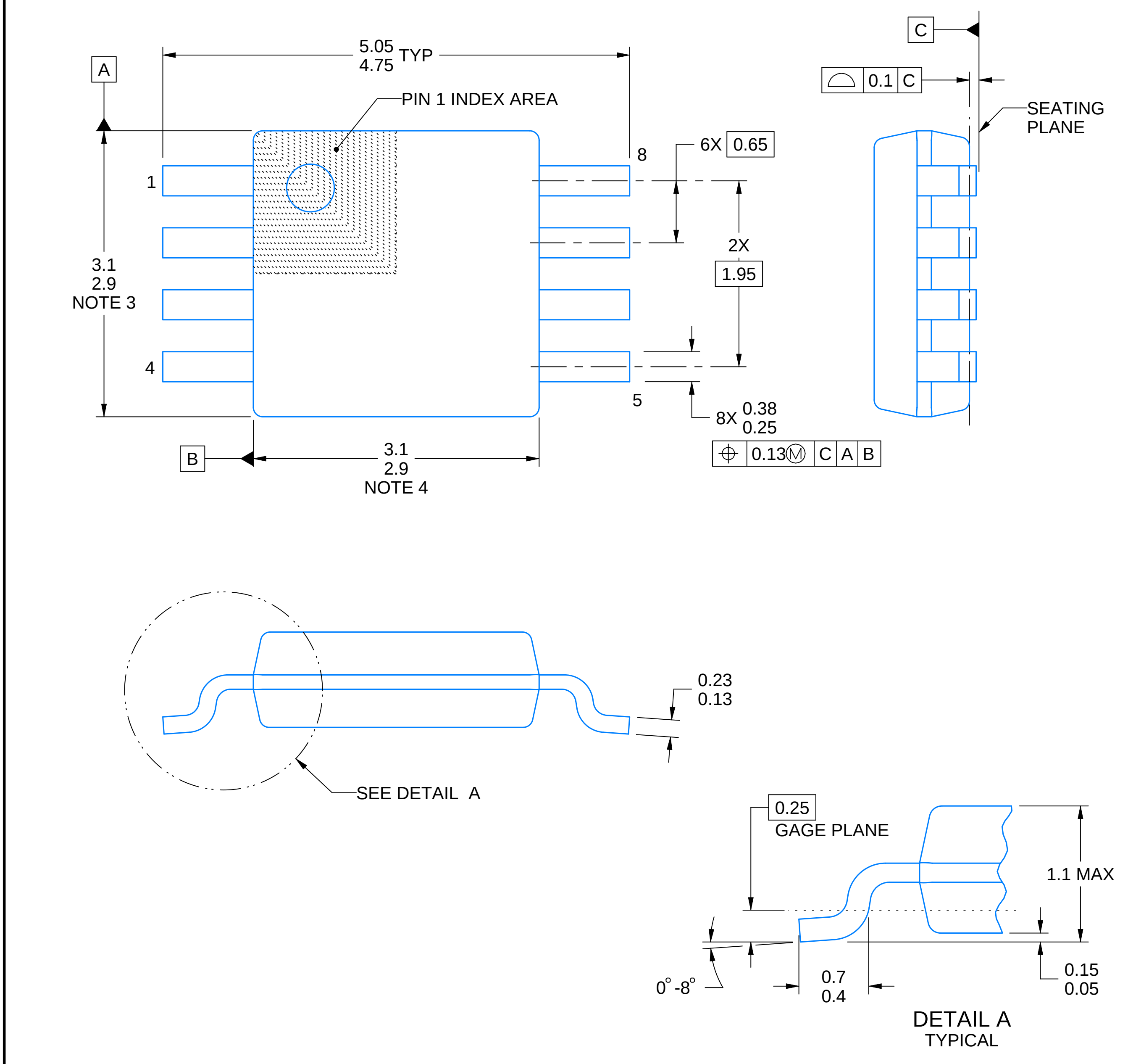
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

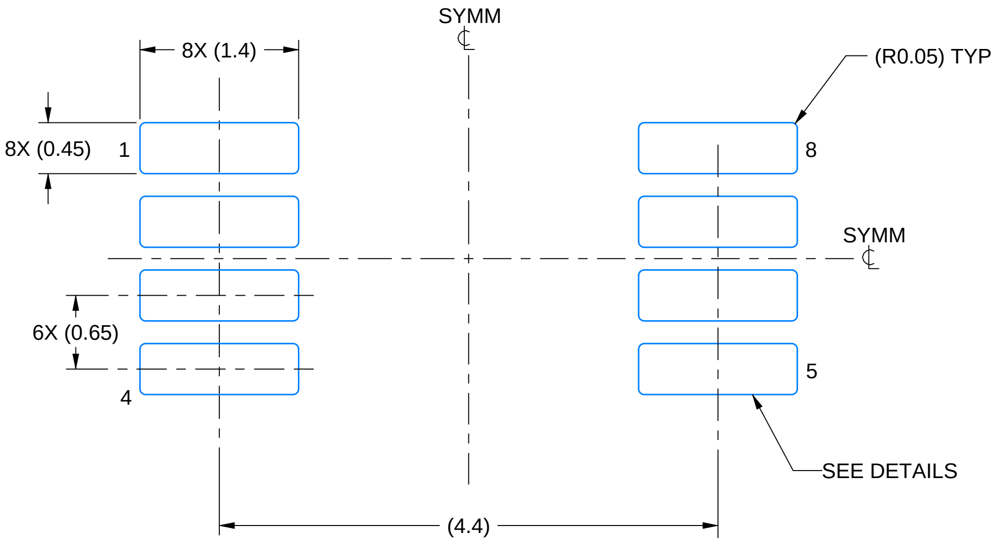


4214862/A 04/2023

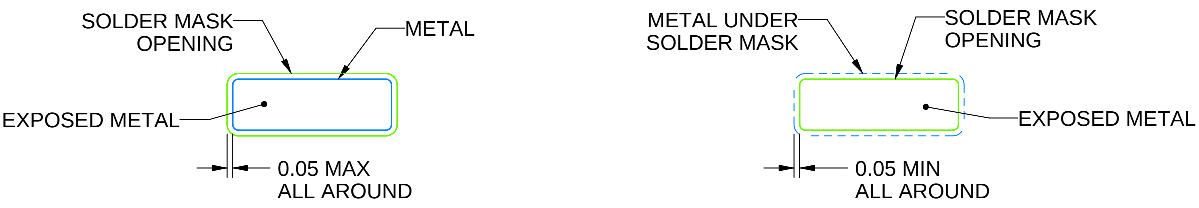
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

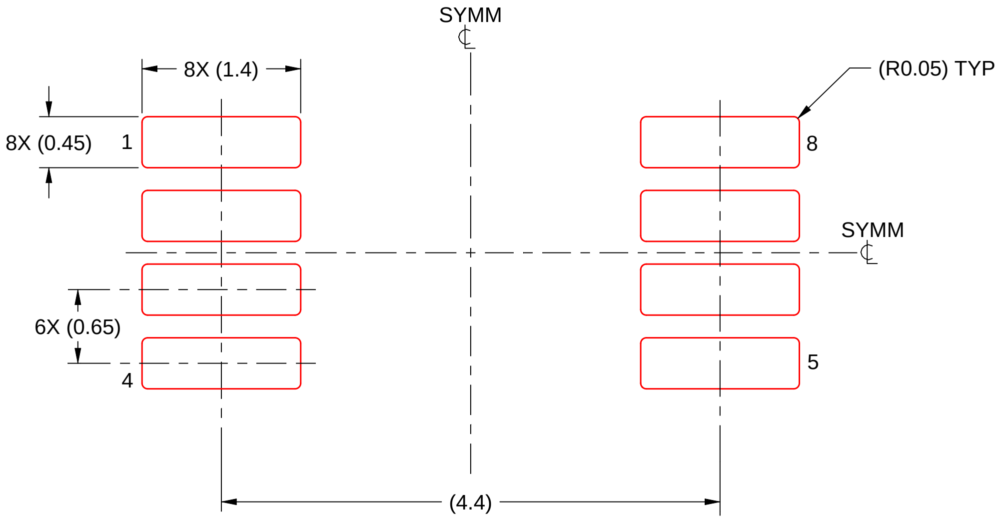
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



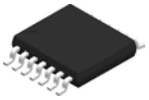
SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

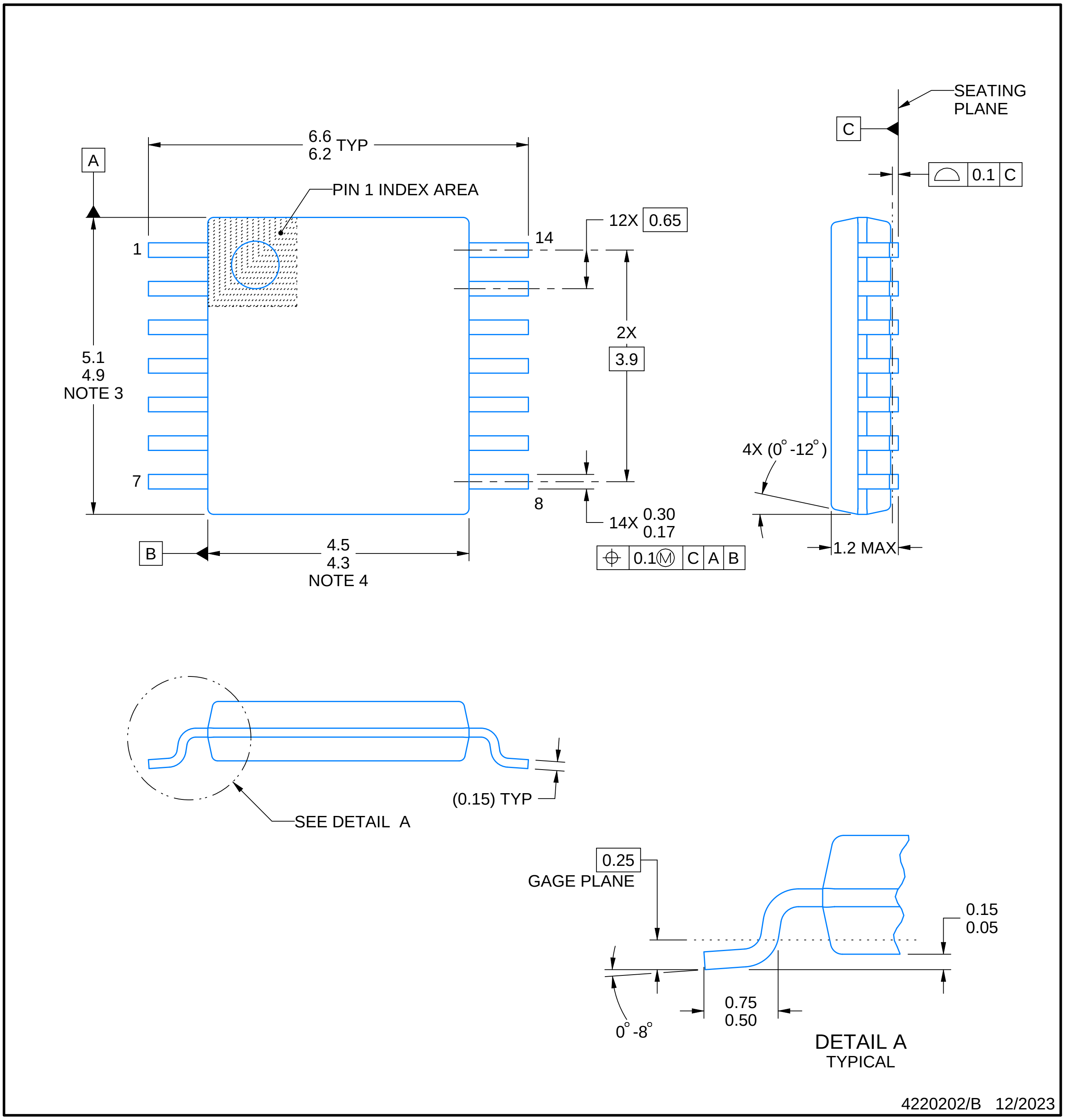
# PW0014A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

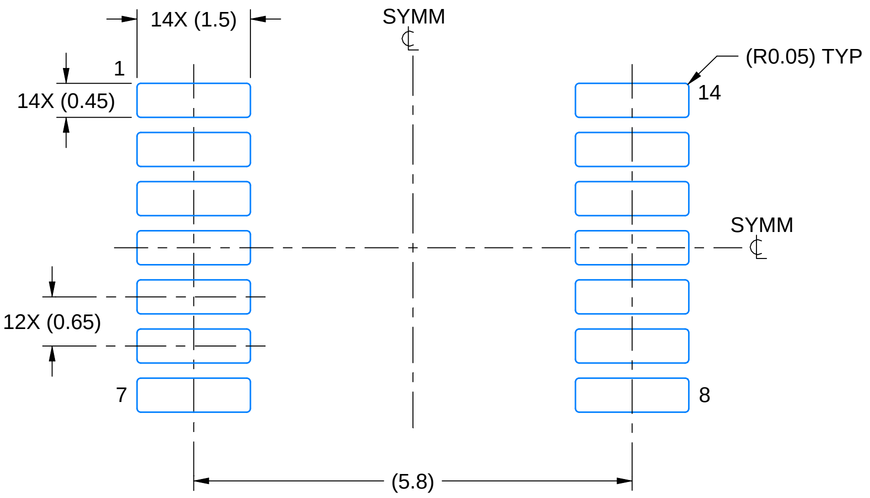
SMALL OUTLINE PACKAGE



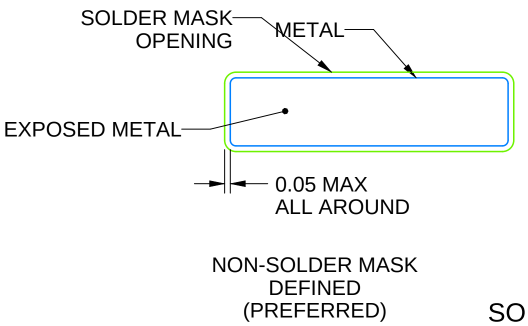
4220202/B 12/2023

NOTES:

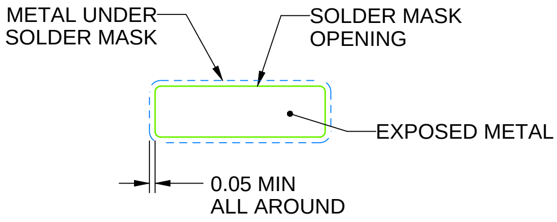
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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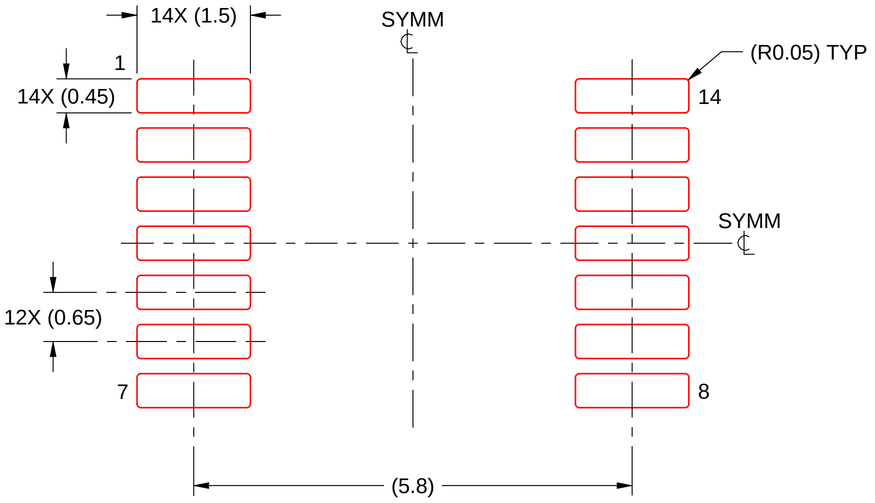
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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