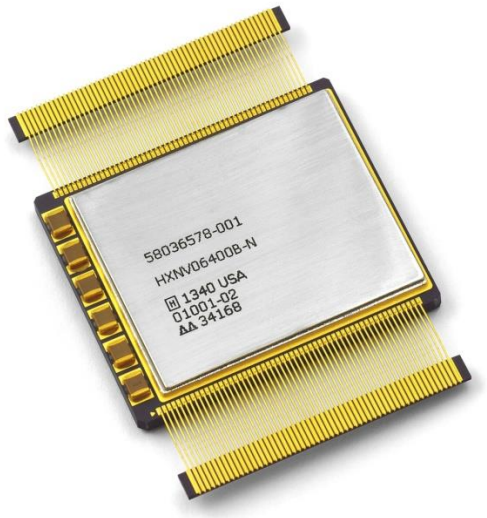
HXNV06400
64Mb Non-Volatile MRAM

The Honeywell 64 Megabit Multi-chip Module (MCM) radiation hardened low power non-volatile Magneto-Resistive Random Access Memory (MRAM) offers high performance and is designed for space and military applications. The part can be configured as either four chip enable selectable 2,097,152 word x 8-bit or four chip selectable 1,048,576 word x 16-bit MRAM through an external pin setting.

The high reliability MRAM is designed for severe space environments and features nearly limitless read and write cycle endurance, integrated Error Correction Circuitry (ECC), and low-voltage write protection. These features ensure the correct operation of the memory and protection from in advertent writes.

The MCM consists of four 16Mb MRAM monolithic chips fabricated with Honeywell's radiation hardened Silicon On Insulator (SOI) technology.

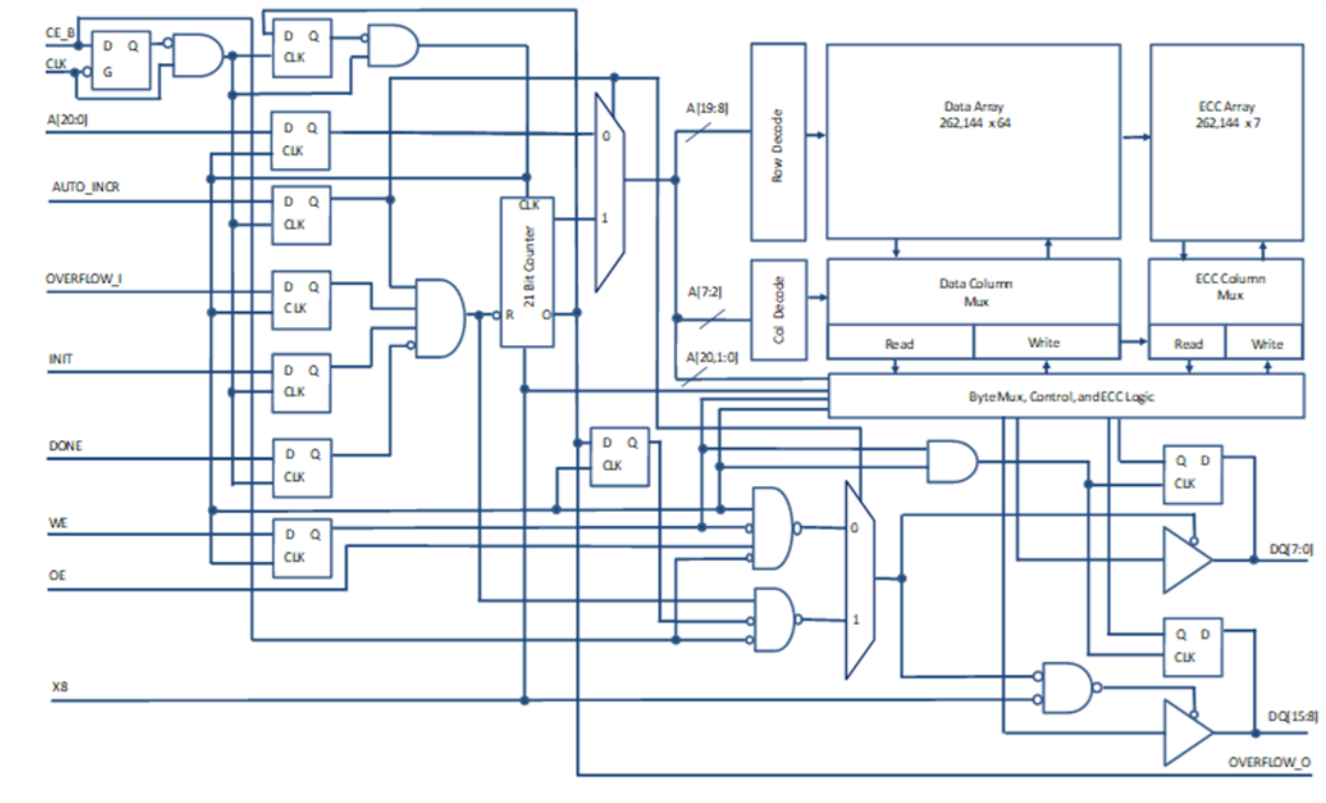


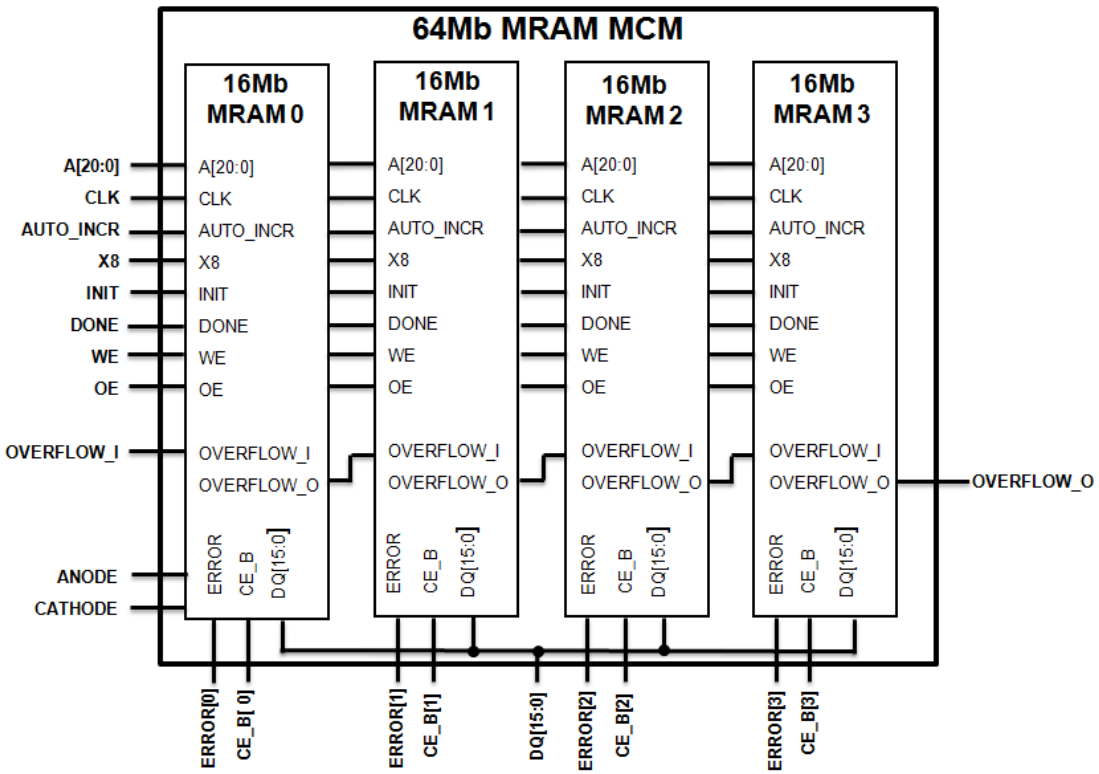
The 64Mb MRAM is designed for use in low-voltage systems operating in radiation environments over a temperature range of -40°C to +125°C with a 3.3 ± 0.3V core power supply and either a 3.3 ± 0.3V or 2.5 ± 0.25V IO power supply.

FEATURES

- Fabricated on S150 Silicon On Insulator (SOI) CMOS
- 150nm Process
- Timing
  100ns Read Access
  130ns Read Cycle
  150ns Write Cycle
- Robust Write and Read Capability
  $1x10^{15}$ cycles minimum
- 15 Yr Data Retention @ 105°C
- Synchronous Operation
- CMOS Compatible I/O
- Total Dose $3x10^{5}$ and $1x10^{6}$ rad(Si)
- Soft Error Rate
  Heavy Ion $1x10^{-10}$ upsets/bit-day
  Proton $1x10^{-11}$ upsets/bit-day
- Neutron Irradiation $1x10^{14}$ n/cm^2
- Dose Rate Upset
  $1x10^{9}$ rad(Si)/s
- Dose Rate Survivability
  $1x10^{12}$ rad(Si)/s
- Latchup Immune
- Core Operating Voltage
  3.3V
- I/O Voltages
  2.5V or 3.3V
- Operating Temperature Range
  -40°C to +125°C
- 112-Lead Ceramic Flat Pack Package

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM (SINGLE 16Mb MRAM)





PACKAGE PINOUT

VSS	1	112	VSS
VDDIO	2	111	VDDIO
TESTOUT1	3	110	TESTOUT24
TESTOUT2	4	109	TESTOUT23
TESTOUT3	5	108	TESTOUT22
TESTOUT4	6	107	TESTOUT21
TESTOUT5	7	106	TESTOUT20
TESTINL1	8	105	TESTINL11
ERROR[0]	9	104	ERROR[1]
CE_B[0]	10	103	CE_B[1]
TESTOUT6	11	102	TESTOUT19
TESTINL2	12	101	TESTINL10
VDD3	13	100	VDD3
OVERFLOW_I	14	99	A[19]
A[20]	15	98	A[17]
A[18]	16	97	A[15]
A[16]	17	96	A[13]
A[14]	18	95	A[11]
A[12]	19	94	DQ[4]
VSS	20	93	VSS
VDD3	21	92	VDD3
A[10]	22	91	TESTINL9
DQ[0]	23	90	DQ[5]
DQ[1]	24	89	DQ[6]
DQ[2]	25	88	DQ[7]
DQ[3]	26	87	TESTINL8
X8	27	86	AUTO_INCR
CLK	28	85	VDDIO
VDDIO	29	84	INIT
WE	30	83	DONE
OE	31	82	TESTINH1
DQ[8]	32	81	DQ[12]
DQ[9]	33	80	DQ[13]
DQ[10]	34	79	DQ[14]
TESTINL3	35	78	DQ[15]
VDD3	36	77	VDD3
VSS	37	76	VSS
DQ[11]	38	75	A[9]
A[8]	39	74	A[7]
A[6]	40	73	A[5]
A[4]	41	72	A[3]
A[2]	42	71	A[1]
A[0]	43	70	OVERFLOW_O
VDD3	44	69	VDD3
TESTINL4	45	68	TESTINL7
TESTOUT7	46	67	TESTOUT18
CE_B[2]	47	66	CE_B[3]
ERROR[2]	48	65	ERROR[3]
TESTINL5	49	64	TESTINL6
TESTOUT8	50	63	TESTOUT17
TESTOUT9	51	62	TESTOUT16
TESTOUT10	52	61	TESTOUT15
TESTOUT11	53	60	TESTOUT14
TESTOUT12	54	59	TESTOUT13
VDDIO	55	58	VDDIO
VSS	56	57	VSS

PIN NAME DEFINITIONS

Pin Name	Definition
CLK	Clock. Rising edge initiates an access of memory from the enabled die. A[20-0], WE, CE_B[3-0], and DQ[15-0] are latched on the rising edge.
CE_B[3-0]	Chip enables. Each 16Mb MRAM is controlled by a separate CE_B. Low state at rising edge of CLK allows normal read or write operation to a 1Mb x 16 MRAM. High state at rising edge of CLK puts the 16Mb MRAM into a deselected state and holds the data output drivers in a high impedance (High-Z) state. Only a single chip enable should be active per rising edge CLK unless in auto increment mode in which all four enables should be active.
A[20-0]	Address input pins. Selects a particular 8-bit word within the memory array on rising edge of CLK. A[20] is not used when in 16-bit mode and should be tied to VSS.
DQ[15-0]	Bi-directional data I/O pins. Data inputs (D) during a write operation. Data outputs (Q) during a read operation. When in 8-bit mode, only DQ[7-0] are active and DQ[15-8] pins should be tied to VSS.
WE	Write enable. High state on rising edge of CLK activates a write operation and holds the data output drivers in a high impedance (High-Z) state. Low state on rising edge of CLK activates normal read operation.
OE	Output enable. Low state holds the data output drivers in a high impedance (High-Z) state. In high state the data output driver state is defined by CLK, CE_B[3:0],and WE. If not used, it must be connected to VDDIO.
X8	Data 8-bit mode enable. In high state, DQ[15-8] are high impendence and A[20:0] provides addressing to 8-bit words. In low state, A[19-0] provides addressing and DQ[15-0] is used for all 16-bit read and write operations and A[20] should be tied to VSS. X8 should be tied directly to VSS or VDDIO.
AUTO_INCR	Auto increment mode enable input. High state at rising edge of CLK initiates a read using an internal address counter. Low state at rising edge of CLK exits auto increment mode and resets internal address counter. In auto increment mode, CE_B[3-0] and WE should be low for correct operation.
INIT	Auto increment control input. Only valid when in AUTO_INCR is high at rising edge of CLK. Low state at rising edge of CLK resets auto increment internal address counter. High state at rising edge of CLK combined with low state of DONE signal and high state of OVERFLOW_I signal at rising edge of CLK enables auto increment of internal address counter.
DONE	Auto increment control input. Only valid when in AUTO_INCR is high at rising edge of CLK. High state at rising edge of CLK resets auto increment internal address counter. Low state at rising edge of CLK combined with high state of INIT signal and high state of OVERFLOW_I signal at rising edge of CLK enables auto increment of internal address counter.
OVERFLOW_I	Auto increment control input. Only valid when in AUTO_INCR is high at rising edge of CLK. Low state at rising edge of CLK resets auto increment internal address counter. High state at rising edge of CLK combined with high state of INIT signal and low state of DONE signal at rising edge of CLK enables auto increment of internal address counter.
OVERFLOW_O	Overflow output. Only valid when in auto increment mode. High state indicates internal address counter has reached the last address.
ERROR[3-0]	ECC output. Following a read or auto increment read operation, high state indicates the error correction circuit detected and corrected an error (single bit correction only). One error flag per 16Mb MRAM.
TESTINLx	These signals are used for manufacturing test only. They must be connected to VSS.
TESTINHx	These signals are used for manufacturing test only. They must be connected to VDDIO.
TESTOUTx	These signals are used for manufacturing test only. They must be left unconnected.
VDDIO	Power input. Supplies power for the I/O and can be either 2.5V or 3.3V nominally.
VDD3	Power input. Supplies power for the MRAM core and must be 3.3V nominally.
VSS	Ground

TRUTH TABLE

CLK	CE_B[3-0] (4)	WE	AUTO_INCR	INIT	DONE	OVERFLOW_I	Function
R	1111	X	X	X	X	X	Chip Disable
R	1110	0	0	X	X	X	MRAM[0] Read Cycle (1)
R	1101	0	0	X	X	X	MRAM[1] Read Cycle (1)
R	1011	0	0	X	X	X	MRAM[2] Read Cycle (1)
R	0111	0	0	X	X	X	MRAM[3] Read Cycle (1)
R	1110	1	0	X	X	X	MRAM[0] Write Cycle (1)
R	1101	1	0	X	X	X	MRAM[1] Write Cycle (1)
R	1011	1	0	X	X	X	MRAM[2] Write Cycle (1)
R	0111	1	0	X	X	X	MRAM[3] Write Cycle (1)
R	0000	X	1	1	0	1	AI Read Cycle (2) (3)
R	XXXX	X	1	0	X	X	AI Chip Disable (3)
R	XXXX	X	1	X	1	X	AI Chip Disable (3)
R	XXXX	X	1	X	X	0	AI Chip Disable (3)

(1) Read and write occurs at memory locations provided by external address pins at rising edge of CLK
(2) Internal address counter starts with Address=0x000000 and increments 1 per rising edge of CLK
(3) Internal counter reset to Address=0x000000
(4) CE_B[3-0]: Only one CE_B low allowed at a time for non-auto increment operations.

OUTPUT DRIVER TRUTH TABLE

	Inputs			Outputs		
Function	CLK	CE_B[3-0]	OE	DQ (1)	OVERFLOW_O (2)	ERROR[3-0] (3)
Chip Disable	X	XXXX	X	Hi-Z	Active	Active
MRAM[3-0] Read Cycle	1	XXXX	1	Active	Active	Active
MRAM[3-0] Read Cycle	1	XXXX	0	Hi-Z	Active	Active
MRAM[3-0] Read Cycle	0	XXXX	X	Hi-Z	Active	Active
MRAM[3-0] Write Cycle	X	XXXX	X	Hi-Z	Active	Active
AI Read Cycle	X	0000	X	Active	Active	Active
AI Read Cycle	X	1111	X	Hi-Z	Active	Active
AI Chip Disable	X	X	X	Hi-Z	Active	Active

(1) If X8=1, DQ[15-8] is always Hi-Z and truth table applies only to DQ[7-0].
(2) Output is always active, but is only valid when in auto increment mode
(3) Output is always active, but only a single ERROR[3-0] output will be valid corresponding to the MRAM[3-0] that read cycle was performed on. Not valid data after write operations.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Ratings		Unit
		Min	Max	
VDDIO	Positive Supply Voltage (I/O) Referenced to VSS	-0.5	4.6	V
VDD3	Positive Supply Voltage (core) Referenced to VSS	-0.5	4.6	V
VPIN	Voltage on Any Input or Output Pin Referenced to VSS	-0.5	VDDIO + 0.5	V
IOUT (2)	Average Output Current		90	mA
TSTORE (3)	Storage Temperature	-65	150	°C
TSOLDER (4)	Soldering Temperature		220	°C
PD (5)	Package Power Dissipation		4.1	W
PJC	Package Thermal Resistance (Junction to Case)		1.2	°C/W
VPROT	Electrostatic Discharge Protection Voltage (Human Body Model)	2000		V
TJ	Junction Temperature		160	°C
HRS (6)	Magnetic Field Exposure Read, Standby, or Unbiased		100	Oersteds
HWR (6)	Magnetic Field Exposure Write		65	Oersteds

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Not to exceed 1 second.
(3) Storage time above 125°C is limited to 504 hours.
(4) Maximum soldering temperature can be maintained for no more than 180 seconds cumulative over the lifetime of the part.
(5) Operating power dissipation plus output driver power dissipation due to external load must not exceed this specification.
(6) Tested at 25°C.

RECOMMENDED OPERATING CONDITIONS (1)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
VDDIO (2)	Positive Supply Voltage (3.3V I/O) Referenced to VSS	3.00	3.30	3.60	V
	Positive Supply Voltage (2.5V I/O) Referenced to VSS	2.25	2.5	2.75	V
VDD3 (2)	Positive Supply Voltage (core) Referenced to VSS	3.00	3.30	3.60	V
TC	Case Temperature	-40	25	125	°C
VIO	Voltage on Any Input or Output Pin Referenced to VSS	-0.3		VDDIO + 0.3	V
LIFETIME (3)	Operation Lifetime			15 @ 105°C	Years
TRAMP	Supply Voltage Ramp Time			1.0	S

(1) Specifications listed in datasheet apply when operated under the Recommended Operating Conditions unless otherwise specified.
(2) There is a 2ms startup time once VDD3 exceeds VDD3(min) and VDDIO exceeds VDDIO3(min).
(3) Lifetime above 105°C up to 125°C is 2 years.

DATA ENDURANCE AND RETENTION (1)

Symbol	Parameter	Limits		Unit
		Min	Max	
DREN	Data Read Endurance	$1x10^{15}$		Cycles
DWEN	Data Write Endurance	$1x10^{15}$		Cycles
DRET (2) (3)	Data Retention	15		Years

(1) Data retention and endurance verified as a part of initial qualification only.
(2) Applies with power on or off.
(3) Data retention above 105°C up to 125°C is 2 years.

RADIATION HARDNESS RATINGS (1)

Symbol	Parameter	Environment Conditions	Limits	Unit
TID	Total Ionizing Dose		$1x10^6$ $3x10^5$	rad(Si)
DRU	Transient Dose Rate Upset	Pulse width ≤ 20ns	$1x10^9$	rad(Si)/s
DRS	Transient Dose Rate Survivability	Pulse width ≤ 20ns	$1x10^{12}$	rad(Si)/s
SER (2)	Projected Soft Error Rate Heavy Ion Proton	Geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield	 $1x10^{-10}$ $1x10^{-11}$	 upsets/bit-day upsets/bit-day
	Neutron Irradiation Damage	1 MeV equivalent energy	$1x10^{14}$	n/cm^2

(1) Device will not latchup when exposed to any of the specified radiation environments.
(2) Calculated using CREME96 with Weibull parameters and other relevant attributes applied.

RADIATION CHARACTERISTICS

Total Ionizing Dose Radiation

The MRAM radiation hardness assurance TID level was qualified by ^{60}Co testing, including overdose and accelerated annealing, per MIL-STD-883 Method 1019. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Single Event Soft Error Rate

Special process, memory cell, circuit and layout design considerations are included in the MRAM to minimize the impact of heavy ion and proton radiation and achieve small projected SER. Weibull parameters and other relevant attributes are available upon request to calculate projected upset rate performance for other orbits and environments.

Transient Dose Rate Ionizing Radiation

Many aspects of product design are addressed to handle the high energy levels associated with the transient dose rate events. This allows the MRAM to be capable of writing, reading, and retaining stored data during and after exposure to a transient dose rate ionizing radiation pulse, up to the specified transient dose rate upset specification. The MRAM will also meet functional and timing specifications after exposure to a transient dose rate ionizing radiation pulse up to the transient dose rate survivability specification.

Neutron Irradiation Damage

SOI CMOS is inherently tolerant to damage from neutron irradiation. The MRAM meets functional and timing specifications after exposure to the specified neutron fluence, based on conventional neutron irradiation testing, on unbiased MRAM parts.

Latchup

The MRAM will not latchup due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabricating with the SOI CMOS substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

PIN CAPACITANCE (1)

Symbol	Parameter	Max	Unit
CCLK	CLK Pin Capacitance	48	pF
CCEB	CE_B[3-0] Pin Capacitance	48	pF
CA	Address Pin Capacitance	48	pF
COE	OE Pin Capacitance	48	pF
CWE	WE Pin Capacitance	48	pF
CX8	X8 Pin Capacitance	48	pF
CAI	AUTO_INCR, DONE, and INIT Pin Capacitance	48	pF
COI	OVERFLOW_I Pin Capacitance	48	pF
CDQ	Data I/O Pin Capacitance	60	pF

(1) Maximum capacitance is verified as part of initial qualification only.

POWER PIN ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		Max		Unit
				VDDIO	VDD3	
IDDSB	Static Supply Current		TA=25°C, pre-TID	6.0	40.0	mA
				12.0	60.0	mA
IDDOPW (1)	Dynamic Supply Current Selected, Write		1.0MHz	40.0	100.0	mA
			6.7MHz	60.0	220.0	mA
IDDOPR (1)	Dynamic Supply Current Selected, Read		1.0MHz	40.0	70.0	mA
			7.7MHz	120.0	150.0	mA

(1) All dynamic operating mode current measurements (IDDOPx) include standby mode current (IDDSB).

SIGNAL PIN ELECTRICAL CHARACTERISTICS (1)

Symbol	Parameter	Conditions	Min	Max	Unit
IIN	Input Leakage Current	VSS ≤ VIN ≤ VDDIO	-10	10	uA
IOZ	Output Leakage Current	DQ = High-Z	-100	100	uA
VIL	Low-Level Input Voltage			0.3 x VDDIO	V
VIH	High-Level Input Voltage		0.7 x VDDIO		V
VOL1	Low-Level Output Voltage for 3.3V I/O	IOL = +6mA		0.5	V
VOH1	High-Level Output Voltage for 3.3V I/O	IOH = -6mA	2.50		V
VOL2	Low-Level Output Voltage for 2.5V I/O	IOL = +6mA		0.5	V
VOH2	High-Level Output Voltage for 2.5V I/O	IOH = -6mA	1.75		V

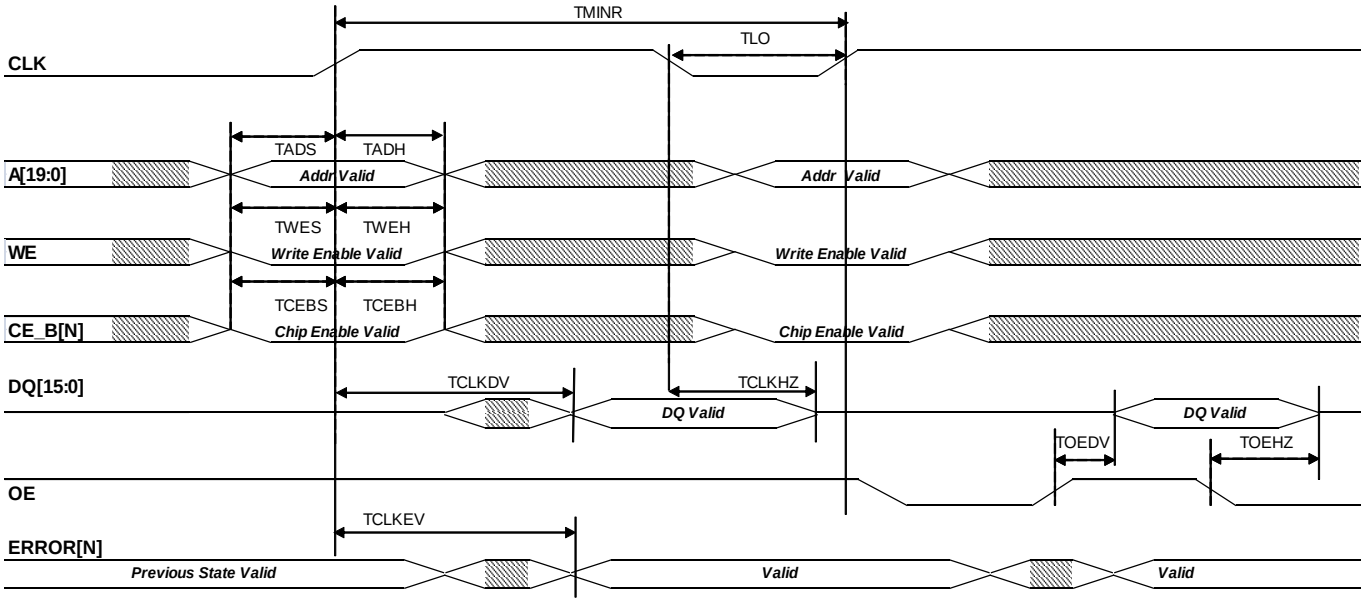
(1) Voltages referenced to VSS.

READ CYCLE TIMING CHARACTERISTICS (1)

Symbol	Parameter	Limits 3.3V & 2.5V I/O		Unit
		Min	Max	
TMINR	Read Cycle Time	130		ns
TCLKDV	Rising Edge of Clock to Data Valid	50	100	ns
TCLKEV	Rising Edge of Clock to Error Valid	50	100	ns
TADS	Address Setup Time	5		ns
TADH	Address Hold Time	15		ns
TWES	Write Enable Setup Time	5		ns
TWEH	Write Enable Setup Time	15		ns
TCEBS	Chip Enable Setup Time	5		ns
TCEBH	Chip Enable Hold Time	15		ns
TOEDV	Output Enable to Data Valid		15	ns
TOEHZ	Output Disable to Data High-Z	1	15	ns
TCLKHZ	Clock Low to Data High-Z	1	15	ns
TLO	Minimum Clock Low Time	15		ns

(1) The timing specifications are referenced to the Timing Input and Output References diagram and the Timing Reference Load Circuit diagram. IBIS models should be used to evaluate timing under application load circuits.

READ CYCLE TIMING WAVEFORMS



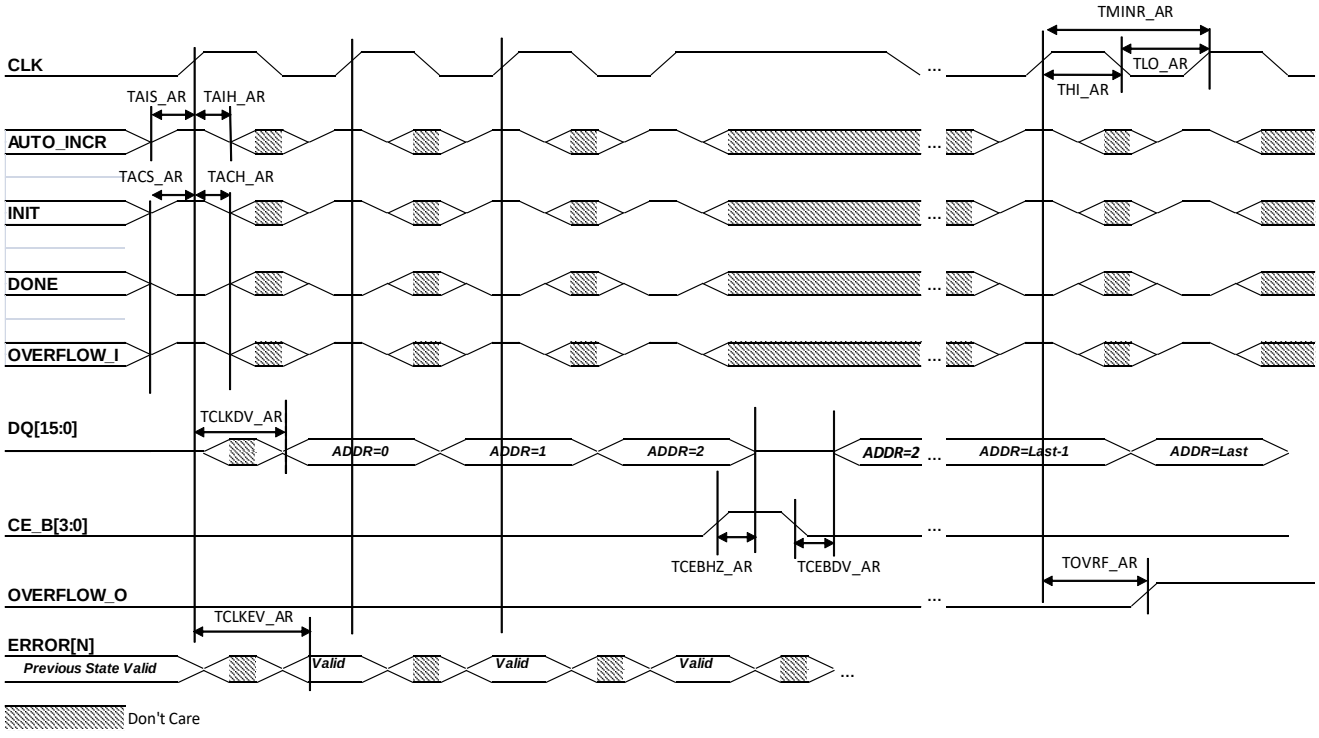
(1) CE_B[N] – For valid read operation, only a single CE_B[3:0] must be low and the remaining three must be high during the “Chip Enable Valid” period.
(2) ERROR[N] - Only a single ERROR[3:0] signal is valid corresponding to the die enabled during the "Chip Enable Valid" period (i.e. CE_B[0] = low, ERROR[0] = valid)
(3) AUTO_INCR - Must be low during read operations, refer to functional truth table.

AUTO INCREMENT READ CYCLE TIMING CHARACTERISTICS (1)

Symbol	Parameter	Limits 3.3V & 2.5V I/O		Unit
		Min	Max	
TMINR_AR	Auto Increment Read Cycle Time	130		ns
TCLKDV_AR	Rising Edge of Clock to Data Valid	50	100	ns
TCLKEV_AR	Rising Edge of Clock to Error Valid	50	100	ns
TAIS_AR	Auto Increment Setup Time	5		ns
TAIH_AR	Auto Increment Hold Time	15		ns
TACS_AR	Auto Increment Control Pin Setup Time (INIT, DONE, OVERFLOW_I)	5		ns
TACH_AR	Auto Increment Control Pin Hold Time (INIT, DONE, OVERFLOW_I)	15		ns
TOVRF_AR	Rising of Clock to Overflow Valid		20	ns
TCEBDV_AR	Chip Enable to Data Valid		15	ns
TCEBHZ_AR	Chip Disable to Data High-Z	1	15	ns
THI_AR	Minimum Clock High Time	15		ns
TLO_AR	Minimum Clock Low Time	15		ns

(1) The timing specifications are referenced to the Timing Input and Output References diagram and the Timing Reference Load Circuit diagram. IBIS models should be used to evaluate timing under application load circuits.

AUTO INCREMENT READ CYCLE TIMING WAVEFORMS



(1) CE_B[N] - For valid auto increment read operation, all CE_B[3:0] signals must be low and WE must be low (not shown, but using Read Cycle Timing Requirements)

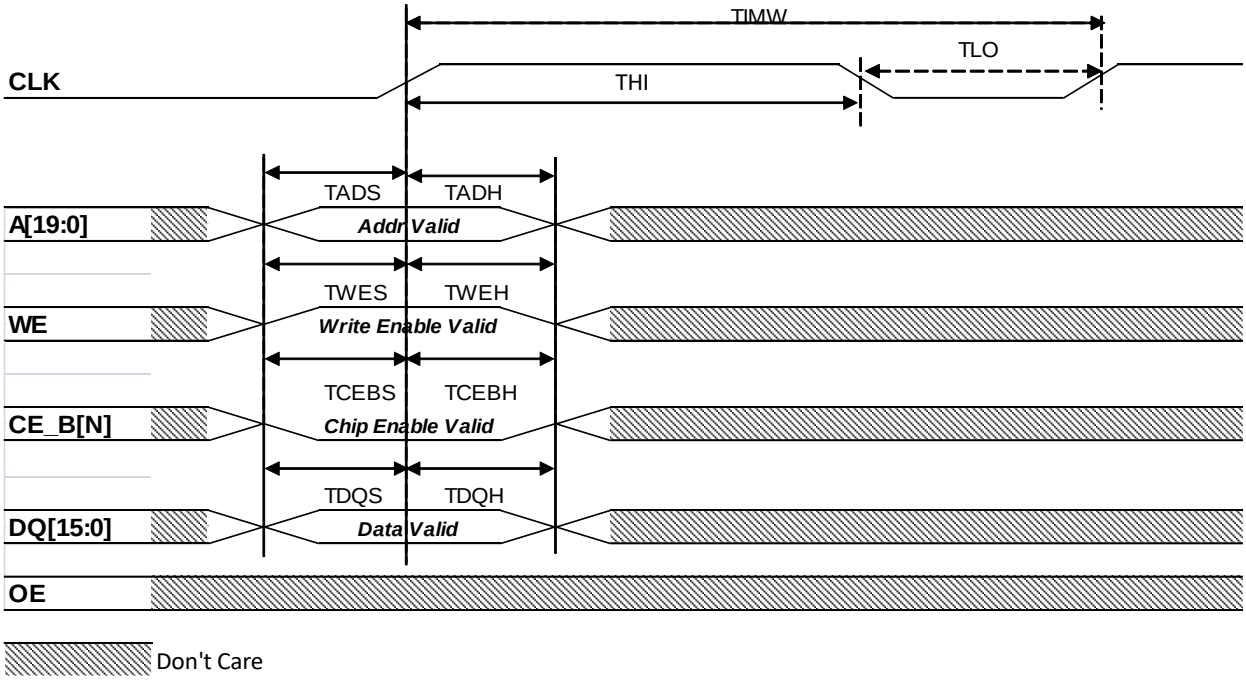
(2) ERROR[N] - Only a single ERROR[3:0] signal is valid at a time depending on which die is active in the auto increment feature (depends on clock cycles and X8 mode).

WRITE CYCLE TIMING CHARACTERISTICS (1)

Symbol	Parameter	Limits 3.3V & 2.5V I/O		Unit
		Min	Max	
TMINW	Write Cycle Time	150		ns
TADS	Address Setup Time	5		ns
TADH	Address Hold Time	15		ns
TWES	Write Enable Setup Time	5		ns
TWEH	Write Enable Setup Time	15		ns
TCEBS	Chip Enable Setup Time	5		ns
TCEBH	Chip Enable Hold Time	15		ns
TDQS	Data Setup Time	5		ns
TDQH	Data Hold Time	15		ns
THI	Clock High Time	15		ns
TLO	Clock Low Time	15		ns

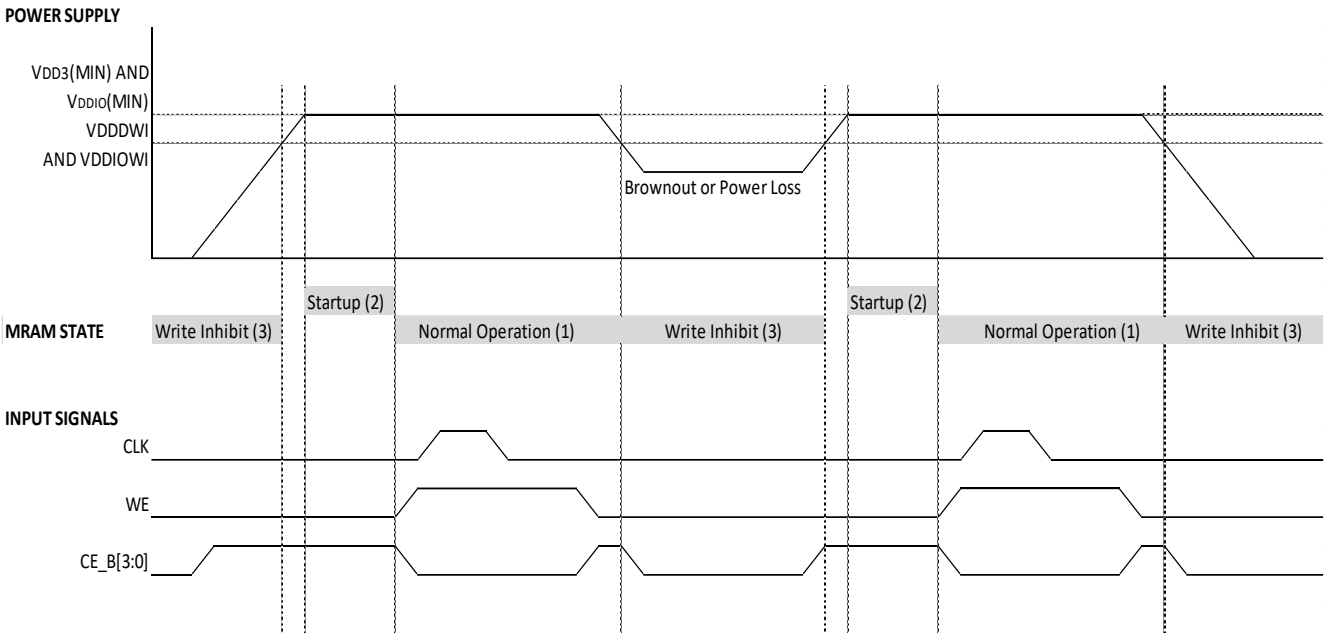
(1) The timing specifications are referenced to the Timing Input and Output References diagram and the Timing Reference Load Circuit diagram. IBIS models should be used to evaluate timing under application load circuits.

WRITE CYCLE TIMING



(1) CE_B[N] - For valid write operation, only a single CE_B[3:0] must be low and the remaing three must be high during the "Chip Enable Valid" period
(2) ERROR[N] - Not Valid on Write Operations
(3) AUTO_INCR - Must be low during write operations, refer to functional truth table

POWER UP AND DOWN TIMING



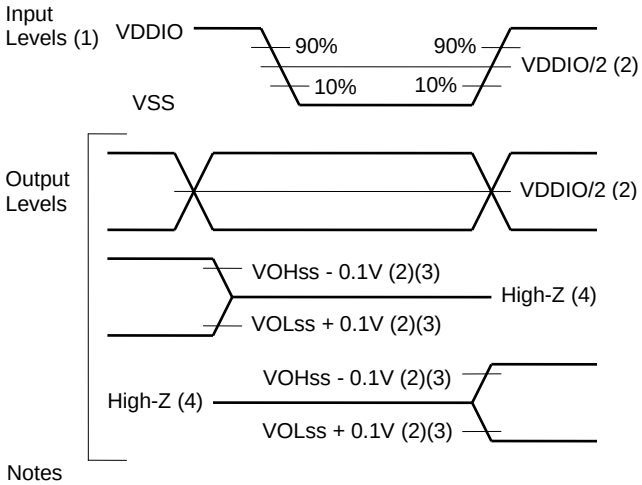
(1) Only a single CE_B[3-0] should be low at a time in read and write modes. Refer to functional truth table.

(2) Once VDD3 and VDDIO are both equal to or above their minimum recommended operating values, a 2ms startup wait time must be observed.

(3) Once VDD3 and VDDIO are below a certain voltage threshold (VDD3WI and VDDIOWI), writes are inhibited.

(4) Following a power-up condition; a no-op (dummy) read clock cycle with CE_B<3:0>=low, auto_incr=low, WE=low and OE=low(high) must be performed to complete part initialization. This no-op clock cycle may be performed in a single clock cycle with all CE_B<3:0>=low and OE must be low or in four individual clock cycles where each of the CE_B<3:0> are individually set low on each clock cycle and OE can be either low(output is high-Z) or high(output is low-Z).

TIMING INPUT AND OUTPUT



Notes

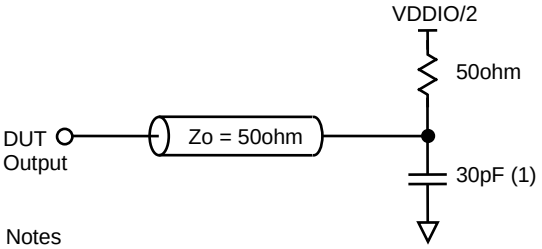
(1) Input rise and fall times = 1ns between 90% and 10% levels.

(2) Timing parameter reference voltage level.

(3) ss: Low-Z VOH and VOL steady-state output voltage.

(4) High-Z output pin pulled to VDDIO/2 by Reference Load Circuit.

TIMING REFERENCE LOAD



Notes

(1) Set to 5pF for T*HZ (Low-Z to High-Z) timing parameters.

FUNCTIONAL DESCRIPTION

MRAM Operation

MRAM is synchronous in operation relative to the rising edge of the CLK signal. With the rising edge of CLK signal, the Chip Enables (CE_B[3-0]), Address (A[20-0]), Auto Increment Control Signals (AUTO_INCR, INIT, DONE, OVERFLOW_I) and Write Enable (WE) signals are captured. Operating modes are defined in the Truth Table.

CE_B[3-0] is used to control which one of the 4 MRAM die is written to or read from. One and only one signal line of CE_B[3-0] can be active (low) on the rising edge of CLK for write and standard read options. For auto increment read operations, all Chip Enable signals must be asserted low (CE_B[3-0]).

MRAM can operate in either 8-bit or 16-bit for all functional modes and is determined by the state of the X8 pin. It must be tied directly to VSS (16-bit) or VDDIO (8-bit). When in 8-bit mode, DQ[7-0] will be used and DQ[15-8] will be High-Z and can be tied to VSS.

Read Operation

During a read operation (WE=low and only a single CE_B[X]=low), the Address pins are registered and the ECC corrected read data is present on the bus TCLKDV after the rising edge of CLK. The output enable pin (OE) controls the output buffers during this time. ERROR[X] will signal if an ECC correction occurred on the read operation TCLKEV after the rising edge of CLK.

Write Operation

During a write operation (WE=high and only a single CE_B[X]=low), the Address pins are registered along with the data to be written. The MRAM first reads the data at the specified location, computes a parity code, then determines which bits are required to toggle. The toggle/write information is passed to the write circuitry which completes the write operation by writing to the data and ECC memory arrays. All write operations are completed by TMINW from the rising edge of CLK.

Auto Increment Read Operation

In addition to the standard read operation to a specific address, each MRAM die supports a sequential read mode that allows the data at each address to be read, starting at Address=0x0 and automatically incrementing on each rising CLK edge. The mode is referred to as auto increment mode and does not require an external address to be supplied. Once the last address is reached, an external indicator called the OVERFLOW_OUT will get asserted. There are four pins that control the enabling and resetting of auto increment mode (AUTO_INCR, INIT, DONE, and OVERFLOW_IN). All CE_B[0-3] pins need to be low in auto increment mode of the 64Mb MRAM MCM.

Following an auto increment overflow condition (OVERFLOW_O = high); a no-op(dummy) clock cycle with CE_B<3:0>=low and auto_incr=low must be performed to clear the internal overflow registers. This no-op clock cycle may be performed in a single clock cycle with all CE_B<3:0>=low or in four individual clock cycles where each of the CE_B<3:0> are individually set low on each clock cycle. During the no-op clock cycle(s) the output is high-Z and no read or write operation(s) occurs.

Signal Integrity

As a general design practice, one should have good signal integrity which means input signals that are free of noise, glitches and ringing with rising and falling edges of ≤10ns. More specifically, an input is considered to have good signal integrity when the input voltage monotonically traverses the region between VIL and VIH in ≤10ns. This is especially important in a selected and enabled state. When the device is selected and enabled, the last transitioning input for the desired operation must have good signal integrity to maintain valid operation. The transitioning inputs that bring the device into and out of a selected and enabled state must also have good signal integrity to maintain valid operation. When the device is deselected and/or disabled, inputs can have poor signal integrity and even float as long as the inputs that are defining the deselected and/or disabled state stay within valid VIL and VIH voltage levels. However, floating inputs for an extended period of time is not recommended.

RELIABILITY

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in 1990. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability and radiation).
- Utilizing a structured and controlled design process.
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

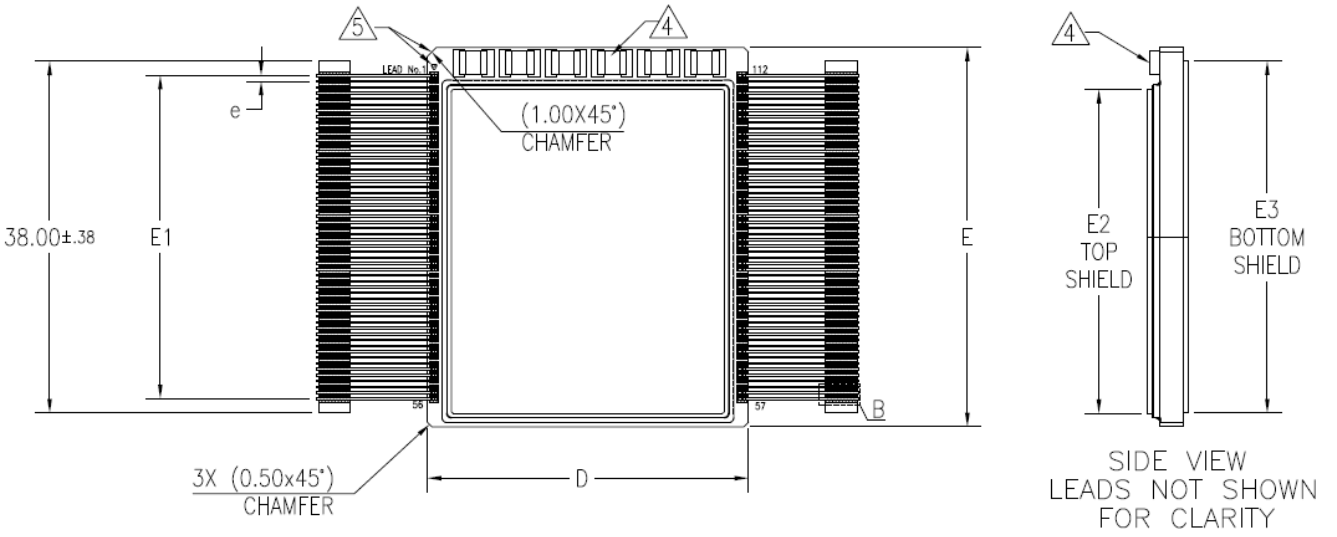
SCREENING AND CONFORMANCE INSPECTION

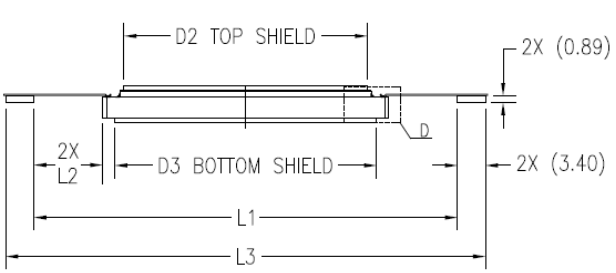
The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

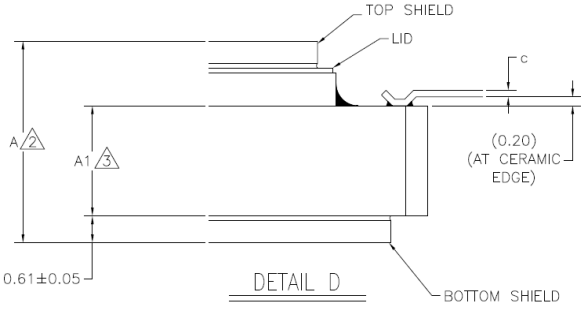
Conformance Summary

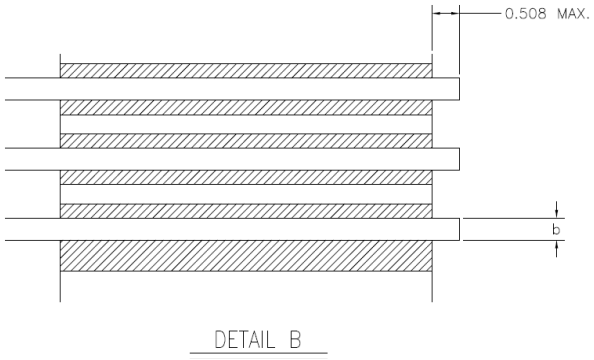
Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests - 1000 hours at 125C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

CASE OUTLINE









SYMBOL	COMMON DIMENSIONS (MILLIMETERS)		
	MIN.	NOM.	MAX.
A	4.16	4.58	5.01
A1	2.25	2.50	2.75
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D	34.35	34.70	35.05
D2	29.61	29.74	29.87
D3	32.03	32.16	32.29
e	0.585	0.635	0.685
E	40.59	41.00	41.41
E1	34.795	34.925	35.055
E2	35.11	35.24	35.37
E3	38.33	38.46	38.59
L1	51.00	51.35	———
L2	7.725	8.325	———
L3	57.65	58.15	58.65

Case Outline Notes

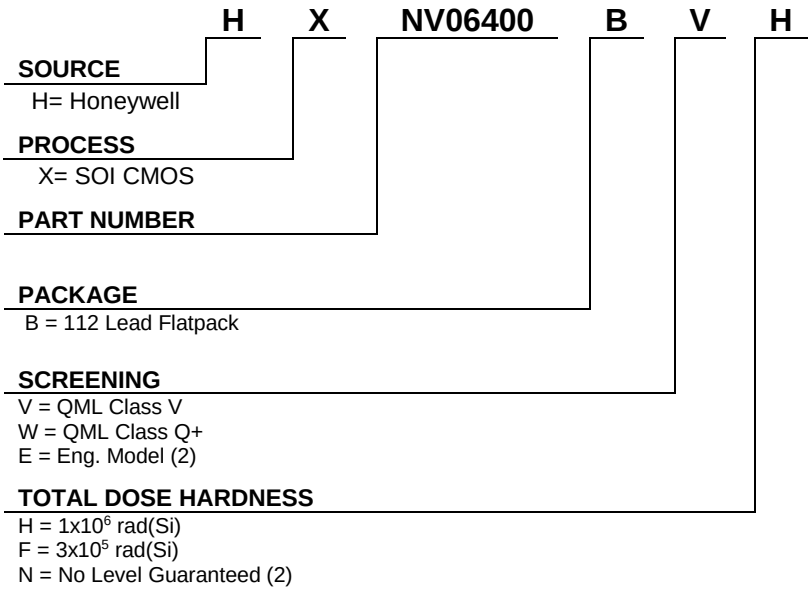
(1) Tolerance unless specified +/-0.2mm
(2) Height of assembled package includes ceramic, seal ring, lid and top and bottom shields.
(3) Height of ceramic body.
(4) Chip capacitors, MIL Style CDR33, max height 1.27, max quantity 6, max capacitor height is less than height of lid plus top shield.
(5) Pin 1 indicated by larger chamfer and mark on ceramic.

HXNV06400

ORDERING INFORMATION (1)

QML qualified MRAM parts shall be ordered to the SMD 5962-14230. The SMD is the governing document and shall take precedence over this datasheet.

Order Code



QCI TESTING (3)

Classification	QCI Testing
QML Q+	No lot specific testing performed. (4)
QML V	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) Please contact our Customer Service Representative at 1-763-954-2474 or 1-800-323-8295 for further information.
(2) Engineering Model Description: Engineering Model suffix for Screening Level and Total Dose Hardness is "EN". Parameters are tested -40°C to 125°C, 48 hour burn-in, no radiation hardness guaranteed.
(3) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell Quality Management Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(4) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

FIND OUT MORE

For more information about Honeywell's family of radiation hardened products and technology, visit www.honeywellmicroelectronics.com.

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