NBM™ Bus Converter

NBM6123x60E12A7yzz

Non-Isolated, Fixed Ratio DC-DC Converter

Features & Benefits

- Up to 170A continuous secondary current
- Up to 3000W/in^3 power density
- 98% peak efficiency
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 6123 through-hole ChiP™ package
  - 2.402 x 0.990 x 0.284in (61.00 x 25.14 x 7.21mm)
- Bidirectional start up and steady state operation

Typical Applications

- DC Power Distribution
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Power Supplies
- Communications Systems
- Transportation

Product Ratings	
V_{PRI} = 54V (36 – 60V)	I_{SEC} = up to 170A
V_{SEC} = 10.8V (7.2 – 12.0V) (NO LOAD)	K = 1/5

Product Description

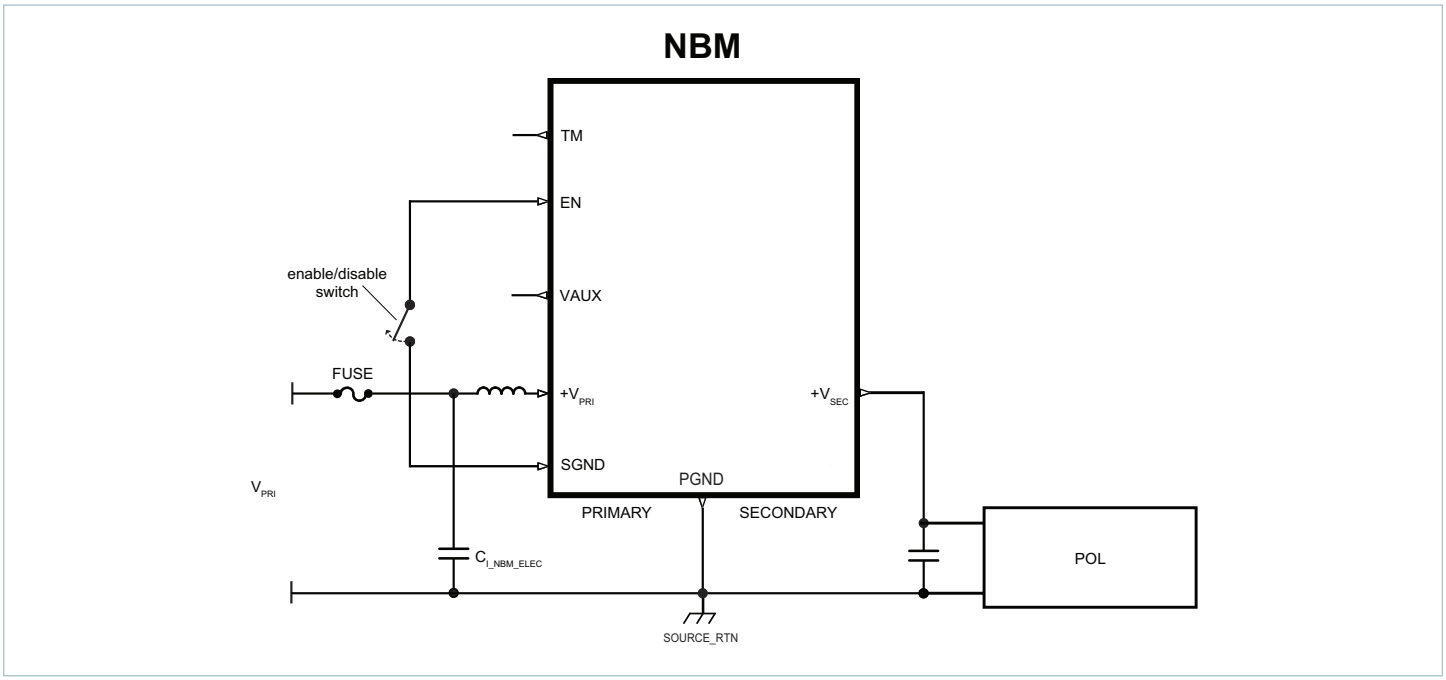
The NBM6123x60E12A7yzz is a high efficiency Non Isolated Bus Converter operating from a 36 – 60V_{DC} primary bus to deliver a non-isolated, ratiometric secondary voltage from 7.2 to 12.0V_{DC}.

The NBM6123x60E12A7yzz offers low noise, fast transient response, and industry leading efficiency and power density. In addition, it provides an AC impedance beyond the bandwidth of most downstream regulators, allowing input capacitance normally located at the input of a PoL regulator to be located at the primary side of the NBM. With a primary to secondary K factor of 1/5, that capacitance value can be reduced by a factor of 25x, resulting in savings of board area, material and total system cost.

Leveraging the thermal and density benefits of Vicor ChiP packaging technology, the NBM offers flexible thermal management options with very low top and bottom side thermal impedances. Thermally-adept ChiP-based power components enable customers to achieve low cost power system solutions with previously unattainable system size, weight and efficiency attributes quickly and predictably.

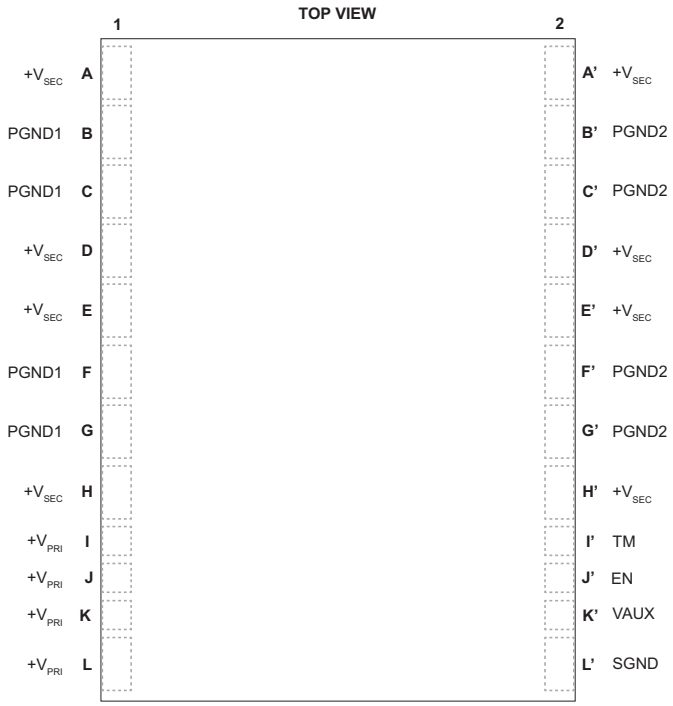
The NBM non-isolated topology allows start up and steady state operation in forward and reverse directions and provides bidirectional protections. However if the power train is disabled by any protection and V_{SEC} is present, then a voltage equal to V_{SEC} minus two diode drops will appear on the primary side.

Typical Applications



NBM6123x60E12A7yzz + Point of Load

Pin Configuration



6123 ChiP Package

Pin Descriptions

Pin Number	Signal Name	Type	Function
I1, J1, K1, L1	$+V_{PRI}$	PRIMARY POWER	Positive primary auto-transformer power terminal
I'2	TM	OUTPUT	Temperature Monitor; Primary side referenced signals
J'2	EN	INPUT	Enables and disables power supply; Primary side referenced signals
K'2	VAUX	OUTPUT	Auxiliary Voltage Source; Primary side referenced signals
L'2	SGND	SIGNAL RETURN	Signal return terminal only. Do not connect to PGND
A1, D1, E1, H1, A'2, D'2, E'2, H'2	$+V_{SEC}$	SECONDARY POWER	Positive secondary auto-transformer power terminal
B1, C1, F1, G1 B'2, C'2, F'2, G'2	PGND [a]	POWER RETURN	Common negative primary and secondary auto-transformer power return terminal

[a] For proper operation an external low impedance connection must be made between listed -PGND1 and PGND2 terminals.

Part Ordering Information

Product Function	Package Size	Package Mounting	Max Primary Input Voltage	Range Identifier	Max Secondary Voltage	Secondary Output Current	Temperature Grade	Option
NBM	6123	x	60	E	12	A7	y	zz
Non-isolated Bus Converter Module	61 = L 23 = W	**T** = TH **S** = SMT	60V	36 – 60V	12V No Load	170A	**T** = –40°C – 125°C **M** = –55°C – 125°C	**00** = Analog Ctrl **01** = PMBus Ctrl **0R** = Reversible Analog Ctrl **0P** = Reversible PMBus Ctrl

All products shipped in JEDEC standard high profile (0.400" thick) trays (JEDEC Publication 95, Design Guide 4.10).

Standard Models

Product Function	Package Size	Package Mounting	Max Primary Input Voltage	Range Identifier	Max Secondary Voltage	Secondary Output Current	Temperature Grade	Option
NBM	6123	T	60	E	12	A7	T	0R

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
$+V_{PRI\_DC}$ to $-V_{PRI\_DC}$		–1	80	V
V_{PRI_DC} or V_{SEC_DC} Slew Rate (Operational)			1	V/µs
$+V_{SEC\_DC}$ to $-V_{SEC\_DC}$		–1	16	V
TM to $-V_{PRI\_DC}$		–0.3	4.6	V
EN to $-V_{PRI\_DC}$			5.5	V
VAUX to $-V_{PRI\_DC}$			4.6	V

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain PRIMARY to SECONDARY Specification (Forward Direction)						
Primary Input Voltage Range (Continuous)	V_{PRI_DC}		**36**		**60**	V
V_{PRI} µController	$V_{\mu C\_ACTIVE}$	V_{PRI_DC} voltage where µC is initialized, (i.e., VAUX = low, powertrain inactive)			15	V
PRI to SEC Input Quiescent Current	I_{PRI_Q}	Disabled, EN low, V_{PRI_DC} = 54V		7		mA
		$T_{INTERNAL}$ ≤ 100°C			12	
PRI to SEC No Load Power Dissipation	P_{PRI_NL}	V_{PRI_DC} = 54V, $T_{INTERNAL}$ = 25°C		10	12	W
		V_{PRI_DC} = 54V	**8**		**19**	
		V_{PRI_DC} = 36 – 60V, $T_{INTERNAL}$ = 25 °C			14	
		V_{PRI_DC} = 36 – 60V			**22**	
PRI to SEC Inrush Current Peak	$I_{PRI\_INR\_PK}$	V_{PRI_DC} = 60V, C_{SEC_EXT} = 3000µF, R_{LOAD_SEC} = 20% of full load current		15		A
		$T_{INTERNAL}$ ≤ 100°C			50	
DC Primary Input Current	$I_{PRI\_IN\_DC}$	At $I_{SEC\_OUT\_DC}$ = 170A, $T_{INTERNAL}$ ≤ 100°C			34.4	A
Transformation Ratio	K	Primary to secondary, K = V_{SEC_DC} / V_{PRI_DC}, at no load		1/5		V/V
Secondary Output Current (Continuous)	$I_{SEC\_OUT\_DC}$				170	A
Secondary Output Current (Pulsed)	$I_{SEC\_OUT\_PULSE}$	10ms pulse, 25% duty cycle, $I_{SEC\_OUT\_AVG}$ ≤ 50% rated $I_{SEC\_OUT\_DC}$			200	A
PRI to SEC Efficiency (Ambient)	η_{AMB}	V_{PRI_DC} = 54V, $I_{SEC\_OUT\_DC}$ = 170A	96.5	97.5		%
		V_{PRI_DC} = 36 – 60 V, $I_{SEC\_OUT\_DC}$ = 170A	95.6			
		V_{PRI_DC} = 54V, $I_{SEC\_OUT\_DC}$ = 85A	97.3	98		
PRI to SEC Efficiency (Hot)	η_{HOT}	V_{PRI_DC} = 54V, $I_{SEC\_OUT\_DC}$ = 170A	96.5	97.1		%
PRI to SEC Efficiency (Over Load Range)	$\eta_{20\%}$	34A < $I_{SEC\_OUT\_DC}$ < 170A	**90**			%
PRI to SEC Output Resistance	R_{SEC_COLD}	V_{PRI_DC} = 54V, $I_{SEC\_OUT\_DC}$ = 170A, $T_{INTERNAL}$ = –40°C	0.5	0.8	1.1	mΩ
	R_{SEC_AMB}	V_{PRI_DC} = 54V, $I_{SEC\_OUT\_DC}$ = 170A	0.8	1.3	1.8	
	R_{SEC_HOT}	V_{PRI_DC} = 54V, $I_{SEC\_OUT\_DC}$ = 170A, $T_{INTERNAL}$ = 100°C	1.1	1.55	2.0	
Switching Frequency	F_{SW}	Frequency of the output voltage ripple = 2x F_{SW}	**1.02**	1.07	**1.12**	MHz
Secondary Output Voltage Ripple	$V_{SEC\_OUT\_PP}$	C_{SEC_EXT} = 0µF, $I_{SEC\_OUT\_DC}$ = 170A, V_{PRI_DC} = 54V, 20MHz BW		125		mV
		$T_{INTERNAL}$ ≤ 100°C			400	
Primary Input Leads Inductance (Parasitic)	$L_{PRI\_IN\_LEADS}$	Frequency 2.5MHz (double switching frequency), simulated lead model		3		nH
Secondary Output Leads Inductance (Parasitic)	$L_{SEC\_OUT\_LEADS}$	Frequency 2.5MHz (double switching frequency), simulated lead model		0.64		nH

Electrical Specifications (Cont.)

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Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain PRIMARY to SECONDARY Specification (Forward Direction) Cont.						
Effective Primary Capacitance (Internal)	C_{PRI_INT}	Effective value at 54V_{PRI_DC}		16.80		µF
Effective Secondary Capacitance (Internal)	C_{SEC_INT}	Effective value at 10.8V_{SEC_DC}		140		µF
Rated Secondary Output Capacitance (External)	$C_{SEC\_OUT\_EXT}$	Excessive capacitance may drive module into short circuit protection			**3000**	µF
Rated Secondary Output Capacitance (External), Parallel Array Operation	$C_{SEC\_OUT\_AEXT}$	$C_{SEC\_OUT\_AEXT}$ Max = N • 0.5 • $C_{SEC\_OUT\_EXT\ MAX}$, where N = the number of units in parallel				
Protection PRIMARY to SECONDARY (Forward Direction)						
Auto Restart Time	$t_{AUTO\_RESTART}$	Start up into a persistent fault condition. Non-latching fault detection given V_{PRI_DC} > V_{PRI_UVLO+}	**940**		**1010**	ms
Primary Overvoltage Lockout Threshold	V_{PRI_OVLO+}		**63**	66	**69**	V
Primary Overvoltage Recovery Threshold	$V_{PRI\_OVLO–}$		**60**	63	**66**	V
Primary Overvoltage Lockout Hysteresis	$V_{PRI\_OVLO\_HYST}$			3		V
Primary Overvoltage Lockout Response Time	t_{PRI_OVLO}			30		µs
Primary Undervoltage Lockout Threshold	$V_{PRI\_UVLO–}$		**28**	30	**32**	V
Primary Undervoltage Recovery Threshold	V_{PRI_UVLO+}		**32**	34	**36**	V
Primary Undervoltage Lockout Hysteresis	$V_{PRI\_UVLO\_HYST}$			4		V
Primary Undervoltage Lockout Response Time	t_{PRI_UVLO}			100		µs
Primary Undervoltage Start Up Delay	$t_{PRI\_UVLO+\_DELAY}$	From V_{PRI_DC} = V_{PRI_UVLO+} to powertrain active, EN floating (i.e., one time start up delay from application of V_{PRI_DC} to V_{SEC_DC})		30		ms
Primary Soft Start Time	$t_{PRI\_SOFT\_START}$	From powertrain active. Fast current limit protection disabled during soft start		1		ms
Secondary Output Overcurrent Trip Threshold	$I_{SEC\_OUT\_OCP}$		**201**	220	**320**	A
Secondary Output Overcurrent Response Time Constant	$t_{SEC\_OUT\_OCP}$	Effective internal RC filter		4		ms
Secondary Output Short Circuit Protection Trip Threshold	$I_{SEC\_OUT\_SCP}$		**250**			A
Secondary Output Short Circuit Protection Response Time	$t_{SEC\_OUT\_SCP}$			1		µs
Overtemperature Shutdown Threshold	t_{OTP+}	Temperature sensor located inside controller IC	**125**			°C
Overtemperature Recovery Threshold	$t_{OTP–}$		105	110	115	°C
Undertemperature Shutdown Threshold	t_{UTP}	Temperature sensor located inside controller IC; protection not available for M-Grade units.			–45	°C
Undertemperature Restart Time	$t_{UTP\_RESTART}$	Start up into a persistent fault condition. Non-latching fault detection given V_{PRI_DC} > V_{PRI_UVLO+}		3		s

Electrical Specifications (Cont.)

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Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain SECONDARY to PRIMARY Specification (Reverse Direction)						
Secondary Input Voltage Range (Continuous)	V_{SEC_DC}		**7.2**		**12.0**	V
SEC to PRI No Load Power Dissipation	P_{SEC_NL}	V_{SEC_DC} = 10.8V, $T_{INTERNAL}$ = 25°C		10	12	W
		V_{SEC_DC} = 10.8V	**8.0**		**19**	
		V_{SEC_DC} = 7.2 – 12.0V, $T_{INTERNAL}$ = 25°C			14	
		V_{SEC_DC} = 7.2 – 12.0V			**22**	
DC Secondary Input Current	$I_{SEC\_IN\_DC}$	At I_{PRI_DC} = 34A, $T_{INTERNAL}$ ≤ 100°C			**172**	A
Primary Output Current (Continuous)	$I_{PRI\_OUT\_DC}$				**34**	A
Primary Output Current (Pulsed)	$I_{PRI\_OUT\_PULSE}$	10ms pulse, 25% duty cycle, $I_{PRI\_OUT\_AVG}$ ≤ 50% rated $I_{PRI\_OUT\_DC}$			**40.8**	A
SEC to PRI Efficiency (Ambient)	η_{AMB}	V_{SEC_DC} = 10.8V, $I_{PRI\_OUT\_DC}$ = 34A	96.1	97.1		%
		V_{SEC_DC} = 7.2 – 12.0V, $I_{PRI\_OUT\_DC}$ = 34A	94.9			
		V_{SEC_DC} = 10.8V, $I_{PRI\_OUT\_DC}$ = 17A	97.3	98		
SEC to PRI Efficiency (Hot)	η_{HOT}	V_{SEC_DC} = 10.8V, $I_{PRI\_OUT\_DC}$ = 34A	96.3	97		%
SEC to PRI Efficiency (Over Load Range)	$\eta_{20\%}$	6.80A < $I_{PRI\_OUT\_DC}$ < 34A	**90**			%
SEC to PRI Output Resistance	R_{PRI_COLD}	V_{SEC_DC} = 10.8V, $I_{PRI\_OUT\_DC}$ = 34A, $T_{INTERNAL}$ = –40°C	22	30	38	mΩ
	R_{PRI_AMB}	V_{SEC_DC} = 10.8V, $I_{PRI\_OUT\_DC}$ = 34A	28	42	56	
	R_{PRI_HOT}	V_{SEC_DC} = 10.8V, $I_{PRI\_OUT\_DC}$ = 34A, $T_{INTERNAL}$ = 100°C	36	45	54	
Primary Output Voltage Ripple	$V_{PRI\_OUT\_PP}$	$C_{PRI\_OUT\_EXT}$ = 0µF, $I_{PRI\_OUT\_DC}$ = 34A, V_{SEC_DC} = 10.8V, 20MHz BW		625		mV
		$T_{INTERNAL}$ ≤ 100°C			**1500**	

Electrical Specifications (Cont.)

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Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Protection SECONDARY to PRIMARY (Reverse Direction)						
Effective Primary Output Capacitance (External)	$C_{PRI\_OUT\_EXT}$	Excessive capacitance may drive module into short circuit protection when starting from Secondary to Primary			**100**	µF
Secondary Overvoltage Lockout Threshold	V_{SEC_OVLO+}		**12.8**	13.2	**13.6**	V
Secondary Overvoltage Recovery Threshold	V_{PRI_OVLO-}		**12**	12.6	**13.2**	V
Secondary Overvoltage Lockout Response Time	t_{PRI_OVLO}			30		µs
Secondary Undervoltage Lockout Threshold	V_{SEC_UVLO-}		**5.6**	6	**6.4**	V
Secondary Undervoltage Recovery Threshold	V_{PRI_UVLO+-}		**6.4**	6.8	**7.2**	V
Secondary Undervoltage Lockout Response Time	t_{SEC_UVLO}			100		µs
Primary Output Overcurrent Trip Threshold	$I_{PRI\_OUT\_OCP}$	Powertrain is stopped but current can flow from Secondary to Primary through MOSFET body diodes	**40**	44	**64**	A
Primary Output Overcurrent Response Time Constant	$t_{PRI\_OUT\_OCP}$	Effective internal RC filter		4		ms
Primary Short Circuit Protection Trip Threshold	I_{PRI_SCP}	Powertrain is stopped but current can flow from Secondary to Primary through MOSFET body diodes	**50**			A
Primary Short Circuit Protection Response Time	t_{PRI_SCP}			1		µs

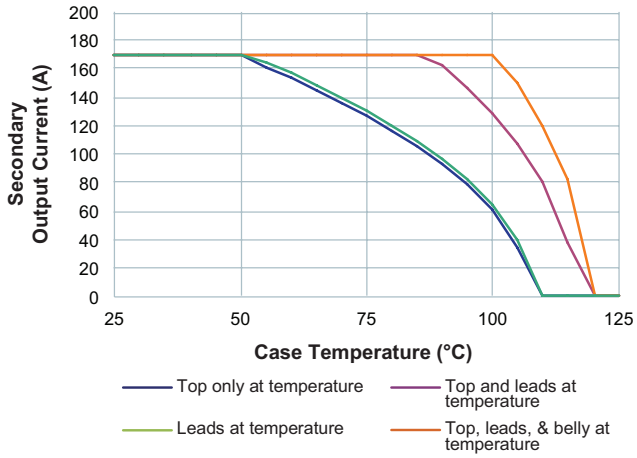


Figure 1 — *Specified thermal operating area*

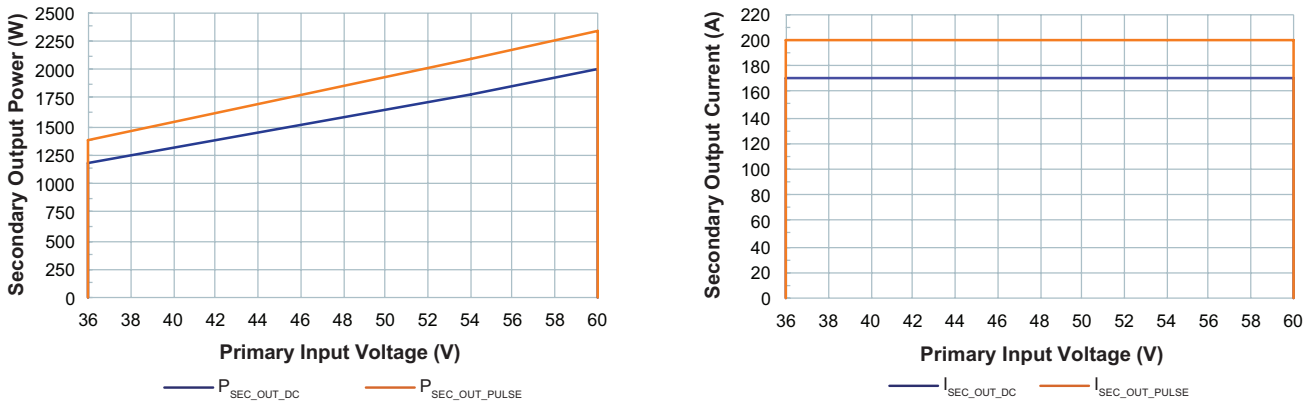


Figure 2 — *Specified electrical operating area using rated R_{SEC_HOT}*

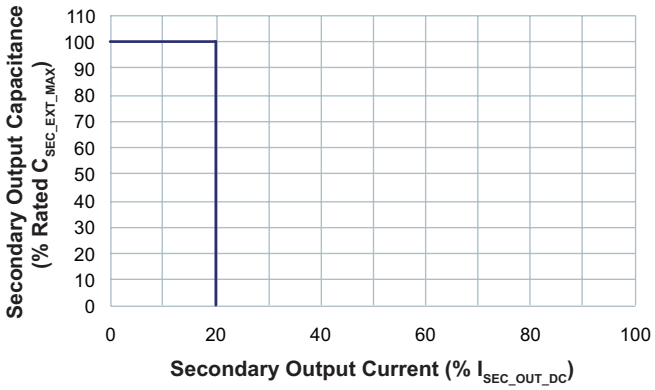


Figure 3 — *Specified primary start up into load current and external capacitance*

Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Temperature Monitor

- The TM pin is a standard analog I/O configured as an output from an internal µC.
- The TM pin monitors the internal temperature of the controller IC within an accuracy of ±5°C.
- µC 250kHz PWM output internally pulled high to 3.3V.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
DIGITAL OUTPUT	Start Up	Powertrain Active to TM Time	t_{TM}			**100**		µs
	Regular Operation	TM Duty Cycle	TM_{PWM}		**18.18**		**68.18**	%
		TM Current	I_{TM}				**4**	mA
		Recommended External filtering						
		TM Capacitance (External)	C_{TM_EXT}	Recommended External filtering		0.01		µF
		TM Resistance (External)	R_{TM_EXT}	Recommended External filtering		1		kΩ
		Specifications using recommended filter						
		TM Gain	A_{TM}			10		mV / °C
		TM Voltage Reference	V_{TM_AMB}	Internal temperature = 27°C		1.27		V
		TM Voltage Ripple	V_{TM_PP}	R_{TM_EXT} = 1kΩ, C_{TM_EXT} = 0.01µF, V_{PRI_DC} = 54V, I_{SEC_DC} = 170A		28		mV
				$T_{INTERNAL}$ ≤ 100°C			40	

Enable / Disable Control

- The EN pin is a standard analog I/O configured as an input to an internal µC.
- It is internally pulled high to 3.3V.
- When held low, the NBM internal bias will be disabled and the powertrain will be inactive.
- In an array of NBMs, EN pins should be interconnected to synchronize start up.
- Unit must not be disabled if a load is present on $+V_{PRI}$ while in reverse operation.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	Start Up	EN to Powertrain active time	t_{EN_START}	V_{PRI_DC} > V_{PRI_UVLO+}, EN held low both conditions satisfied for T > $t_{PRI\_UVLO+\_DELAY}$		**10**		ms
	Regular Operation	EN Voltage Threshold	V_{EN_TH}		**2.3**			V
		EN Resistance (Internal)	R_{EN_INT}	Internal pull up resistor		1.5		kΩ
		EN Disable Threshold	$V_{EN\_DISABLE\_TH}$				**1**	V

Signal Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Auxiliary Voltage Source

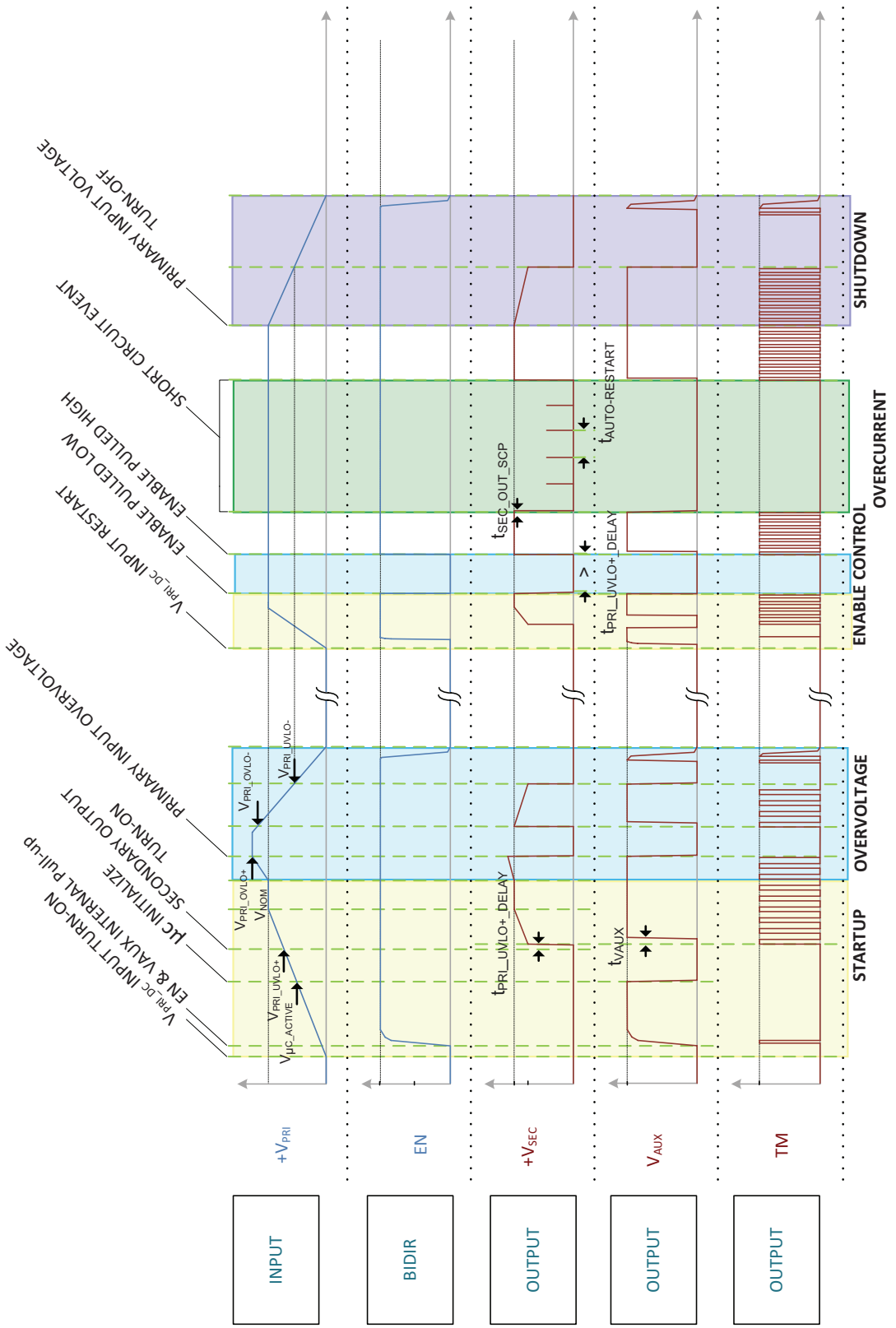
- The VAUX pin is a standard analog I/O configured as an output from an internal µC.
- VAUX is internally connected to µC output and internally pulled high to a 3.3V regulator with 2% tolerance, a 1% resistor of 1.5kΩ.
- VAUX can be used as a "Ready to process full power" flag. This pin transitions VAUX voltage after a 2ms delay from the start of powertrain activating, signaling the end of softstart.
- VAUX can be used as "Fault flag". This pin is pulled low internally when a fault protection is detected.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Start Up	Powertrain active to VAUX time	t_{VAUX}	Powertrain active to VAUX High		**2**		ms
	Regular Operation	VAUX Voltage	V_{VAUX}		**2.8**		**3.3**	V
		VAUX Available Current	I_{VAUX}				**4**	mA
		VAUX Voltage Ripple	V_{VAUX_PP}			50		mV
				$T_{INTERNAL}$ ≤ 100°C			**100**	
		VAUX Capacitance (External)	C_{VAUX_EXT}				0.01	µF
		VAUX Resistance (External)	R_{VAUX_EXT}	$V_{PRI\_DC} < V_{µC\_ACTIVE}$	1.5			kΩ
	Fault	VAUX Fault Response Time	t_{VAUX_FR}	From fault to V_{VAUX} = 2.8V, C_{VAUX} = 0pF		10		µs

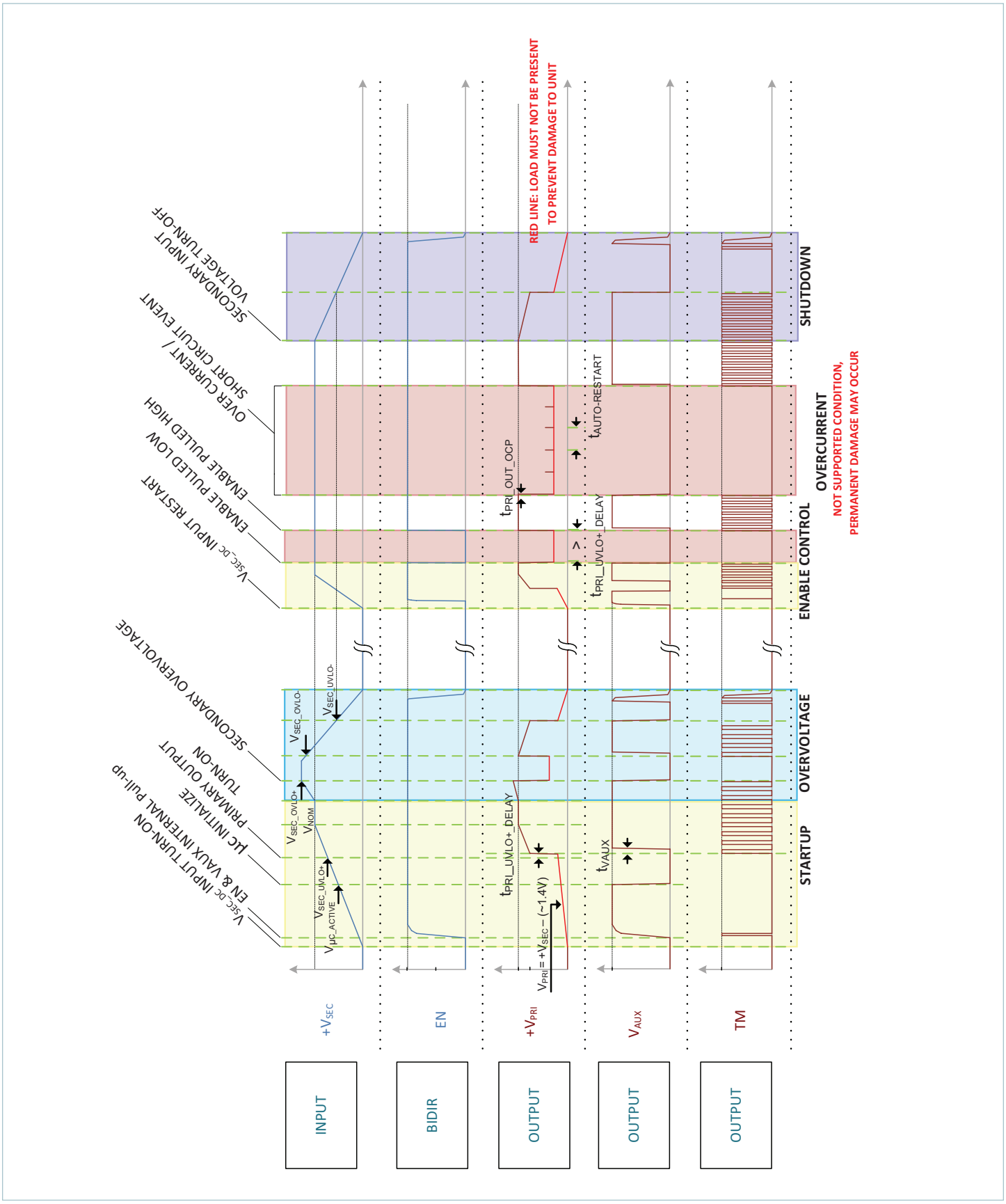
Signal Ground

- Signal ground is internally connect to PGND through a zero ohm resistor.
- Internal SGND traces are not designed to support high current.

NBM Forward Direction Timing Diagram

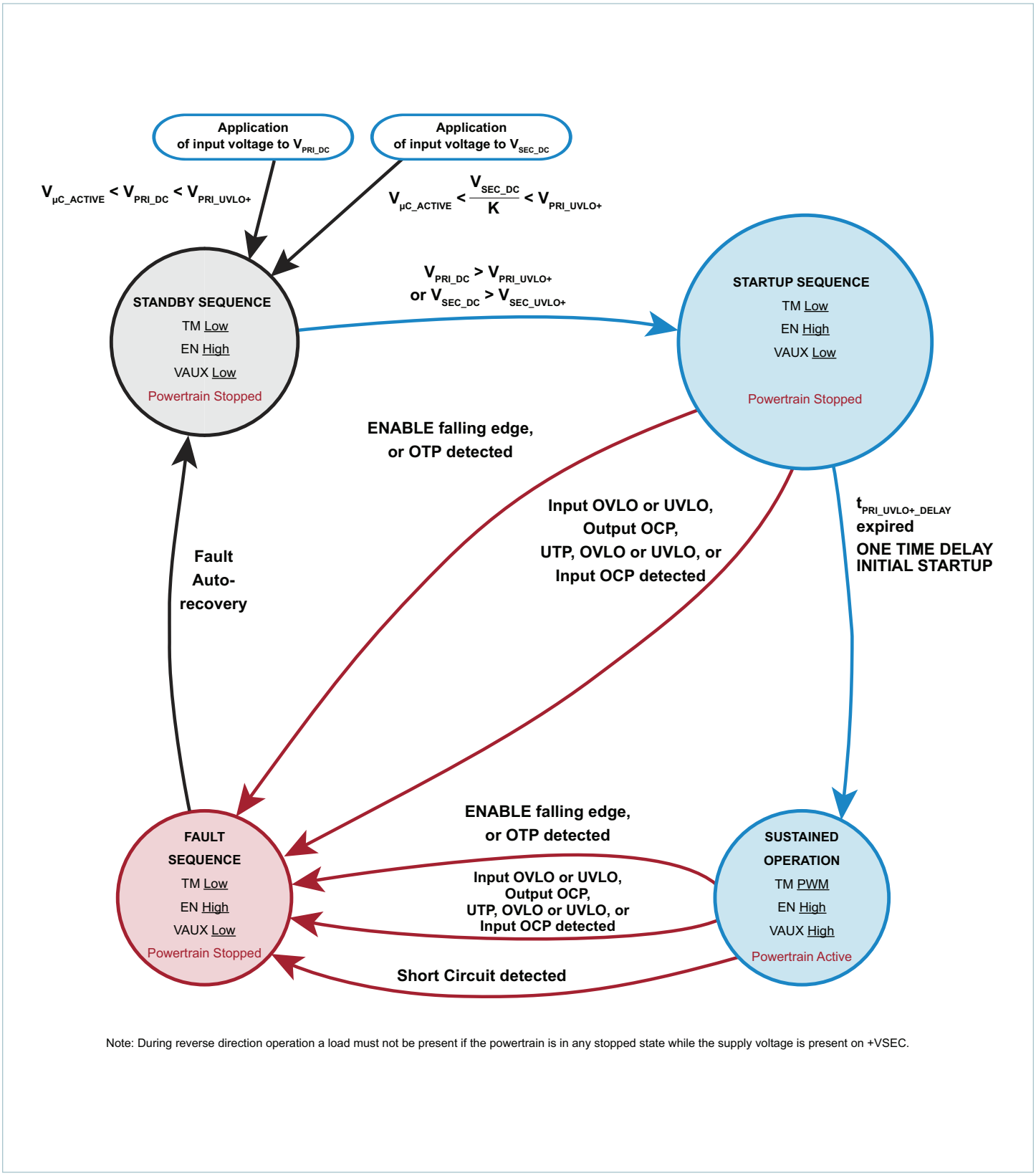


NBM Reverse Direction Timing Diagram



High Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



Note: During reverse direction operation a load must not be present if the powertrain is in any stopped state while the supply voltage is present on +VSEC.

Application Characteristics

Temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected from primary sourced units processing power in forward direction. See associated figures for general trend data.

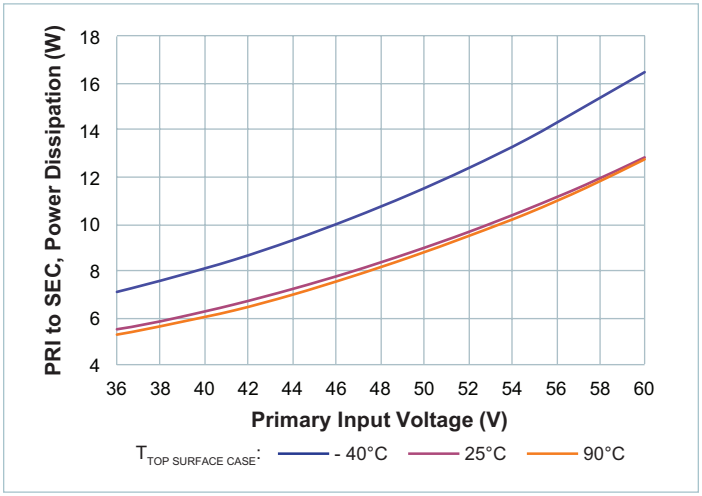


Figure 4 — *No load power dissipation vs. V_{PRI_DC}*

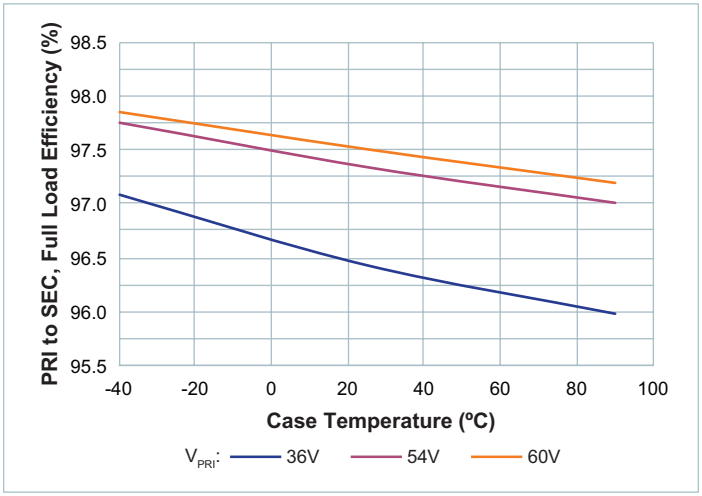


Figure 5 — *Full load efficiency vs. temperature; V_{PRI_DC}*

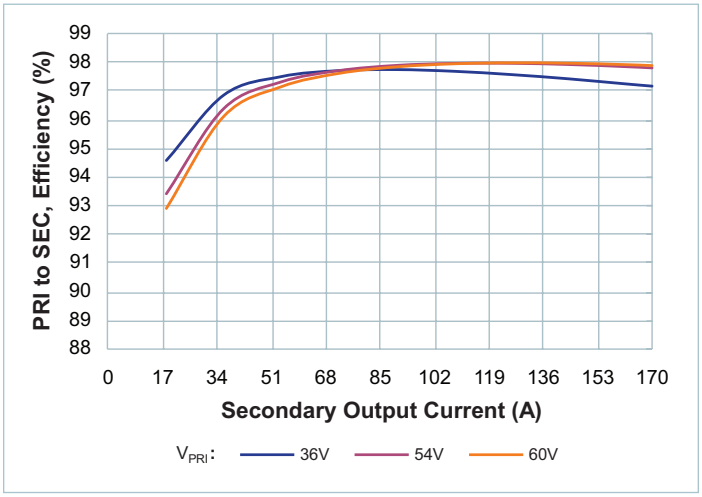


Figure 6 — *Efficiency at T_{CASE} = –40°C*

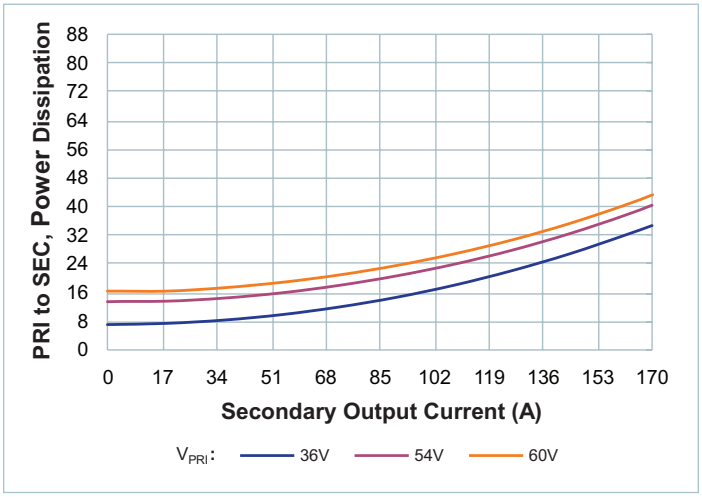


Figure 7 — *Power dissipation at T_{CASE} = –40°C*

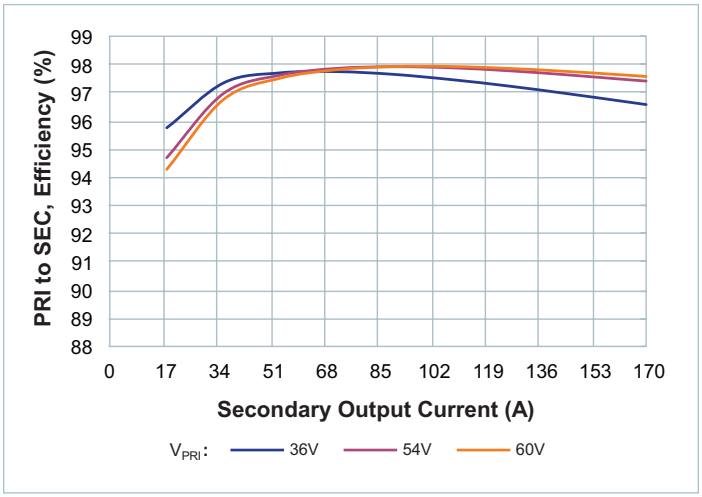


Figure 8 — *Efficiency at T_{CASE} = 25°C*

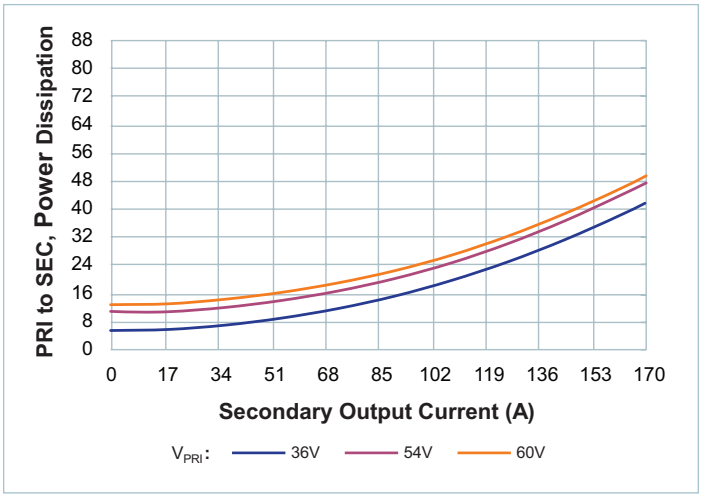


Figure 9 — *Power dissipation at T_{CASE} = 25°C*

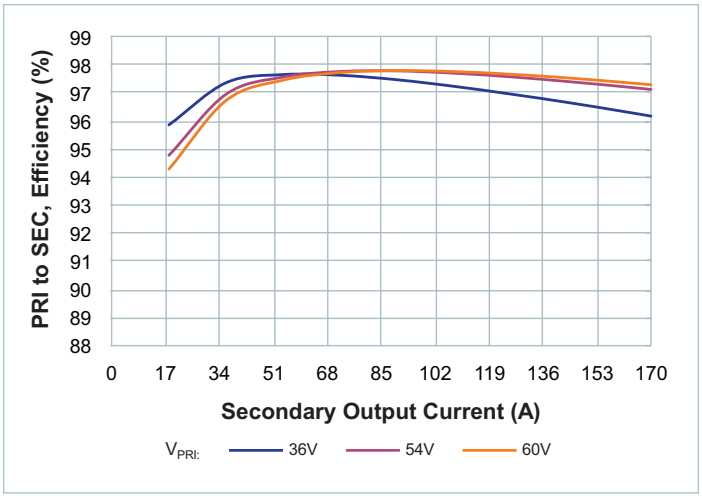


Figure 10 — *Efficiency at T_{CASE} = 90°C*

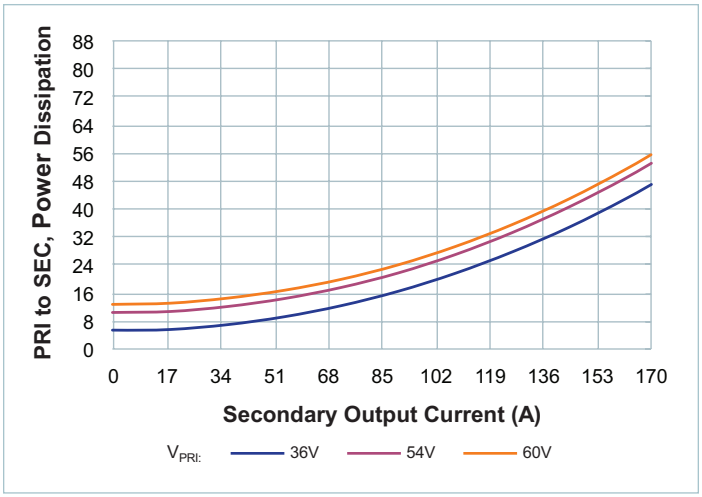


Figure 11 — *Power dissipation at T_{CASE} = 90°C*

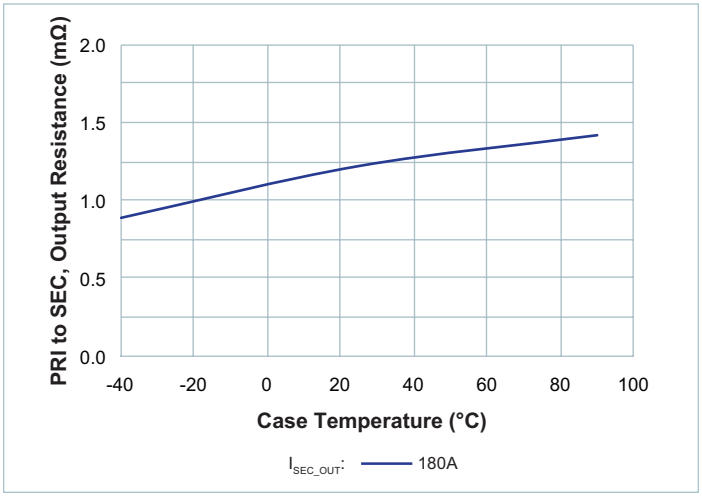


Figure 12 — *R_{SEC} vs. temperature; Nominal V_{PRI_DC} I_{SEC_DC} = 100A at T_{CASE} = 90°C*

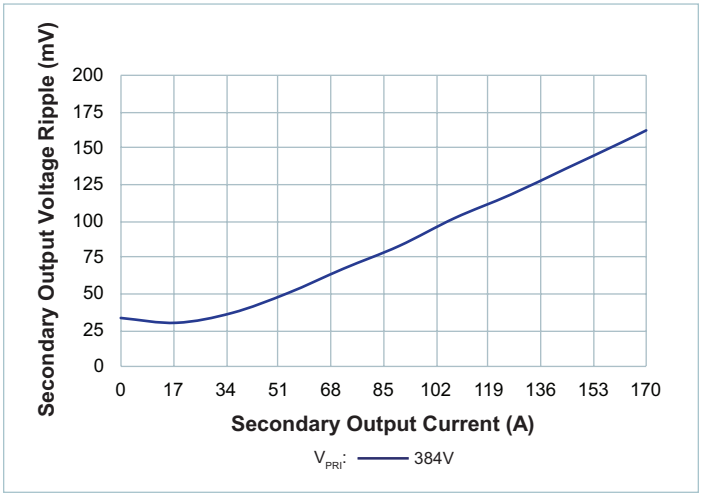


Figure 13 — *$V_{SEC\_OUT\_PP}$ vs. I_{SEC_DC} ; No external $C_{SEC\_OUT\_EXT.}$ Board mounted module, scope setting: 20MHz analog BW*

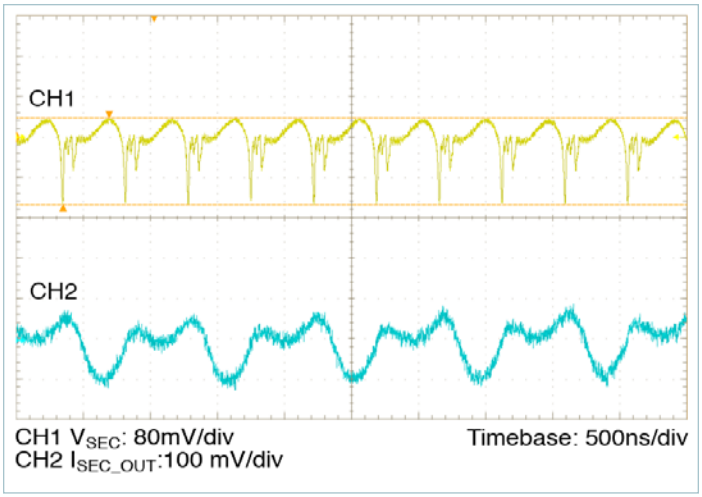


Figure 14 — *Full load secondary voltage ripple, 270µF $C_{PRI\_IN\_EXT}$; No external $C_{SEC\_IN\_EXT}$. Board mounted module, scope setting: 20MHz analog BW*

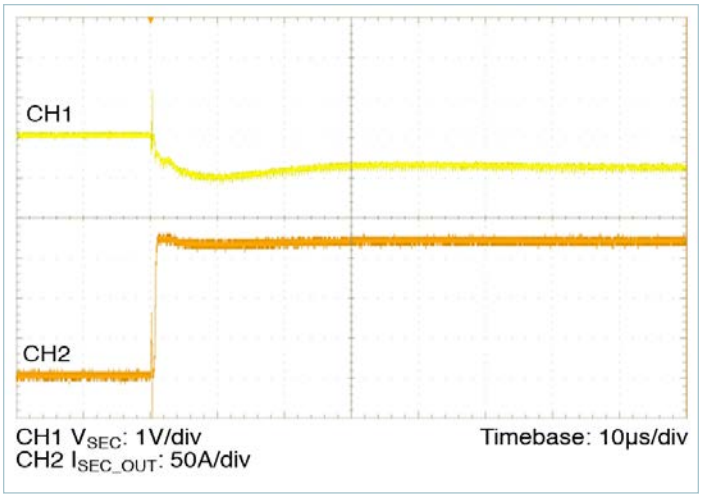


Figure 15 — *0 – 170A transient response: $C_{PRI\_IN\_EXT}$ = 270µF, no external $C_{SEC\_OUT\_EXT}$*

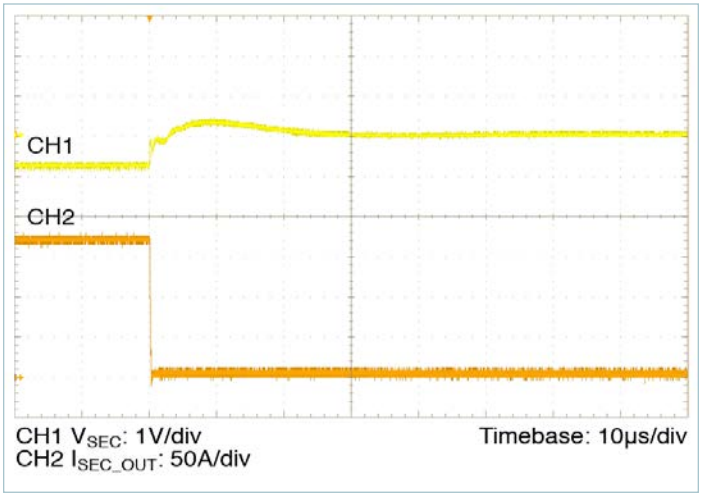


Figure 16 — *170 – 0A transient response: $C_{PRI\_IN\_EXT}$ = 270µF, no external $C_{SEC\_OUT\_EXT}$*

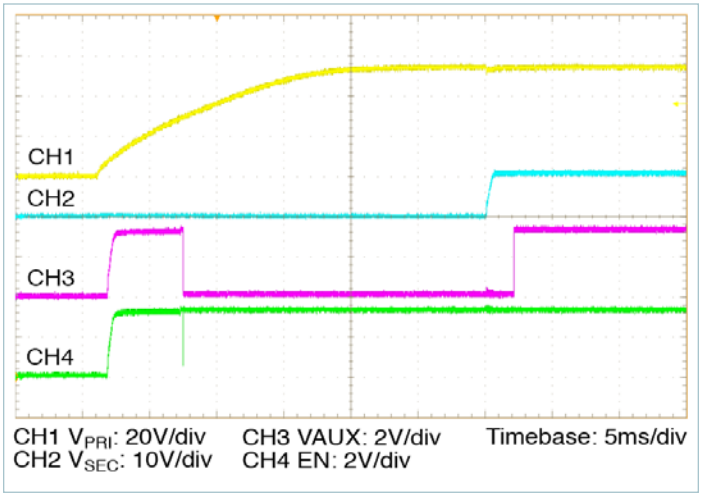


Figure 17 — *Start up from application of V_{PRI_DC} = 54V, 20% $I_{SEC\_OUT\_DC}$, 100% $C_{SEC\_OUT\_EXT}$*

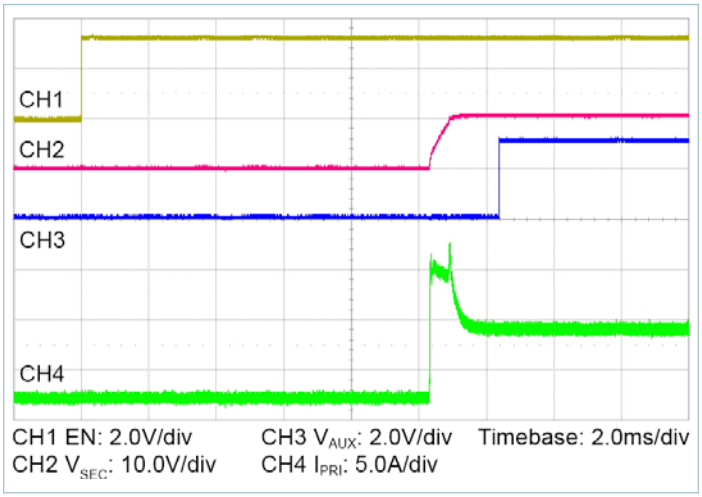


Figure 18 — *Start up from application of EN with pre-applied V_{PRI_DC} = 54V, 20% $I_{SEC\_OUT\_DC}$, 100% $C_{SEC\_OUT\_EXT}$*

General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		60.87 [2.396]	61.00 [2.402]	61.13 [2.407]	mm [in]
Width	W		24.76 [0.975]	25.14 [0.990]	25.52 [1.005]	mm [in]
Height	H		7.11 [0.280]	7.21 [0.284]	7.31 [0.288]	mm [in]
Volume	Vol	Without heatsink		11.06 [0.675]		cm^3 [in^3]
Weight	W			41 [1.45]		g [oz]
Lead Finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
Thermal						
Operating Temperature	$T_{INTERNAL}$	NBM6123T60E12A7T0R (T-Grade)	–40		125	°C
Thermal Resistance Top Side	$\theta_{INT-TOP}$	Estimated thermal resistance to maximum temperature internal component from isothermal top		1.28		°C/W
Thermal Resistance Leads	$\theta_{INT-LEADS}$	Estimated thermal resistance to maximum temperature internal component from isothermal leads		1.24		°C/W
Thermal Resistance Bottom Side	$\theta_{INT-BOTTOM}$	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		1.18		°C/W
Thermal Capacity				34		Ws/°C
Assembly						
Storage Temperature		NBM6123T60E12A7T0R (T-Grade)	–40		125	°C
ESD Withstand	ESD_{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2kV)				
	ESD_{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V)				

General Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Soldering [b]						
Peak Temperature Top Case					135	°C
Safety						
Isolation voltage / Dielectric Test	V_{HIPOT}	PRIMARY to SECONDARY	**N/A**			V
		PRIMARY to CASE	**2250**			
		SECONDARY to CASE	**2250**			
Isolation Capacitance	C_{PRI_SEC}	Unpowered Unit	**N/A**	N/A	**N/A**	pF
Insulation Resistance	R_{PRI_SEC}	At 500V_{DC}	**0**			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		3.34		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		5.26		MHrs
Agency Approvals / Standards		cTÜVus EN 60950-1				
		cURus UL 60950-1				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

[b] Product is not intended for reflow solder attach.

NBM in a ChiP

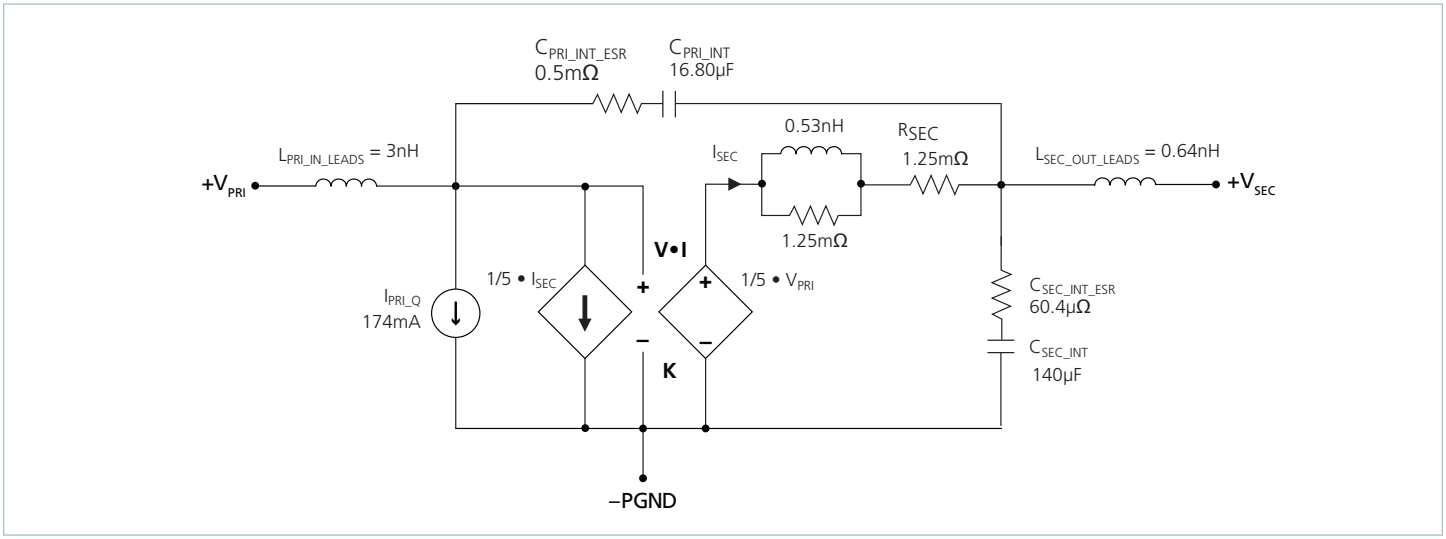


Figure 19 — *NBM AC model*

The NBM uses a high frequency resonant tank to move energy from primary to secondary and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of the primary voltage and the secondary current. A small amount of capacitance embedded in the primary and secondary stages of the module is sufficient for full functionality and is key to achieving high power density.

The NBM6123x60E12A7yzz can be simplified into the model shown in Figure 19.

At no load:

$$V_{SEC} = V_{PRI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the NBM.
Rearranging Eq (1):

$$K = \frac{V_{SEC}}{V_{PRI}} \qquad (2)$$

In the presence of a load, V_{SEC} is represented by:

$$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R_{SEC} \qquad (3)$$

and I_{SEC} is represented by:

$$I_{SEC} = \frac{I_{PRI} - I_{PRI\_Q}}{K} \qquad (4)$$

R_{SEC} represents the impedance of the NBM, and is a function of the R_{DS_ON} of the primary and secondary MOSFETs and the winding resistance of the power transformer. I_{PRI_Q} represents the quiescent current of the NBM controller, gate drive circuitry and core losses.

The effective DC voltage transformer action provides additional interesting attributes. Assuming that R_{SEC} = 0Ω and I_{PRI_Q} = 0A, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with V_{PRI}.

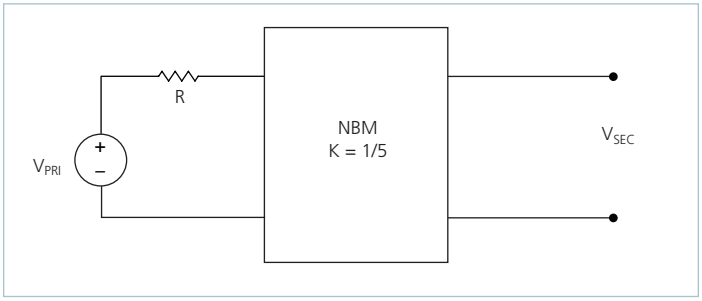


Figure 20 — *K = 1/5 NBM with series primary resistor*

The relationship between V_{PRI} and V_{SEC} becomes:

$$V_{SEC} = \left(V_{PRI} - I_{PRI} \bullet R\right) \bullet K \qquad (5)$$

Substituting the simplified version of Eq. (4) (I_{PRI_Q} is assumed = 0A) into Eq. (5) yields:

$$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Eq. (3), where R_{SEC} is used to represent the characteristic impedance of the NBM. However, in this case a real resistor, R, on the primary side of the NBM is effectively scaled by K^2 with respect to the secondary.

Assuming that R = 1Ω, the effective R as seen from the secondary side is 40mΩ, with K = 1/5.

A similar exercise can be performed with the additon of a capacitor or shunt impedance at the primary of the NBM. A switch in series with V_{PRI} is added to the circuit. This is depicted in Figure 21.

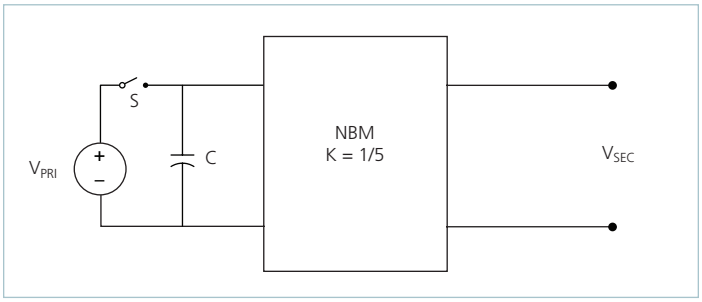


Figure 21 — *NBM with primary capacitor*

A change in V_{PRI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\,\frac{dV_{PRI}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{PRI}, the switch is opened and the capacitor is discharged through the idealized NBM. In this case,

$$I_C = I_{SEC} \bullet K \qquad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{SEC}(t) = \frac{C}{K^2} \bullet \frac{dV_{SEC}}{dt} \qquad (9)$$

The equation in terms of the secondary has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the secondary when expressed in terms of the primary. With K = 1/5 as shown in Figure 21, C = 1µF would appear as C = 25µF when viewed from the secondary.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a NBM between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, these benefits are not achieved if the series impedance of the NBM is too high. The impedance of the NBM must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the NBM low involves switching at a high frequency. This enables the use of small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the NBM are:

- No load power dissipation (P_{PRI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{SEC}}$): refers to the power loss across the NBM modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{PRI\_NL} + P_{R_{SEC}} \qquad (10)$$

Therefore,

$$P_{SEC\_OUT} = P_{PRI\_IN} - P_{DISSIPATED} = P_{PRI\_IN} - P_{PRI\_NL} - P_{R_{SEC}} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{SEC\_OUT}}{P_{PRI\_IN}} = \frac{P_{PRI\_IN} - P_{PRI\_NL} - P_{R_{SEC}}}{P_{PRI\_IN}} \qquad (12)$$

$$= \frac{V_{PRI} \bullet I_{PRI} - P_{PRI\_NL} - (I_{SEC})^2 \bullet R_{SEC}}{V_{PRI} \bullet I_{PRI}}$$

$$= 1 - \left(\frac{P_{PRI\_NL} + (I_{SEC})^2 \bullet R_{SEC}}{V_{PRI} \bullet I_{PRI}} \right)$$

Input and Output Filter Design

A major advantage of NBM systems versus conventional PWM converters is that the auto-transformer based NBM does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of primary voltage and secondary current and efficiently transfers charge through the auto-transformer. A small amount of capacitance embedded in the primary and secondary stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- *Guarantee low source impedance:*

  To take full advantage of the NBM's dynamic response, the impedance presented to its primary terminals must be low from DC to approximately 5MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the primary should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be as high as 1µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

- *Further reduce primary and/or secondary voltage ripple without sacrificing dynamic response:*

  Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the primary source will appear at the secondary of the module multiplied by its K factor.

- *Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:*

  The module primary/secondary voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating primary range. Even when disabled, the powertrain is exposed to the applied voltage and the power MOSFETs must withstand it.

Total load capacitance of the NBM module shall not exceed the specified maximum. Owing to the wide bandwidth and low secondary impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the primary of the module. At frequencies <500kHz the module appears as an impedance of R_{SEC} between the source and load.

Within this frequency range, capacitance at the primary appears as effective capacitance on the secondary per the relationship defined in Eq. (13).

$$C_{SEC\_EXT} = \frac{C_{PRI\_EXT}}{K^2} \qquad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Thermal Considerations

The ChiP module provides a high degree of flexibility in that it presents three pathways to remove heat from the internal power dissipating components. Heat may be removed from the top surface, the bottom surface and the leads. The extent to which these three surfaces are cooled is a key component in determining the maximum curent that is available from a ChiP, as can be seen from Figure 1.

Since the ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. Given that there are three pathways to remove heat from the ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 22 shows the "thermal circuit" for a 6123 ChiP NBM in an application where the top, bottom, and leads are cooled. In this case, the NBM power dissipation is PD_{TOTAL} and the three surface temperatures are represented as T_{CASE_TOP}, T_{CASE_BOTTOM}, and T_{LEADS}. This thermal system can now be very easily analyzed using a SPICE simulator with simple resistors, voltage sources, and a current source. The results of the simulation provide an estimate of heat flow through the various dissipation pathways as well as internal temperature.

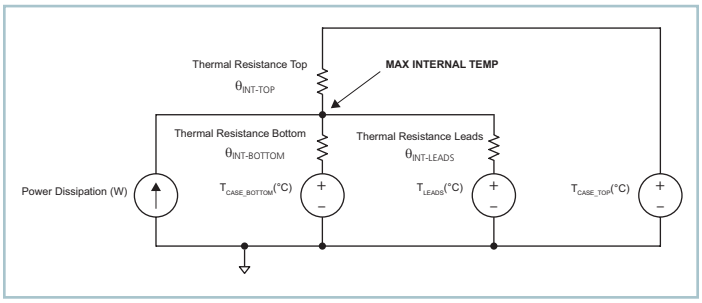


Figure 22 — *Top case, Bottom case and leads thermal model*

Alternatively, equations can be written around this circuit and analyzed algebraically:

$$T_{INT} - PD_1 \bullet \theta_{INT\text{-}TOP} = T_{CASE\_TOP}$$

$$T_{INT} - PD_2 \bullet \theta_{INT\text{-}BOTTOM} = T_{CASE\_BOTTOM}$$

$$T_{INT} - PD_3 \bullet \theta_{INT\text{-}LEADS} = T_{LEADS}$$

$$PD_{TOTAL} = PD_1 + PD_2 + PD_3$$

Where T_{INT} represents the internal temperature and PD_1, PD_2, and PD_3 represent the heat flow through the top side, bottom side, and leads, respectively.

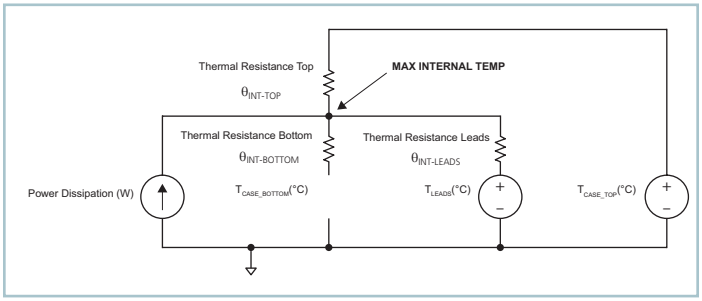


Figure 23 — *Top case and leads thermal model*

Figure 23 shows a scenario where there is no bottom side cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$$T_{INT} - PD_1 \bullet \theta_{INT\text{-}TOP} = T_{CASE\_TOP}$$

$$T_{INT} - PD_3 \bullet \theta_{INT\text{-}LEADS} = T_{LEADS}$$

$$PD_{TOTAL} = PD_1 + PD_3$$

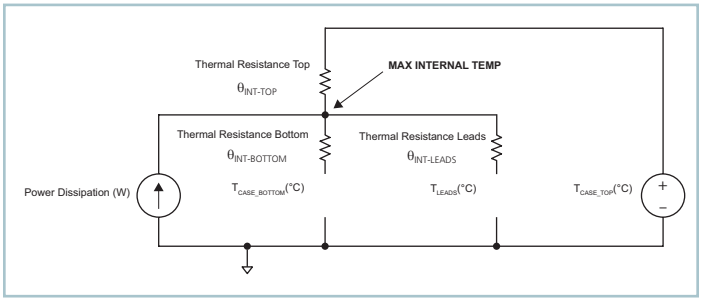


Figure 24 — *Top case thermal model*

Figure 24 shows a scenario where there is no bottom side and leads cooling. In this case, the heat flow paths to the bottom and leads are left open and the equations now simplify to:

$$T_{INT} - PD_1 \bullet \theta_{INT\text{-}TOP} = T_{CASE\_TOP}$$

$$PD_{TOTAL} = PD_1$$

Please note that Vicor has a suite of online tools, including a simulator and thermal estimator that greatly simplify the task of determining whether or not a NBM thermal configuration is valid for a given condition. These tools can be found at: http://www.vicorpower.com/powerbench.

Current Sharing

The performance of the NBM topology is based on efficient transfer of energy through a auto-transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal auto-transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple NBMs of a given part number are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load. Ensuring equal current sharing among modules requires that NBM array impedances be matched.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- A dedicated input filter for each NBM in an array is required to prevent circulating currents.

For further details see:
AN:016 Using BCM Bus Converters in High Power Arrays

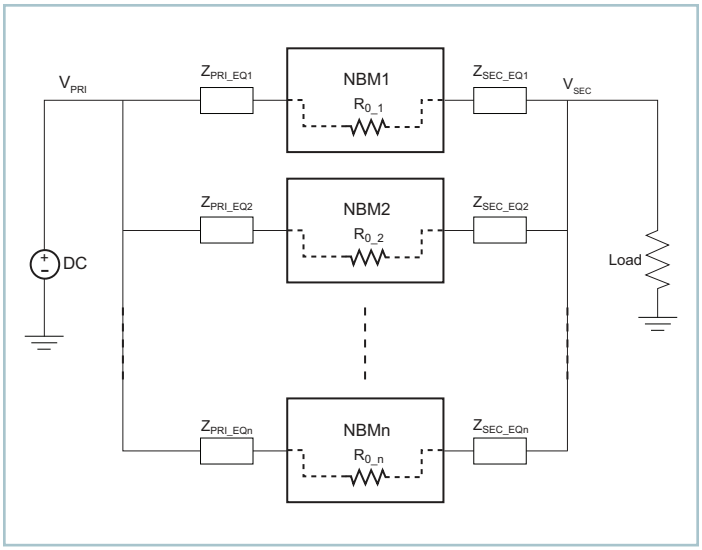


Figure 25 — *NBM parallel array*

Fuse Selection

In order to provide flexibility in configuring power systems, ChiP modules are not internally fused. Input line fusing of ChiP products is recommended at the system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of NBM)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: ≤ 60A Littelfuse TLS Series or Littelfuse 456 Series rated 40A (primary side)

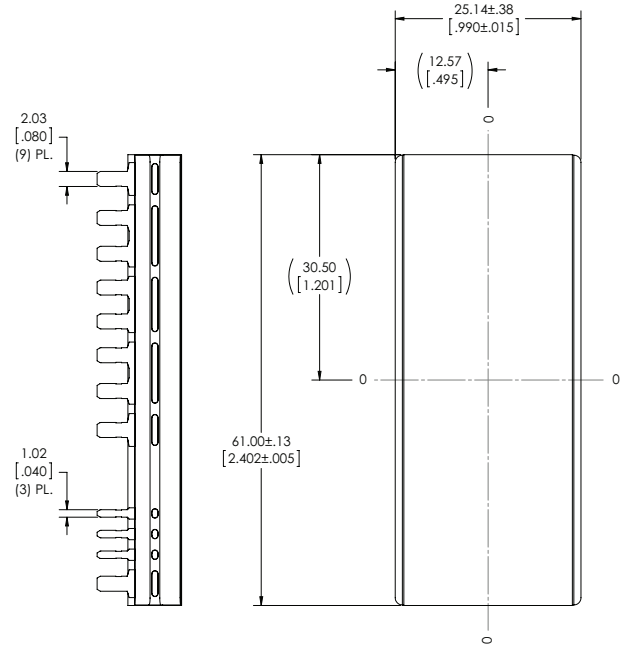
Start Up and Reverse Operation

The NBM6123T60E12A7T0R is capable of start up in forward and reverse direction once the applied voltage is greater than the undervoltage lockout threshold.

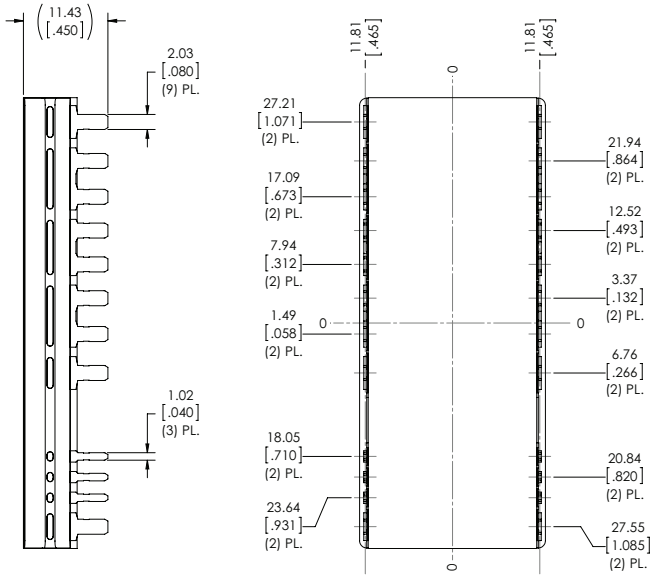
The non-isolated bus converter modules are capable of reverse power operation. Once the unit is enabled, energy can be transferred from secondary back to the primary whenever the secondary voltage exceeds $V_{PRI} \bullet K$. The module will continue operation in this fashion for as long as no faults occur.

Start up loading must be set to no greater than 20% of rated max current respectively in the forward or reverse direction. A load must not be present on the $+V_{PRI}$ pin if the powertrain is not actively switching. Primary side MOSFET body diode conduction will occur if the unit stops switching while a load is present on the $+V_{PRI}$ and $+V_{SEC}$ voltage is two diodes drop higher than $+V_{PRI}$. Remove the $+V_{PRI}$ load prior to disabling the module using EN pin, +SEC power or prior to faults.

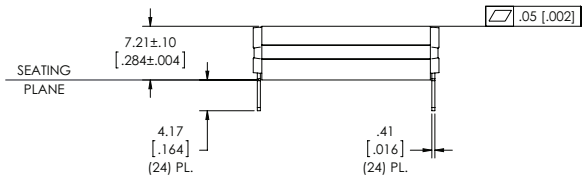
NBM Through Hole Package Mechanical Drawing and Recommended Land Pattern



TOP VIEW (COMPONENT SIDE)

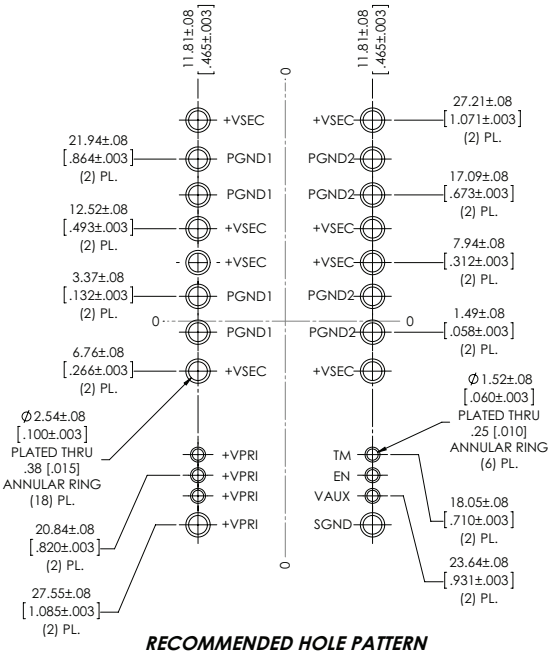


BOTTOM VIEW



NOTES:

1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.
2- UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE : INCH / [MM]



RECOMMENDED HOLE PATTERN
(COMPONENT SIDE)

Revision History

Revision	Date	Description	Page Number(s)
1.0	09/08/15	Initial Release	n/a
1.1	09/28/15	Changed PRI to SEC Input Quiescent Current Added certifications	5 1 & 15
1.2	07/26/16	Removed redundant information Updated information	new 19 All
1.3	08/29/16	Corrected the Secondary Output Overcurrent Response Time Constant Specification	6
1.4	09/12/2016	Corrected the enable to powertrain active time	10
1.5	05/26/17	Efficiency and bidirectional start up and steady state summary points added Content improvements	1 All
1.6	07/28/17	Updated height specifications	1, 10, 24
1.7	09/21/17	Updated overcurrent protection specifications	6, 8
1.8	11/22/17	Updated TM voltage reference note	10

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