SN74AHCT1G08 Single 2-Input Positive-AND Gate

1 Features

- Operating Range: 4.5 V to 5.5 V
- Maximum t_{pd} of 7.1 ns at 5 V
- Low Power Consumption: Maximum I_{CC} of 10-µA
- ±8-mA Output Drive at 5 V
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- TV, Set-Top Box, and Audio
- Wireless Infrastructure
- Factory Automation and Control
- PC and Notebooks
- Building Automation
- Grid Infrastructure
- Medical, Healthcare, and Fitness
- Printers
- Test and Measurement
- EPOS (Electronic Point of Sale)
- Telecom Infrastructure
- Projectors

3 Description

The SN74AHCT1G08 device is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \times B$ or $Y = \overline{A + B}$ in positive logic. Low I_{CC} current allows this device to be used in power-sensitive or battery-powered applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74AHCT1G08	DBV (SOT-23, 5)	2.8 mm × 2.8 mm
	DCK (SC70, 5)	2.00 mm × 1.25 mm
	DRL (SOT, 5)	1.60 mm x 1.6 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Logic Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Q (April 2016) to Revision R (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated thermal values for DCK package from RθJA = 277.5 to 289.2, RθJC(top) = 92.9 to 205.8, RθJB = 64.2 to 176.2, ΨJT = 1.9 to 117.6, ΨJB = 63.5 to 175.1, RθJC(bot) = N/A, all values in °C/W	5

Changes from Revision P (May 2013) to Revision Q (April 2016)	Page
• Added *Applications* section, *Device Information* table, *Table of Contents*, *Pin Configuration and Functions* section, *Specifications* section, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics* section, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

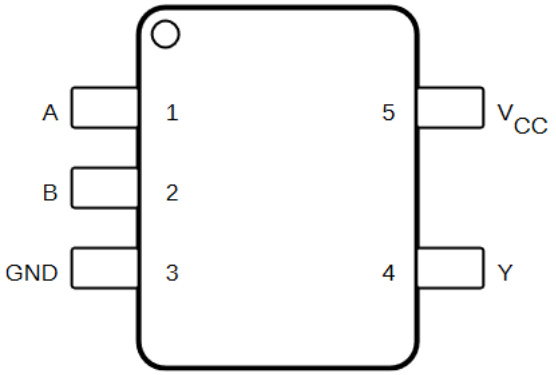


Figure 5-1. DBV, DCK, and DRL Packages 5-Pin SOT-23, SC70, and SOT (Top View)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
GND	3	—	Ground Pin
V_{CC}	5	—	Supply Pin
Y	4	O	Output

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Output voltage(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
Δt/Δv	Input transition rise and fall rate		20	ns/V
T_A	Operating free-air temperature	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC[1]		SN74AHCT1G08			UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	226	289.2	242.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	165	205.8	77.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.1	176.2	77.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	45.5	117.6	9.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.3	175.1	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bot) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –50 µA, V_{CC} = 4.5 V	T_A = 25°C	4.4	4.5		V
			T_A = –40°C to 125°C	4.4			
		I_{OH} = –8 mA, V_{CC} = 4.5 V	T_A = 25°C	3.94			
			T_A = –40°C to 125°C	3.8			
V_{OL}	Low-level output voltage	I_{OL} = 50 µA, V_{CC} = 4.5 V				0.1	V
		I_{OL} = 8 mA, V_{CC} = 4.5 V	T_A = 25°C			0.36	
			T_A = –40°C to 125°C			0.44	
I_I	Input current	V_I = 5.5 V or GND, V_{CC} = 0 V to 5.5 V	T_A = 25°C			±0.1	µA
			T_A = –40°C to 125°C			±1	
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0, V_{CC} = 5.5 V	T_A = 25°C			1	µA
			T_A = –40°C to 125°C			10	
ΔI_{CC} [1]	Change in supply current	One input at 3.4 V, Other Inputs at V_{CC} or GND, V_{CC} = 5.5 V	T_A = 25°C			1.35	mA
			T_A = –40°C to 125°C			1.5	
C_I	Input capacitance	V_I = V_{CC} or GND, V_{CC} = 5 V			4	10	pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

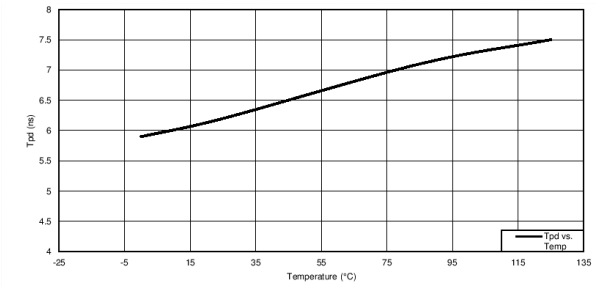
PARAMETER		FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low to high transition	A or B	Y	C_L = 15 pF	T_A = 25°C		5	6.2	ns
					T_A = –40°C to 85°C	1		7.1	
					T_A = –40°C to 125°C	1		7.5	
t_{PHL}	Propagation delay, high to low transition	A or B	Y	C_L = 15 pF	T_A = 25°C		5	6.2	ns
					T_A = –40°C to 85°C	1		7.1	
					T_A = –40°C to 125°C	1		7.5	
t_{PLH}	Propagation delay, low to high transition	A or B	Y	C_L = 50 pF	T_A = 25°C		5.5	7.9	ns
					Propagation delay, high to low transition	1		9	
					T_A = –40°C to 125°C	1		10	
t_{PHL}	Propagation delay, high to low transition	A or B	Y	C_L = 50 pF	T_A = 25°C		5.5	7.9	ns
					T_A = –40°C to 85°C	1		9	
					T_A = –40°C to 125°C	1		10	

6.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	18	pF

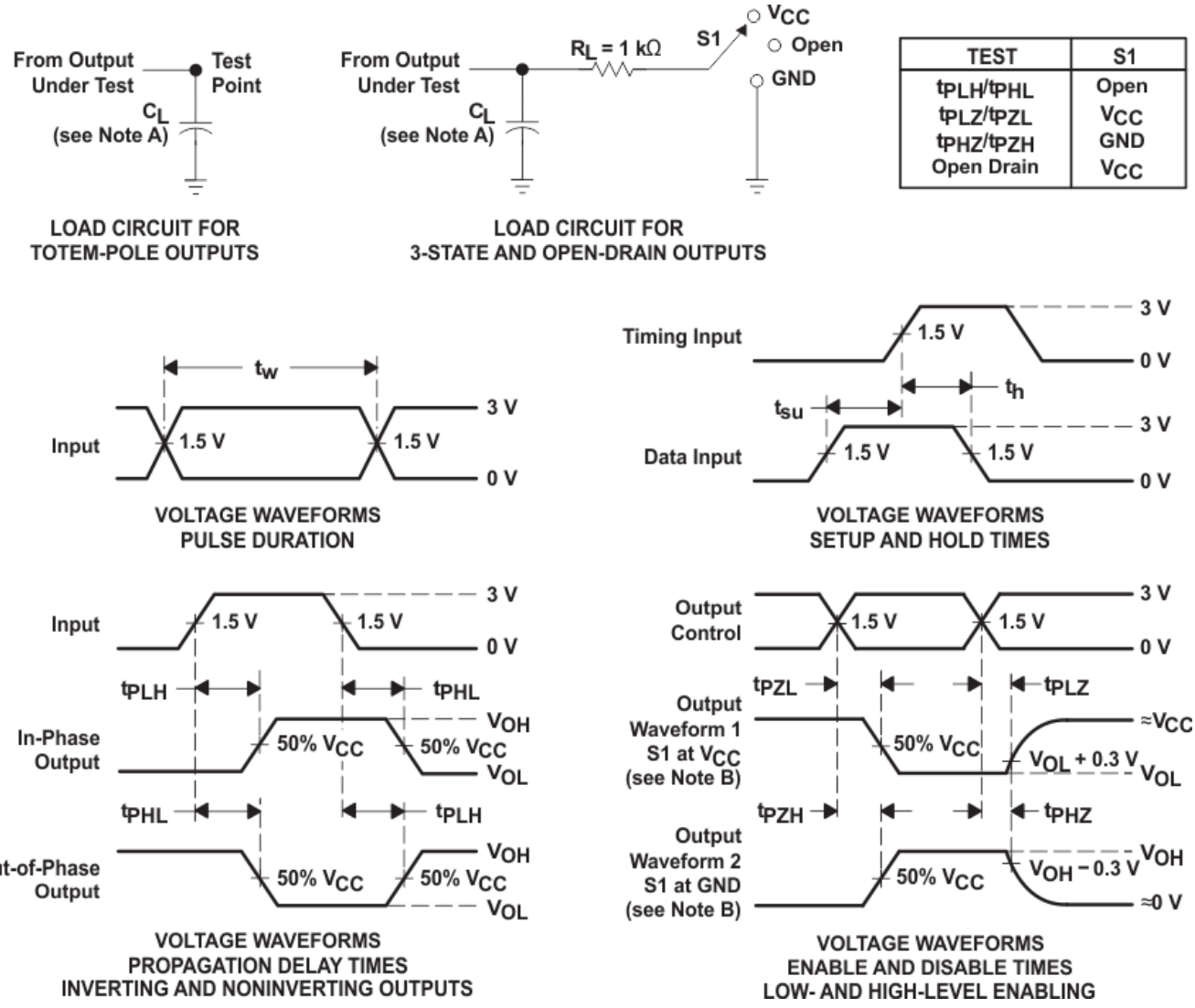
6.8 Typical Characteristics



C_L = 15 pF

Figure 6-1. T_{pd} vs Temperature

7 Parameter Measurement Information



C_L includes probe and jig capacitance.
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
The outputs are measured one at a time with one input transition per measurement.
All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AHCT1G08 device is a single 2-input positive-AND gate. The device performs the Boolean AND function ($Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$) in positive logic. Low I_{CC} current allows this device to be used in power-sensitive or battery-powered applications. Robust inputs allow the device to up-translate with a propagation delay of 20 ns.

8.2 Functional Block Diagram

Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The V_{CC} for the device is optimized at 5 V.

Up voltage translation from 3.3 V to 5 V is allowed. The inputs accept V_{IH} levels of 2 V.

Output ringing is minimized by slow edge rates.

Inputs are TTL-Voltage compatible.

8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SN74AHCT1G08.

Table 8-1. Function Table

INPUTS(1)		OUTPUT(2)
A	B	Y
H	H	H
L	X	L
X	L	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74AHCT1G08 device is a single AND gate, which is often used for many common functions like power sequencing or an *on* LED indicator. Because the device is configured to output LOW unless all inputs are HIGH, an LED tied to the output of the device will only turn HIGH when all systems connected are sending a HIGH, or *ready* signal.

9.2 Typical Application

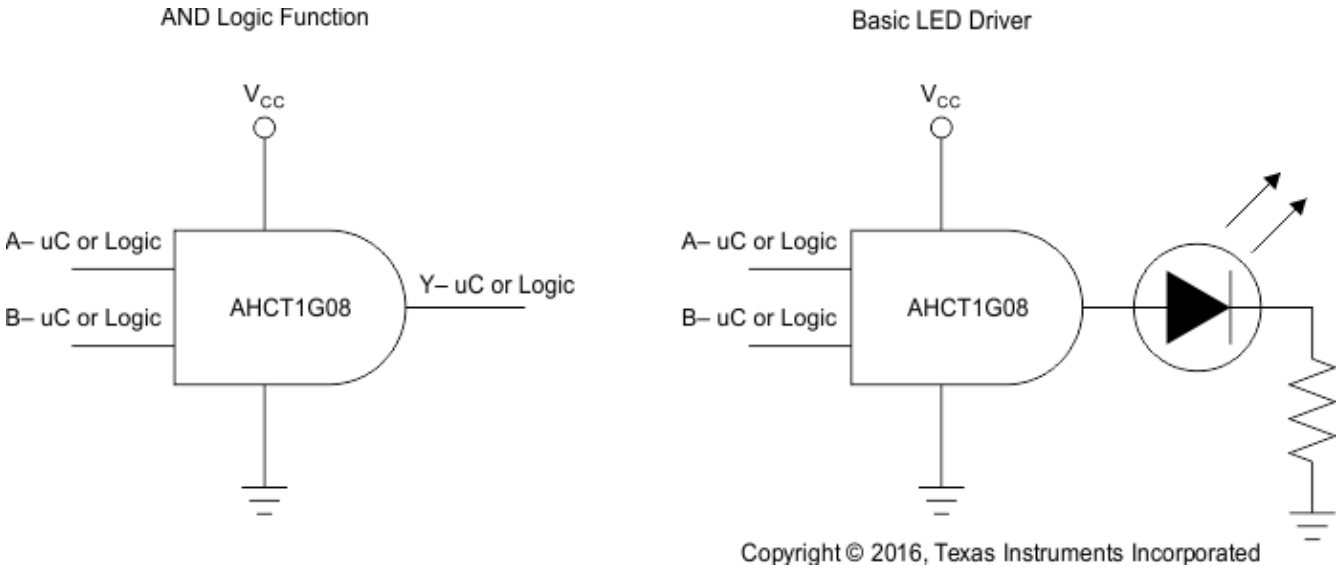


Figure 9-1. Typical Application Diagram

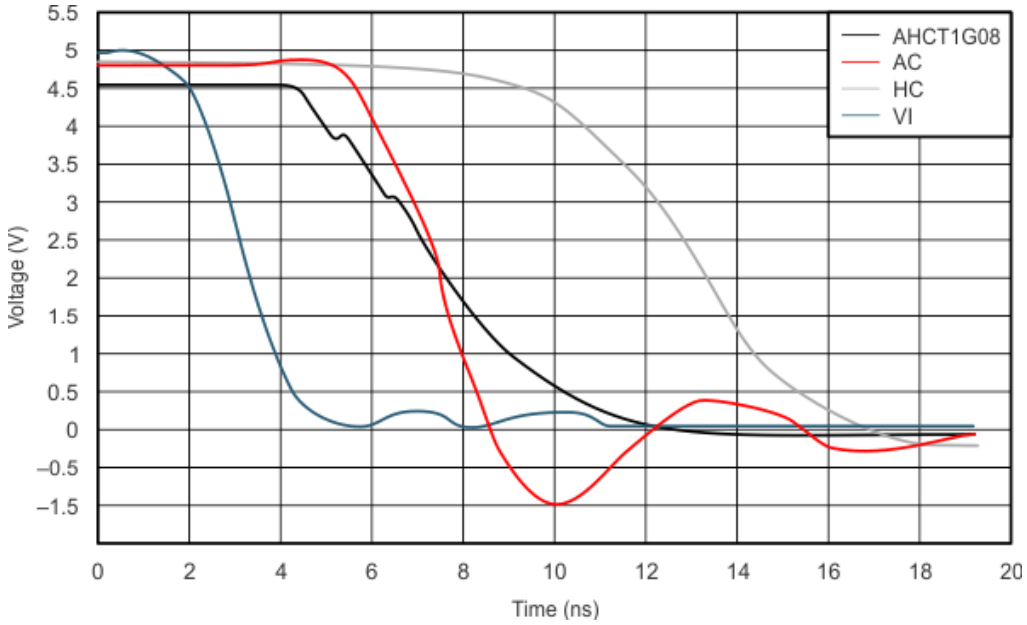
9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in *Section 6.3*.
   - For specified high and low levels, see V_{IH} and V_{IL} in *Section 6.3*.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions
   - Load currents must not exceed 25 mA per output and 50 mA total for the part.
   - Outputs must not be pulled above V_{CC}.

9.2.3 Application Curve



V_{CC} = 5 V Load = 50 Ω / 50 pF

Figure 9-2. Typical Switching Characteristics

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. TI recommends a 0.1-µF capacitor for devices with a single supply; and a 0.01-µF or 0.022-µF capacitor for each power pin if there are multiple V_{CC} pins. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Observe the following rules under all circumstances.

- All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.
- The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever make more sense or is more convenient.

9.4.1.1 Layout Example

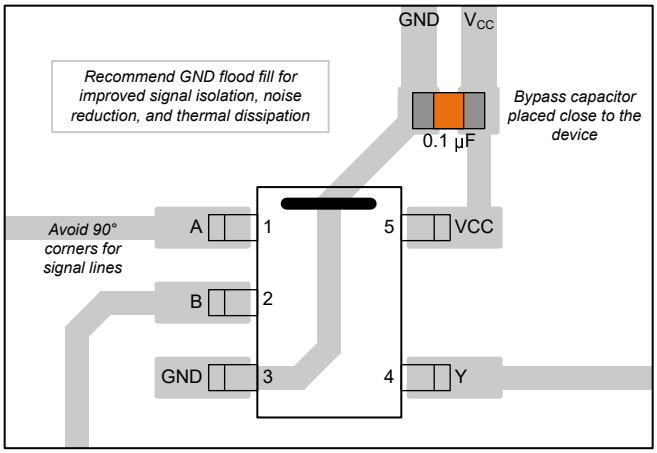


Figure 9-3. Layout Example for the SN74AHCT1G08

10 Device and Documentation Support

10.1 Documentation Support (Analog)

10.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AHCT1G08DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B08G	Samples
74AHCT1G08DCKRE4	LIFEBUY	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(1PJ, BE3, BEG, BEJ, BEL, BES)	
74AHCT1G08DCKRG4	LIFEBUY	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(1PJ, BE3, BEG, BEJ, BEL, BES)	
74AHCT1G08DCKTG4	LIFEBUY	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BE3, BEG, BEL, BES)	
74AHCT1G08DRLRG4	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(BEB, BES)	Samples
SN74AHCT1G08DBV3	ACTIVE	SOT-23	DBV	5	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 125	B08Y	Samples
SN74AHCT1G08DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(B083, B08G, B08J, B08L, B08S)	Samples
SN74AHCT1G08DCK3	ACTIVE	SC70	DCK	5	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 125	BEY	Samples
SN74AHCT1G08DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(1PJ, BE3, BEG, BEJ, BEL, BES)	Samples
SN74AHCT1G08DCKT	LIFEBUY	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BE3, BEG, BEL, BES)	
SN74AHCT1G08DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(BEB, BES)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74AHCT1G08 :

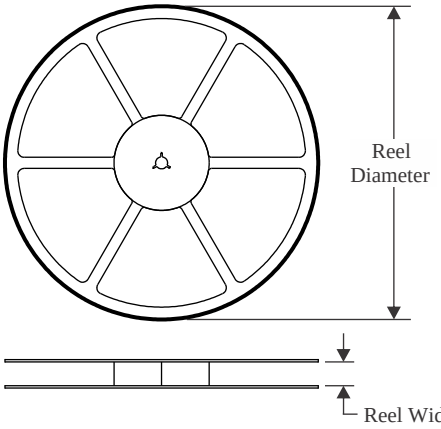
- Automotive : SN74AHCT1G08-Q1

NOTE: Qualified Version Definitions:

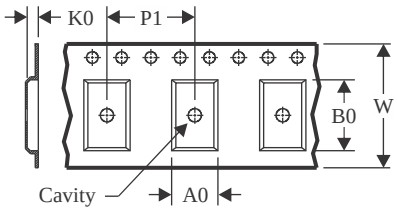
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

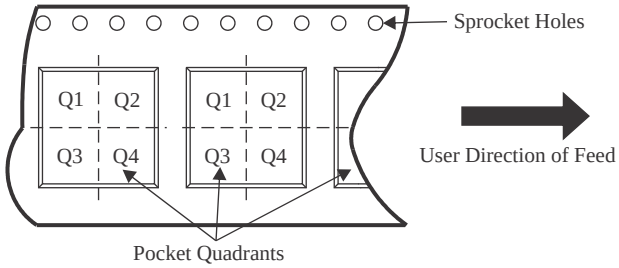


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

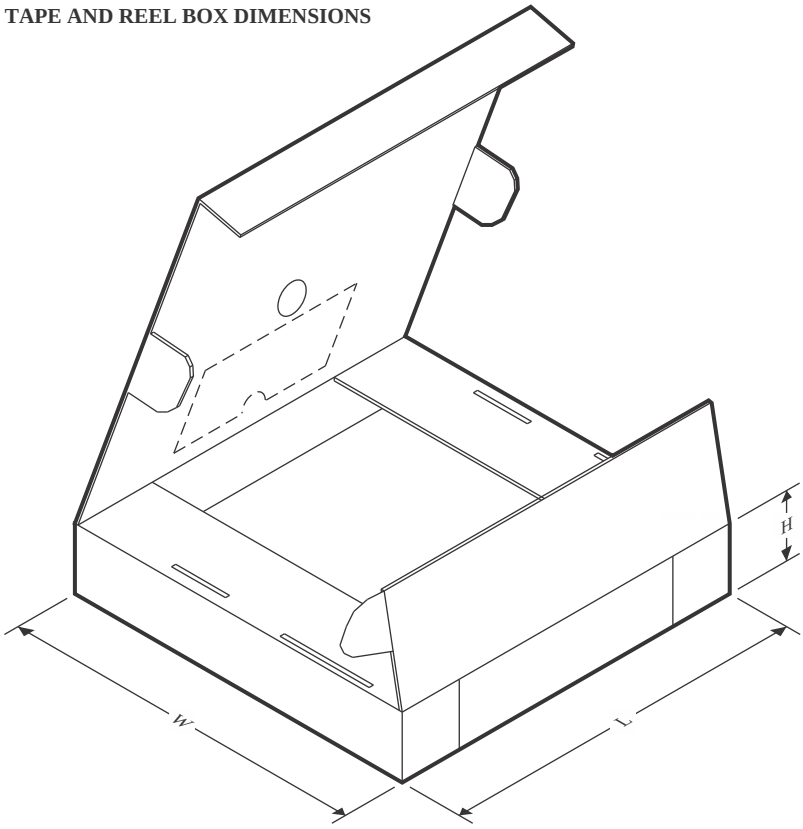
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHCT1G08DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHCT1G08DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G08DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHCT1G08DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G08DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHCT1G08DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AHCT1G08DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G08DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHCT1G08DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AHCT1G08DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

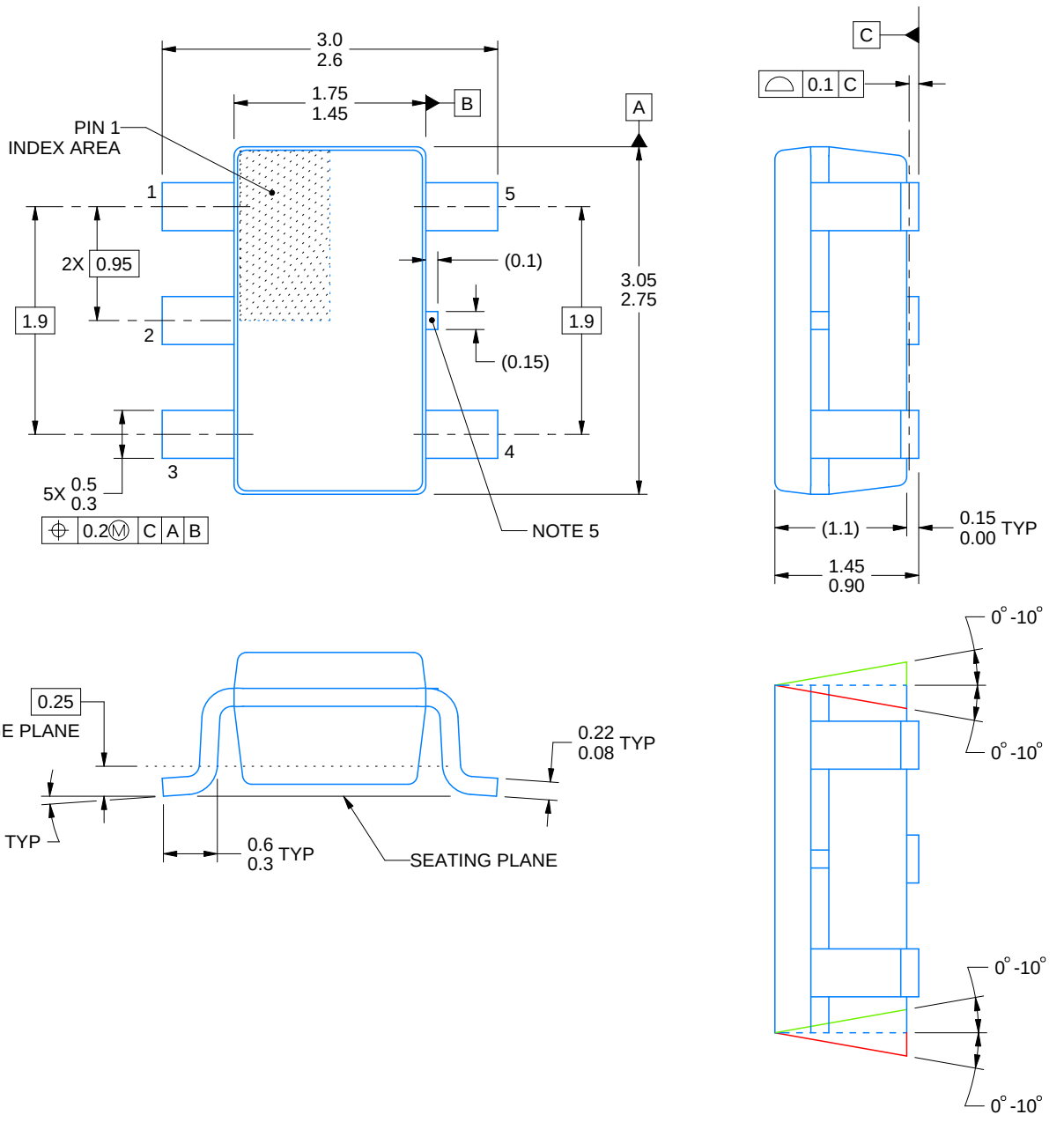
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHCT1G08DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHCT1G08DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHCT1G08DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AHCT1G08DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHCT1G08DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHCT1G08DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AHCT1G08DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHCT1G08DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHCT1G08DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AHCT1G08DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

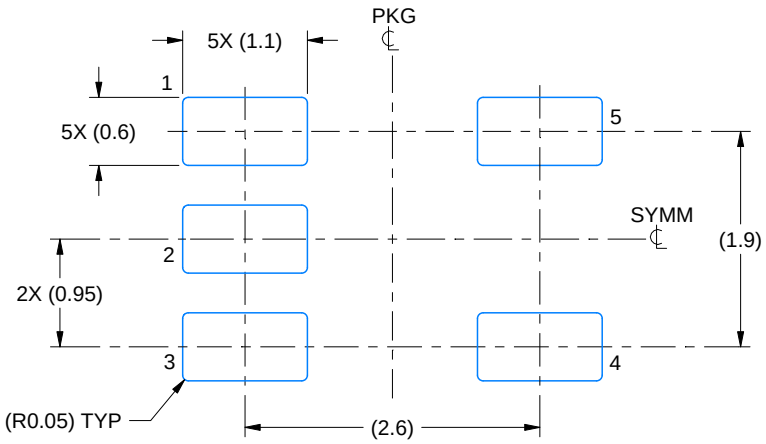


ALTERNATIVE PACKAGE SINGULATION VIEW

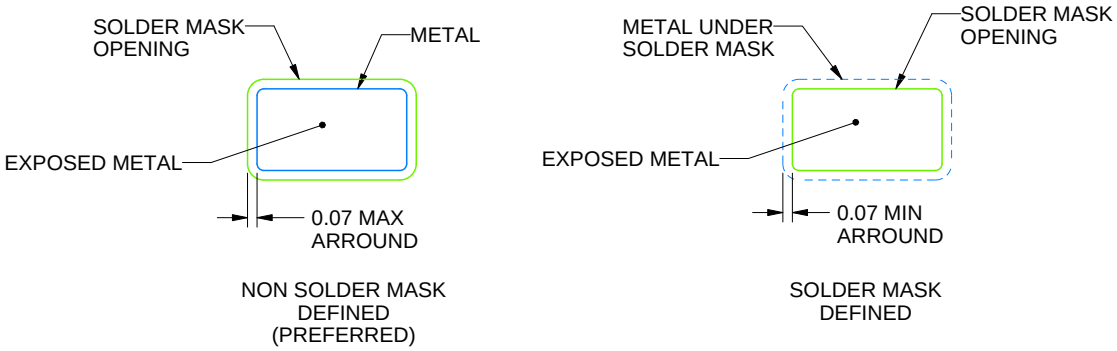
4214839/H 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

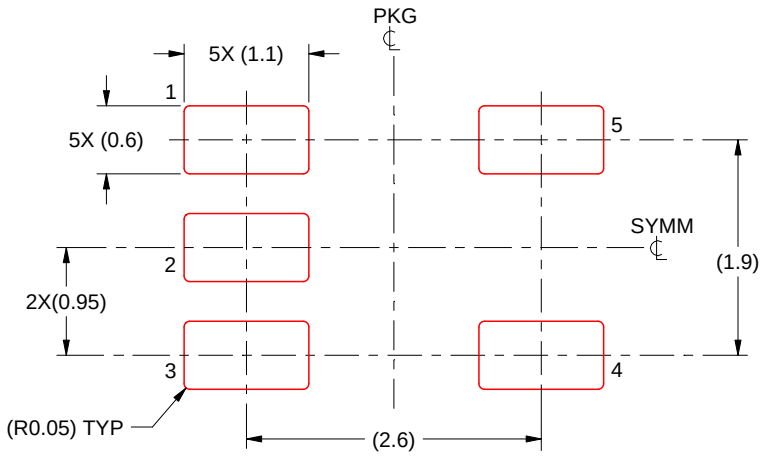


SOLDER MASK DETAILS

4214839/H 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/H 09/2023

NOTES: (continued)

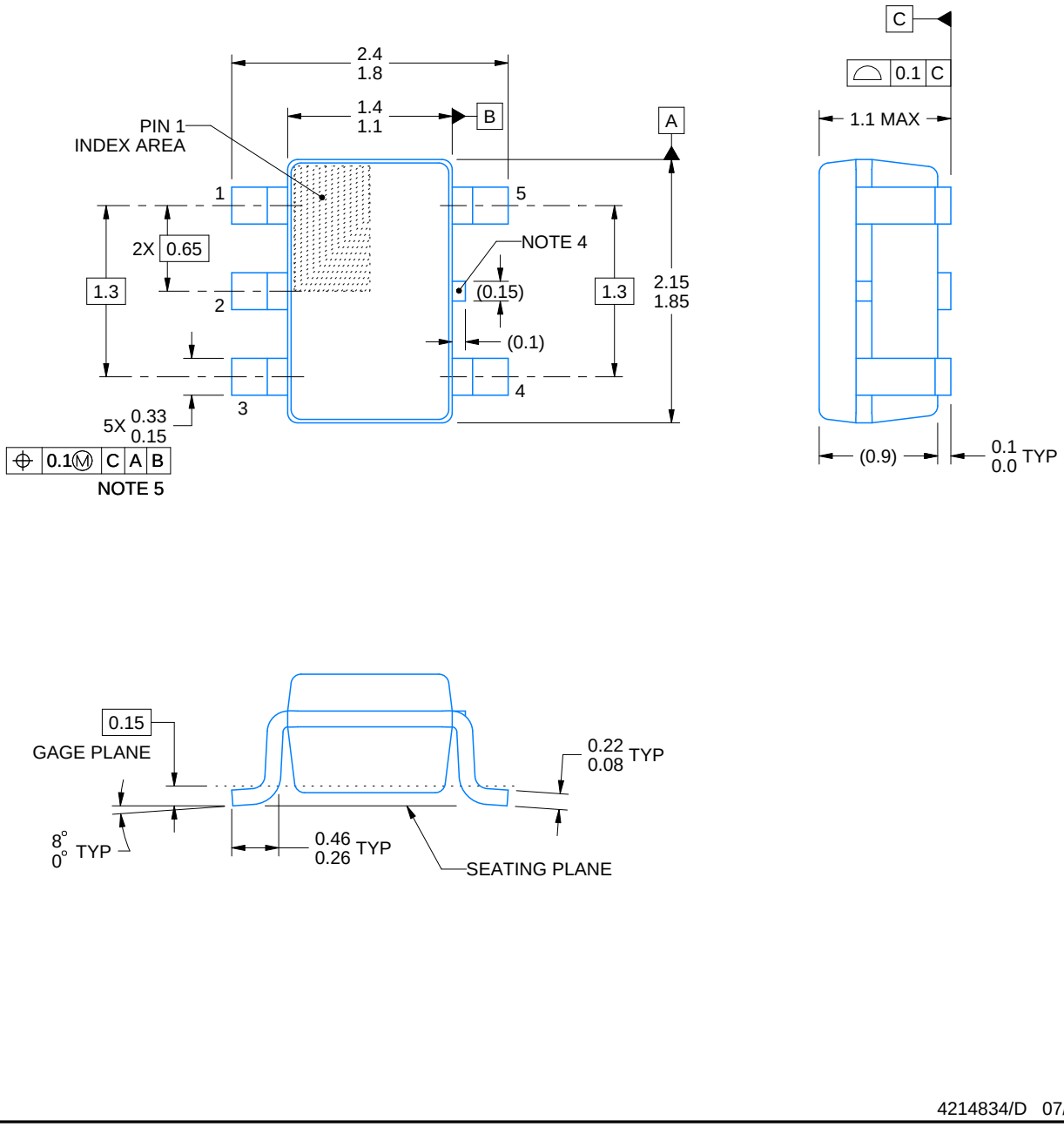
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

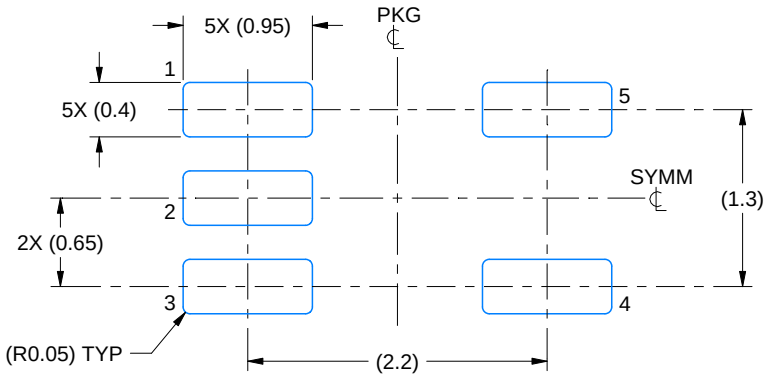
SMALL OUTLINE TRANSISTOR



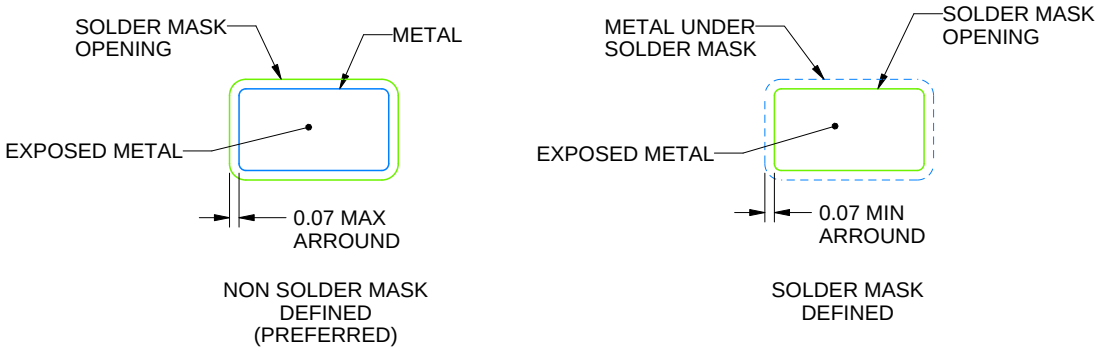
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

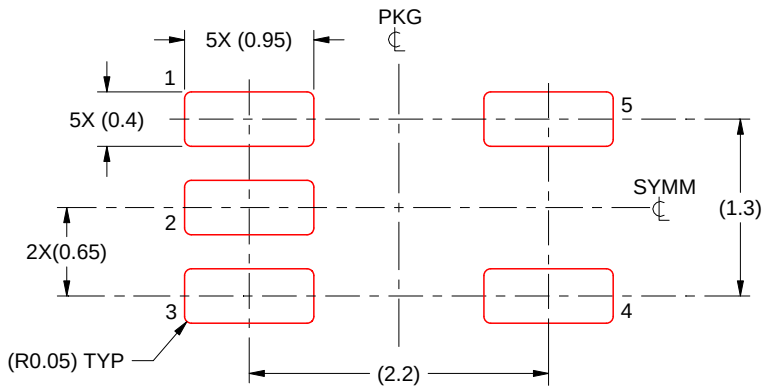


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

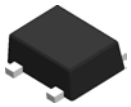


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

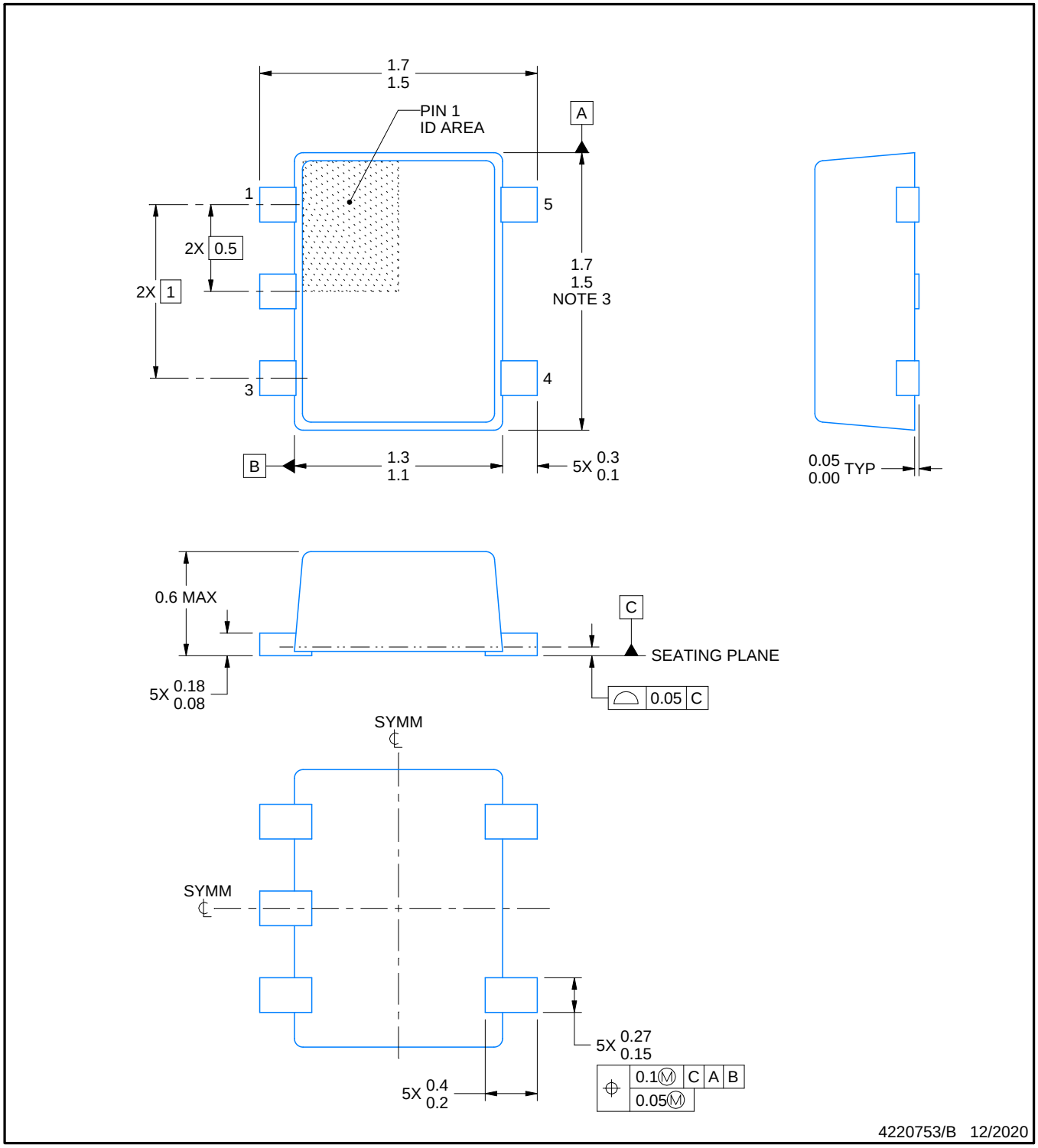


PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

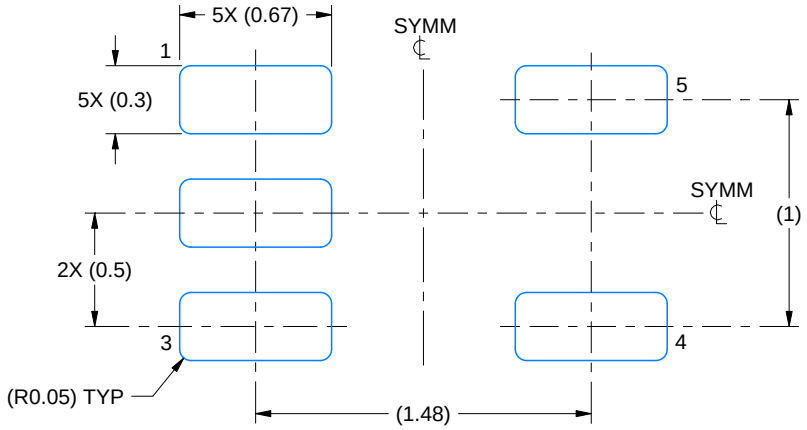
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

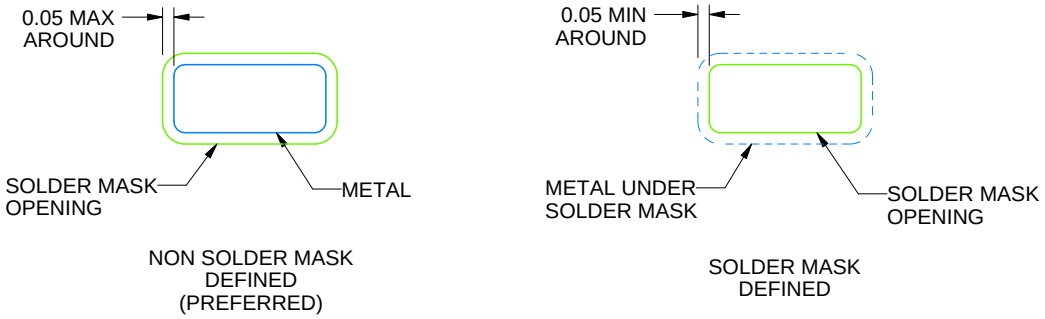
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

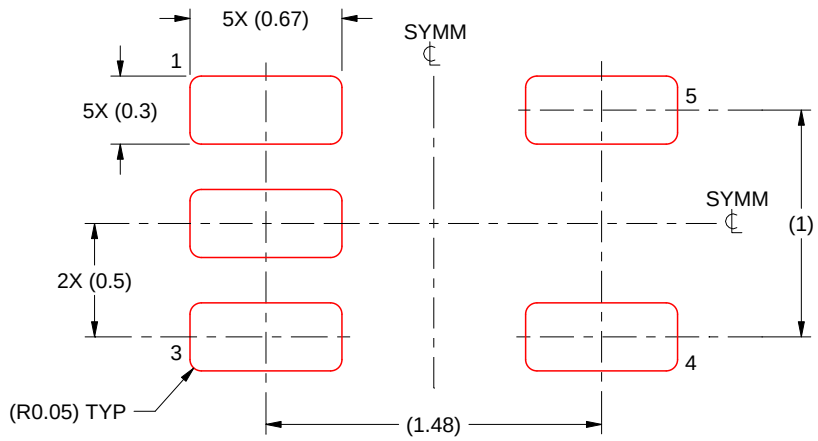
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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