Sanken Electric Co., Ltd.

3 phase BLDC Controller IC

SI-6633C

Application Note

July, 2013 Ver.1.1

MCD division low voltage motor group

This application note is applied to SI-6633C, which is controller for 3-phase brushless motor.
About the latest information, please refer to our charge section.

(Index)

1. General description

This is a pre-driver IC for a 3-phase brushless DC motor. This device can be combined with a wide variety of N channel power MOSFETs, and is ready for motor power voltage of up to 30V. Phase is switched by hall elements arranged at an interval of 120°.

This is provided with functions of PWM electric current control to limit inrush electric current, and of overheat shutdown and synchronous rectification, etc.

The synchronous rectification function rectifies by MOSFET of low temperature resistance instead of body diode and can reduce power loss at the time of regeneration.

This product has enable, direction, and brake inputs, and can control electric current by internal PWM. In addition, rotation of the motor can be detected by logic output FG.

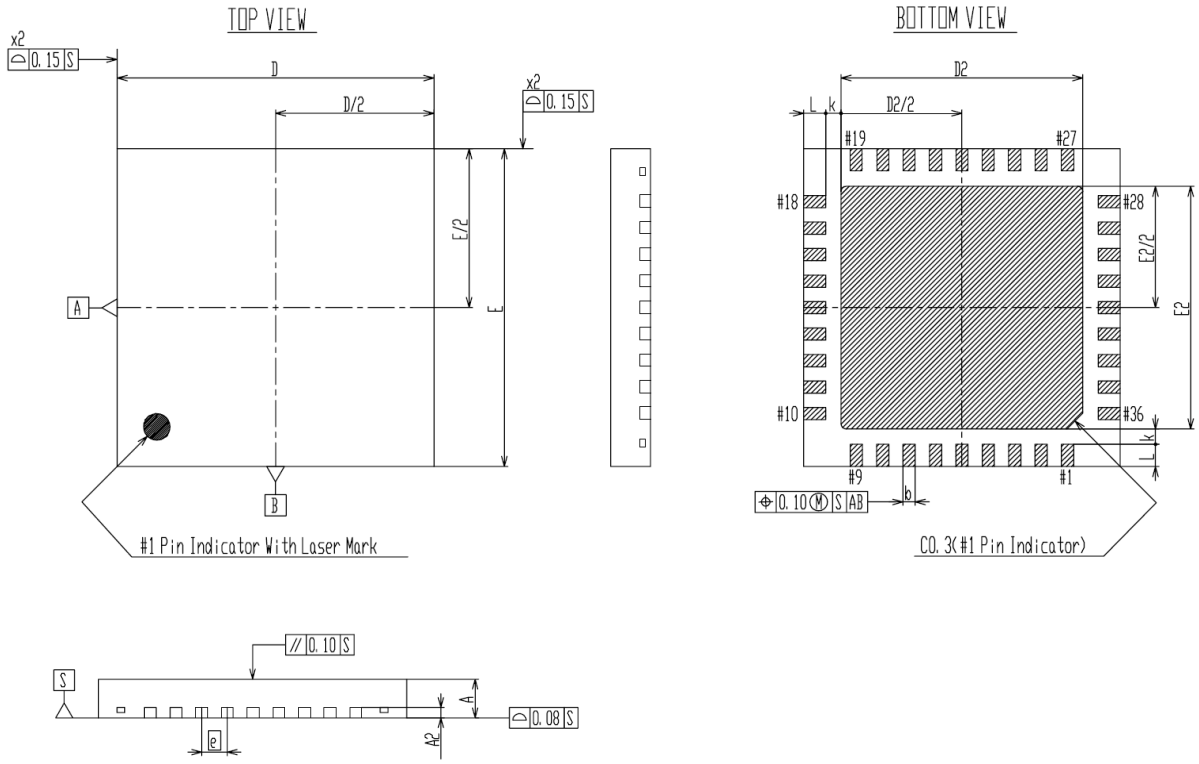
2. Features

- N channel MOSFET of 6 elements is driven.
- Ready for hall input
- Various protection functions are built in.
  - Overvoltage protection
  - Low voltage protection
  - Overcurrent protection (ready for supply fault, load short-circuit)
  - Thermal protection
  - Lock detection
  - Through-current prevention function
- Alarm output function at time of error
- Synchronous rectification to reduce power loss
- PWM current limit
- FG output
- Standby mode

3. Package information, recommended foot print

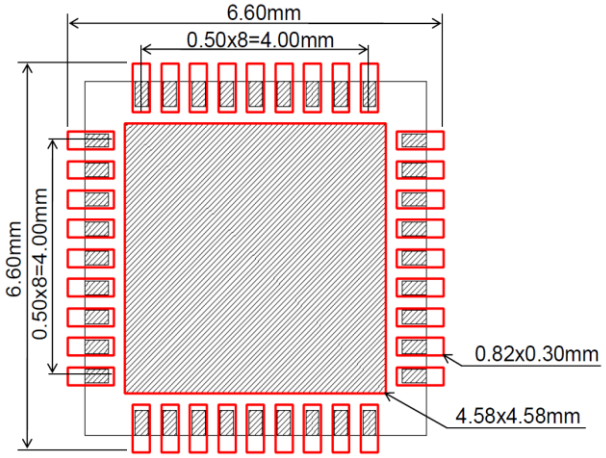
Unit: mm

QFN36Pin package with thermal pad

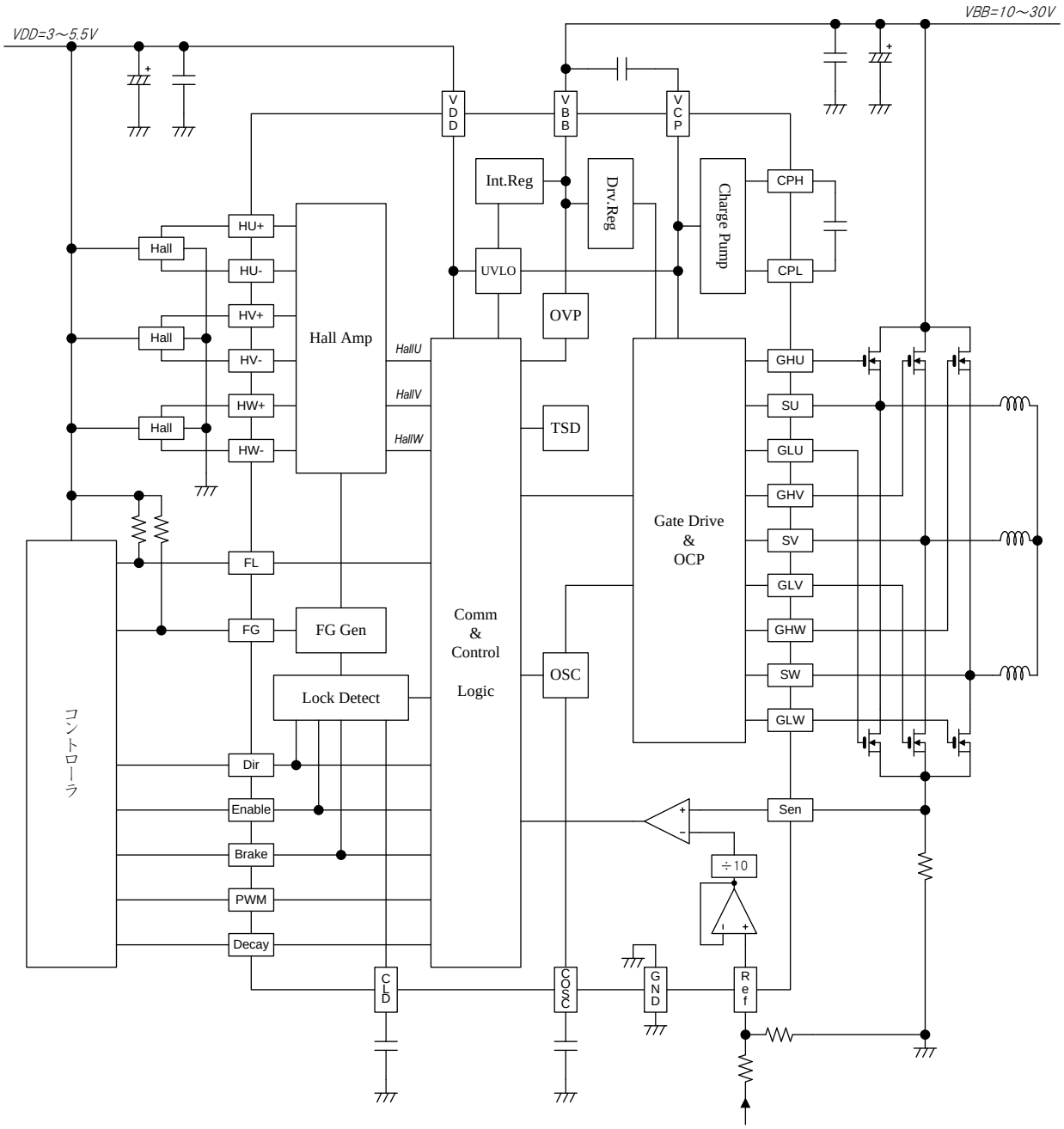


SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A2		0.20 REF.	
b	0.18	0.23	0.28
D	5.90	6.00	6.10
D2	4.43	4.58	4.73
E	5.90	6.00	6.10
E2	4.43	4.58	4.73
e		0.50 BSC.	
k	0.25	—	—
L	0.32	0.42	0.52

Recommended foot print (red line area)

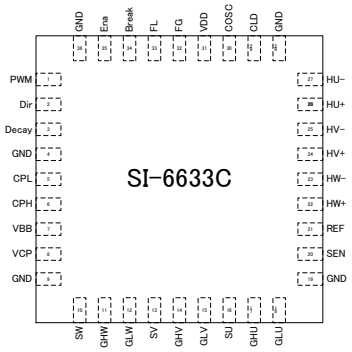


4. Block diagram and application circuit



5. Pin assignment

No.	Pin name	Pin function
1	PWM	PWM signal input pin
2	Dir	Current direction switching pin
3	Decay	Decay signal input pin
4	GND	Ground pin
5	CPL	Capacitor pin for charge pump suction Low
6	CPH	Capacitor pin for charge pump suction High
7	VBB	Motor power supply input pin
8	VCP	Capacitor pin for charge pump charge up
9	GND	Ground pin
10	SW	Output pin OUTW
11	GHW	High side gate output pin W
12	GLW	Low side gate output pin W
13	SV	Output terminal OUTV
14	GHV	High side gate output pin V
15	GLV	Low side gate output pin V
16	SU	Output pin OUTU
17	GHU	High side gate output pin U
18	GLU	Low side gate output pin U
19	GND	Ground pin
20	Sen	Current detection pin
21	Ref	Internal PWM current setting pin
22	HW+	Hall device input pin HW+
23	HW-	Hall device input pin HW-
24	HV+	Hall device input pin HV+
25	HV-	Hall device input pin HV-
26	HU+	Hall device input pin HU+
27	HU-	Hall device input pin HU-
28	GND	Ground pin
29	CLD	Lock detection time setting pin
30	COSC	Switching frequency setting pin
31	VDD	Logic power supply pin
32	FG	FG output pin
33	FL	Abnormality detection output pin
34	Brake	Brake input pin
35	Ena	Lock counter reset signal And Enable signal input pin
36	GND	Ground pin



6. Absolute maximum rating

Item	Symbol	Conditions	Rated value	Unit
Power supply voltage	V_{BB}		38	V
Output voltage	V_{OUT}		38	V
Logic input voltage	$V_{IN(Logic)}$		-0.3 - 6	V
Ref input voltage	V_{Ref}		-0.3 - 6	V
Detection voltage	V_{SENSE}		±2	V
Maximum junction temperature	$T_{J(max)}$		150	°C
Storage temperature	T_{stg}		-40 - 150	°C
Operation ambient temperature	T_A		-20 - 85	°C
Package thermal resistance	$R_{\theta JA}$	4 phase board used (QFN36)	TBD	°C /W
	$R_{\theta JP}$	Between junction and pad	TBD	°C /W

(*) The output current may be limited by duty cycle, ambient temperature, and heat release state. The specified rated current and maximum junction temperature (Tj=150°C) shall not be exceeded under any condition.

7. Recommended operating range

Item	Symbol	Rated value	Unit	Notes
Power supply voltage	V_{BB}	10 - 30	V	
Control power supply voltage	V_{DD}	3 - 5.5	V	
Logic input voltage	$V_{IN(Logic)}$	0 - 5.5	V	
Ref input voltage	V_{Ref}	0.5 - 5.5	V	Current control accuracy is significantly reduced at 0.5 V or less.
Detection voltage	V_{SENSE}	±0.5	V	
Package temperature	T_C	105	°C	
Operation ambient temperature	T_A	-20 - 85	°C	

8. Power dissipation

Derating when package used

TBD

※when JEDEC standard 4-phase board used

9. Electrical characteristics

T_A=+25°C、V_{BB}=24V, V_{DD}=5V, unless otherwise specified

Item	Symbol	Rated value			Unit	Test conditions
		MIN	TYP	MAX		
Output Drivers						
VBB voltage range	V_{BB}	10	-	V_{BBOV}	V	in operation
Main power supply current	I_{BB}	-	-	TBD	mA	Operation state (output is off)
		-	-	(200)	μA	Standby mode
Control Logic						
VDD voltage range	V_{DD}	3	-	5.5	V	in operation
VDD pin current	I_{DD}	-	-	TBD	mA	Operation state (output is off)
		-	-	(500)	μA	Standby mode
Logic input voltage	$V_{IN(0)}$	-	-	VDD×0.25	V	
	$V_{IN(1)}$	VDD×0.75	-	-	V	
Logic input current	$I_{IN(0)}$	-	±1	±10	μA	$V_{IN(0)}$, V_{IN}=0V
	$I_{IN(1)}$	-	±1	±10	μA	$V_{IN(1)}$, V_{IN}=5V
Input pin filter	t_{LOGIC}	-	(0.5)	-	μs	
COSC pin oscillation frequency	f_{OSC}	-	25	-	KHz	C_{OSC}=330pF
Gate Drive						
High side output voltage	$V_{GS(H)}$	6	-	(9)	V	I_{GATE}=2mA for Vbb
Low side output voltage	$V_{GS(L)}$	6	-	(9)	V	I_{GATE}=2mA
Drive current	I_{GATE}	TBD	30	-	mA	GH=GL=4V、VCP=VBB+TBD
Dead time	t_{dead}	TBD	1000	TBD	ns	
Internal PWM						
Ref pin input current	I_{ref}	-	±10	-	μA	
Ref pin input voltage range	V_{Ref}	0.5	-	5.5	V	
Sen pin input current	I_{Sen}	-	±10	-	μA	V_{Sen}=0 - 1V
Detection voltage	V_{Sen}	-	V_{REF}×0.1	-	V	V_{Ref}=1 - 5V
Current detection filter time	t_{LPFSen}	-	2	(4)	μs	Design assurance

※1：Use Typ data as design information.

※2：Negative current in the table represents current flowing out from the product pin.

T_A=＋25°C, V_{BB}=24V、V_{DD}=5V, unless otherwise specified

Item	Symbol	Rated value			Unit	Test conditions	
		MIN	TYP	MAX			
Protection							
FL output saturation voltage	$V_{FI(ON)}$	-	0.45	(0.7)	V	I_{FG}=2mA	
FL output pin on current	$I_{FI(ON)}$	(5)	7.5		mA	V_{FI}=2V	
FL output leak current	$I_{FI(OFF)}$	-	-	50	μA	V_{FG}=5.5V	
Overcurrent detection voltage	V_{OCP}	(1.4)	1.5	(1.65)	V	Low side MOSFET detection (between OUT and GND)	
Overcurrent detection filter time	t_{FLTOCP}	-	TBD	TBD	μs	Design assurance	
OCP output OFF timer count	N_{OCP_OFF}	-	256	-			
VBB overcurrent protection threshold voltage	V_{BBOV}	-	35	(37)	V		
VBB overvoltage protection hysteresis	$V_{BBOVhys}$	-	2	-	V		
CLD pin oscillation frequency	f_{LD}	-	128	-	Hz	C_{LD}=0.1μF	
Lock detection timer count	N_{LD}	-	256	-			
Thermal protection operation temperature	T_{JTSD}	-	170	-	°C	When temperature rises	Design assuarnce
Thermal protection hysteresis	$T_{JTSDhys}$	-	(15)	-	°C		
VDD low voltage protection release voltage	V_{DDUV}	-	2.8	2.95	V	When V_{DD} voltage rises	
VDD low voltage protection hysteresis	$V_{DDUVhys}$	-	(0.15)	-	V		
VBB low voltage protection release voltage	V_{BBUV}	-	(9)	(9.75)	V	When V_{BB} voltage rises	
VBB low voltage protection hysteresis	$V_{BBUVhys}$	-	TBD	-	V		
FG							
FG output saturation voltage	$V_{FG(sat)}$	-	0.45	(0.7)	V	I_{FG}=2mA	
FG output leak current	I_{FGlkg}	-	-	50	μA	V_{FG}=5.5V	
Hall Logic							
Hall input current	I_{HALL}	-2	-0.1	1	μA	V_{IN}=0.2～4V	
Common mode input voltage range	V_{CMR}	0.2	-	(4)	V		
AC input voltage range	V_{HALL}	60	-	-	mV_{p-p}		
Hysteresis	V_{HYS}	TBD	40	(VHALL)	mV	Design assurance	
Pulse removal filter	t_{pulse}	-	2	-	μs		

※1：Use Typ data as design information.

※2：Negative current in the table represents current flowing out from the product pin.

10. Truth table, timing chart

10.1. Excitation control input (Hall and Logic input)

Table. 10-1 Hall input and each control input

State	Input					Output status					
						DIR=H			DIR=L		
	HallU※1	HallV※1	HallW※1	Enable	Brake	OUTU	OUTV	OUTW	OUTU	OUTV	OUTW
F1	+	−	+	L	H	H	L	Z	L	H	Z
F2	+	−	−	L	H	H	Z	L	L	Z	H
F3	+	+	−	L	H	Z	H	L	Z	L	H
F4	−	+	−	L	H	L	H	Z	H	L	Z
F5	−	+	+	L	H	L	Z	H	H	Z	L
F6	−	−	+	L	H	Z	L	H	Z	H	L
Error	−	−	−	L	H	Z	Z	Z	Z	Z	Z
Error	+	+	+	L	H	Z	Z	Z	Z	Z	Z
brake	X	X	X	L	L	L	L	L	L	L	L
disable※2	X	X	X	H	H	Z	Z	Z	Z	Z	Z
StandBy	X	X	X	H	L	Z	Z	Z	Z	Z	Z

X : don't care Z : High Impedance

※1 HallU、HallV、HallW：'+'=H+>H- 、'-' =H+<H-

※2 There are some conditions for becoming Disable.

- There are some conditions for becoming Disable.
- These are internal logic signal names.
- See the diagrams for conditions for becoming Disable.

10.2. FL output (flag output)

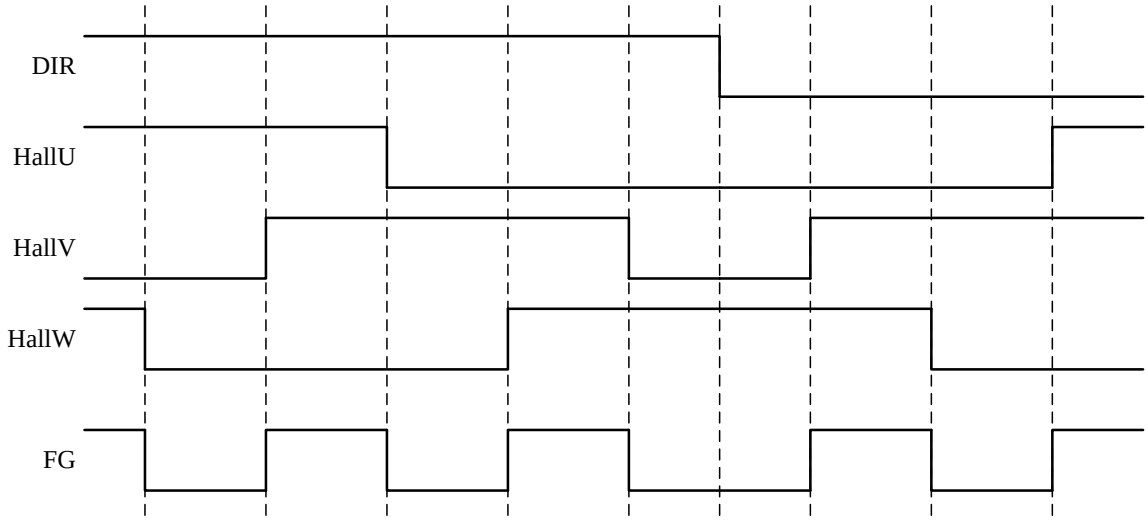
Table.10-2 FL output

FL output	State	
Hi-Z	Operation state	
L	Abnormality detection	Low voltage protection (UVLO)
		Thermal shutdown (TSD)
		Overvoltage protection (OVP)
		Overcurrent protection and output OFF period (OCP)

・Note that the internal circuit incompletely operates in a state of low power voltage (VBB, VDD) and correct diagnosis result may not be output.

10.3. FG signal

Fig. 10-1

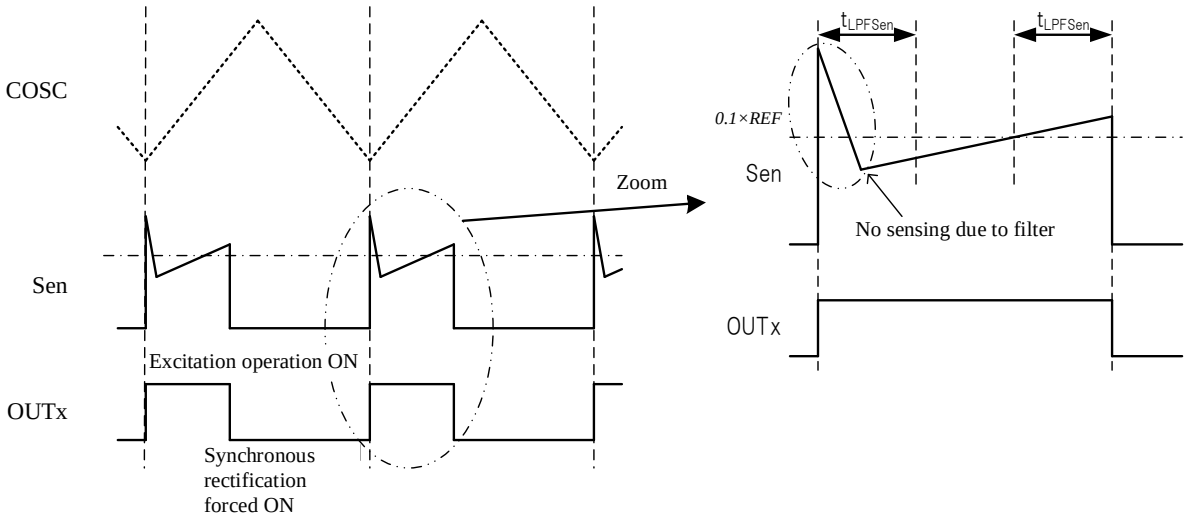


・Refer to “Excitation control input (hall & Logic input)” for HalU, HallV and HallW.

・FG is put into toggle-operation in which the logic reverses every time when excitation phase is switched by hall input.

10.4. Internal PWM control

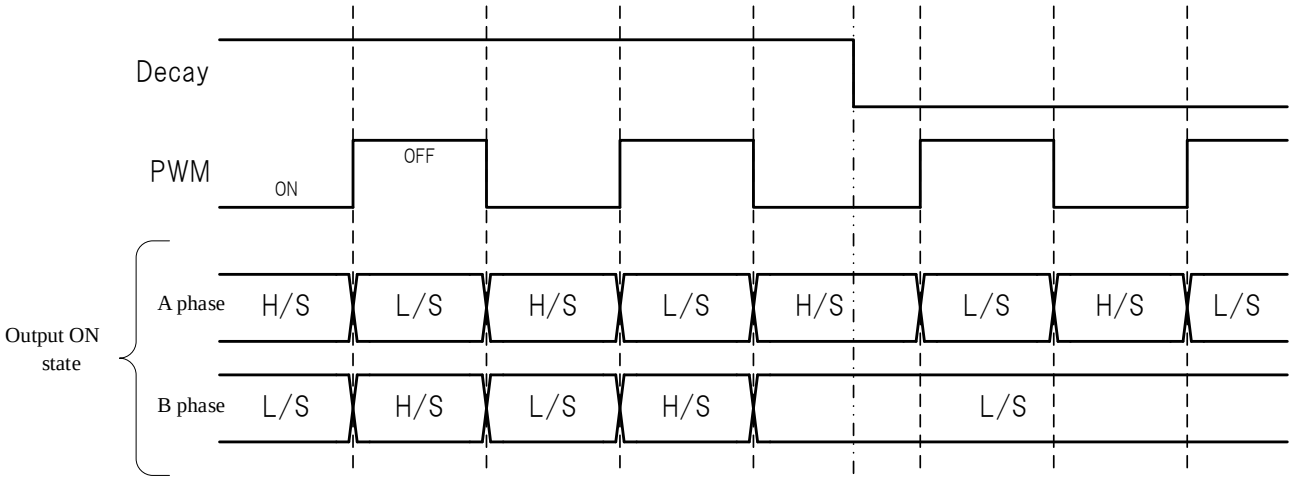
Fig.10-2



・When not using this control, connect Sen to GND, and connect REF to VDD.

10.5. PWM control input (PWM and Decay)

Fig. 10-3

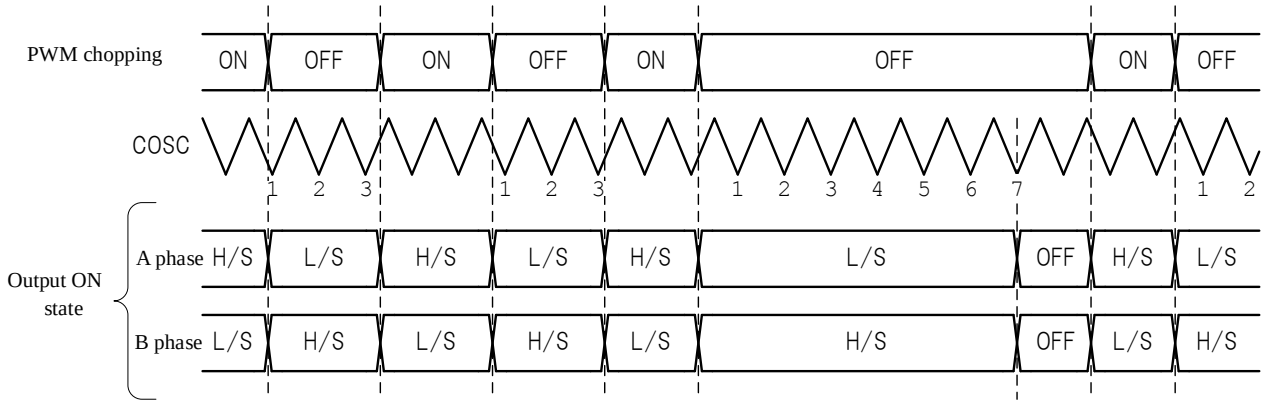


・Input signals on PWM pin and Decay pin are neglected at the time of Brake.

・When PWM control input is not used, the pin should be set to 'L.'

10.6. Disable function for synchronous rectification (Fast Decay only)

Fig. 10-4

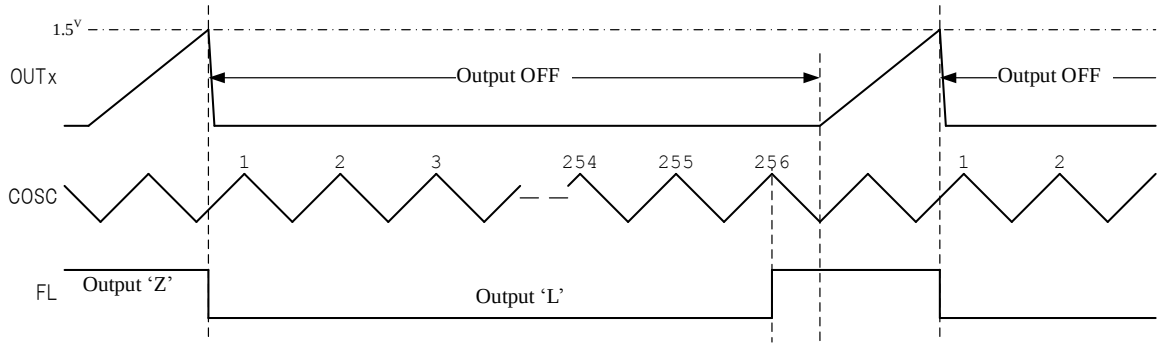


・If a PWM chopping OFF period has continued for a certain time (approximately 7 cycles of COSC), synchronous rectification operation is stopped.

・This function does not operate at time of Brake.

10.7. OCP control

Fig. 10-5



(※Numerical values in the diagram are typ values)

・After overcurrent is detected, output is OFF for a certain time (256 cycles of COSC), and then auto-restarts.

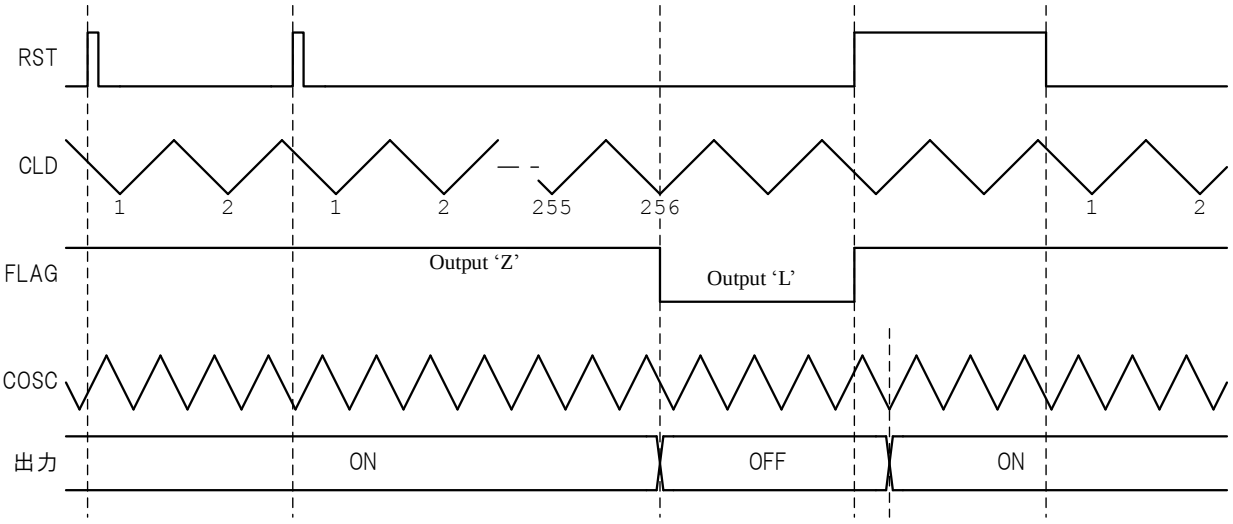
・Timer count for output OFF time and FL output release are performed in timing of top of COSC.

・OFF period is released in timing of bottom of COSC.

・Timer count for output OFF time is not also reset as an output Disable.

10.8. Motor lock

Fig. 10-6



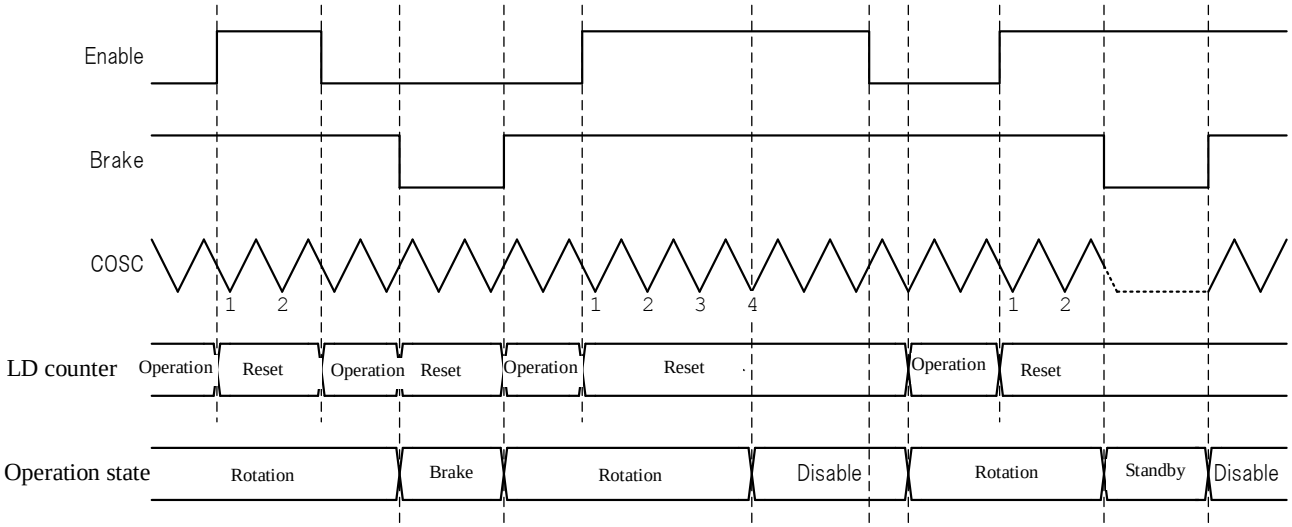
・Lock detection operates only in a rotation state (Enable pin ='L', Brake pin ='H').

・If there occurred no signal (RST) to release the lock detection for approximately 256 cycles in the oscillation cycle of CLD, it is judged to be motor lock and output is shut down.

・For RST signal, see Fig. 10 - 6 and "Lock Detect" in "11. Circuit configuration (individual circuit)."

10.9. Enable and Break

Fig. 10-7



・Enable pin has the following three functions in a sequence of prioritized operation.

①Standby control (combination with Brake pin)

Combination of Brake='L' and Enable='H' brings the operating state into standby, and out of this combination it restarts from the standby.

In addition, the charge pump circuit and internal Reg stop at the time of standby. For this reason, it takes some time until start of actual operation from release of standby.

Furthermore, the FL pin becomes 'H' at the time of standby, and output is performed according to the internal state after release.

②Lock counter reset

The lock counter is in reset state during a period of Enable='H'.

③Output Enable/Disable operation

Output Disable occurs when the number of oscillations (counted in timing of bottom) of COSC is the 4th time after 'L' on the Enable pin changes to 'H'.

Output Enable occurs in the timing of on-trigger (bottom of COSC) next after 'H' on the Enable pin changes to 'L'.

11. Functional description; individual block

11.1. UVLO

This circuit protects when the power state reaches down to normally operable voltage value or less.

Voltage raised by the internal powers of the VDC, IC and the charge pump is monitored with low voltage protection.

The output is shut down when the voltage monitored is lower than the set value.

11.2. TSD

This is a protection circuit to monitor junction temperature of the control IC and prevent thermal shutdown of the product.

The thermal shutdown protection shuts down the output when temperature of the IC rises up to near 170°C.

Then, when the temperature of the IC lowers by approximately 15°C, output shutdown is released.

In addition, this function is not used on a routine operation basis, therefore, conduct thermal design so as to avoid this function from operating and use.

11.3. OVP

When main power voltage (VBB) applied to the product increases to approximately absolute maximum ratings, output is shut down and the product moves to an overvoltage protection (OVP) in which the most withstand is obtained against the overvoltage.

The OVP of this product functions at approximately 35V.

In addition, even if any voltage higher than this is applied, the motor cannot be operated.

11.4. Charge Pump

This is a boost power to drive Nch MOSFET on the high side (upper arm).

The CP pin is in a potential state where its voltage is higher than that of the main power (VBB) by approximately 7V during normal operation.

A capacitor is required for boost operation, so be careful of the following.

☆Between CP and VBB

The CP pin has higher potential than the VBB pin during normal operation, however, the voltage on the CP pin may lower by approximately 1V relative to the VBB pin during a time by which the voltage of the CP pin is increased.

☆Between CPH and CPL

Since voltage equivalent to that on the VBB is applied, be careful of the withstand voltage.

11.5. Gate Drive and OCP

The Gate Drive is a circuit for pre-driver to receive signals of Control Logic and drive output Nch MOS FET.

A dead time is also set by this block. The dead time prevents through current which must be noted when the high side (upper arm) and low side (lower arm) are simultaneously put into switching operation.

In addition, this product is also equipped with an overcurrent protection circuit (OCP).

This overcurrent protection circuit monitors drain voltage (voltage between OUT pin and GND) when low side MOSFET is ON, and the threshold voltage is 1.5V (typ).

11.6. Hall Amp

Connect standard hall elements.

11.7. FG Gen

This receives signals from the Hall Amp and outputs a motor rotation pulse from the FG pin.

This simultaneously generates signals for resetting lock detection.

11.8. Commutation and Control Logic

This synthesizes the ON/OFF signal of power MOSFET sent to the Gate Drive from positional signals, PWM control signals obtained from the Hall Amp, and output off signals from the protection circuit system or the like.

11.9. Internal PWM

This controls peak current flowing through the motor coil according to the externally input current reference signal (analog voltage).

This is equipped with a filter for noise generated when chopping is on.

For PWM operation, chopping is turned on by a trigger signal from the OSC, and chopping is turned off when the coil current reaches the set current (peak current value I_{Opeak}).

The switching frequency becomes constant at f_{OSC} described in the term of OSC.

Set value of I_{Opeak} can be calculated by the following calculating formula.

$$I_{Opeak} \approx 0.1 \times V_{REF} / R_S \quad [A]$$

Wherein, V_{REF}: REF pin voltage RS: Current detecting resistance value

When this function is not used, the internal PWM control does not function by connecting the Sen pin to GND and connecting the REF pin to VDD.

11.10. OSC

This determines many operation timings and time of the product.

For this reason, it is necessary to operate in oscillation by always connecting a capacitor.

Oscillation frequency f_{OSC} is determined by the capacitor connected to the OSC pin and is calculated by the following calculating formula.

$$f_{OSC}[kHz] \approx 8.3 / C_{OSC}[nF]$$

11.11. Lock Detect

This functions to detect a motor lock state.

When there is a state in which a hall input signal does not change for a certain time which is determined by a capacitor (C_{LD}) on the CLD pin and internal frequency dividing rate, it is judged to be a motor lock state and power to the motor is shut down. At the same time, voltage on the FL pin becomes Low to inform that it is in a lock state.

The relationship between the CLD pin capacity and lock detecting time t_{LD} is calculated by the following calculating formula.

$$t_{LD} \approx 20 \times C_{LD}[\mu F]$$

In order to reset the internal counter and return from shutdown state after lock detection, it is necessary to enter any of the following signals.

☆Change hall input.

☆Set logic of Brake pin to brake (‘L’).

☆Set logic of Enable pin to Disable (‘H’).

☆Switch logic of Dir pin.

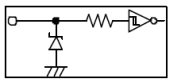
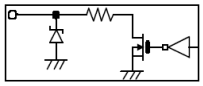
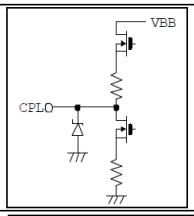
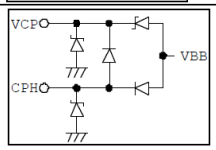
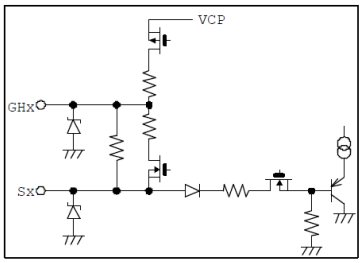
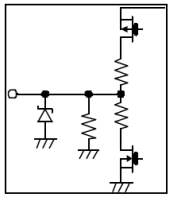
☆Turn on power again.

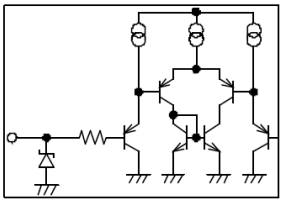
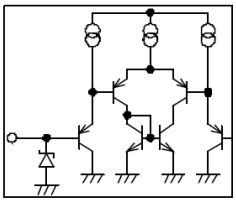
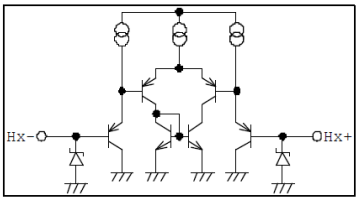
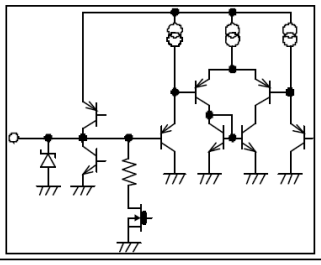
When the motor rotates by any cause and a hall input is switched after the motor stops by lock detection, the counter is reset and return from the lock detection status.

If you attempt to compulsorily avoid lock detection in a state where the motor is excited, switch logic of the Dir pin in a cycle shorter than the lock detection time, or enter a pulse of ‘H’ with a narrow width (less than approximately 4 cycles of COSC) avoiding a Disable state.

Furthermore, in operations of protection functions (Reg, and UVLO、TSD、OVP、OCP between CP and VBB), the lock counter is not reset and the timer count is continued. When the motor stops by these protection functions, it is judged to be locked and the motor may be put into stop state by this protection function.

12. Pin diagram

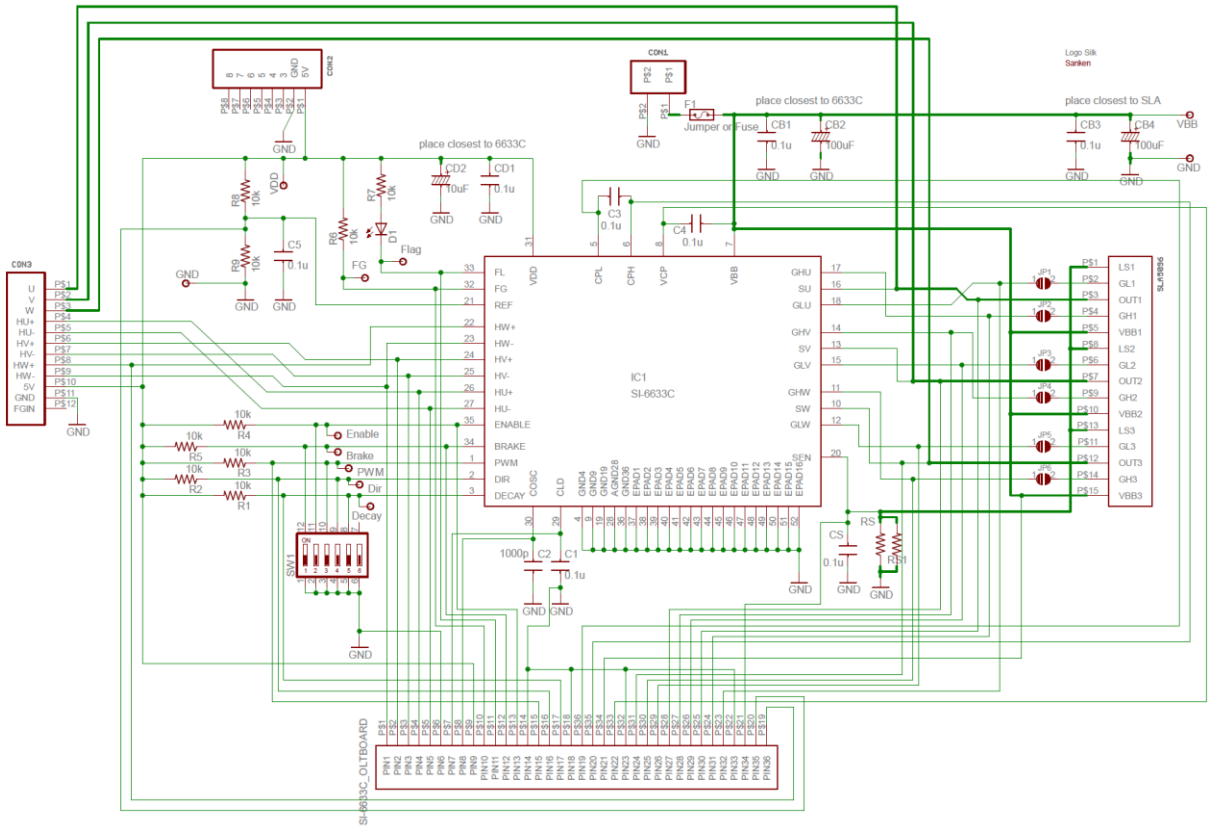
No.	Pin 名	回路
1	PWM	
2	Dir	
3	Decay	
34	Brake	
35	Ena	
32	FG	
33	FL	
5	CPL	
6	CPH	
8	VCP	
11	GHW	
10	SW	
14	GHV	
13	SV	
17	GHU	
16	SU	
12	GLW	
15	GLV	
18	GLU	

20	Sen	
21	Ref	
22	HW+	
23	HW-	
24	HV+	
25	HV-	
26	HU+	
27	HU-	
29	CLD	
30	COSC	
7	VBB	
31	VDD	
4	GND	
9	GND	
19	GND	
28	GND	
36	GND	

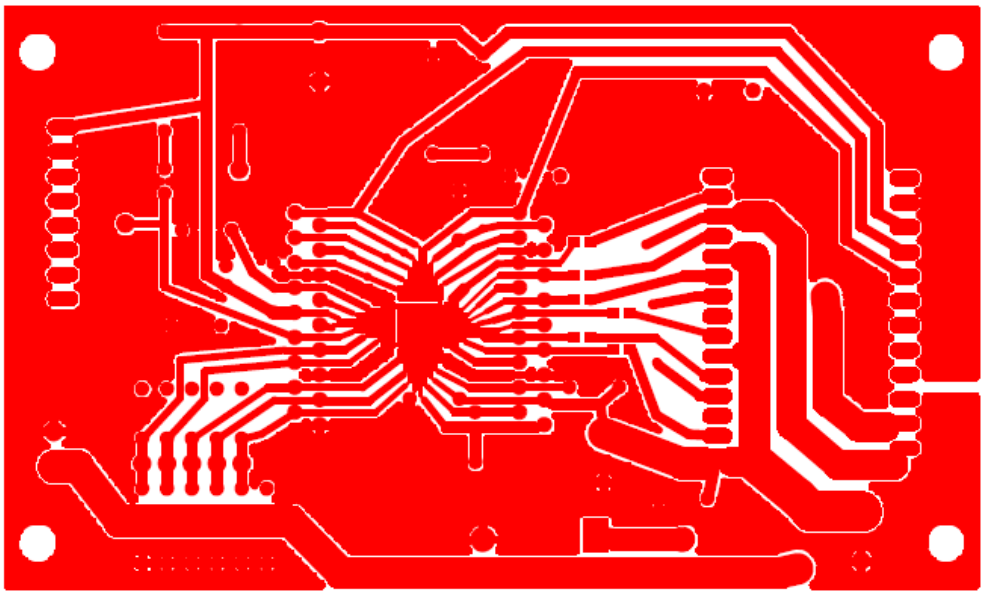
13. Operation waveform

TBD

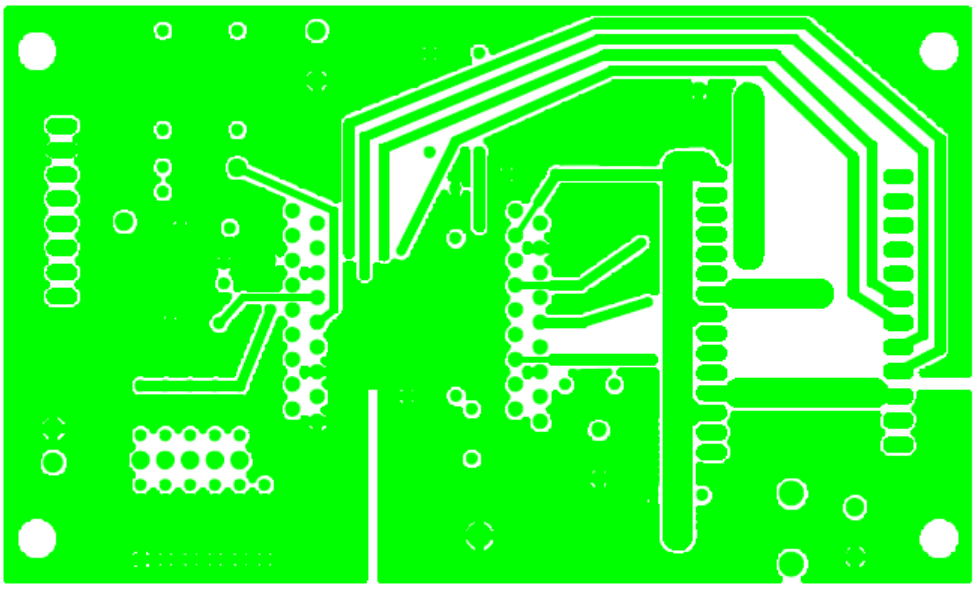
14. Evaluation board circuit diagram



15. Pattern layout for evaluation board



Component side



Solder side

※Please note that there are some locations (such as pattern on QFN land part) partly different from the actual one due to the influence of PDF formatting.