S-8235A Series

FOR AUTOMOTIVE BATTERY PROTECTION IC FOR 3-SERIAL TO 5-SERIAL CELL PACK (SECONDARY PROTECTION)

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The S-8235A Series, for automotive use, is utilized for secondary protection of lithium-ion rechargeable batteries, and incorporates high-accuracy voltage detection circuits and delay circuits. Short-circuiting between cells makes it possible for serial connection of 3-cell to 5-cell. By connecting in cascade, the S-8235A Series protects 6-serial or more cells lithium-ion rechargeable battery pack.
The S-8235A Series performs a self-test operation to confirm overcharge detection.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.

■ Features

- High-accuracy voltage detection circuit for each cell
  Overcharge detection voltage n (n = 1 to 5)
  3.60 V to 4.50 V (50 mV step)
  Accuracy ±20 mV (Ta = +25°C)
  Accuracy ±30 mV (Ta = −5°C to +55°C)
  Overcharge hysteresis voltage n (n = 1 to 5)
  0.0 mV to −550 mV (50 mV step)
  −300 mV to −550 mV Accuracy ±20%
  −100 mV to −250 mV Accuracy ±50 mV
  0.0 mV to −50 mV Accuracy ±25 mV
- Self-test operation to confirm overcharge detection is available.
- Cascade connection is available.
- Delay times for overcharge detection can be set by an internal circuit only (External capacitors are unnecessary).
- High-withstand voltage: Absolute maximum rating 26 V
- Wide operation voltage range: 6 V to 24 V
- Wide operation temperature range: Ta = −40°C to +85°C
- Low current consumption
  At V_{CUn} − 1.0 V for each cell: 10 μA max. (Ta = +25°C)
  At 2.3 V for each cell: 8 μA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified *1

***1.** Contact our sales office for details.

■ Application

- Lithium-ion rechargeable battery pack (for secondary protection)

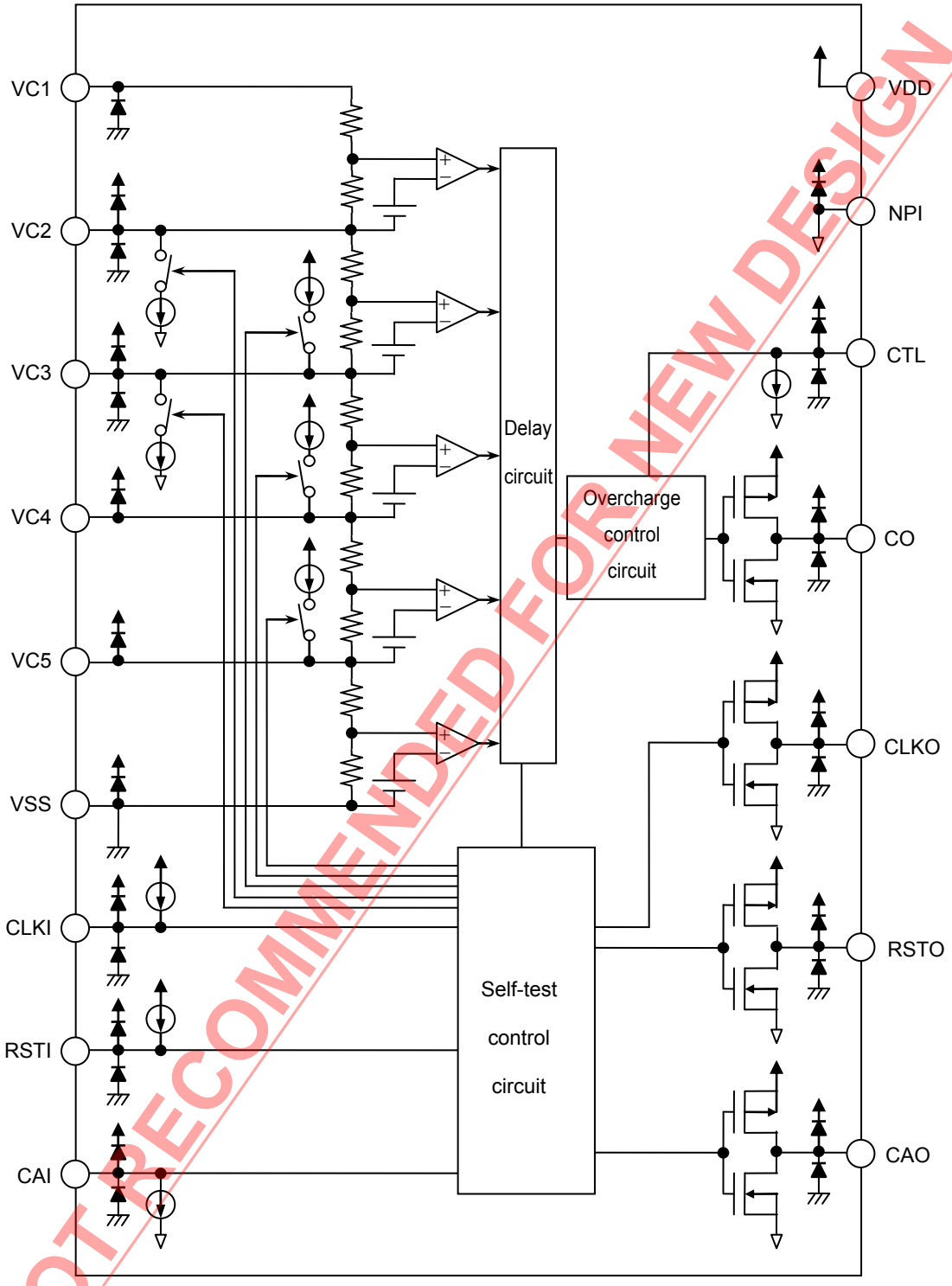
■ Package

- 16-Pin TSSOP

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■ Block Diagram



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Remark The diodes in the figure are parasitic diodes.

Figure 1

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■ AEC-Q100 Qualified

This IC supports AEC-Q100 for the operation temperature grade 3.
Contact our sales office for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name

S-8235A xx - TCT1 U

- Environmental code
  U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  TCT1: 16-Pin TSSOP, Tape
- Serial code*2
  Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
16-Pin TSSOP	FT016-A-P-SD	FT016-A-C-SD	FT016-A-R-S1

3. Product name list

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Hysteresis Voltage [V_{HC}]	Overcharge Detection Delay Time*1 [t_{CU}]
S-8235AAA-TCT1U	4.050 V	−0.050 V	1.0 s
S-8235AAB-TCT1U	4.050 V	−0.250 V	1.0 s
S-8235AAC-TCT1U	4.250 V	−0.250 V	2.0 s
S-8235AAD-TCT1U	4.350 V	−0.150 V	2.0 s
S-8235AAE-TCT1U	4.350 V	−0.150 V	1.0 s
S-8235AAG-TCT1U	4.550 V	−0.250 V	1.0 s
S-8235AAH-TCT1U	3.825 V	−0.250 V	4.0 s
S-8235AAI-TCT1U	4.450 V	−0.150 V	1.0 s
S-8235AAJ-TCT1U	4.500 V	−0.350 V	512 ms
S-8235AAK-TCT1U	4.250 V	−0.100 V	1.0 s
S-8235AAL-TCT1U	4.700 V	−0.350 V	512 ms
S-8235AAM-TCT1U	4.300 V	−0.250 V	2.0 s

***1.** Overcharge detection delay time is selectable in 1.0 s / 2.0 s / 4.0 s / 8.0 s.

Remark Please contact our sales office for products with detection voltage values other than those specified above.

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■ Pin Configuration

1. 16-Pin TSSOP

Top view

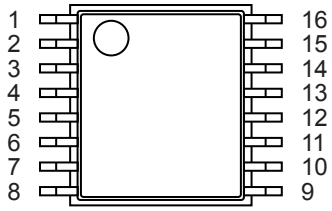


Figure 2

Table 3

Pin No.	Symbol	Description
1	VDD	Input pin for positive power supply
2	VC1	Positive voltage monitoring pin of battery 1
3	VC2	Negative voltage monitoring pin of battery 1, Positive voltage monitoring pin of battery 2
4	VC3	Negative voltage monitoring pin of battery 2, Positive voltage monitoring pin of battery 3
5	VC4	Negative voltage monitoring pin of battery 3, Positive voltage monitoring pin of battery 4
6	VC5	Negative voltage monitoring pin of battery 4, Positive voltage monitoring pin of battery 5
7	VSS	Negative voltage monitoring pin of battery 5
8	NPI	Input pin for negative power supply
9	CO	Connection pin of charge control FET gate
10	CAO	Output pin for chip active signal
11	CLKI	Input pin for clock signal
12	RSTI	Input pin for reset signal
13	RSTO	Output pin for reset signal
14	CLKO	Output pin for clock signal
15	CAI	Input pin for chip active signal
16	CTL	Input pin for charge control

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■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 26	V
Input voltage between VDD pin and NPI pin	V_{DN}	VDD	V_{NPI} − 0.3 to V_{NPI} + 26	V
Input pin voltage	V_{IN}	VC1	V_{SS} − 0.3 to V_{SS} + 26	V
		VC2, VC3, CLKI, RSTI, CAI, CTL	V_{SS} − 0.3 to V_{DD} + 0.3	V
		VC4, VC5	V_{DD} − 26 to V_{DD} + 0.3	V
Output pin voltage	V_{OUT}	CO, CAO, CLKO, RSTO	V_{SS} − 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	−	1100*1	mW
Operation ambient temperature	T_{opr}	−	−40 to +85	°C
Storage temperature	T_{stg}	−	−40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

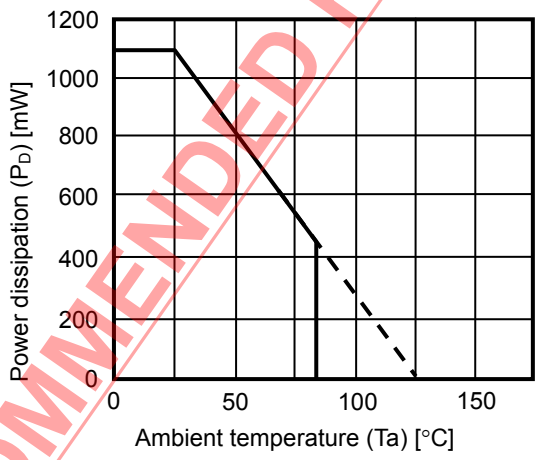


Figure 3 Power Dissipation of Package (When Mounted on Board)

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■ Electrical Characteristics

Table 5

(Ta = +25°C, $V_{DN} = V_{DD} - V_{NPI} = V1 + V2 + V3 + V4 + V5 = 17.5$ V, unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection Voltage						
Overcharge detection voltage n (n = 1 to 5)	V_{CUn}	–	$V_{CU} - 0.020$	V_{CU}	$V_{CU} + 0.020$	V
		Ta = –5°C to +55°C*1	$V_{CU} - 0.030$	V_{CU}	$V_{CU} + 0.030$	V
Overcharge hysteresis voltage n (n = 1 to 5)	V_{HCn}	–550 mV ≤ V_{HC} ≤ –300 mV	$V_{HC} \times 0.8$	V_{HC}	$V_{HC} \times 1.2$	V
		–250 mV ≤ V_{HC} ≤ –100 mV	$V_{HC} - 0.050$	V_{HC}	$V_{HC} + 0.050$	V
		V_{HC} = –50 mV, 0 mV	$V_{HC} - 0.025$	V_{HC}	$V_{HC} + 0.025$	V
Input Voltage						
Operation voltage between VDD pin and NPI pin	V_{DNOP}	–	6	–	24	V
CLKI pin voltage "H"	V_{CLKIH}	–	$V_{NPI} + 0.5$	–	–	V
CLKI pin voltage "L"	V_{CLKIL}	–	–	–	$V_{NPI} + 0.05$	V
RSTI pin voltage "H"	V_{RSTIH}	–	$V_{NPI} + 0.5$	–	–	V
RSTI pin voltage "L"	V_{RSTIL}	–	–	–	$V_{NPI} + 0.05$	V
CAI pin voltage "H"	V_{CAIH}	–	$V_{DD} - 0.05$	–	–	V
CAI pin voltage "L"	V_{CAIL}	–	–	–	$V_{DD} - 0.5$	V
CTL pin voltage "H"	V_{CTLH}	–	$V_{DD} - 0.05$	–	–	V
CTL pin voltage "L"	V_{CTLL}	–	–	–	$V_{DD} - 0.5$	V
Input Current						
Current consumption during operation	I_{OPE}	V1 = V2 = V3 = V4 = V5 = V_{CU} – 1.0 V	–	5	10	µA
Current consumption during overdischarge	I_{OPED}	V1 = V2 = V3 = V4 = V5 = 2.3 V	–	4	8	µA
VCn pin current (n = 1 to 5)	I_{VCn}	V1 = V2 = V3 = V4 = V5 = V_{CU} – 1.0 V	–1.0	0	1.0	µA
VCn pin pull-down current (n = 2, 3)	I_{VCLn}	V1 = V2 = V3 = V4 = V5 = V_{CU} – 1.0 V	0.9	1.0	1.1	mA
		Ta = –40°C to +85°C*1	0.7	1.0	1.3	mA
VCn pin pull-up current (n = 3 to 5)	I_{VCHn}	V1 = V2 = V3 = V4 = V5 = V_{CU} – 1.0 V	–1.1	–1.0	–0.9	mA
		Ta = –40°C to +85°C*1	–1.3	–1.0	–0.7	mA
CLKI pin current "H"	I_{CLKIH}	–	3.0	10	20	µA
CLKI pin current "L"	I_{CLKIL}	$V_{CLKI} = V_{NPI}$	–1.0	–0.7	–0.4	µA
RSTI pin current "H"	I_{RSTIH}	–	3.0	10	20	µA
RSTI pin current "L"	I_{RSTIL}	$V_{RSTI} = V_{NPI}$	–1.0	–0.7	–0.4	µA
CAI pin current "H"	I_{CAIH}	$V_{CAI} = V_{DD}$	0.4	0.7	1.0	µA
CAI pin current "L"	I_{CAIL}	–	–20	–10	–3.0	µA
CTL pin current "H"	I_{CTLH}	$V_{CTL} = V_{DD}$	0.4	0.7	1.0	µA
CTL pin current "L"	I_{CTLL}	–	–20	–10	–3.0	µA
Output Current						
CO pin source current	I_{COH}	–	–	–	–20	µA
CO pin sink current	I_{COL}	–	400	–	–	µA
CAO pin source current	I_{CAOH}	–	–	–	–10	µA
CAO pin sink current	I_{CAOL}	–	10	–	–	µA
RSTO pin source current	I_{RSTOH}	–	–	–	–10	µA
RSTO pin sink current	I_{RSTOL}	–	10	–	–	µA
CLKO pin source current	I_{CLKOH}	–	–	–	–10	µA
CLKO pin sink current	I_{CLKOL}	–	10	–	–	µA
Delay Time						
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.8$	t_{CU}	$t_{CU} \times 1.2$	s
Overcharge timer reset delay time	t_{TR}	–	6	12	20	ms

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

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■ Test Circuit

In **Figure 4**, the following statuses are the initial statuses 1 to 4.

Initial status 1: Set V1 = V2 = V3 = V4 = V5 = 2.8 V, SW_{CO} = SW_{CAO} = SW_{RSTO} = SW_{CLKO} = OFF, V8 = 0 V, V9 = 5 V, V12 = V13 = 0 V.
Initial status 2: Set V1 = V2 = V3 = V4 = V5 = 3.5 V in initial status 1.
Initial status 3: Set V9 = 0 V in initial status 2, and output 8 clocks*1 from V8.
Initial status 4: Set V1 = V2 = V3 = V4 = V5 = 2.8 V, V8 = 0 V, V9 = 0 V, V12 = V13 = 0 V.

***1.** 1 clock is defined as follows.
"H": Output of 5 V for 50 ms or more
"L": Output of 0 V for 50 ms or more

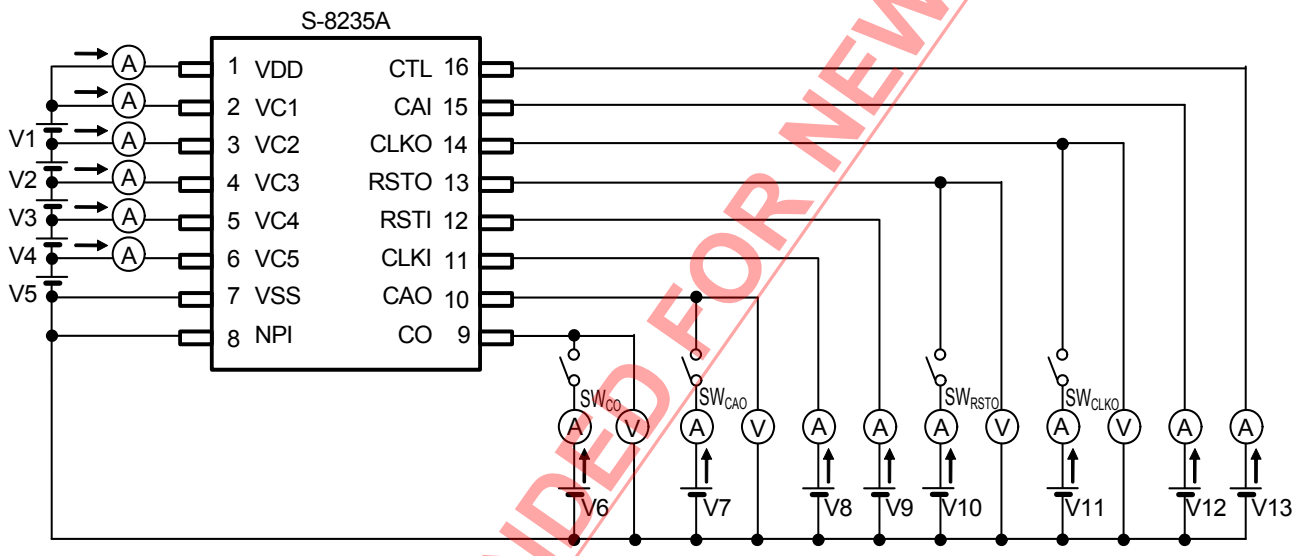


Figure 4 Test Circuit

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1. Overcharge detection voltage n (V_{CUn}), Overcharge hysteresis voltage n (V_{HCn})

Set V1 = V2 = V3 = V4 = V5 = V_{CU} – 0.050 V in initial status 1. V_{CU1} is defined as the voltage V1 when the CO pin output changes after the V1 voltage is gradually increased. V_{CUn} (n = 2 to 5) can also be defined in the same way as V_{CU1}.
Moreover, set V1 = V_{CU} + 0.050 V, V2 = V3 = V4 = V5 = 2.8 V in initial status 1. V_{HC1} is defined as the difference between V1 and V_{HC1} when the CO pin output changes again after the V1 voltage is gradually decreased. V_{HCn} (n = 2 to 5) can also be defined in the same way as V_{HC1}.

2. CLKI pin voltage "H" (V_{CLKIH}), CLKI pin voltage "L" (V_{CLKIL}), RSTI pin voltage "L" (V_{RSTIL}), RSTI pin voltage "H" (V_{RSTIH})

V_{CLKIH} is defined as the voltage V8 when the CLKO pin output changes after the voltage V8 is gradually increased in initial status 3. After that, V_{CLKIL} is defined as the voltage V8 when the CLKO pin output changes again after the voltage V8 is gradually decreased.
V_{RSTIL} is defined as the voltage V9 when the CLKO pin output changes after the voltage V9 is gradually decreased in initial status 2. After that, V_{RSTIH} is defined as the voltage V9 when the CLKO pin output changes again after the voltage V9 is gradually increased.

3. CAI pin voltage "H" (V_{CAIH}), CAI pin voltage "L" (V_{CAIL})

Set V12 = V_{DN} – 0.5 V, V9 = 0 V in initial status 2. Repeat increasing the voltage V12 and outputting 9 clocks from V8. V_{CAIH} is defined as the minimum voltage V12 when the CAO pin output changes.
Set V12 = V_{DN}, V9 = 0 V in initial status 2. Repeat decreasing the voltage V12 and outputting 9 clocks from V8. V_{CAIL} is defined as the maximum voltage V12 when the CAO pin output does not change.

4. CTL pin voltage "H" (V_{CTLH}), CTL pin voltage "L" (V_{CTLL})

Set V13 = V_{DN} – 0.5 V in initial status 2. V_{CTLH} is defined as the voltage V13 when the CO pin output changes after the voltage V13 is gradually increased.
Set V13 = V_{DN} in initial status 2. V_{CTLL} is defined as the voltage V13 when the CO pin output changes again after the voltage V13 is gradually decreased.

5. Current consumption during operation (I_{OPE}), Current consumption during overdischarge (I_{OPED})

Set V1 = V2 = V3 = V4 = V5 = V_{CU} – 1.0 V, V8 = V9 = V_{DN} in initial status 1. I_{OPE} is defined as the total current which flows in the VDD pin and the VC1 pin.
Set V1 = V2 = V3 = V4 = V5 = 2.3 V, V8 = V9 = V_{DN} in initial status 1. I_{OPED} is defined as the total current which flows in the VDD pin and the VC1 pin.

6. VCn pin current (I_{VCn})

Set V1 = V2 = V3 = V4 = V5 = V_{CU} – 1.0 V in initial status 1. I_{VCn} is defined as the current which flows in the VCn pin (n = 1 to 5), respectively.

7. VCn pin pull-down current (I_{VCLn}), VCn pin pull-up current (I_{VCHn})

Set V1 = V2 = V3 = V4 = V5 = V_{CU} – 1.0 V, V9 = 0 V in initial status 1. I_{VCL2} is defined as the current which flows in the VC2 pin after increasing the voltage V8 up to 5 V.
I_{VCL3} is defined as the current which flows in the VC3 pin subsequently after decreasing the voltage V8 down to 0 V and increasing the voltage V8 up to 5 V. After that, each time increasing the voltage V8 up to 5 V from 0 V, the current which flows in the VCn pin (n = 3 to 5) is defined in order of I_{VCH3}, I_{VCH4}, and I_{VCH5}, respectively.

8. CLKI pin current "H" (I_{CLKIH}), CLKI pin current "L" (I_{CLKIL})

Set V8 = V_{DN} – 2.0 V, V9 = 0 V in initial status 2. I_{CLKIH} is defined as the maximum current which flows in the CLKI pin when voltage V8 is gradually increased. I_{CLKIL} is defined as the current which flows in the CLKI pin after setting V9 = 0 V in initial status 2.

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9. RSTI pin current "H" (I_{RSTIH}), RSTI pin current "L" (I_{RSTIL})

Set V9 = V_{DN} – 2.0 V in initial status 2. I_{RSTIH} is defined as the maximum current which flows in the RSTI pin when the voltage V9 is gradually increased. I_{RSTIL} is defined as the current which flows in the RSTI pin after setting V9 = 0 V in initial status 2.

10. CAI pin current "H" (I_{CAIH}), CAI pin current "L" (I_{CAIL})

I_{CAIH} is defined as the current which flows in the CAI pin after setting V9 = 0 V, V12 = V_{DN} in initial status 2.
Set V12 = 2.0 V, V9 = 0 V. I_{CAIL} is defined as the minimum current which flows in the CAI pin when the voltage V12 is gradually decreased.

11. CTL pin current "H" (I_{CTLH}), CTL pin current "L" (I_{CTLL})

I_{CTLH} is defined as the current which flows in the CTL pin after setting V13 = V_{DN} in initial status 2.
Set V13 = 2.0 V, V9 = 0 V in initial status 2. I_{CTLL} is defined as the minimum current which flows in the CTL pin when the voltage V13 is gradually decreased.

12. CO pin sink current (I_{COL}), CO pin source current (I_{COH})

I_{COL} is defined as the current which flows in the CO pin after setting SW_{CO} = ON, V6 = 0.5 V in initial status 2.
I_{COH} is defined as the current which flows in the CO pin after setting SW_{CO} = ON, V13 = V_{DN}, V6 = V_{DN} – 0.5 V in initial status 2.

13. CAO pin sink current (I_{CAOL}), CAO pin source current (I_{CAOH})

I_{CAOL} is the current which flows in the CAO pin after setting SW_{CAO} = ON, V7 = 0.5 V in initial status 2.
I_{CAOH} is the current which flows in the CAO pin after setting SW_{CAO} = ON, V9 = 0.5 V, V8 = 5 V, V7 = V_{DN} – 0.5 V in initial status 2.

14. RSTO pin sink current (I_{RSTOL}), RSTO pin source current (I_{RSTOH})

I_{RSTOL} is defined as the current which flows in the RSTO pin after setting SW_{RSTO} = ON, V10 = 0.5 V in initial status 3.
I_{RSTOH} is defined as the current which flows in the RSTO pin after setting SW_{RSTO} = ON, V10 = V_{DN} – 0.5 V in initial status 2.

15. CLKO pin sink current (I_{CLKOL}), CLKO pin source current (I_{CLKOH})

I_{CLKOL} is defined as the current which flows in the CLKO pin after setting SW_{CLKO} = ON, V9 = 0 V, V11 = 0.5 V in initial status 2.
I_{CLKOH} is defined as the current which flows in the CLKO pin after setting SW_{CLKO} = ON, V11 = V_{DN} – 0.5V in initial status 2.

16. Overcharge detection delay time (t_{CU})

t_{CU} is defined as the time period until the CO pin output changes after increasing the voltage V1 up to 5.0 V in initial status 1.

17. Overcharge timer reset delay time (t_{TR})

Increase the voltage V1 up to 5.0 V in initial status 1 (first rising), and decrease the voltage V1 down to 2.8 V within t_{CU}. After that, increase voltage V1 up to 5.0 V again (second rising), and measure the time period until the CO pin output changes. If the time period from when the voltage V1 is decreased to the second rising is short, CO pin output changes after t_{CU} is elapsed from the first rising. When the time period is gradually made longer, CO pin output changes after t_{CU} is elapsed from the second rising. t_{TR} is defined as the time period from when the voltage V1 is decreased to the second rising.

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■ Operation

1. Normal status

If the voltage of each of the batteries is lower than "overcharge detection voltage n (V_{CUn}) + overcharge hysteresis voltage n (V_{HCn})", CO pin output changes to "L". This is called normal status.

2. Overcharge status

When the voltage of one of the batteries exceeds V_{CUn} during a charging operation at normal status, and the status is retained for overcharge detection delay time (t_{CU}) or longer, CO pin output changes to "H". This is called overcharge status.

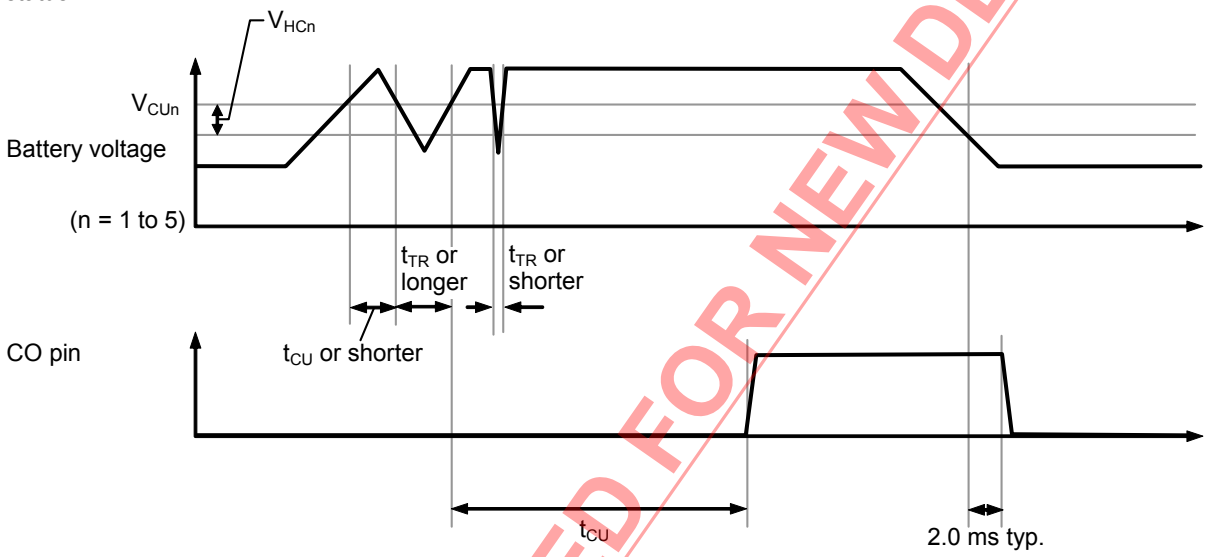


Figure 5 Overcharge Detection Operation

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3. Overcharge timer reset function

The S-8235A Series has an overcharge timer reset function.
If overcharge release noise which temporarily falls below overcharge detection voltage n (V_{CUn}) is input during overcharge detection delay time (t_{CU}) from when the voltage of one of the batteries during a charging operation exceeds V_{CUn} until when charging is stopped, t_{CU} is continuously counted if the time of overcharge release noise is shorter than overcharge timer reset delay time (t_{TR}). On the other hand, under the same status, if the time of overcharge release noise is t_{TR} or longer, counting of t_{CU} is reset once. After that, when V_{CUn} is exceeded, counting t_{CU} resumes.

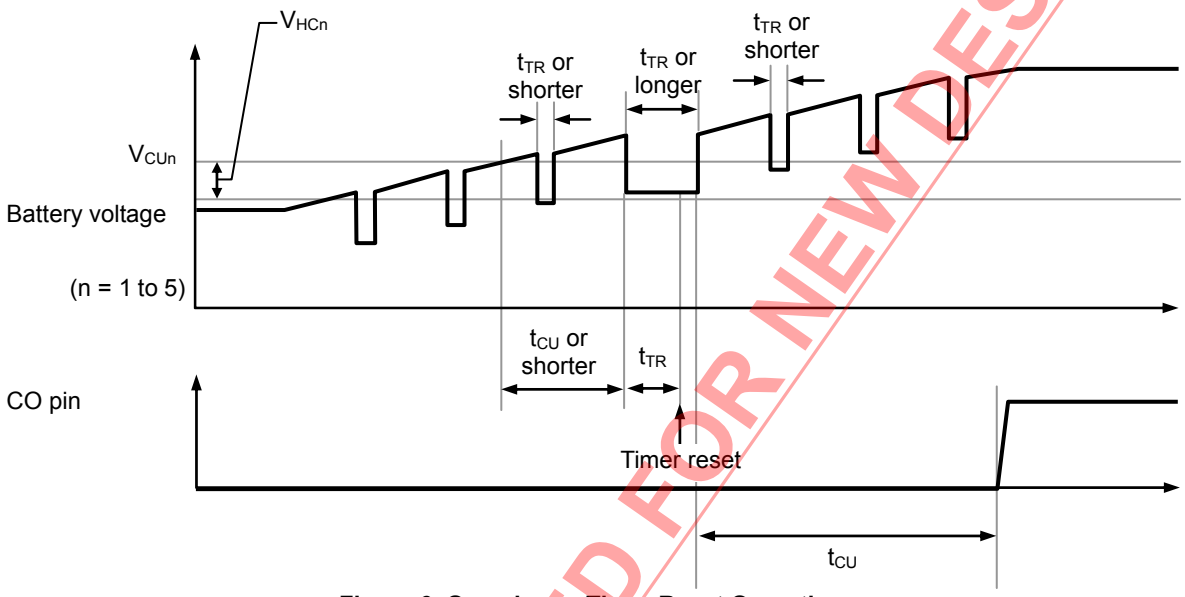


Figure 6 Overcharge Timer Reset Operation

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■ Battery Protection IC Connection Example

1. 8-serial cell (5-cell + 3-cell, cascade connection)

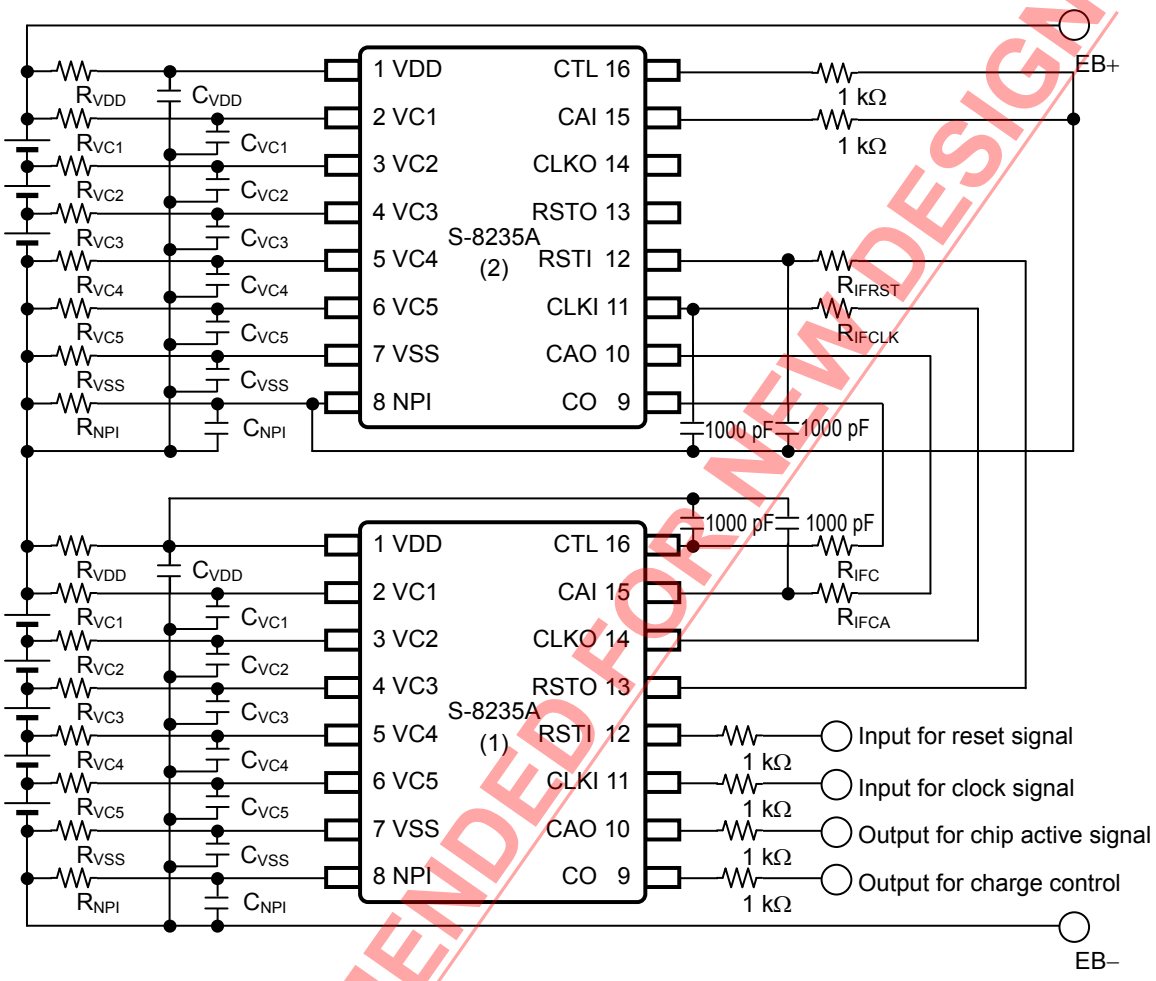


Figure 7

Table 6 Constants for External Components

Part	Min.	Typ.	Max.	Unit
R_{VDD}, R_{NPI}	0.1	1	1	kΩ
R_{VCn}, R_{VSS}	0.25	1.2	1.2	kΩ
R_{IFC}, R_{IFCA}, R_{IFCLK}, R_{IFRST}	–	5.1	–	MΩ
C_{VDD}, C_{NPI}	0.075	0.1	1	μF
C_{VCn}, C_{VSS}	0.075	0.1	1	μF

Caution
1. The above constants are subject to change without prior notice.
2. The example of connection shown above and the constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.
3. R_{VC1} to R_{VC5} should be the same constant. C_{VDD}, C_{VC1} to C_{VC5}, C_{VSS}, and C_{NPI} should be the same constant.
4. Set R_{VDD} and C_{VDD} so that the condition $R_{VDD} \times C_{VDD} \geq 7.5 \times 10^{-5}$ is satisfied.
5. Set R_{VCn} and C_{VCn} so that the condition $1.0 \leq (R_{VCn} \times C_{VCn}) / (R_{VDD} \times C_{VDD}) \leq 1.2$ is satisfied.
6. Connect R_{IFC}, R_{IFCA}, R_{IFCLK}, and R_{IFRST} as close to the input pin as possible.

Remark n = 1 to 5

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■ Self-test Function

The S-8235A Series has a self-test function to confirm overcharge detection operation.
Due to the self-test function, a current flows in an external resistor, the voltage between voltage monitoring pins expands, and then the S-8235A Series spuriously becomes overcharge status (Refer to **Figure 8**). I_{VCLn} or I_{VCHn} flows in R_{VCn} during the self-test operation. Since the S-8235A Series detects overcharge when the voltage between voltage monitoring pins exceeds overcharge detection voltage n (V_{CUn}), it is possible to confirm whether the S-8235A Series normally detects the overcharge or not by monitoring the CO pin output signal.

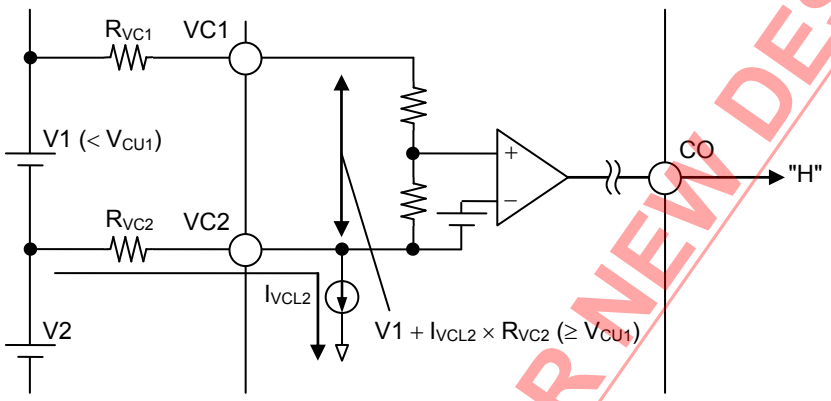


Figure 8 Self-test Operation between VC1 Pin and VC2 Pin

When not using the self-test function, short-circuit the CLKI pin and the VDD pin, the RSTI pin and the VDD pin via a resistor of 1 kΩ, respectively. And short-circuit the CAI pin and the NPI pin via a resistor of 1 kΩ.

1. Description of Input pin

1. 1 RSTI (Input for reset signal) pin

The RSTI pin inputs a reset signal for the self-test function. When "H" is input to the RSTI pin, the S-8235A Series exits from the self-test function, and carries out the battery protection operation. When "L" is input to the RSTI pin, the self-test function is activated.
The RSTI pin current changes depending on the input voltage as the characteristics shown in **Figure 9**.

1. 2 CTL (Input for charge control) pin

The CTL pin controls the CO (Connection of charge control FET gate) pin. When "H" is input to the CTL pin, the CO pin outputs "H" after 1.0 ms typ. in normal status, and maintains "H" in the overcharge status.
The CTL pin current changes depending on the input voltage as the characteristics shown in **Figure 10**.

1. 3 CLKI (Input for clock signal) pin

The CLKI pin inputs clock signal for the self-test function. While the self-test function is activated, the each output pin outputs the signal by synchronizing with this clock signal.
The CLKI pin current changes depending on the input voltage as the characteristics shown in **Figure 9**.

1. 4 CAI (Input for chip active signal) pin

The CAI pin inputs the chip active signal for the self-test function in cascade connection.
The CAI pin current changes depending on the input voltage as the characteristics shown in **Figure 10**.

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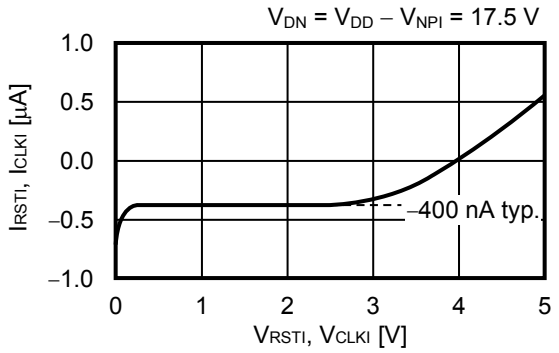


Figure 9 RSTI / CLKI Pin Current Characteristics

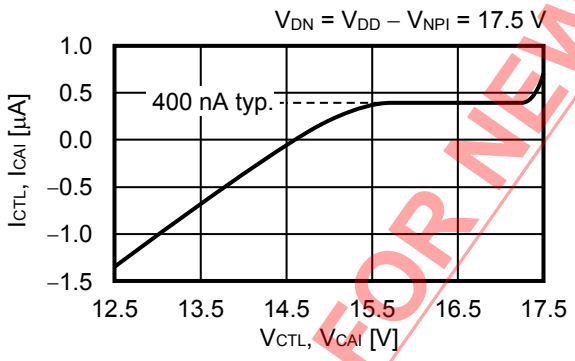


Figure 10 CTL / CAI Pin Current Characteristics

The status of pins for the S-8235A Series is shown in **Table 7**.

Table 7

I/O	Symbol	Battery Protection Operation								Self-test Operation							
Input	RSTI	"H"				"L"				"L"							
	CTL	"H"				"L"				"H"				"L"			
	CLKI	"H"		"L"		"H"		"L"		"H"		"L"		"H"		"L"	
	CAI	"H"	"L"	"H"	"L"	"H"	"L"	"H"	"L"	"H"	"L"	"H"	"L"	"H"	"L"	"H"	"L"
Output	CO	"H"				"L" (Normal status) / "H" (Overcharge status)				"H"				"L" (Normal status) / "H" (Overcharge status)			
	RSTO	"H"								Refer to "**3. RSTO (Output for reset signal) pin**"							
	CLKO	"H"								Refer to "**4. CLKO (Output for clock signal) pin**"							
	CAO	"L"								Refer to "**5. CAO (Output for chip active signal) pin**"							

2. Self-test operation at the time of cascade connection

The S-8235A Series devices can be connected in cascade.
By connecting as shown in **Figure 7**, the S-8235A Series protects 6-serial or more cells lithium-ion rechargeable battery pack.

At the time of cascade connection, the CO pin output signal for upper device of the S-8235A Series is transmitted by connecting the CO pin and the CTL pin, and is output from the CO pin at the lower device. Therefore, it is possible to confirm whether all devices of the S-8235A Series normally detects the overcharge or not by monitoring the CO pin output signal for the lowest device of the S-8235A Series.

On the other hand, the CAO pin output signal for the upper device of the S-8235A Series is transmitted by connecting the CAO pin and the CAI pin, and is output from the CAO pin at the lower device. Therefore, it is possible to confirm which device of the S-8235A Series is in a self-test operation by monitoring the CAO pin output signal for the lowest device of the S-8235A Series.

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3. RSTO (Output for reset signal) pin

The RSTO pin outputs a reset signal to the next device. The reset signal is transmitted from the lower device to the upper device. When "H" is input to the RSTI pin, the S-8235A Series is reset and performs a normal operation. When inputting "L", the reset operation is released, and a self-test operation is initiated.
The RSTO pin outputs "L" after the 8th clock falling when inputting a clock signal (10 Hz typ.) to the CLKI pin (a1 in **Figure 11**). Thereby, a self-test operation in the next device is initiated.
The RSTO pin outputs "H" when inputting "H" to the RSTI pin (a2 in **Figure 11**).

4. CLKO (Output for clock signal) pin

The CLKO pin outputs a clock signal to the next device. The clock signal is transmitted from the lower device to the upper device. The CLKO pin outputs "L" when inputting "L" to the RSTI pin (b1 in **Figure 11**). After that, the CLKO pin outputs "H" at the 9th clock or subsequent clocks, and outputs "L" after falling (b2 in **Figure 11**). Thereby, a clock signal is input to the next device.
The CLKO pin outputs "H" when inputting "H" to the RSTI pin (b3 in **Figure 11**).

5. CAO (Output for chip active signal) pin

The CAO pin outputs a chip active signal to the next device. The signal is to confirm which device of the S-8235A Series is in a self-test operation. The chip active signal is transmitted from the upper device to the lower device. The CAO pin output signal from the 1st clock to the 8th clock is controlled according to a clock signal that is input to the CLKI pin, and, at the 9th clock or subsequent clocks, it is controlled according to a signal that is input to the CAI pin of the lower device from the CAO pin of the upper device.
The CAO pin outputs "H" at the 1st clock rising when inputting a clock signal to the CLKI pin after inputting "L" to the RSTI pin (c1 in **Figure 11**). Thereby, it is possible to confirm that a self-test operation is performed.
And then, the CAO pin outputs "L" at the 8th clock falling (c2 in **Figure 11**).
At the 9th clock or subsequent clocks, the CAO pin outputs "H" at the next clock rising when inputting "H" to the CAI pin (c3 in **Figure 11**). For this reason, the CAO pin of each device outputs "H" with a delay of 1 clock. Therefore, it is possible to confirm which device is in a self-test operation if the CAO pin output of the lowest device is monitored. When a self-test operation is performed in a device of "m" stage, the CAO pin output of the lowest device is as follows. After that, the CAO pin outputs "L" when inputting "L" to the CAI pin (c4 in **Figure 11**).

m = 1:	The CAO pin outputs "H" at the 1st clock rising after inputting "L" to the RSTI pin.
m = 2 to 8:	The CAO pin outputs "H" at m clock rising after it outputs "L".
$m \geq 9$:	The CAO pin maintains "L" after it outputs "L".

The CAO pin outputs "L" when inputting "H" to the RSTI pin (c5 in **Figure 11**).

6. VCn Pin (n = 2 to 5)

When inputting a clock signal to the CLKI pin, I_{VCL2} flows from the VC2 pin from the 1st clock rising to its falling (d1 in **Figure 11**). I_{VCL3} flows from the VC3 pin from the 2nd clock rising to its falling (d2 in **Figure 11**). And I_{VCH3} flows from the VC3 pin from the 3rd clock rising until its falling (d3 in **Figure 11**). I_{VCH4} flows from the VC4 pin at the 4th clock (d4 in **Figure 11**). I_{VCH5} flows from the VC5 pin at the 5th clock (d5 in **Figure 11**).

7. Overcharge detection delay time (t_{CU}) during self-test operation

When inputting a clock signal to the CLKI pin, t_{CU} is shortened to 8 ms typ. from the 1st clock rising to the 7th clock rising. The time period from when inputting "L" to the RSTI pin until the 1st clock rising and the time period from the 7th clock rising to the 8th clock falling are shortened to 32 ms typ., respectively. t_{CU} changes to the original value at the 9th or subsequent clocks.

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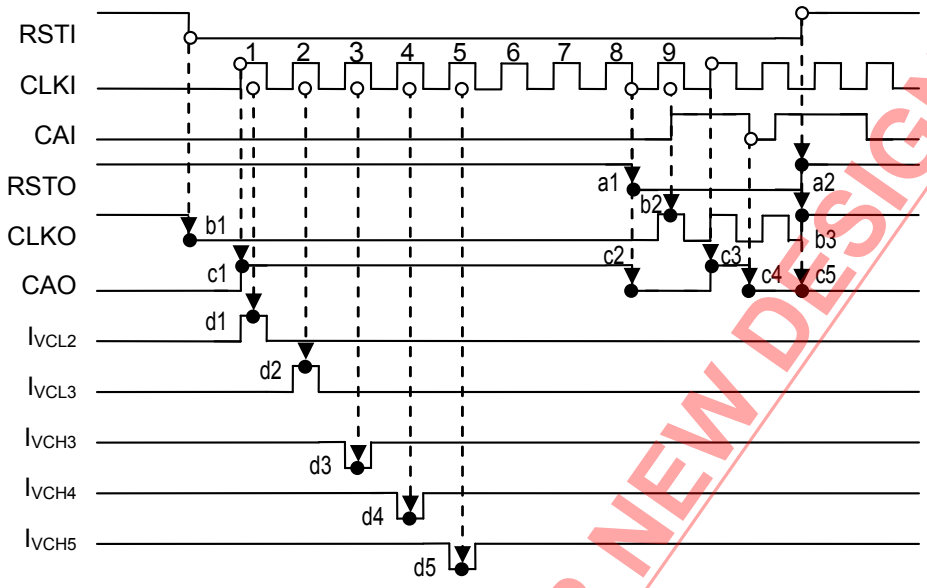


Figure 11

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8. Example of self-test operation

By connecting in cascade, the S-8235A Series performs a self-test operation in 6-serial or more cells protection circuit. The example of a self-test operation at the time of cascade connection is as follows.
Refer to **Table 7** in "■ **Self-test Function**" for the output pin voltage to be set depending on the input pin voltage.

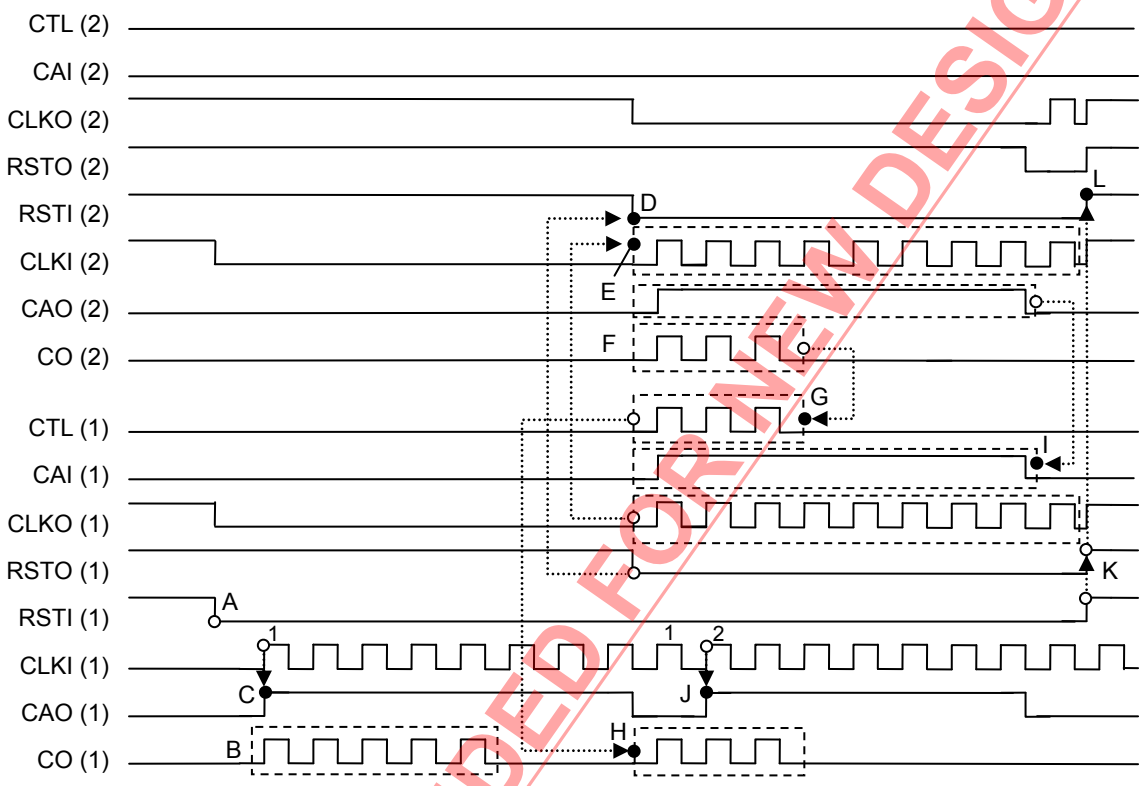


Figure 12 Timing Chart during Self-test Operation in 8-serial Cell (5-cell + 3-cell) Protection Circuit

<A> When inputting "L" to the RSTI pin of the S-8235A (1) (hereinafter, it is indicated as (1)), the self-test operation is initiated.
<B> When a clock signal is input to the CLKI pin of (1), the overcharge detection operation of (1) is confirmed.
<C> It is possible to confirm that the self-test operation is performed in (1).
<D> The RSTO pin of (1) outputs "L", and then the voltage is input to the RSTI pin of the S-8235A (2) (hereinafter, it is indicated as (2)).
<E> The CLKO pin output of (1) is input to the CLKI pin of (2).
<F> When a clock signal is input to the CLKI pin of (2), the overcharge detection operation of (2) is confirmed.
<G> The CO pin output of (2) is input to the CTL pin of (1).
<H> The CO pin output of (2) is output from the CO pin of (1).
<I> The CAO pin output of (2) is input to the CAI pin of (1).
<J> It is possible to confirm that the self-test operation is performed in (2).
<K> When inputting "H" to the RSTI pin of (1), the RSTO pin outputs "H".
<L> When "H" is input to the RSTI pin of (2), the self-test operation is terminated.

Caution 1. The S-8235A Series changes to the overcharge status if the voltage between voltage monitoring pins exceeds overcharge detection voltage n (V_{CUn}) during a self-test operation.
2. Since the voltage between voltage monitoring pins does not exceed V_{CUn} when a self-test operation is performed in battery voltage drop, the S-8235A Series may not detect the overcharge.

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■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

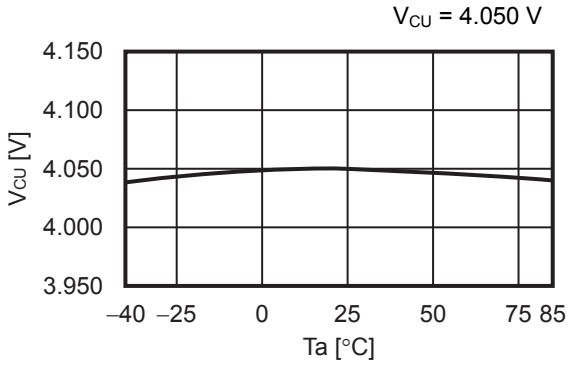
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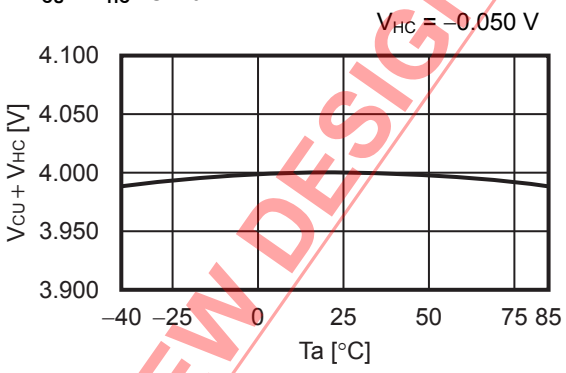
■ Characteristics (Typical Data)

1. Detection voltage

1. 1 V_{CU} vs. Ta

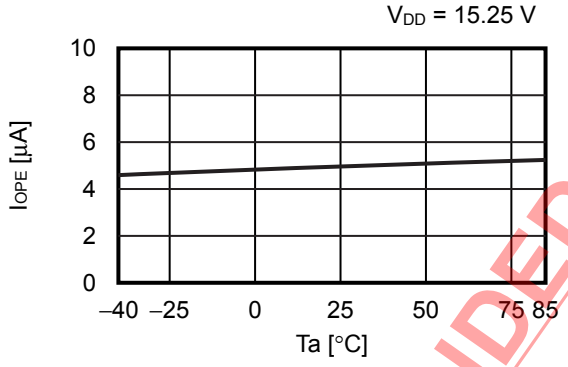


1. 2 V_{CU} + V_{HC} vs. Ta

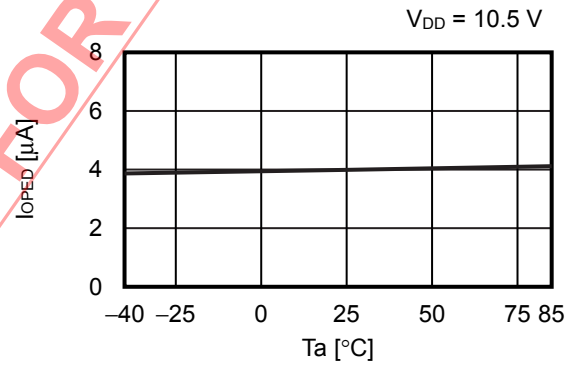


2. Current consumption

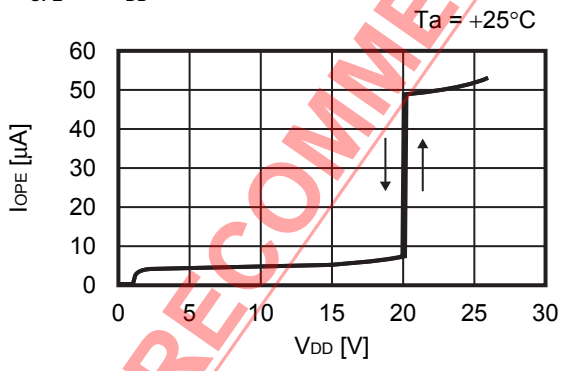
2. 1 I_{OPE} vs. Ta



2. 2 I_{OPED} vs. Ta



2. 3 I_{OPE} vs. V_{DD}

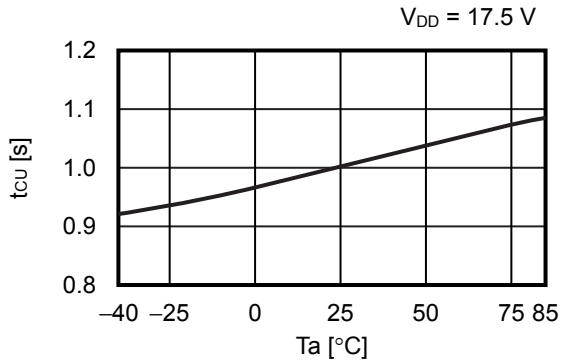


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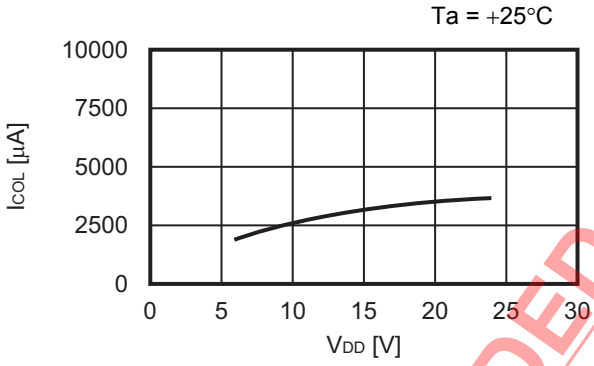
3. Delay time

3. 1 t_{CU} vs. Ta

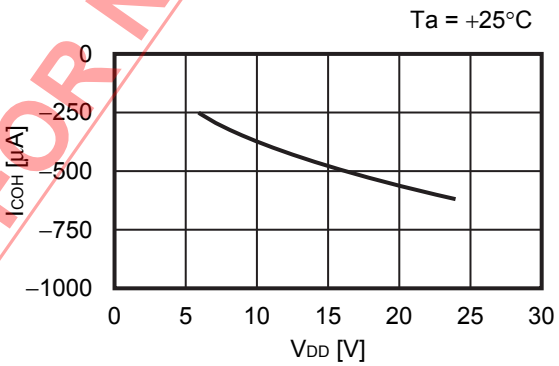


4. Output current

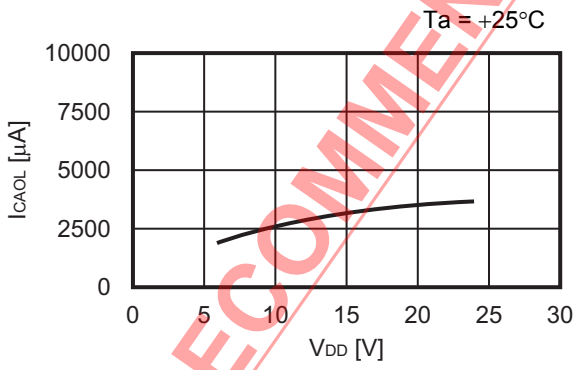
4. 1 I_{COL} vs. V_{DD}



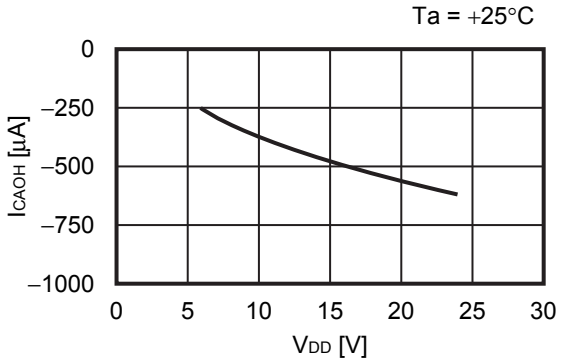
4. 2 I_{COH} vs. V_{DD}



4. 3 I_{CAOL} vs. V_{DD}



4. 4 I_{CAOH} vs. V_{DD}

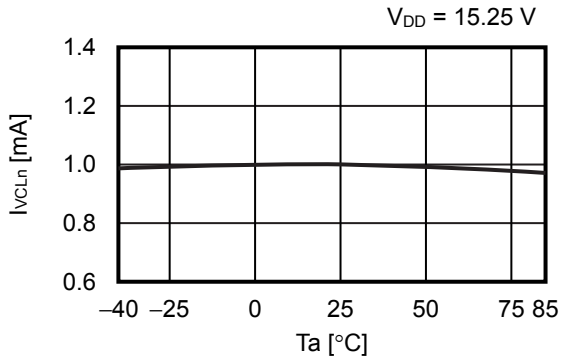


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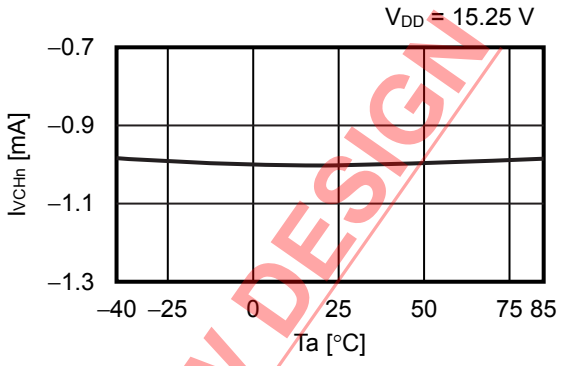
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5. Input current

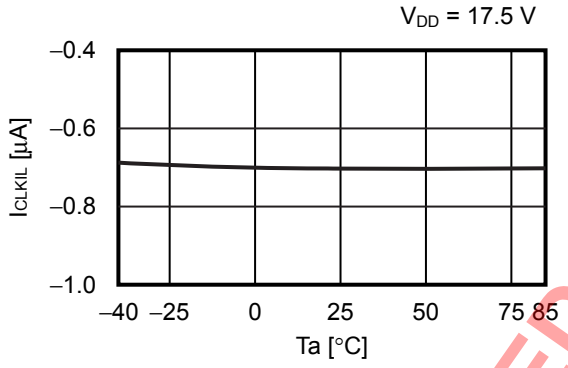
5. 1 I_{VCLn} vs. Ta



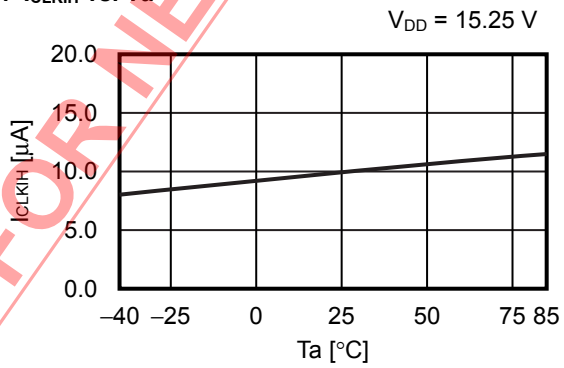
5. 2 I_{VCHn} vs. V_{DD}



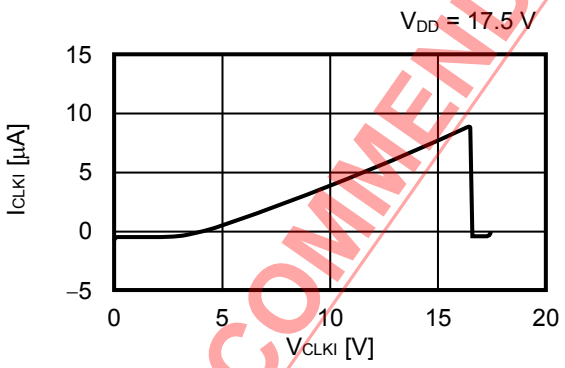
5. 3 I_{CLKIL} vs. Ta



5. 4 I_{CLKIH} vs. Ta



5. 5 I_{CLKI} vs. V_{CLKI}

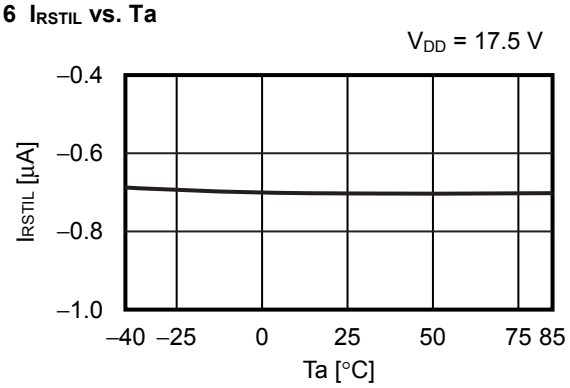


Remark n = 1 to 5

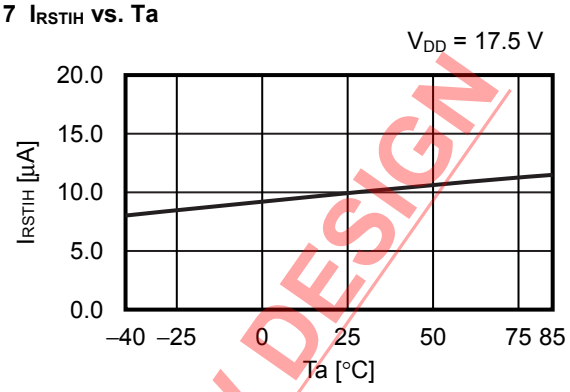
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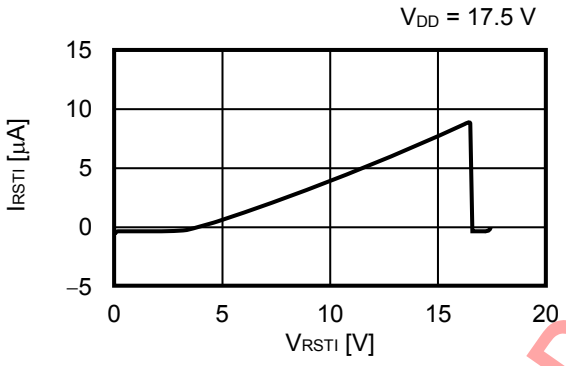
5. 6 I_{RSTIL} vs. Ta



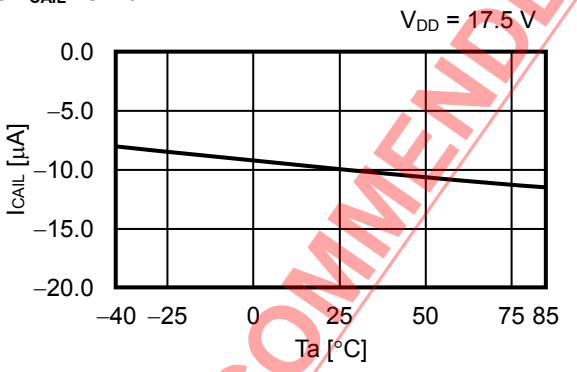
5. 7 I_{RSTIH} vs. Ta



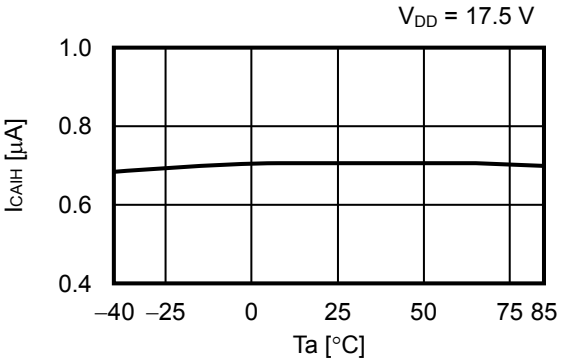
5. 8 I_{RSTI} – V_{RSTI}



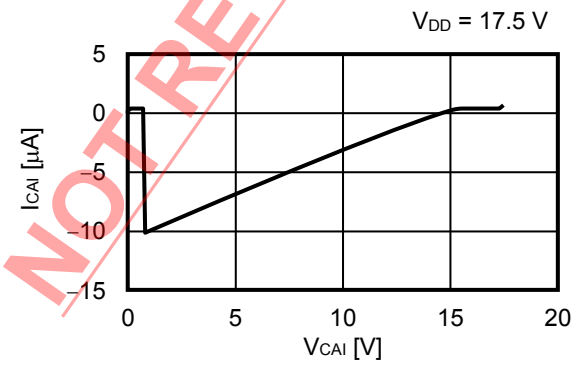
5. 9 I_{CAIL} vs. Ta



5. 10 I_{CAIH} vs. Ta



5. 11 I_{CAI} vs. V_{CAI}

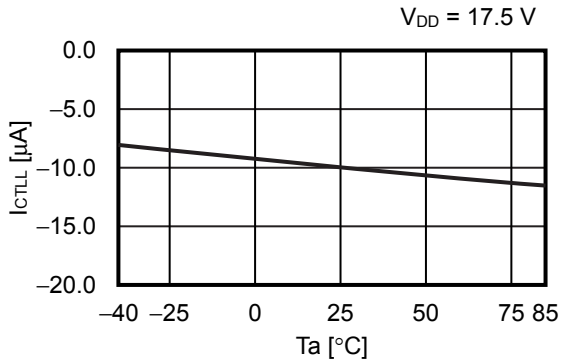


Remark n = 1 to 5

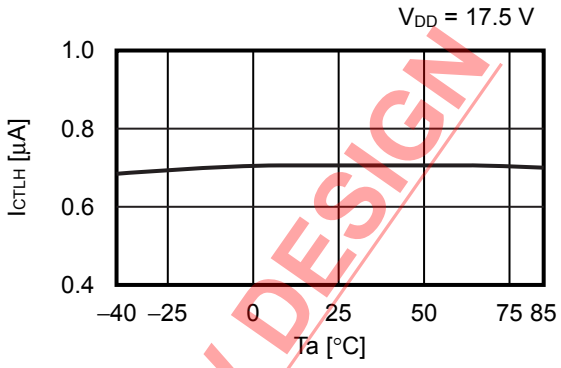
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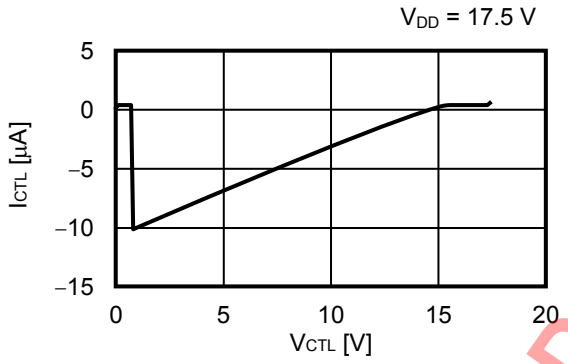
5. 12 I_{CTLL} vs. Ta



5. 13 I_{CTLH} vs. Ta



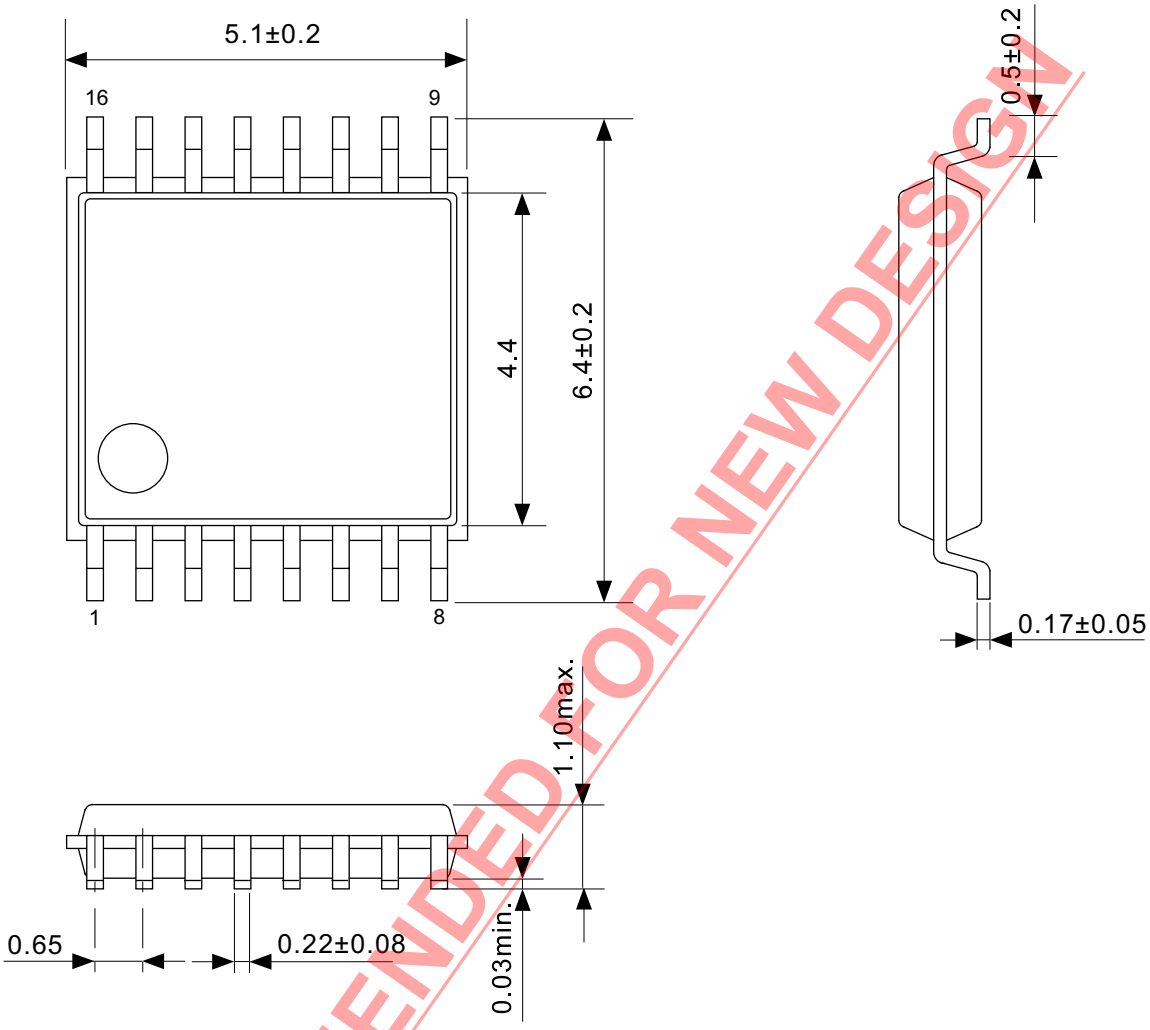
5. 14 I_{CTL} vs. V_{CTL}



Remark n = 1 to 5

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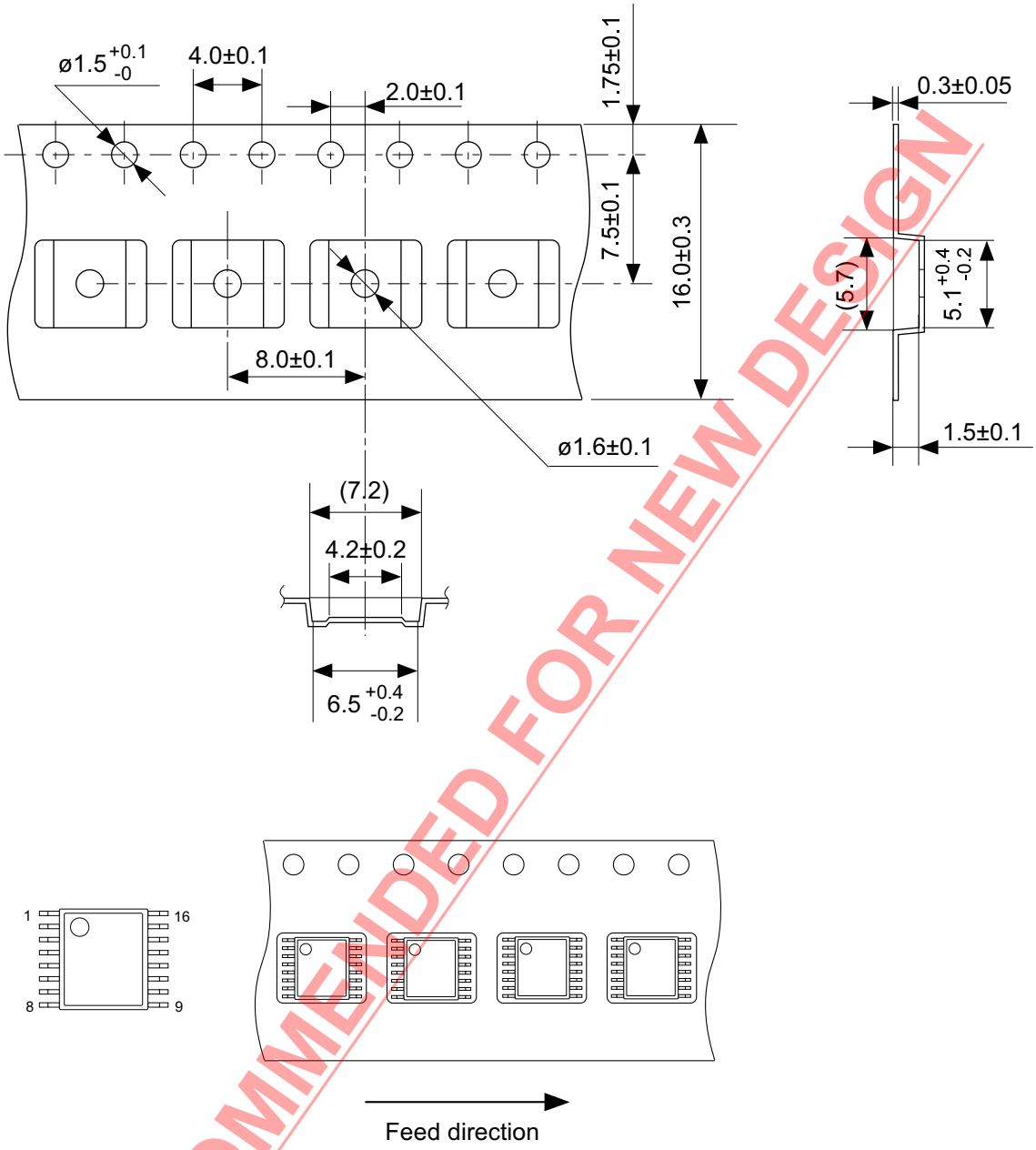
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No. FT016-A-P-SD-1.2

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No.	FT016-A-P-SD-1.2
ANGLE	
UNIT	mm

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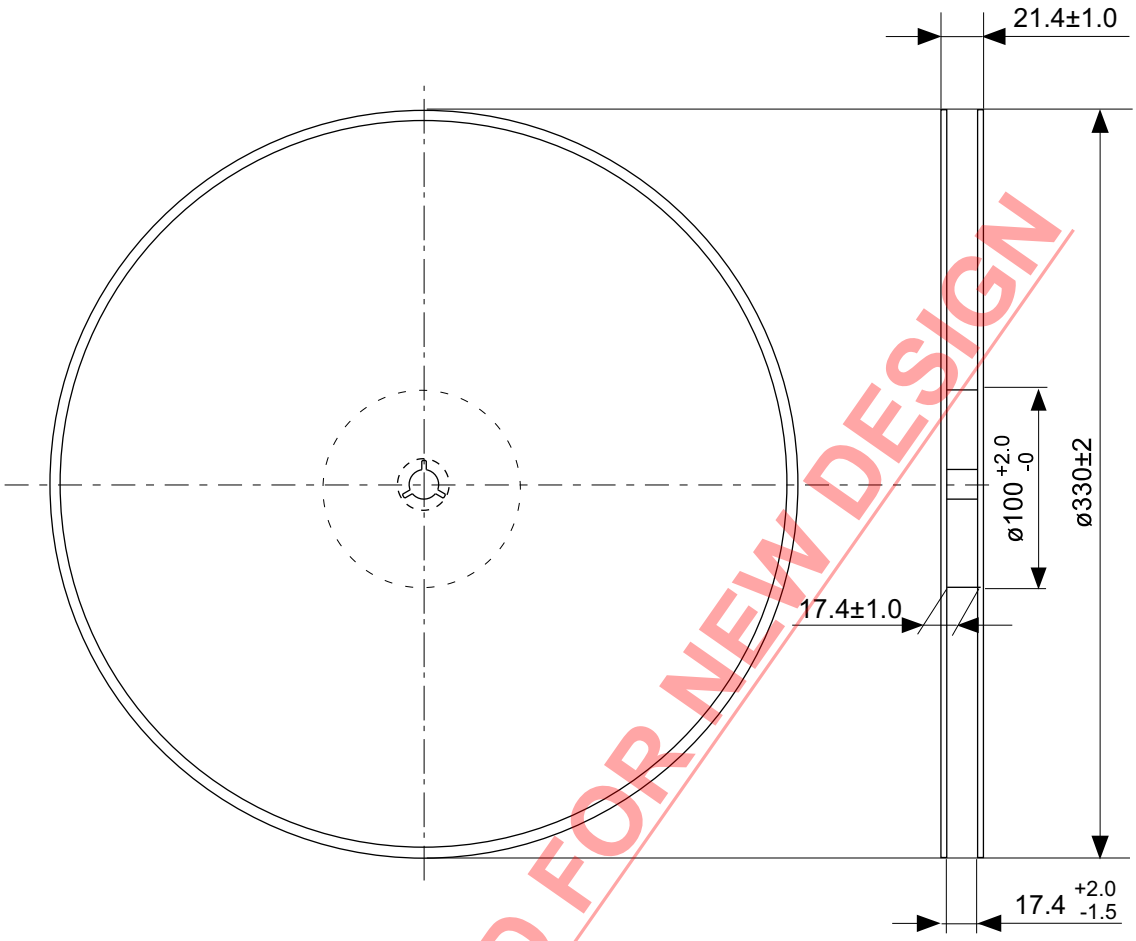


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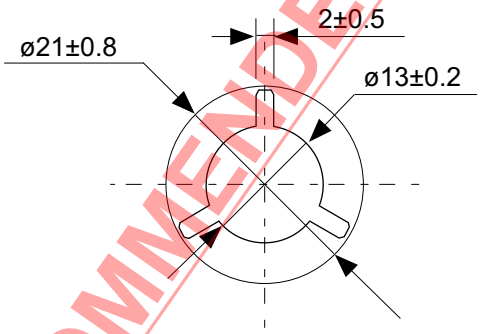
No. FT016-A-C-SD-1.1

TITLE	TSSOP16-A-Carrier Tape
No.	FT016-A-C-SD-1.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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Enlarged drawing in the central part



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No. FT016-A-R-S1-1.0

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-S1-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
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