

DUAL FREQUENCY VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR (VCXO) 10 TO 810 MHz

Features

- Available with any-rate output frequencies from 10 to 810 MHz
- Two selectable output frequencies
- 3rd generation DSPLL[®] with superior jitter performance
- Internal fixed fundamental mode crystal frequency ensures high reliability and low aging
- Available CMOS, LVPECL, LVDS, and CML outputs
- 3.3, 2.5, and 1.8 V supply options
- Industry-standard 5 x 7 mm package and pinout
- Pb-free/RoHS-compliant
- -40 to +85 °C operating range

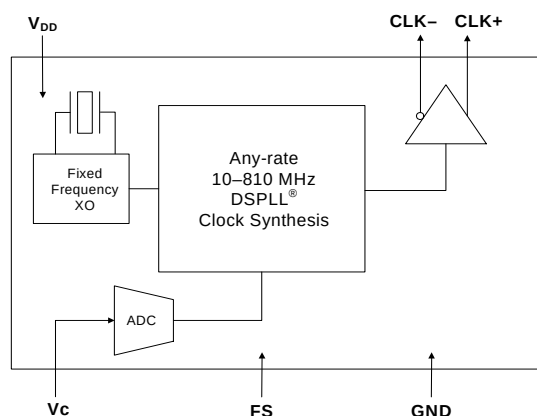
Applications

- SONET/SDH (OC-3/12/48)
- Networking
- SD/HD SDI/3G SDI video
- FTTx
- Clock recovery and jitter cleanup PLLs
- FPGA/ASIC clock generation

Description

The Si596 dual-frequency VCXO utilizes Silicon Laboratories' advanced DSPLL[®] circuitry to provide a low-jitter clock at high frequencies. The Si596 is available with any-rate output frequency from 10 to 810 MHz. Unlike traditional VCXOs, where a different crystal is required for each output frequency, the Si596 uses one fixed crystal to provide a wide range of output frequencies. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides supply noise rejection, simplifying the task of generating low-jitter clocks in noisy environments. The Si596 IC-based VCXO is factory-configurable for a wide variety of user specifications including frequency, supply voltage, output format, tuning slope, and absolute pull range (APR). Specific configurations are factory programmed at time of shipment, thereby eliminating the long lead times associated with custom oscillators.

Functional Block Diagram



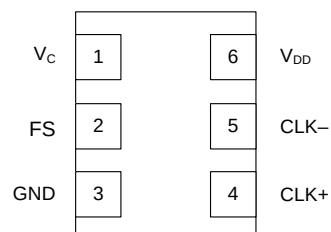
Ordering Information:

See page 7.

Pin Assignments:

See page 6.

(Top View)



1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage ¹	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	
		1.8 V option	1.71	1.8	1.89	
Supply Current	I_{DD}	LVPECL	—	120	135	mA
		CML	—	110	120	
		LVDS	—	100	110	
		CMOS	—	90	100	
Frequency Select (FS) ²		V_{IH}	$0.75 \times V_{DD}$	—	—	V
		V_{IL}	—	—	0.5	
Operating Temperature Range	T_A		−40	—	85	°C
Notes: 1. Selectable parameter specified by part number. See 3. "Ordering Information" on page 7 for further details. 2. FS pin includes an internal 17 kΩ pullup resistor to V_{DD}. When the FS is left floating, the pullup causes FS = 1 = second frequency selected.						

Table 2. V_C Control Voltage Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Control Voltage Tuning Slope ^{1,2,3}	K_V	10 to 90% of V_{DD}	—	45 95 125 185 380	—	ppm/V
Control Voltage Linearity ⁴	L_{VC}	BSL	−5	±1	+5	%
		Incremental	−10	±5	+10	
Modulation Bandwidth	BW		9.3	10.0	10.7	kHz
V_C Input Impedance	Z_{VC}		500	—	—	k Ω
V_C Input Capacitance	C_{VC}		—	50	—	pF
Nominal Control Voltage	V_{CNOM}	@ f_O	—	$V_{DD}/2$	—	V
Control Voltage Tuning Range	V_C		0		V_{DD}	V
Notes: 1. Positive slope; selectable option by part number. See 3. "Ordering Information" on page 7. 2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information. 3. K_V variation is ±10% of typical values. 4. BSL determined from deviation from best straight line fit with V_C ranging from 10 to 90% of V_{DD}. Incremental slope determined with V_C ranging from 10 to 90% of V_{DD}.						

Table 3. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Frequency ^{1,2,3}	f_O	LVDS/CML/LVPECL	10	—	810	MHz
		CMOS	10	—	160	
Temperature Stability ^{1,4}		$T_A = -40$ to $+85$ °C	-20 -50	— —	+20 +50	ppm
Absolute Pull Range ^{1,4}	APR		±10	—	±370	ppm
Power up Time ⁵	t_{OSC}		—	—	10	ms
Settling Time After FS Change	T_{FRQ}		—	—	10	ms

Notes:

1. See Section 3. "Ordering Information" on page 7 for further details.
2. Specified at time of order by part number.
3. Nominal output frequency set by $V_{CNOM} = V_{DD}/2$.
4. Selectable parameter specified by part number.
5. Time from power up or tristate mode to f_O .

Table 4. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option ¹	V_O	mid-level	$V_{DD} - 1.42$	—	$V_{DD} - 1.25$	V
	V_{OD}	swing (diff)	1.1	—	1.9	V_{PP}
	V_{SE}	swing (single-ended)	0.55	—	0.95	V_{PP}
LVDS Output Option ²	V_O	mid-level	1.125	1.20	1.275	V
	V_{OD}	swing (diff)	0.5	0.7	0.9	V_{PP}
CML Output Option ²	V_O	2.5/3.3 V option mid-level	—	$V_{DD} - 1.30$	—	V
		1.8 V option mid-level	—	$V_{DD} - 0.36$	—	
	V_{OD}	2.5/3.3 V option swing (diff)	1.10	1.50	1.90	V_{PP}
		1.8 V option swing (diff)	0.35	0.425	0.50	
CMOS Output Option ³	V_{OH}		$0.8 \times V_{DD}$	—	V_{DD}	V
	V_{OL}		—	—	0.4	
Rise/Fall time (20/80%)	t_R, t_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with $C_L = 15$ pF	—	2	—	ns
Symmetry (duty cycle)	SYM	LVPECL: $V_{DD} - 1.3$ V (diff) LVDS: 1.25 V (diff) CMOS: $V_{DD}/2$	45	—	55	%

Notes:

1. 50Ω to $V_{DD} - 2.0$ V.
2. $R_{term} = 100 \Omega$ (differential).
3. $C_L = 15$ pF. Sinking or sourcing 12 mA for $V_{DD} = 3.3$ V, 6 mA for $V_{DD} = 2.5$ V, 3 mA for $V_{DD} = 1.8$ V.

Table 5. CLK± Output Phase Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS) ^{1,2} for F _{OUT} of 50 MHz ≤ F _{OUT} 810 MHz	ϕ _J	Kv = 45 ppm/V 12 kHz to 20 MHz	—	0.5	—	ps
		Kv = 95 ppm/V 12 kHz to 20 MHz	—	0.5	—	
		Kv = 125 ppm/V 12 kHz to 20 MHz	—	0.5	—	
		Kv = 185 ppm/V 12 kHz to 20 MHz	—	0.5	—	
		Kv = 380 ppm/V 12 kHz to 20 MHz	—	0.7	—	

Notes:

1. Refer to AN256 for further information.

2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application’s minimum APR requirements. See “AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)” for more information.

Table 6. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	J _{PER}	RMS	—	3	—	ps
		Peak-to-Peak	—	35	—	
*Note: Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information.						

Table 7. CLK± Output Phase Noise (Typical)

Offset Frequency	74.25 MHz 185 ppm/V LVPECL	148.5 MHz 185 ppm/V LVPECL	155.52 MHz 95 ppm/V LVPECL	Units
100 Hz	−77	−68	−77	dBc/Hz
1 kHz	−101	−95	−101	
10 kHz	−121	−116	−119	
100 kHz	−134	−128	−127	
1 MHz	−149	−144	−144	
10 MHz	−151	−147	−147	
20 MHz	−150	−148	−148	

Table 8. Environmental Compliance and Package Information

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Contact Pads	Gold over Nickel

Table 9. Thermal Characteristics(Typical values $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	84.6	—	$^{\circ}\text{C/W}$
Thermal Resistance Junction to Case	θ_{JC}	Still Air	—	38.8	—	$^{\circ}\text{C/W}$
Ambient Temperature	T_A		-40	—	85	$^{\circ}\text{C}$
Junction Temperature	T_J		—	—	125	$^{\circ}\text{C}$

Table 10. Absolute Maximum Ratings¹

Parameter	Symbol	Rating	Units
Maximum Operating Temperature	T_{AMAX}	85	$^{\circ}\text{C}$
Supply Voltage	V_{DD}	-0.5 to +3.8	V
Input Voltage	V_I	-0.5 to $V_{DD} + 0.3$	
Storage Temperature	T_S	-55 to +125	$^{\circ}\text{C}$
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2500	V
Soldering Temperature (Pb-free profile) ²	T_{PEAK}	260	$^{\circ}\text{C}$
Soldering Temperature Time @ T_{PEAK} (Pb-free profile) ²	t_P	20–40	seconds

Notes:

- Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
- The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download from www.silabs.com/VCXO for further information, including soldering profiles.

2. Pin Descriptions

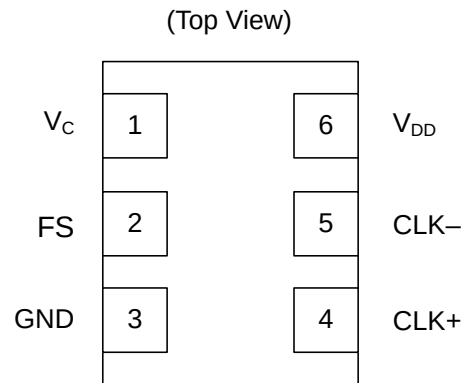


Table 11. Si596 Pin Descriptions

Pin	Name	Type	Function
1	V _C	Analog Input	Control Voltage
2	FS*	Input	Frequency Select: 0 = first frequency selected 1 = second frequency selected
3	GND	Ground	Electrical and Case Ground
4	CLK+	Output	Oscillator Output
5	CLK– (N/C for CMOS)	Output	Complementary Output (N/C for CMOS, do not make external connection)
6	V _{DD}	Power	Power Supply Voltage
*Note: FS pin includes a 17 kΩ resistor to V _{DD} . When the FS is left floating, the pullup causes FS = 1 = second frequency selected. See 3. "Ordering Information" on page 7 for details on frequency select ordering options.			

3. Ordering Information

The Si596 supports a variety of options including frequency, temperature stability, tuning slope, output format, and V_{DD} . Specific device configurations are programmed into the Si596 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. Refer to www.silabs.com/VCXOPartNumber to access this tool and for further ordering instructions. The Si596 VCXO series is supplied in an industry-standard, RoHS compliant, lead-free, 6-pad, 5 x 7 mm package. Tape and reel packaging is an ordering option.

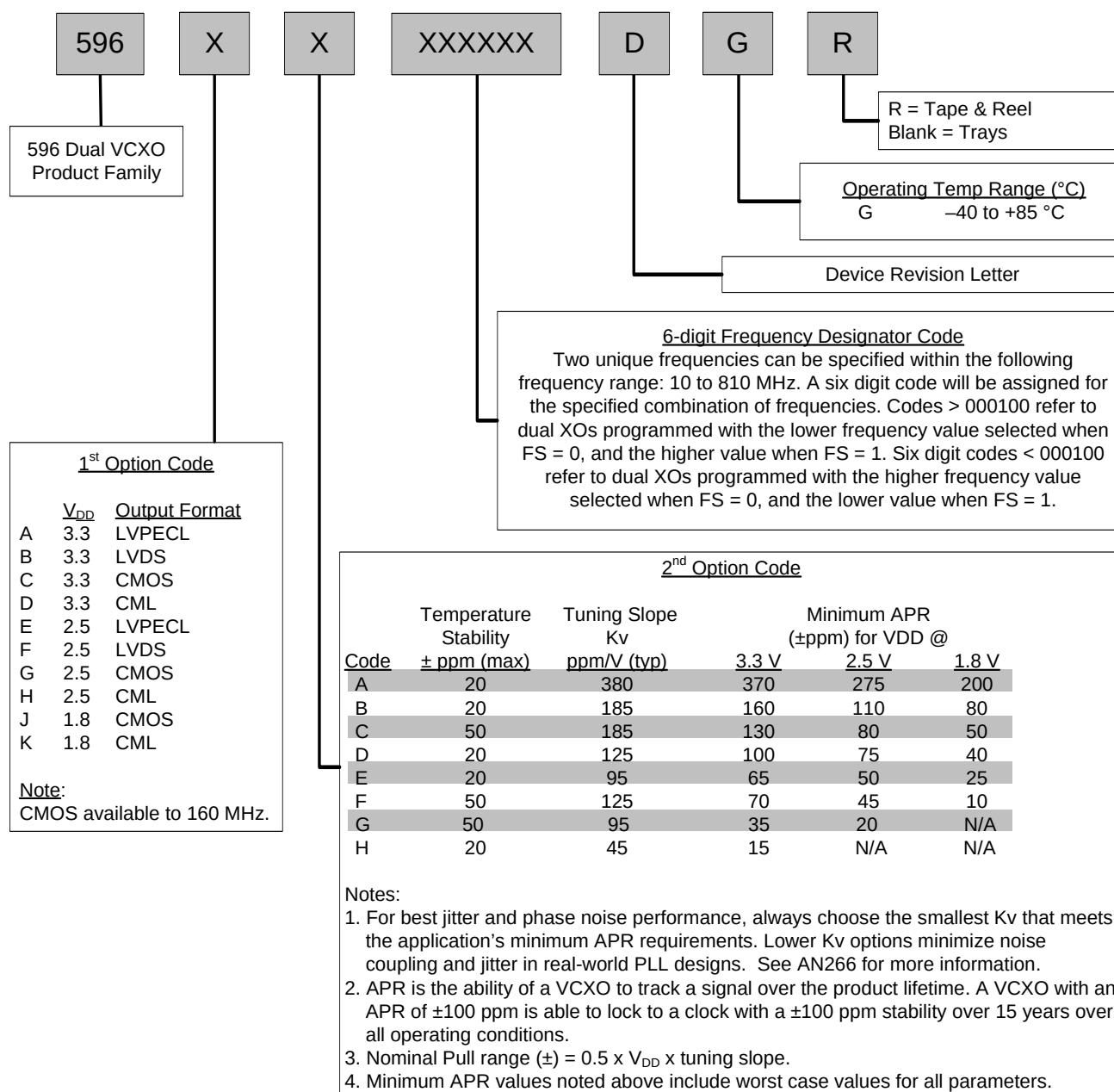


Figure 1. Part Number Convention

4. Outline Diagram and Suggested Pad Layout

Figure 2 illustrates the package details for the Si596. Table 12 lists the values for the dimensions shown in the illustration.

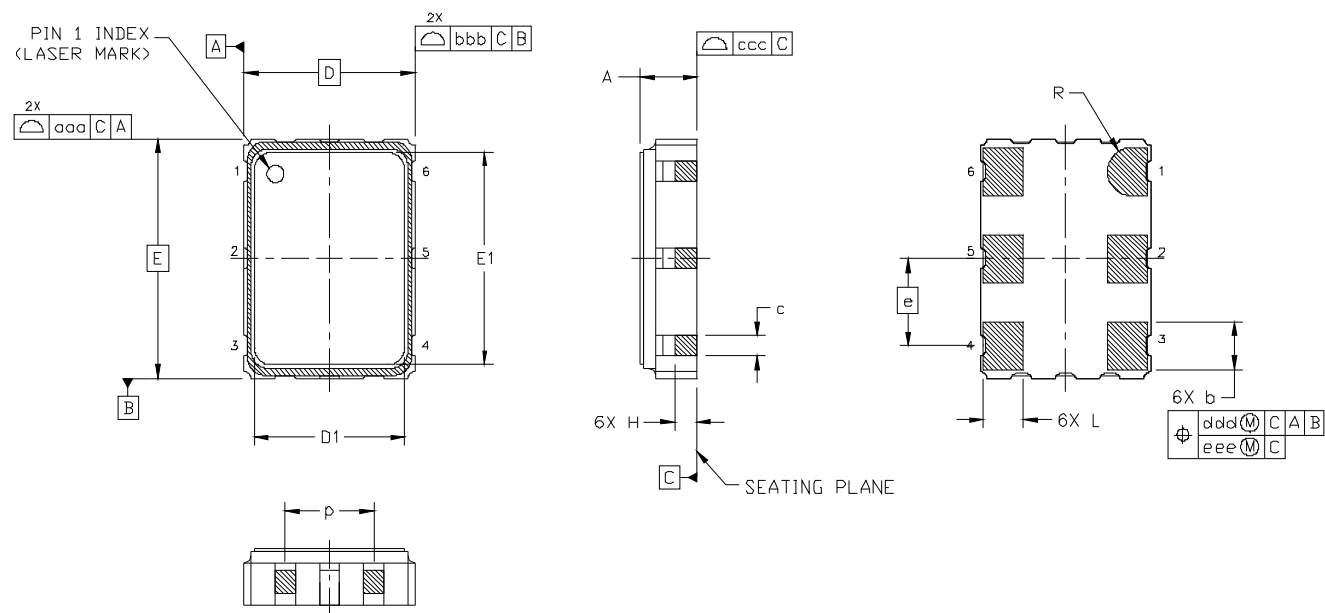


Figure 2. Si596 Outline Diagram

Table 12. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
c	0.50	0.60	0.70
D	5.00 BSC		
D1	4.30	4.40	4.50
e	2.54 BSC.		
E	7.00 BSC.		
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
p	1.80	—	2.60
R	0.70 REF		
aaa	0.15		
bbb	0.15		
ccc	0.10		
ddd	0.10		
eee	0.50		

5. Si5xx Mark Specification

Figure 3 illustrates the mark specification for the Si596. Table 13 lists the line information.

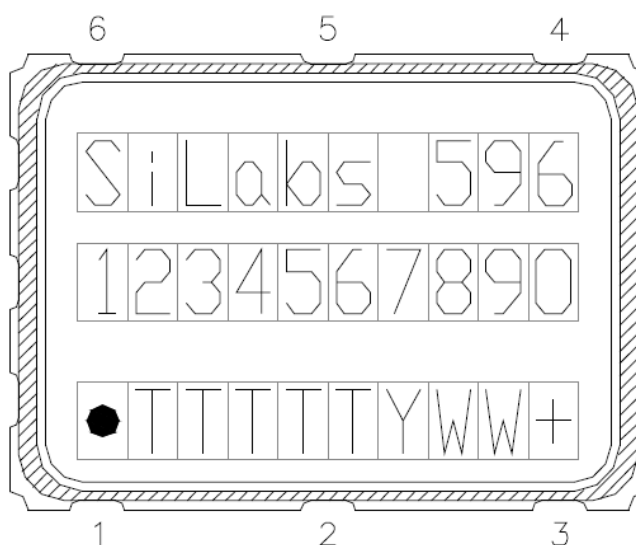


Figure 3. Mark Specification

Table 13. Si596 Top Mark Description

Line	Position	Description
1	1–10	“SiLabs”+ Part Family Number, 596 (First 3 characters in part number)
2	1–10	Si596: Option1+Option2+Freq(6)+Temp
3	Trace Code	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2009 = 9)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	“+” to indicate Pb-Free and RoHS-compliant

6. 6-Pin PCB Land Pattern

Figure 4 illustrates the 6-pin PCB land pattern for the Si596. Table 14 lists the values for the dimensions shown in the illustration.

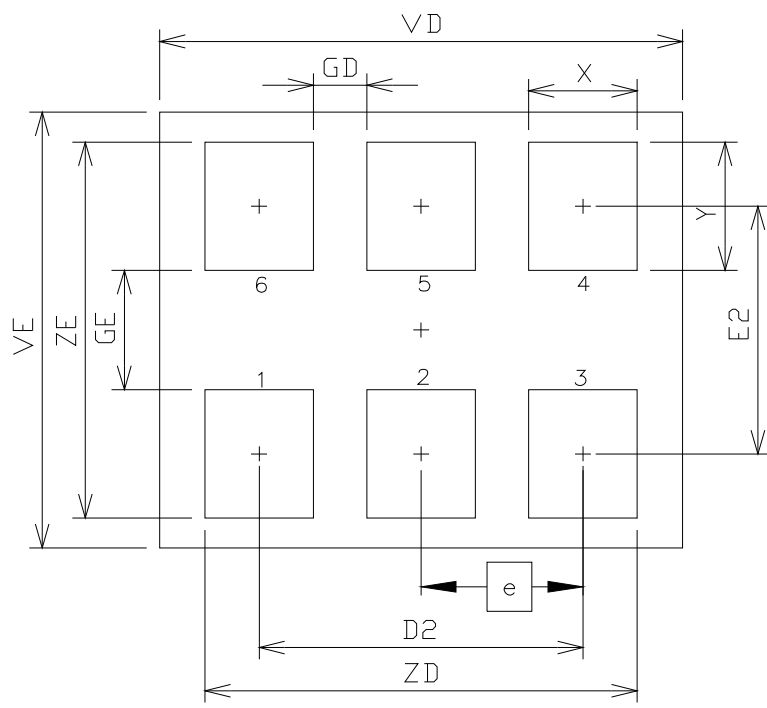


Figure 4. Si596 PCB Land Pattern

Table 14. PCB Land Pattern Dimensions (mm)

Dimension	Min	Max
D2	5.08 REF	
e	2.54 BSC	
E2	4.15 REF	
GD	0.84	—
GE	2.00	—
VD	8.20 REF	
VE	7.30 REF	
X	1.70 TYP	
Y	2.15 REF	
ZD	—	6.78
ZE	—	6.30

Notes:

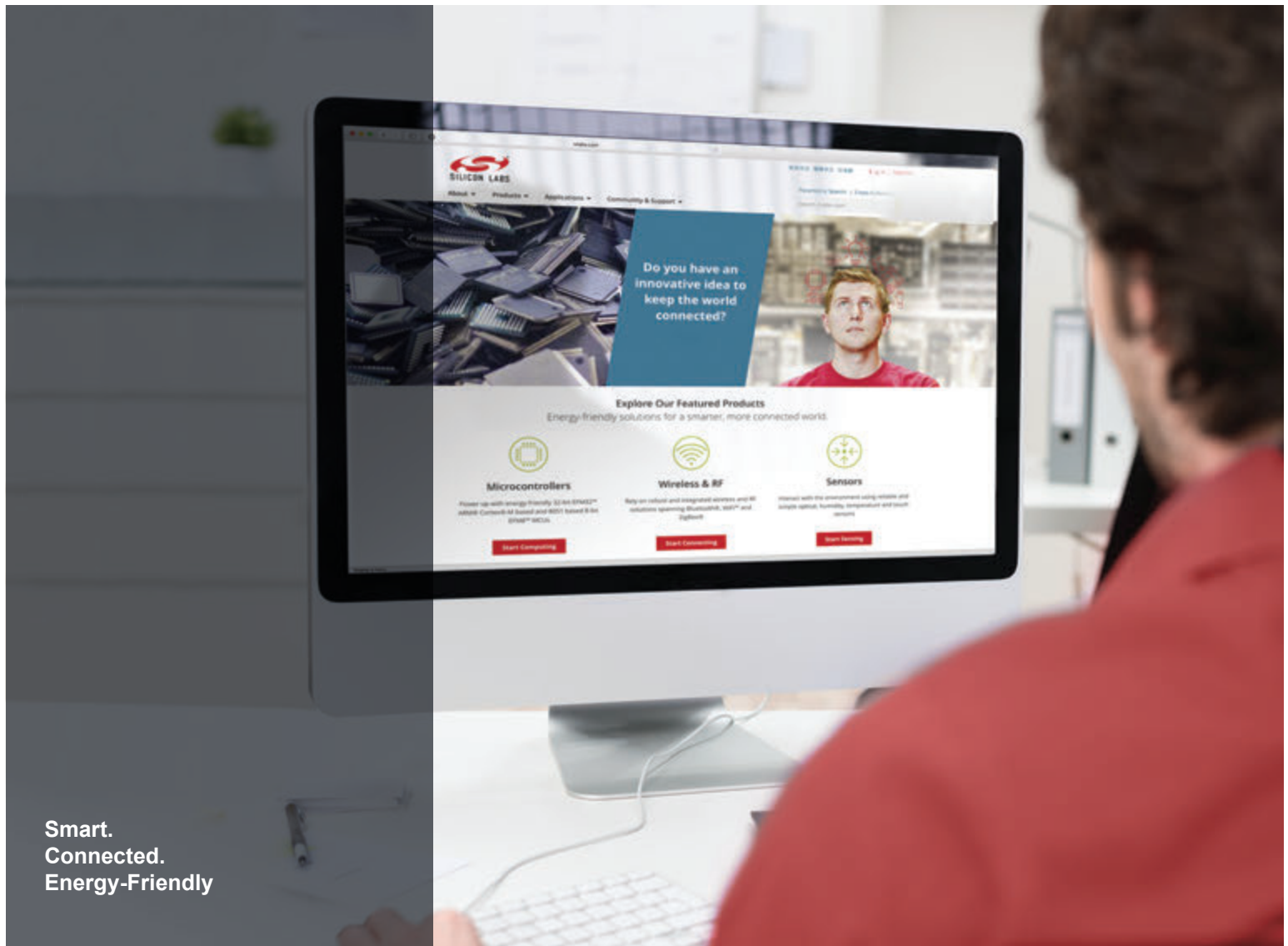
1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design based on IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

DOCUMENT CHANGE LIST

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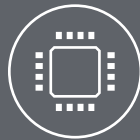
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