NCT6102D / NCT6106D

Nuvoton LPC I/O

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1. GENERAL DESCRIPTION

The NCT6102D / NCT6106D is a member of Nuvoton's Super I/O product line. The NCT6102D / NCT6106D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the NCT6102D / NCT6106D adopts the Current Mode (dual current source) and thermistor sensor approach. The NCT6102D / NCT6106D also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ IV, which makes the system more stable and user-friendly.

The NCT6102D / NCT6106D supports four – 360K, 720K, 1.2M, 1.44M, or 2.88M – disk drive types and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1 Mb/s, and 2 Mb/s. The disk drive adapter supports the functions of floppy disk drive controller (compatible with the industry standard 82077/ 765), data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. Such a wide range of functions integrated into one NCT6102D / NCT6106D greatly reduce the number of required components to interface with floppy disk drives.

The NCT6102D supports 2 high-speed serial communication port (UART), and the NCT6106D supports 6 high-speed serial communication port (UART). Each UART includes a 128-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The NCT6102D / NCT6106D supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP). The NCT6102D / NCT6106D supports keyboard and mouse interface which is 8042-based keyboard controller.

The NCT6102D / NCT6106D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The NCT6102D / NCT6106D supports the Intel® PECI (Platform Environment Control Interface), AMD® SB-TSI interface, and Intel® Deep Sleep Well glue logic which helps customers to reduce the external circuits needed while using Deep Sleep Well function.

The NCT6102D / NCT6106D supports to decode port 80 diagnostic messages on the LPC bus. This could help on system power on debugging. It also supports two-color LED control to indicate system power states, Consumer IR function for remote control purpose, and also Advanced Power Saving function to further reduce the power consumption while the system is at S5 state.

The configuration registers inside the NCT6102D / NCT6106D support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows, making the allocation of the system resources more efficient than ever.

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2. FEATURES

General

Meet LPC Spec. 1.1
Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
Integrated hardware monitor functions
Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
Programmable configuration settings
Single 24-MHz or 48-MHz clock input
Support selective pins of 5 V tolerance

FDC

Variable write pre-compensation with track-selection capability
Support vertical recording format
DMA-enable logic
16-byte data FIFO
Support floppy disk drives and tape drives
Detect all overrun and underrun conditions
Built-in address mark detection circuit to simplify the read electronics
FDD anti-virus functions with software write protect and FDD-write enable signal (write data signal forced to be inactive)
Support 3.5-inch or 5.25-inch floppy disk drives
Compatible with industry standard 82077
360K / 720K / 1.2M / 1.44M / 2.88M formats
250K, 300K, 500K, 1M, 2M bps data transfer rate
Support 3-mode FDD and its Windows driver

UART

NCT6102D - 2 high-speed, 16550-compatible UART with 128-byte send / receive FIFO
NCT6106D - 6 high-speed, 16550-compatible UART with 128-byte send / receive FIFO
Support RS485
--- Supports auto flow control
Fully programmable serial-interface characteristics:
--- 5, 6, 7 or 8-bit characters
--- Even, odd or no parity bit generation / detection
--- 1, 1.5 or 2 stop-bit generation
Internal diagnostic capabilities:
--- Loop-back controls for communications link fault isolation
--- Break, parity, overrun, framing error simulation
Programmable baud rate generator allows division of clock source by any value from 1 to $(2^{16}-1)$
Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5 M bps.

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Parallel Port

- Compatible with IBM® parallel port
- Support PS/2-compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection

Keyboard Controller

- 8042-based keyboard controller
- Asynchronous access to two data registers and one status register
- Software-compatible with 8042
- Support PS/2 mouse
- Support Port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 12MHz operating frequency

Hardware Monitor Functions

- Smart Fan control system
- Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in the Thermal Cruise™ mode
- Support Current Mode (dual current source) temperature sensing method
- Eight voltage inputs (CPUVCORE, VIN[0..2], 3VCC, AVCC, 3VSB and VBAT)
- Three fan-speed monitoring inputs
- Three fan-speed controls
- Dual mode for fan control (PWM and DC) for SYSFANOUT, CPUFANOUT and AUXFANOUT
- Built-in case open detection circuit
- Programmable hysteresis and setting points for all monitored items
- Issue SMI#, OVT# (Over-temperature) to activate system protection
- Nuvoton Health Manager support
- Provide I^2C master / slave interface to read / write registers

CIR and IR (Infrared)

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support Consumer IR, including CIRTX, CIRRX, CIRRXWB

General Purpose I/O Ports

- GPIO0 ~ GPIO7 programmable general purpose I/O ports
- Two access channels, indirect (via 2E/2F or 4E/4F) and direct (Base Address) access.

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ACPI Configuration

Support Glue Logic functions
Support general purpose Watch Dog Timer functions

OnNow Functions

Keyboard Wake-Up by programmable keys
Mouse Wake-Up by programmable buttons
OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

PECI Interface

Support PECI 1.1, 2.0 and 3.0 specification
Support 2 CPU addresses and 2 domains per CPU address

AMD SB-TSI Interface

Support AMD® SB-TSI specification

SMBus Interface

Support SMBus Slave interface to report Hardware Monitor device data
Support SMBus Master interface to get thermal data from PCH
Support SMBus Master interface to get thermal data from MXM module

Power Measurement

Support Power Consumption measurement
Fading LED driver control for power status and diagnostic indications

Advanced Power Saving

Advanced Sleep State Control to save motherboard Stand-by power consumption

Operation voltage

3.3 voltage

Package

128-pin LQFP
Green

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3. BLOCK DIAGRAM

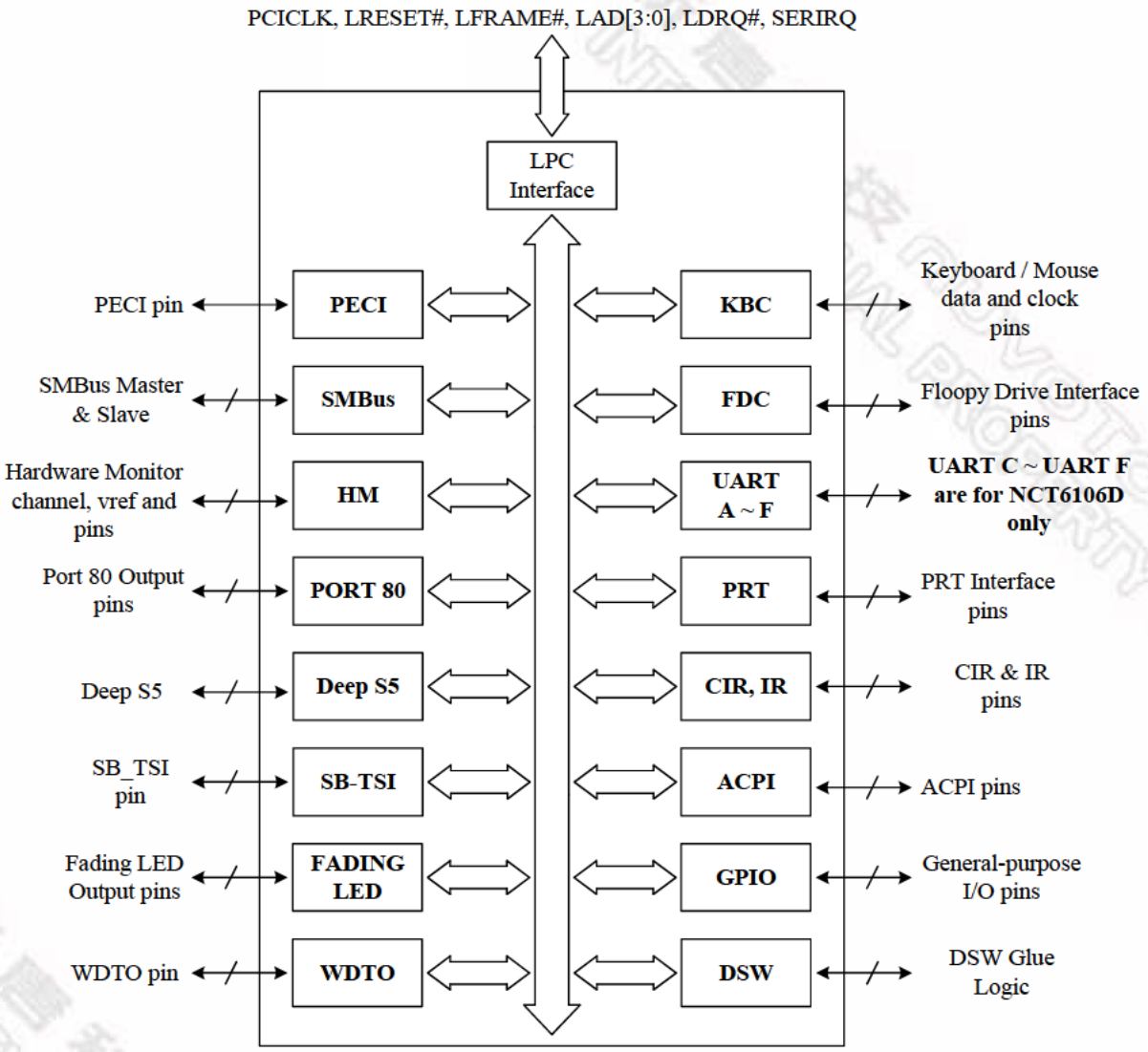

Figure 3-1 NCT6102D / NCT6106D Block Diagram

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4. PIN LAYOUT

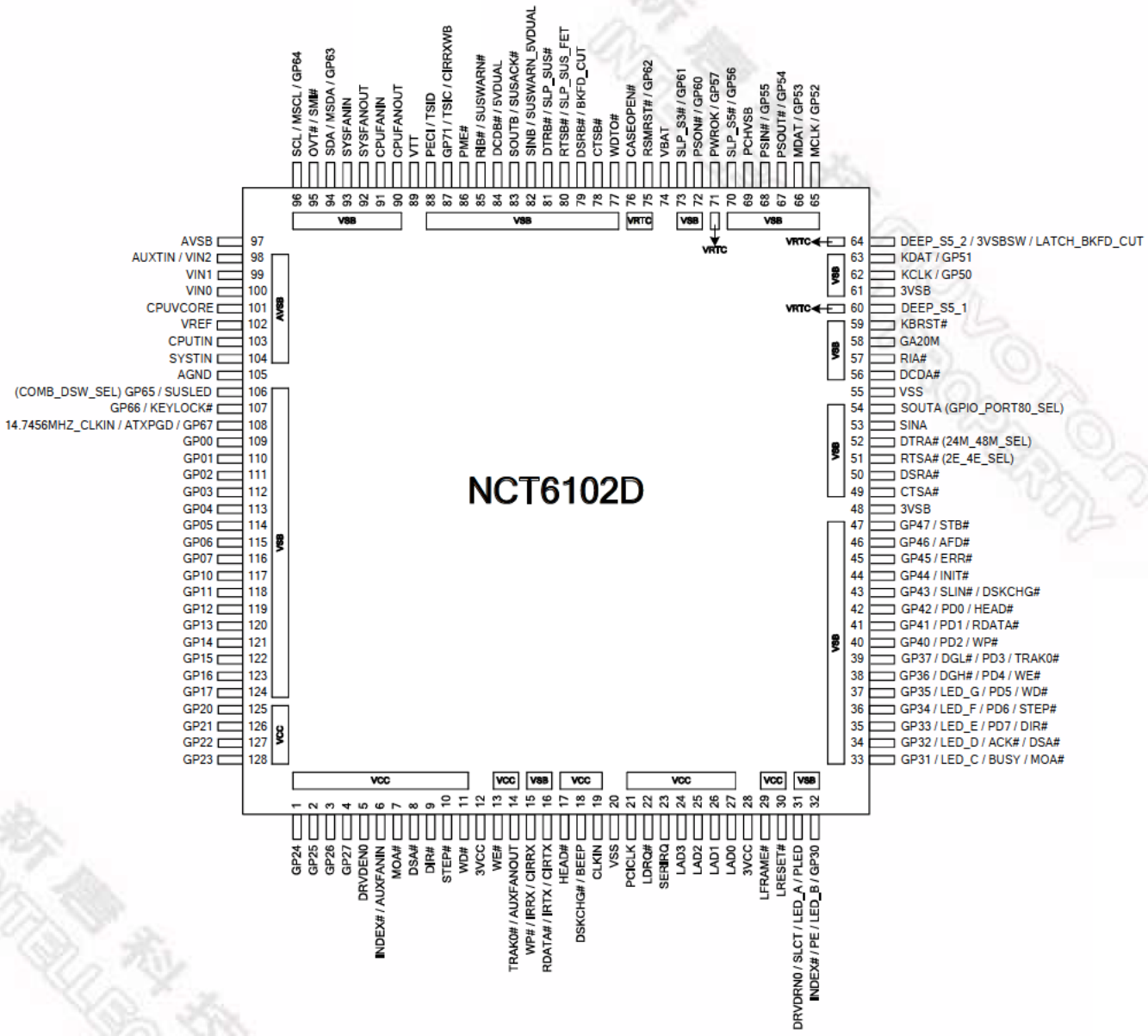

Figure 4-1 NCT6102D Pin Layout

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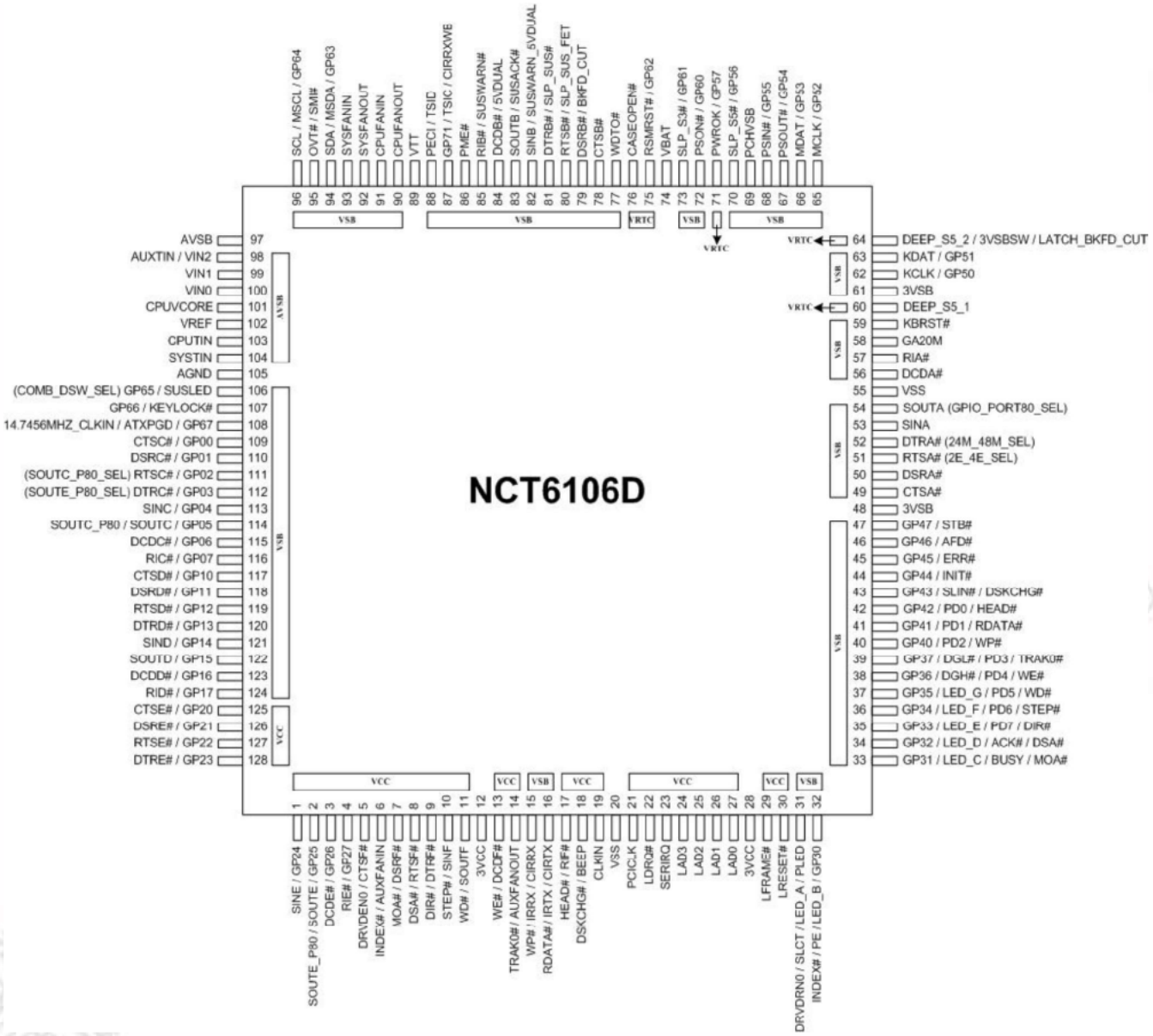

Figure 4-2 NCT6106D Pin Layout

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5. PIN DESCRIPTION

Note: Please refer to 24.2 DC CHARACTERISTICS for details.

AOUT	- Analog output pin
AIN	- Analog input pin
IN_{tp3}	- 3.3V TTL-level input pin
IN_{tsp3}	- 3.3V TTL-level, Schmitt-trigger input pin
IN_{gp5}	- 5V GTL-level input pin
IN_{tp5}	- 5V TTL-level input pin
IN_{tscup5}	- 5V TTL-level, Schmitt-trigger, input buffer with controllable pull-up
IN_{tsp5}	- 5V TTL-level, Schmitt-trigger input pin
IN_{tdp5}	- 5V TTL-level input pin with internal pull-down resistor
IN_{tup5}	- 5V TTL-level input pin with internal pull-up resistor
O_8	- output pin with 8-mA source-sink capability
OD_8	- open-drain output pin with 8-mA sink capability
O_{12}	- output pin with 12-mA source-sink capability
OD_{12}	- open-drain output pin with 12-mA sink capability
O_{24}	- output pin with 24-mA source-sink capability
OD_{24}	- open-drain output pin with 24-mA sink capability
O_{48}	- output pin with 48-mA source-sink capability
OD_{48}	- open-drain output pin with 48-mA sink capability
I/O_{v3}	- Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O_{v4}	- Bi-direction pin with source capability of 6 mA
O_{12cu}	- output pin 12-mA source-sink capability with controllable pull-up
OD_{12cu}	- open-drain 12-mA sink capability output pin with controllable pull-up

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5.1 LPC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
19	CLKIN	I	IN_{tp5}	VCC	System clock input, either 24MHz or 48MHz. The actual frequency must be specified by 24M_48M_SEL strapping.
86	PME#	O	OD_{12}	VSB	Generated PME event.
21	PCICLK	I	IN_{tp3}	VCC	PCI-clock 33-MHz input.
22	LDRQ#	O	O_{12}	VCC	Encoded DMA Request signal.
23	SERIRQ	I/O	IN_{tp3} O_{12} OD_{12}	VCC	Serialized IRQ input / output.
24-27	LAD[3:0]	I/O	IN_{tp3} OD_{12}	VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
29	LFRAME#	I	IN_{tp3}	VCC	Indicates the start of a new cycle or the termination of a broken cycle.
30	LRESET#	I	IN_{tp3}	VCC	Reset signal. It can be connected to the PCIRST# signal on the host.

5.2 FDC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
5	DRVDEN0	O	OD_{24}	VCC	Drive Density Select bit 0.
31	DRVDEN0	O	OD_{12}	VSB	Drive Density Select bit 0.
6	INDEX#	I	IN_{tsp5}	VCC	This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the beginning of a track marked by an index hole. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
32	INDEX#	I	IN_{tsp5}	VSB	This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the beginning of a track marked by an index hole. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
7	MOA#	O	OD_{24}	VCC	Motor A On. When set to 0, this pin activates disk drive A. This is an open-drain output.
33	MOA#	O	OD_{12}	VSB	Motor A On. When set to 0, this pin activates disk drive A. This is an open-drain output.
8	DSA#	O	OD_{24}	VCC	Drive Select A. When set to 0, this pin activates disk drive A. This is an open-drain output.

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
34	DSA#	O	OD_{12}	VSB	Drive Select A. When set to 0, this pin activates disk drive A. This is an open-drain output.
9	DIR#	O	OD_{24}	VCC	Direction of the head step motor. An open-drain output. Logic 1 = outward motion Logic 0 = inward motion
35	DIR#	O	OD_{12}	VSB	Direction of the head step motor. An open-drain output. Logic 1 = outward motion Logic 0 = inward motion
10	STEP#	O	OD_{24}	VCC	Step output pulses. This active-low open-drain output produces a pulse to move the head to another track.
36	STEP#	O	OD_{12}	VSB	Step output pulses. This active-low open-drain output produces a pulse to move the head to another track.
11	WD#	O	OD_{24}	VCC	Write data. This logic-low open-drain writes pre-compensation serial data to the selected FDD. An open-drain output.
37	WD#	O	OD_{12}	VSB	Write data. This logic-low open-drain writes pre-compensation serial data to the selected FDD. An open-drain output.
13	WE#	O	OD_{24}	VCC	Write enable. An open-drain output.
38	WE#	O	OD_{24}	VSB	Write enable. An open-drain output.
14	TRAK0#	I	IN_{tsp5}	VCC	Track 0. This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the outermost track. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
39	TRAK0#	I	IN_{tsp5}	VSB	Track 0. This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the outermost track. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
15	WP#	I	IN_{tsp5}	VCC	Write protected. This active-low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
40	WP#	I	IN_{tsp5}	VSB	Write protected. This active-low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
16	RDATA#	I	IN_{tsp5}	VCC	The read-data input signal from the FDD. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
41	RDATA#	I	IN_{tsp5}	VSB	The read-data input signal from the FDD. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
17	HEAD#	O	OD_{24}	VCC	Head selection. This open-rain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
42	HEAD#	O	OD_{12}	VSB	Head selection. This open-rain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
18	DSKCHG#	I	IN_{tsp5}	VCC	Diskette change. This signal is active-low at power-on and whenever the diskette is removed. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
43	DSKCHG#	I	IN_{tsp5}	VSB	Diskette change. This signal is active-low at power-on and whenever the diskette is removed. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.

5.3 Multi-Mode Parallel Port

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
31	SLCT	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
32	PE	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input on this pin indicates that the printer has detected the end of the paper. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
33	BUSY	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input indicates that the printer is not ready to receive data. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
34	ACK#	I	IN_{tsp5}	VSB	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data. See the descriptions of the parallel port for the definition of this pin in ECP and EPP modes.
45	ERR#	I	IN_{tsp5}	VSB	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error condition. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
43	SLIN#	O	O_{12}	VSB	PRINTER MODE: SLIN# Output line for detection of printer selection. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
44	INIT#	O	O_{12}	VSB	PRINTER MODE: INIT# Output line for the printer initialization. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
46	AFD#	O	O_{12}	VSB	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
47	STB#	O	O_{12}	VSB	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
42	PD0	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD0 Parallel port data bus bit 0. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
41	PD1	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD1 Parallel port data bus bit 1. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
40	PD2	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD2 Parallel port data bus bit 2. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
39	PD3	I/O	IN_{tsp5} O_{24}	VSB	PRINTER MODE: PD3 Parallel port data bus bit 3. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
38	PD4	I/O	IN_{tsp5} O_{24}	VSB	PRINTER MODE: PD4 Parallel port data bus bit 4. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
37	PD5	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD5 Parallel port data bus bit 5. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
36	PD6	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD6 Parallel port data bus bit 6. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
35	PD7	I/O	IN_{tsp5} O_{24}	VSB	PRINTER MODE: PD7 Parallel port data bus bit 7. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

5.4 Serial Port Interface (UART C ~ UART F are for NCT6106D only)

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
57	RIA#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
56	DCDA#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
54	SOUTA	O	O_{12}	VSB	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
53	SINA	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
52	DTRA#	O	O_{12}	VSB	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
51	RTSA#	O	O_{12}	VSB	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
50	DSRA#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
49	CTSA#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
85	RIB#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
84	DCDB#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
83	SOUTB	O	O_{12}	VSB	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
82	SINB	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
81	DTRB#	O	O_{12}	VSB	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
80	RTSB#	O	O_{12}	VSB	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
79	DSRB#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
78	CTSB#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
116	RIC#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
115	DCDC#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
114	SOUTC	O	O_{12}	VSB	UART C Serial Output. This pin is used to transmit serial data out to the communication link.
114	SOUTC_P80	O	O_{12}	VSB	PORT80 to UART Serial Output. This pin is used to transmit serial data out to the communication link.
113	SINC	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
112	DTRC#	O	O_{12}	VSB	UART C Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
111	RTSC#	O	O_{12}	VSB	UART C Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
110	DSRC#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
109	CTSC#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
124	RID#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
123	DCDD#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
122	SOUTD	O	O_{12}	VSB	UART D Serial Output. This pin is used to transmit serial data out to the communication link.
121	SIND	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
120	DTRD#	O	O_{12}	VSB	UART D Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
119	RTSD#	O	O_{12}	VSB	UART D Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
118	DSRD#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
117	CTSD#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
4	RIE#	I	IN_{tp5}	VCC	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
3	DCDE#	I	IN_{tp5}	VCC	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
2	SOUTE	O	O_{12}	VCC	UART E Serial Output. This pin is used to transmit serial data out to the communication link.
2	SOUTE_P80	O	O_{12}	VCC	PORT80 to UART Serial Output. This pin is used to transmit serial data out to the communication link.
1	SINE	I	IN_{tp5}	VCC	Serial Input. This pin is used to receive serial data through the communication link.
128	DTRE#	O	O_{12}	VCC	UART E Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
127	RTSE#	O	O_{12}	VCC	UART E Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
126	DSRE#	I	IN_{tp5}	VCC	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
125	CTSE#	I	IN_{tp5}	VCC	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
17	RIF#	I	IN_{tp5}	VCC	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
13	DCDF#	I	IN_{tp5}	VCC	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
11	SOUTF	O	O_{24}	VCC	UART F Serial Output. This pin is used to transmit serial data out to the communication link.
10	SINF	I	IN_{tp5}	VCC	Serial Input. This pin is used to receive serial data through the communication link.
9	DTRF#	O	O_{24}	VCC	UART F Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
8	RTSF#	O	O_{24}	VCC	UART F Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
7	DSRF#	I	IN_{tp5}	VCC	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
5	CTSF#	I	IN_{tp5}	VCC	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
108	14.7456MHZ _CLKIN	I	IN_{tp5}	VSB	UART-clock 14.7456-MHz input

5.5 KBC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
58	GA20M	O	O_{12}	VSB	Gate A20 output. This pin is high after system reset. (KBC P21)
59	KBRST#	O	O_{12}	VSB	Keyboard reset. This pin is high after system reset. (KBC P20)
62	KCLK	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Clock.
63	KDAT	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Data.
65	MCLK	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Clock.
66	MDAT	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Data.
107	KEYLOCK #	I	IN_{tup5}	VSB	Keyboard inhibits control bits. This pin is after system reset. Internal pull high. (KBC P17)

5.6 CIR Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
15	CIRRX	I	IN_{tsp5}	VSB	CIR input for long length
16	CIRTX	O	O_{12}	VSB	CIR transmission output
87	CIRRXWB	I	IN_{tp5}	VSB	CIR input for wide band

5.7 Hardware Monitor Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
76	CASEOPEN#	I	IN_{tp5}	VRTC	CASE OPEN detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the system is in G3 state. Pulling up a 2-MΩ resistor to VBAT is recommended if not in use.
98	VIN2 / AUXTIN	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
99	VIN1	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
100	VIN0	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
101	CPUVCORE	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
102	VREF	O	AOUT	AVSB	Reference Voltage (around 2.048 V).
103	CPUTIN	I	AIN	AVSB	The input of temperature sensor 2. It is used for CPU temperature sensing.
104	SYSTIN	I	AIN	AVSB	The input of temperature sensor 1. It is used for system temperature sensing.
95	OVT#	O	OD_{12}	VSB	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
95	SMI#	O	OD_{12}	VSB	System Management Interrupt channel output.
6	AUXFANIN	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
14	AUXFANOUT	O	AOUT O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
91	CPUFANIN	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
90	CPUFANOUT	O	AOUT O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
93	SYSFANIN	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
92	SYSFANOUT	O	AOUT O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control. DC voltage output for fan speed control.
18	BEEP	O	OD_{12}	VCC	Beep function for hardware monitor.

5.8 Intel® PECI Interface

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
88	PECI	I/O	I/O_{V3}	Vtt	INTEL® CPU PECI interface. Connect to CPU.
89	VTT	I	Power	Vtt	INTEL® CPU Vtt Power.

5.9 Advanced Configuration & Power Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
68	PSIN#	I	IN_{tp5}	VSB	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.
67	PSOUT#	O	OD_{12}	VSB	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.
75	RSMRST#	O	OD_{12}	VRTC	Resume reset signal output.
73	SLP_S3#	I	IN_{tp5}	VSB	SLP_S3# input.
70	SLP_S5#	I	IN_{tp5}	VSB	SLP_S5# input.
108	ATXPGD	I	IN_{tp5}	VSB	ATX power good signal.
72	PSON#	O	OD_{12}	VSB	Power supply on-off output.
71	PWROK	O	O_{12} OD_{12}	VRTC	3VCC PWROK signal.
64	3VSBSW#	O	OD_{24}	VRTC	Switch 3VSB power to memory when in S3 state.

5.10 Advanced Sleep State Control Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
60	DEEP_S5_1	O	OD_{24}	VSB	This pin is to control system power for entering “more power saving mode”.
64	DEEP_S5_2	O	OD_{24}	VSB	This pin is to control system power for entering “more power saving mode”.

5.11 Port 80 Message Display

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
38	DGH#	O	O_{24}	VSB	Common cathode output of high nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
39	DGL#	O	O_{24}	VSB	Common cathode output of low nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
31	LED_A	O	O_{12}	VSB	Anode outputs for 7-Segment LED.

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
32	LED_B	O	O_{12}	VSB	Anode outputs for 7-Segment LED.
33	LED_C	O	O_{12}	VSB	Anode outputs for 7-Segment LED.
34	LED_D	O	O_{12}	VSB	Anode outputs for 7-Segment LED.
35	LED_E	O	O_{12}	VSB	Anode outputs for 7-Segment LED.
36	LED_F	O	O_{12}	VSB	Anode outputs for 7-Segment LED.
37	LED_G	O	O_{12}	VSB	Anode outputs for 7-Segment LED.

5.12 SMBus Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
96	SCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave clock.
94	SDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave bi-directional Data.
96	MSCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master clock.
94	MSDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master bi-directional Data.

5.13 Power Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
48, 61	3VSB	I		3VSB	+3.3 V stand-by power supply for the digital circuits.
74	VBAT	I		VBAT	+3 V on-board battery for the digital circuits.
12, 28	3VCC	I		3VCC	+3.3 V power supply for driving 3 V on host interface.
97	AVSB	I		AVSB	Analog +3.3 V power input. Internally supply power to all analog circuits.
105	CPUD- / AGND	I		CPUD- / AGND	Analog ground. The ground reference for all analog input. Internally connected to all analog circuits. This pin should be connected to ground.
20, 55	VSS	I		VSS	Ground.
89	VTT	I		VTT	INTEL® CPU Vtt power.

5.14 AMD SB-TSI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
87	TSIC	O	OD_{12}	VCC	AMD SB-TSI clock output.
88	TSID	I/O	IN_{tsp3} OD_{12}	VCC	AMD SB-TSI data input / output.

5.15 Dual Voltage Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
79	BKFD_CUT	O	OD_{12}	VSB	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S3 sleep state.
64	LATCH_BKFD_CUT	O	O_{24}	VRTC	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S5 sleep state.

5.16 DSW

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
81	SLP_SUS#	I	IN_{tp5}	VSB	This pin connects to SLP_SUS# in CPT PCH
82	SUSWARN_5VDUAL	O	OD_{12}	VSB	This pin links to external 5VDUAL control circuits
83	SUSACK#	O	OD_{12}	VSB	This pin connects to SUSACK# in CPT PCH
84	5VDUAL	I	AIN	VSB	Analog input to monitor 5VDUAL voltage
85	SUSWARN#	I	IN_{tp5}	VSB	This pin connects to SUSWARN# in CPT PCH
80	SLP_SUS_FET	O	OD_{12}	VSB	This pin connects to VSB power switch
69	PCHVSB	I	AIN	VSB	PCHVSB function

5.17 WatchDog

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
77	WDTO#	O		VSB	Watchdog Timer output signal.

5.18 IR

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
15	IRRX	I	IN_{tsp5}	VSB	IR Receiver input.
16	IRTX	O	O_{12}	VSB	IR Transmitter output.

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5.19 SUSPEND LED

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
106	SUSLED	O	O_{12}	VSB	Suspend Led signal. This pin can be reflects sleep s5 state through fading led register setting.

5.20 General Purpose I/O Port

5.20.1 GPIO-0 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
109	GP00	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 0.
110	GP01	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 1.
111	GP02	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 2.
112	GP03	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 3.
113	GP04	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 4.
114	GP05	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 5.
115	GP06	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 6.
116	GP07	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 7.

5.20.2 GPIO-1 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
117	GP10	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 0.
118	GP11	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 1.
119	GP12	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 2.
120	GP13	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 3.
121	GP14	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 4.
122	GP15	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 5.
123	GP16	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 6.
124	GP17	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 7.

5.20.3 GPIO-2 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
125	GP20	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 2 bit 0.
126	GP21	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 2 bit 1.

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
127	GP22	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 2 bit 2.
128	GP23	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 2 bit 3.
1	GP24	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 2 bit 4.
2	GP25	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 2 bit 5.
3	GP26	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 2 bit 7.
4	GP27	I/O	IN_{tp5} O_{12} OD_{12}	VCC	General-purpose I/O port 2 bit 7.

5.20.4 GPIO-3 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
32	GP30	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 0.
33	GP31	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 1.
34	GP32	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 2.
35	GP33	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 3.

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
36	GP34	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 4.
37	GP35	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 5.
38	GP36	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 3 bit 6.
39	GP37	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 3 bit 7.

5.20.5 GPIO-4 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
40	GP40	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 0.
41	GP41	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 1.
42	GP42	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 2.
43	GP43	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 3.
44	GP44	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 4.
45	GP45	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 5.

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
46	GP46	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 6.
47	GP47	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 7.

5.20.6 GPIO-5 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
62	GP50	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 0.
63	GP51	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 1.
65	GP52	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 2.
66	GP53	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 3.
67	GP54	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 4.
68	GP55	I/O	IN_{tp5} O_{8} OD_{8}	VSB	General-purpose I/O port 5 bit 5.
70	GP56	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 6.
71	GP57	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 7.

5.20.7 GPIO-6 Interface

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
72	GP60	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 0.
73	GP61	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 1.
75	GP62	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 2.
94	GP63	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 3.
96	GP64	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 4.
106	GP65	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 5.
107	GP66	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 6.
108	GP67	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 7.

5.20.8 GPIO-7 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
87	GP71	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 1.

5.21 Strapping Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

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PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
51	2E_4E_SEL	I	IN_{tdp5}	VSB	SIO I/O address selection. (Strapped by LRESET#) Strapped to high: SIO I/O address is 4Eh/4Fh. Strapped to low: SIO I/O address is 2Eh/2Fh.
52	24M_48M_SEL	I	IN_{tdp5}	VSB	Input clock rate selection (Strapped by VCC [internal Power OK signal without any delay]) Strapped to high: The clock input on pin 19 is 48MHz. Strapped to low: The clock input on pin 19 is 24MHz.
54	GPIO_PORT80_SEL	I	IN_{tdp5}	VSB	Function selection. (Strapped by VCC [internal Power OK signal without any delay]) See configuration register.
106	COMB_DSW_SEL	I	IN_{tdp5}	VSB	Pin78-85 function selection. (Strapped by VSB power [internal RSMRST# signal]) Strapped to high: DSW Strapped to low: UART
111	SOUTC_P80_SEL	I	IN_{tdp5}	VSB	Pin114 function selection. (Strapped by VCC [internal Power OK signal without any delay]) See configuration register.
112	SOUTE_P80_SEL	I	IN_{tdp5}	VSB	Pin2 function selection. (Strapped by VCC [internal Power OK signal without any delay]) See configuration register.

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

1) VSB Strapping result can be programming by LPC, and reset by RSMRST#.
2) VCC Strapping result can be programming by LPC, and reset by PWROK.
3) LRESET# Strapping (2E_4E_SEL) can be programming by LPC, and reset by LRESET#.

5.22 Internal pull-up, pull-down pins

Signal	Pin(s)	Power well	Type	Resistor	Note
Strapping Pins					
2E_4E_SEL	51	VSB	Pull-down	47.4K	1

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Signal	Pin(s)	Power well	Type	Resistor	Note
24M_48M_SEL	52	VSB	Pull-down	47.4K	1
GPIO_PORT80_SEL	54	VSB	Pull-down	47.4K	1
COMB_DSW_SEL	106	VSB	Pull-down	47.4K	2
SOUTC_P80_SEL	111	VSB	Pull-down	47.4K	1
SOUTE_P80_SEL	112	VSB	Pull-down	47.4K	1
Advanced Configuration & Power Interface					
PSIN#	68	VSB	Pull-up	47.03K	
KEYLOCK#	107	VSB	Pull-up	47.03K	

Note1. Active only during VCC Power-up reset
Note2. Active only during VSB Power-up reset

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6. GLUE LOGIC

6.1 ACPI Glue Logic

Table 6-1 Pin Description

SYMBOL	PIN	DESCRIPTION
SLP_S5#	70	SLP_S5# input.
PWROK	71	This pin generates the PWROK signals while 3VCC is present.
RSMRST#	75	The RSMRST# signal is a reset output and is used as the VSB power on reset signal for the South Bridge. When the NCT6102D / NCT6106D detects the 3VSB voltage rises to "V1", it then starts a delay – "t1" before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below "V2", the RSMRST# de-asserts immediately.

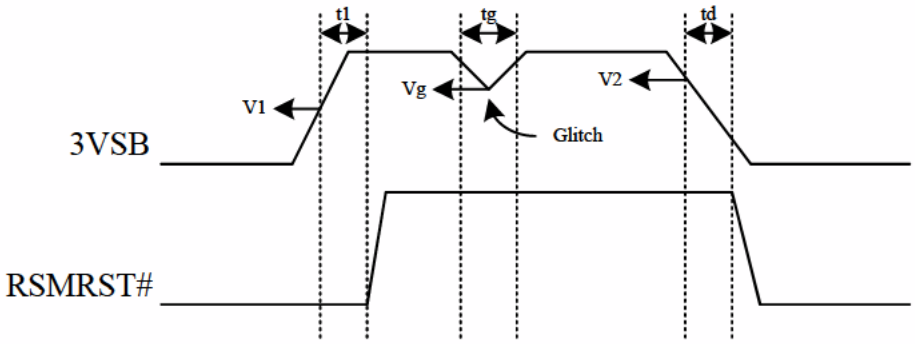

Figure 6-1 RSMRST#

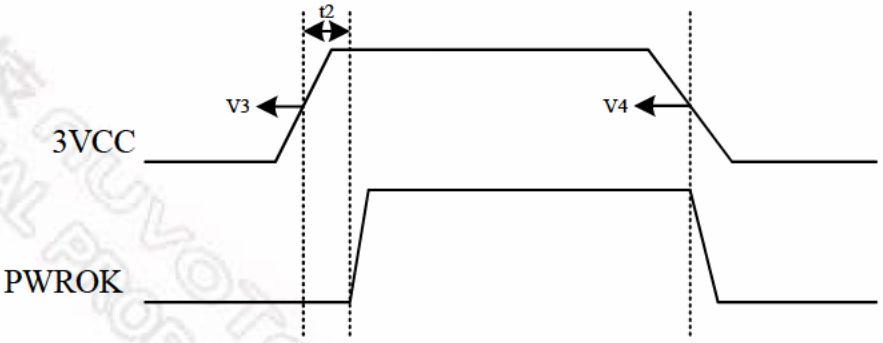

Figure 6-2 PWROK

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TIMING	PARAMETER	MIN	MAX	UNIT
t1	Valid 3VSB to RSMRST# inactive	200	300	mS
tg	3VSB Glitch allowance		1	uS
td	Falling 3VSB supply Delay		1	uS
t2	Valid 3VCC to PWROK active	300	500	mS

DC	PARAMETER	MIN	MAX	UNIT
V1	3VSB Valid Voltage	-	3.033	Volt
V2	3VSB Ineffective Voltage	2.882	-	Volt
V3	3VCC Valid Voltage	-	2.83	Volt
V4	3VCC Ineffective Voltage	2.68	-	Volt
Vg	3VSB drops by Power noise	2	-	Volt

Note： 1. The values above are the worst-case results of R&D simulation.

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6.2 BKFD_CUT & LATCH_BKFD_CUT

NCT6102D / NCT6106D supports BKFD_CUT & LATCH_BKFD_CUT functions, please refer the timing diagram below.

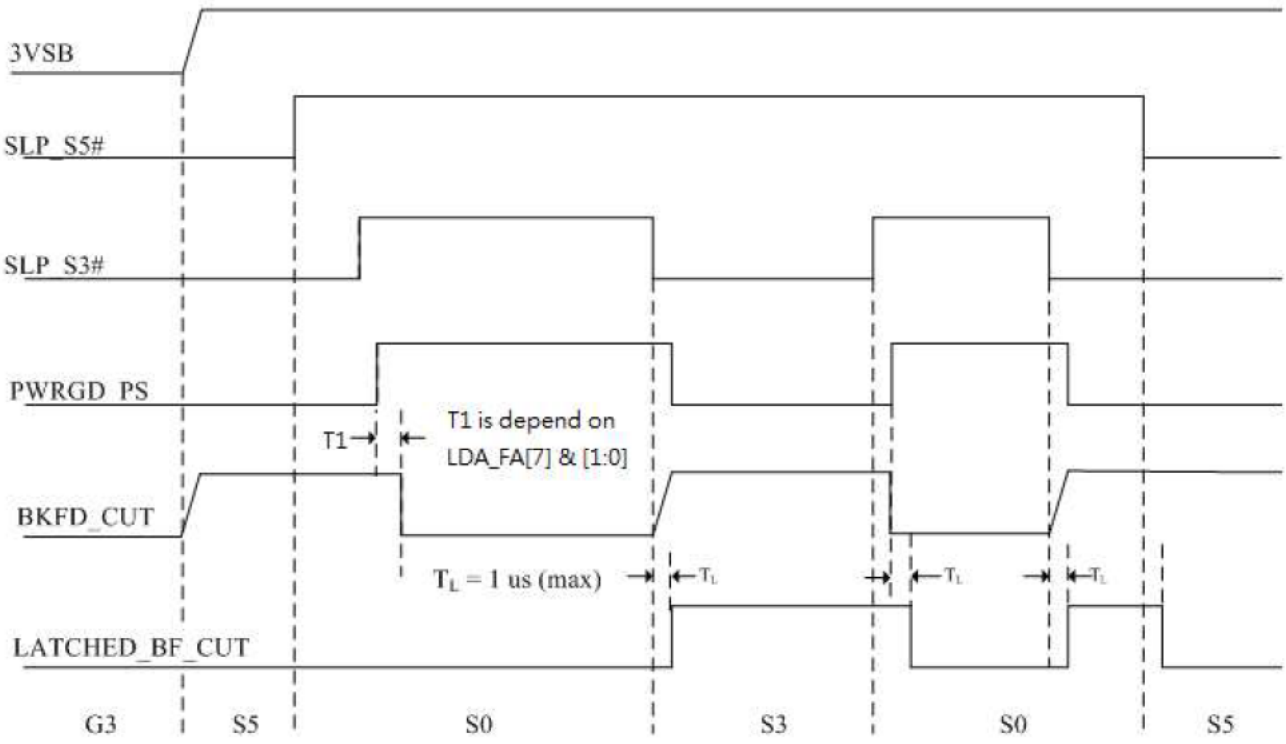

Figure 6-3 BKFD_CUT and LATCH_BKFD_CUT

BKFD_CUT (Backfeed_Cut) – When high, switches dual rails to standby power.

LATCH_BKFD_CUT (Latched_Backfeed_Cut) – When high, switches dual rails to standby power.

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6.3 3VSBSW#

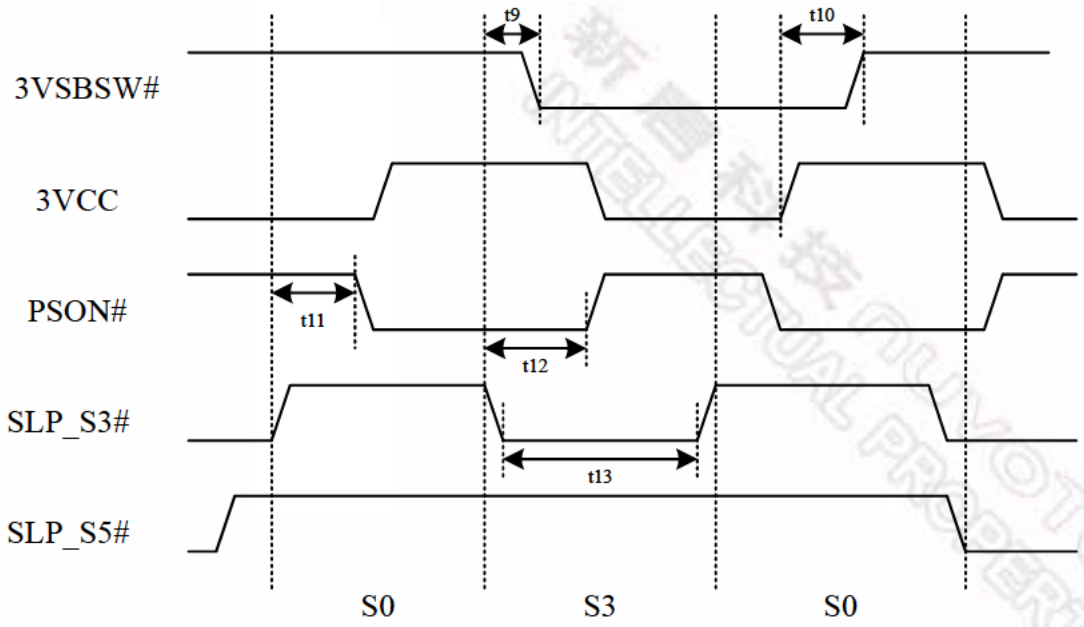

Figure 6-4 3VSBSW#

TIMING	PARAMETER	MIN	MAX	UNIT
t3	SLP_S3# active to 3VSBSW# active	0	30	mS
t4	3VCC active to 3VSBSW# inactive	90	142	mS
t5	SLP_S3# inactive to PSON# active	0	80	nS
t6	SLP_S3# active to PSON# inactive	15	45	mS
t7	SLP_S3# minimal Low Time	40	-	mS

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6.4 PSON# Block Diagram

The PSON# function controls the main power on/off. The main power is turned on when PSON# is low. Please refer to the figure below.

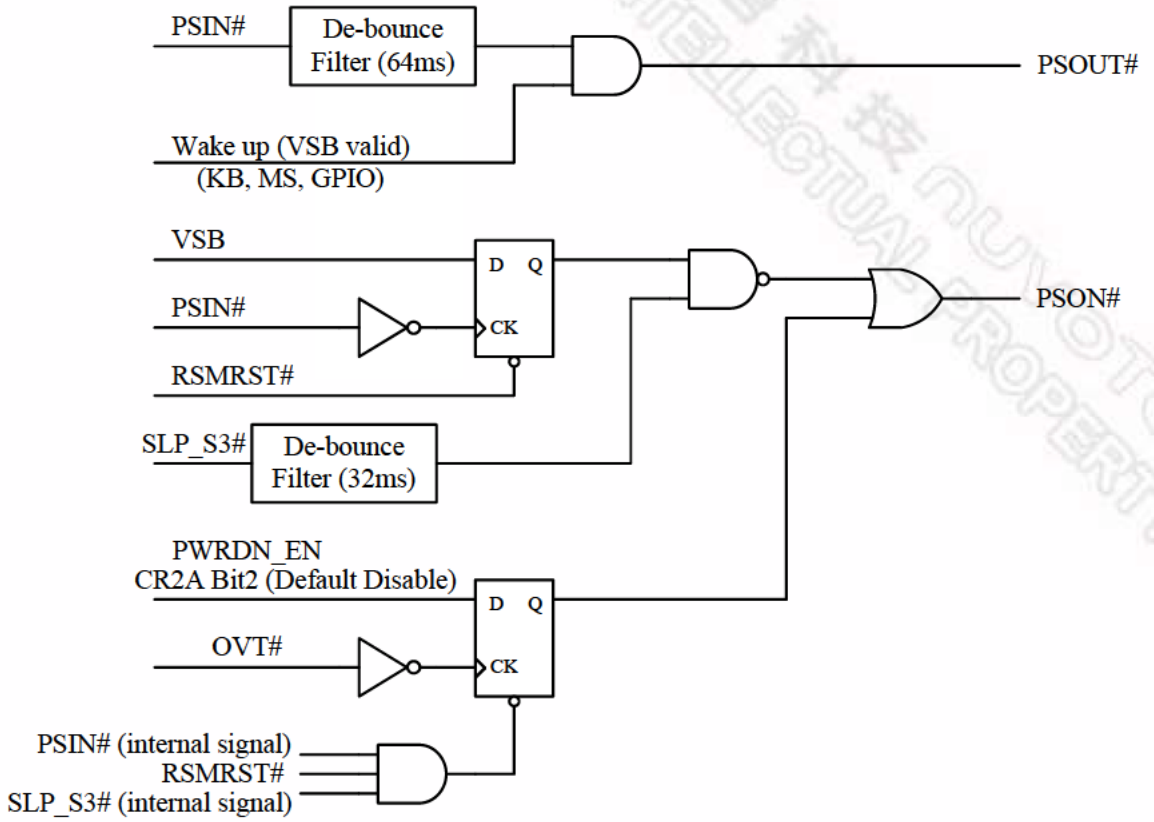

Figure 6-5 PSON#

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6.5 PWROK

PWROK Signal indicates the main power (VCC Power) is valid. Besides, valid PWROK signal also requires the following conditions, as shown in the figure below.

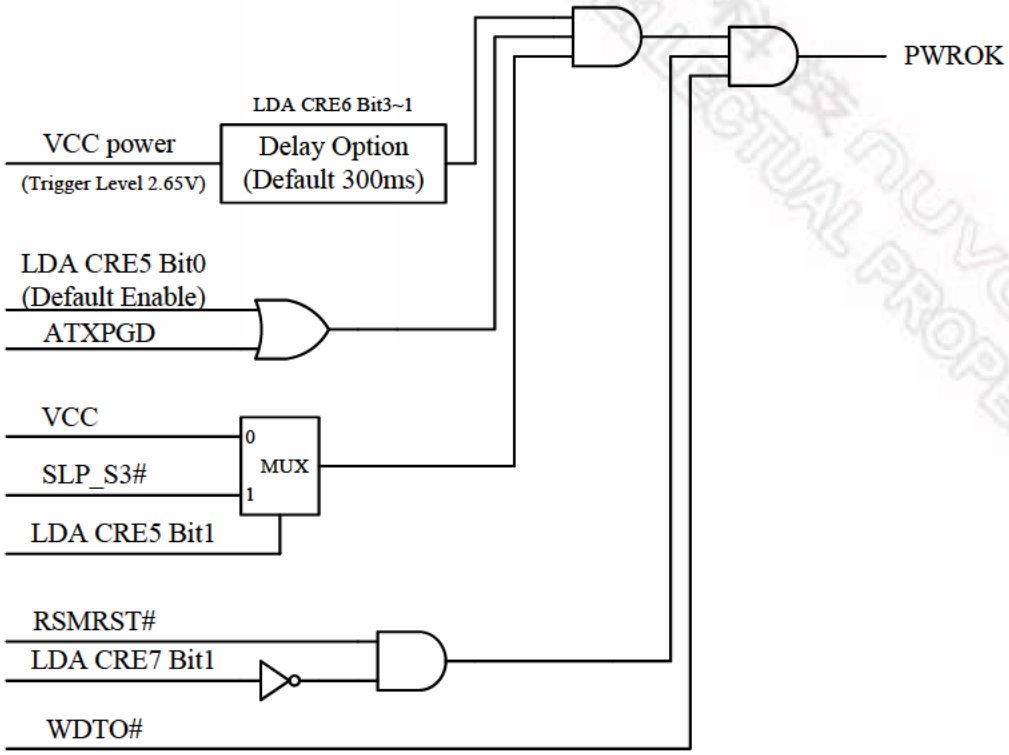

Figure 6-6 PWROK Block Diagram

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6.6 Front Panel LEDs

NCT6102D / NCT6106D supports two LED control to some GPIO pins – GRN_LED and YLW_LED.

For dual-color LED application:

(1)GRN_LED pin is connected to a 470ohm resistor to 5VSB, and the cathode of the green LED and the anode of the yellow LED.

(2)YLW_LED pin is connected to a 470ohm resistor to 5VSB, and the cathode of the yellow LED and the anode of the green LED.

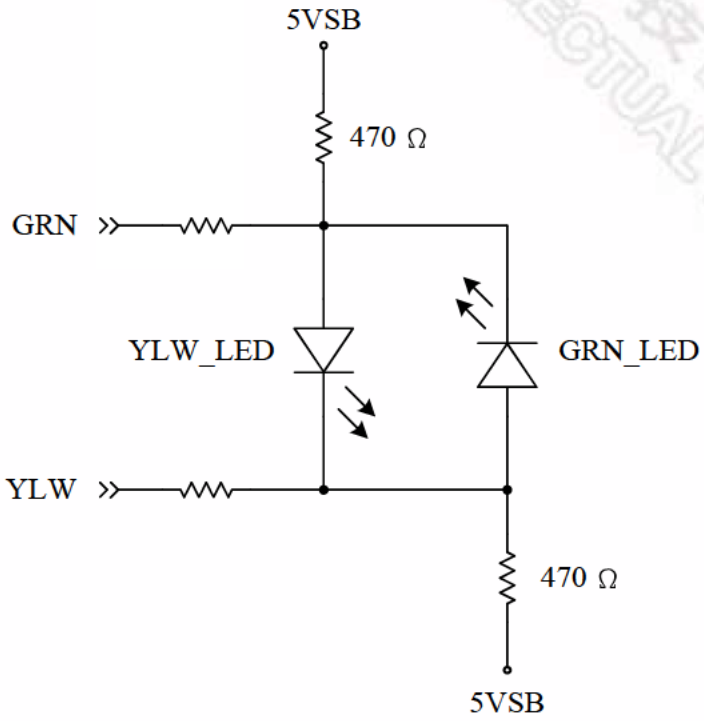

Figure 6-7 Illustration of Dual Color LED application

GRN_LED and YLW_LED pins are designed to show currently power states. There are Manual Mode and Automatic Mode:

6.6.1 Automatic Mode

Power state is S0 or S1: GRN_LED will be asserted by default.

Power state is S3: YLW_LED will be asserted by default.

Power state is S4 or S5: Both GRN_LED and YLW_LED will be de-asserted by default.

AUTO_EN	GRN_LED_RST (YLW_LED_RST)	Pwr State	SLP_S3#	SLP_S5#	GRN_LED	YLW_LED
1	X	S0,S1	1	1	GRN_BLK_FREQ	HIGH-Z
1	X	S3	0	1	HIGH-Z	YLW_BLK_FREQ

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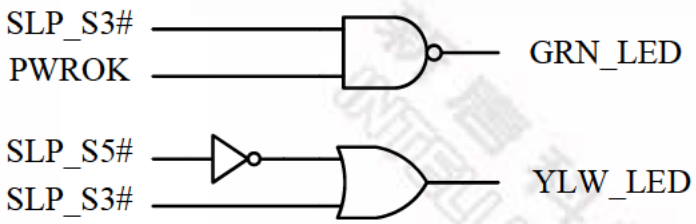
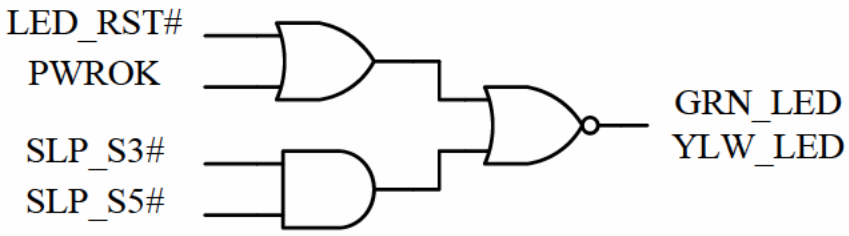
1	X	S4,S5	X	0	HIGH-Z	HIGH-Z



6.6.2 Manual Mode

AUTO_EN	GRN_LED_RST#	Pwr State	SLP_S3#	SLP_S5#	GRN_LED	YLW_LED
0	0	S0,S1	1	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	0	S3	0	1	HIGH-Z	HIGH-Z
0	0	S4,S5	X	0	HIGH-Z	HIGH-Z
0	1	S0,S1	1	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	1	S3	0	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	1	S4,S5	X	0	GRN_BLK_FREQ	YLW_BLK_FREQ



6.6.3 S0~S5 LED Blink Block Diagram

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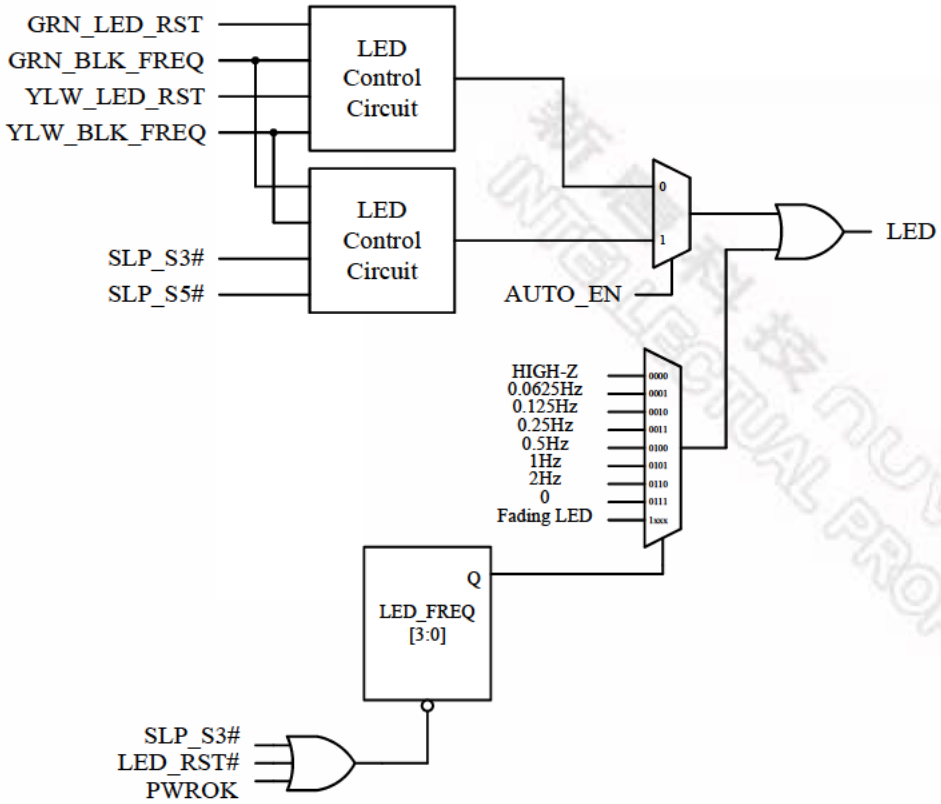

6.6.4 LED Pole (LED_POL)

Set to 0b, GRN_LED output is active low, as the following Figure (a)
Set to 1b, GRN_LED output is active high, as the following Figure (b)

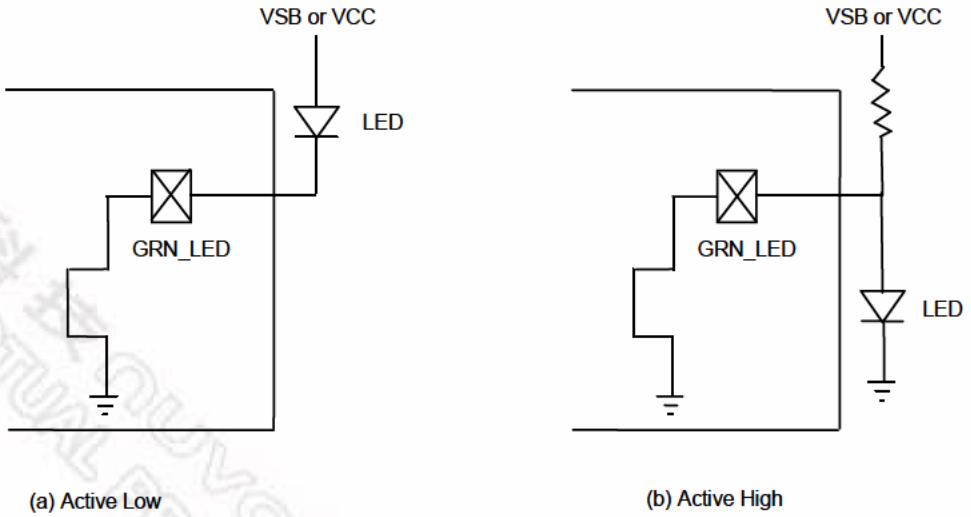

Figure 6-8 Illustration of LED polarity

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6.6.5 Deeper Sleeping State Detect Function

These two LED pins could also be used to indicate if the system is in Deeper Sleeping State. For more detail, please refer to the section of Advanced Sleep State Control Function.

Enable_DEEP_S5	GRN_DEEPS#_Disable (YLW_DEEPS#_Disable)	Pwr State	GRN_LED	YLW_LED
1	0	DEEP_S5	DeepS5_GRN_BLK_FREQ	DeepS5_YLW_BLK_FREQ
1	1	DEEP_S5	HIGH-Z	HIGH-Z
0	X	S0~S5	S0~S5 behavior	S0~S5 behavior

Enable_DEEP_S3	GRN_DEEPS#_Disable (YLW_DEEPS#_Disable)	Pwr State	GRN_LED	YLW_LED
1	0	DEEP_S3	DeepS3_GRN_BLK_FREQ	DeepS3_YLW_BLK_FREQ
1	1	DEEP_S3	HIGH-Z	HIGH-Z
0	X	S0~S5	S0~S5 behavior	S0~S5 behavior

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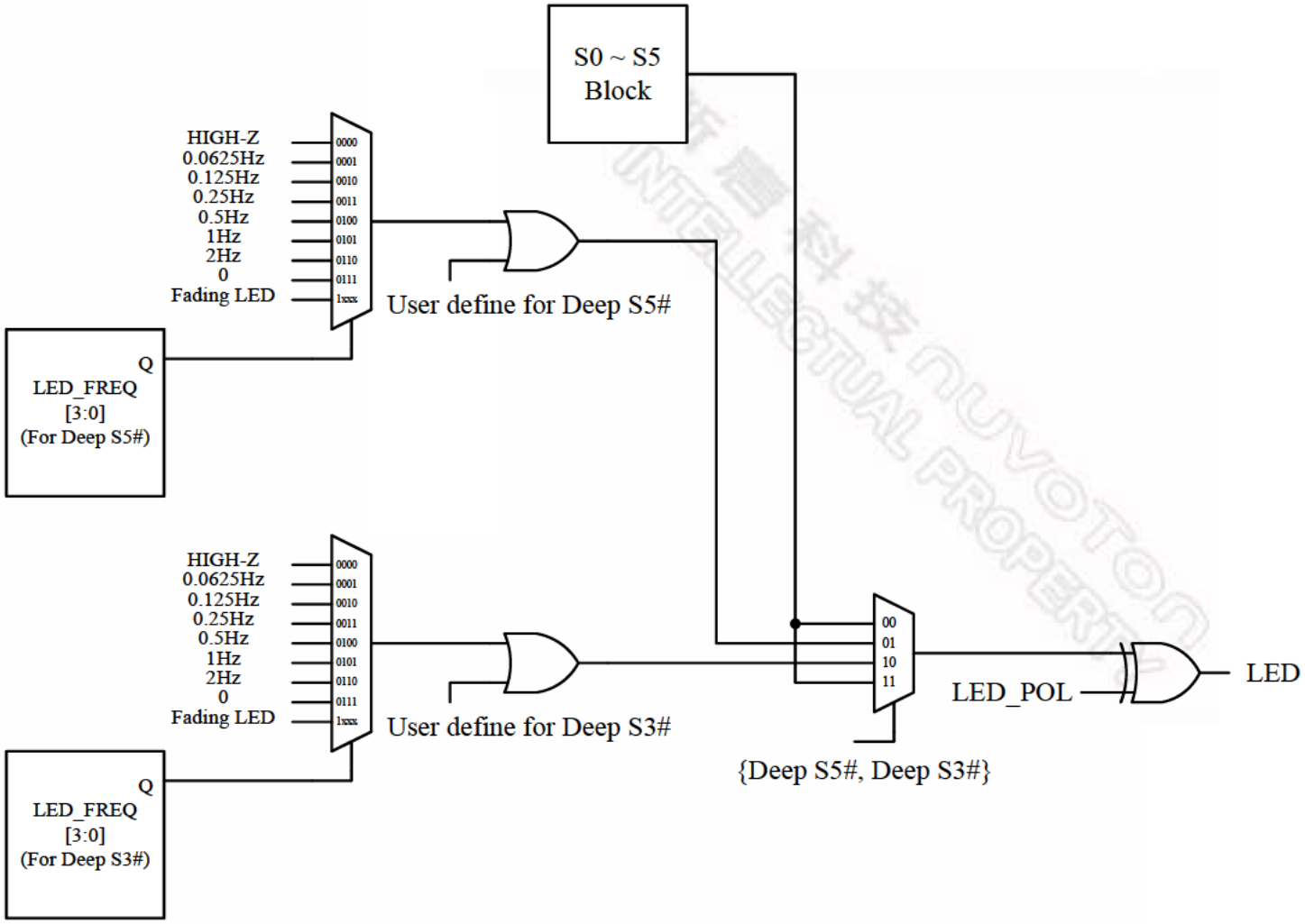

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6.7 Advanced Sleep State Control (ASSC) Function

Advanced Sleep State Control (ASSC) Function is used to control the system power at S3 or S5 state. The purpose of this function is to provide a method to reduce power consumption at S3 or S5 state. This function is disabled by default. When VCC power is first supplied, BIOS can program the register to enable ASSC Function. The register is powered by 3VSB_IO and some is powered by VBAT. The related registers are located at Logic Device 16 CRE0h ~ CRE3h.

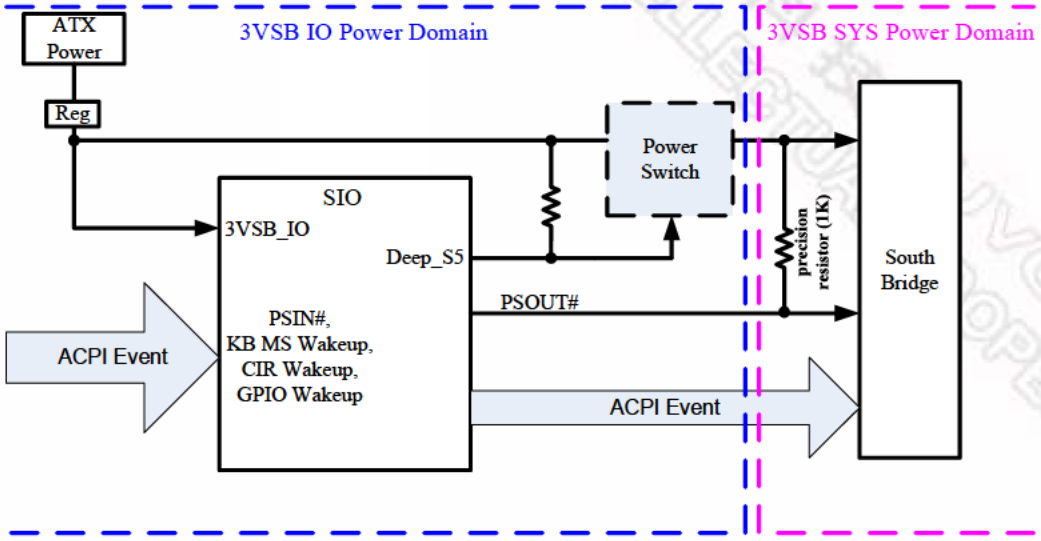
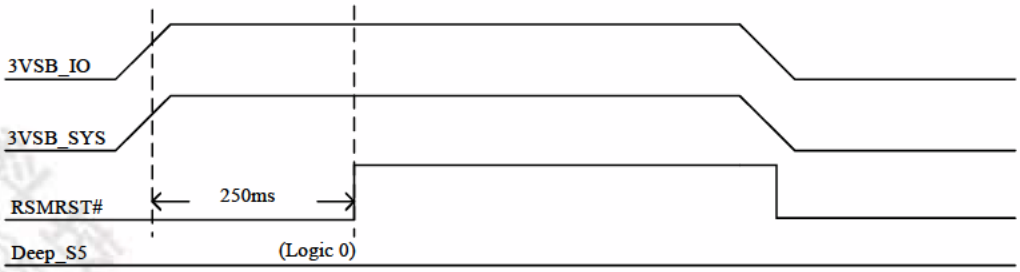


Figure 6-9 ASSC Application Diagram

6.7.1 When ASSC is disabled



When ASSC is disabled, ACPI function is as same as the normal ACPI behavior.

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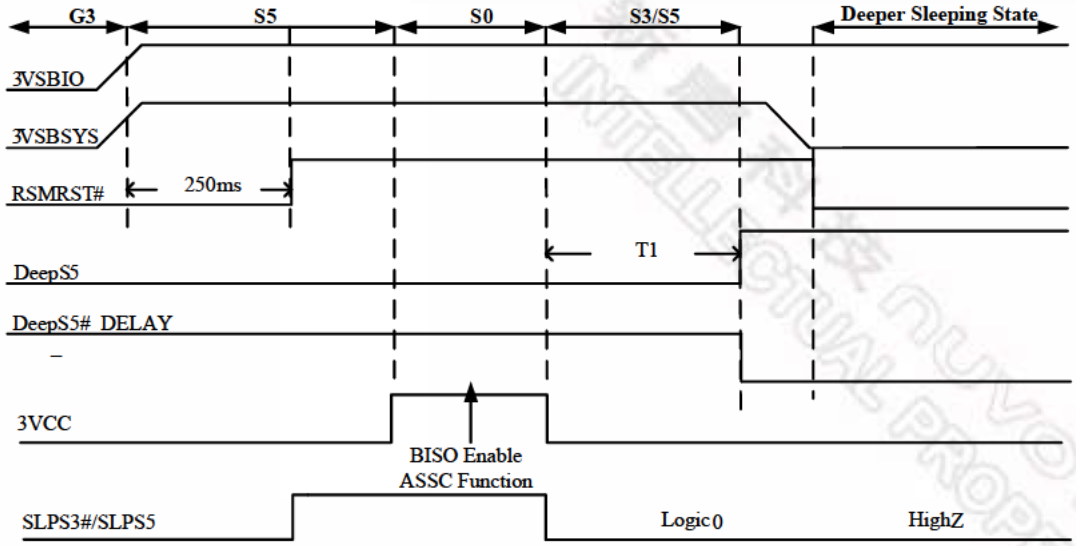
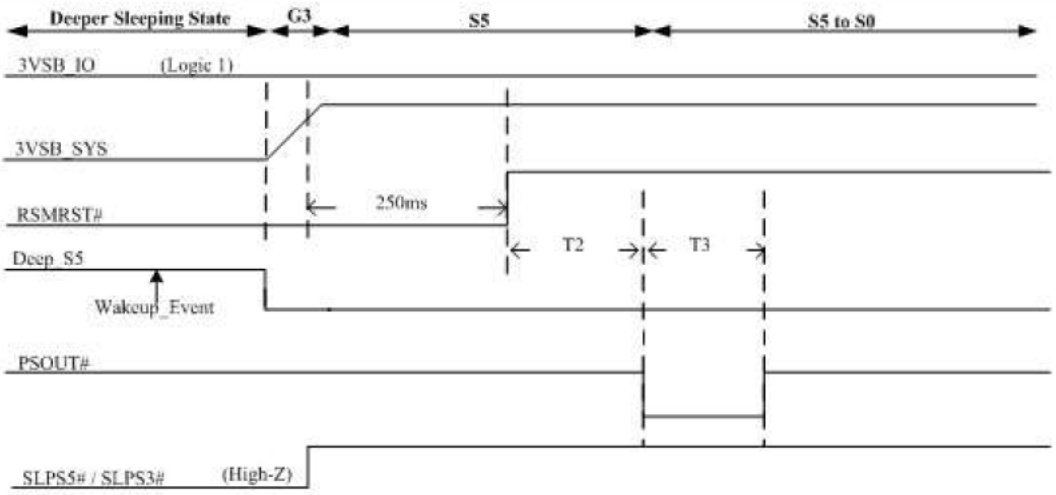
6.7.2 When ASSC is enabled (Enter into Deeper Sleeping State)



When the first time AC plug in and enter into S0 State, BIOS can enable ASSC Function (DeepS3 or DeepS5), when the system enters S3/S5 state, the pin DEEP_S5 will be asserted after pre configuration delay time (power_off_dly_time, LD16 CRE2) to make the system entering the "Deeper Sleeping State (DSS)" where system's VSB power is cut off. When pin DEEP_S5 asserts, the pin RSMRST# will de-assert by detecting PSOUT# signal (monitor 3VSB SYS Power).

6.7.3 When ASSC is enabled (Exit Deeper Sleeping State)



When any Wakeup Event (PSIN#, KB MS Wakeup, CIR wakeup, GPIO Wakeup) happened, pin DEEP_S5 will be de-asserted to turn on the VSB power to the system. The pin RSMRST# will de-assert when 3VSB_SYS power reach valid voltage. And then the pin PSOUT# will issue a low pulse (T3) turn on the system after T2 time (wakeup

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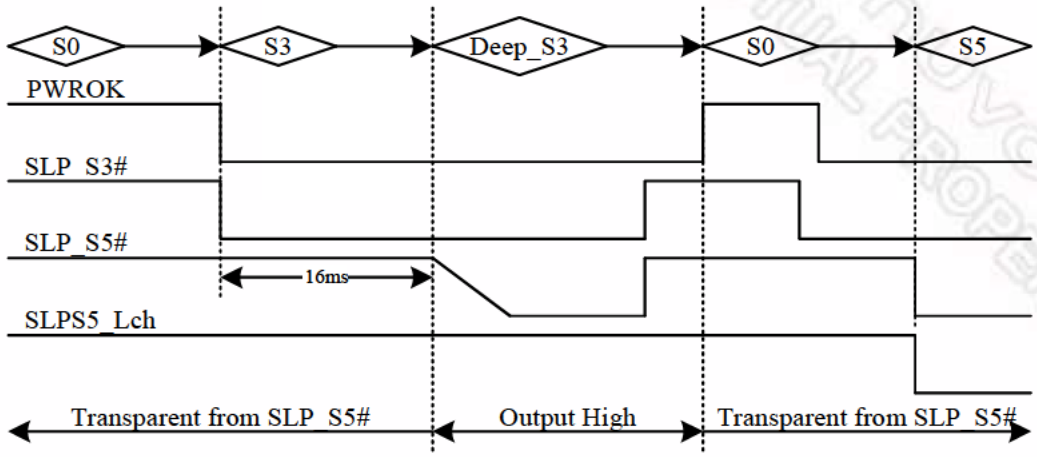
delay time, LD16 CRE0). The PSOUT# low pulse is also programmable (LD16 CRE1). The T4 time is the delay from Deep_S5 ds-assert to Deeo_S5#_DELAY de-assert.

6.7.4 SLP_S5#_LATCH Control Function

SLP_S5#_LATCH control signal is similar to SLPS5# signal. When System is at S0 ~ S5 state, SLP_S5#_LATCH follows the SLPS5# signal. When system is at DeepS5 State, SLP_S5#_LATCH will keep low state till system returns to S0 state. When system is at DeepS3 State, SLP_S5#_LATCH will keep high till system returns to S0 state. Please see the following timing diagram.



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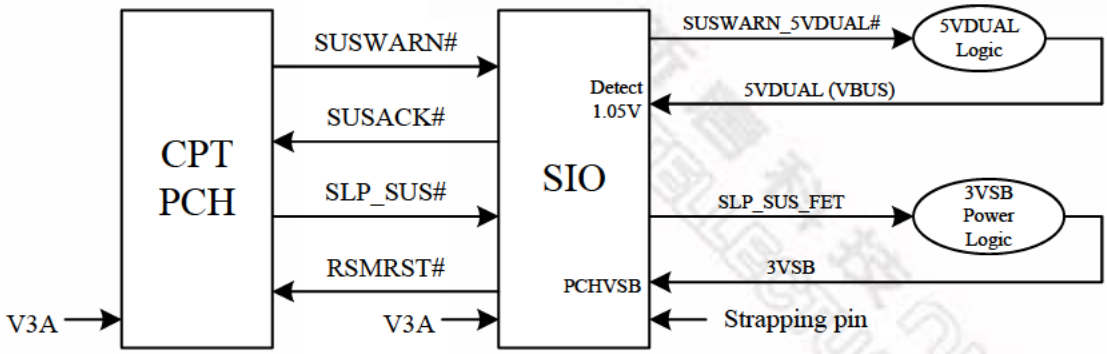
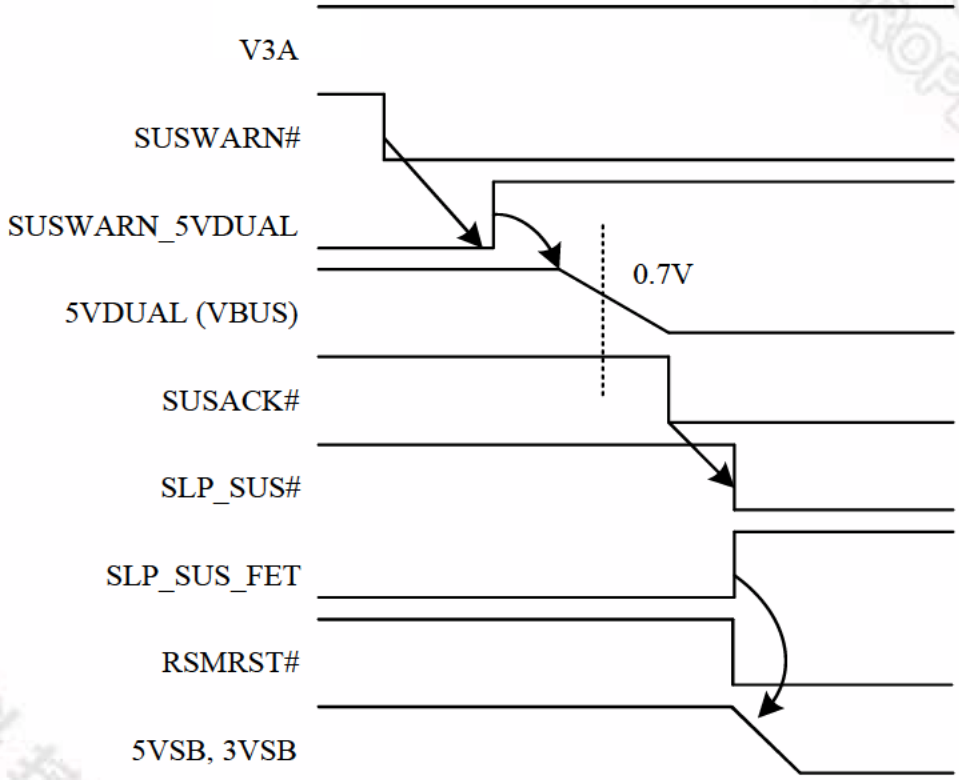
6.8 Intel DSW Function



6.8.1 Enter DSW State timing diagram



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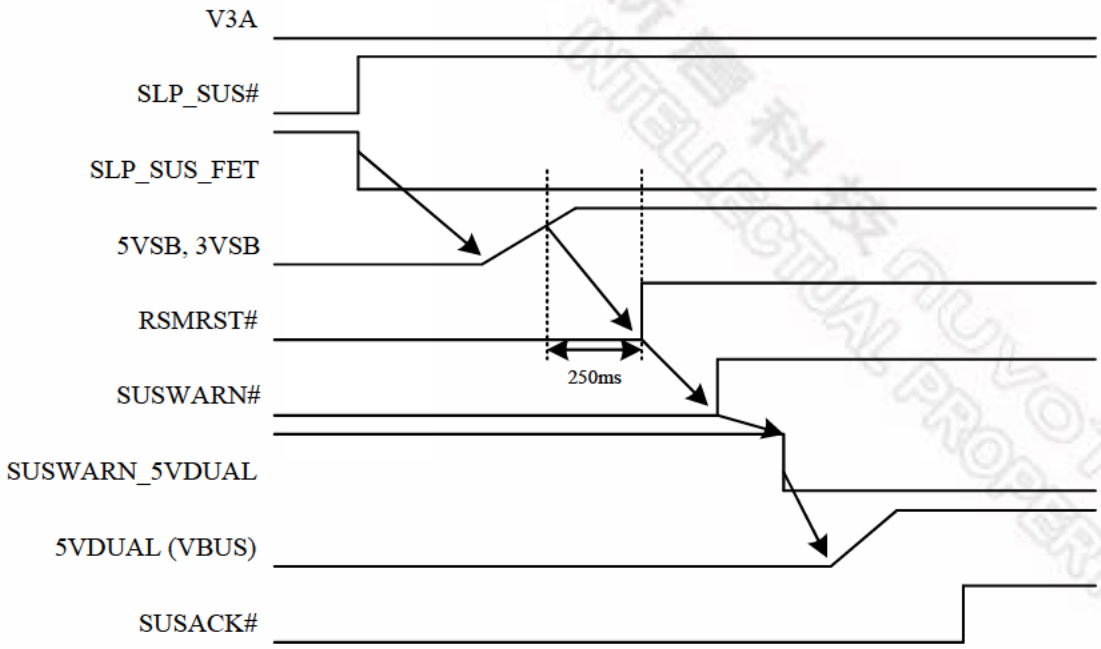
6.8.2 Exit DSW State timing diagram



6.8.3 Application Circuit

The NCT6102D / NCT6106D can not only provide SIO Deep S5/S3 function, but Intel DSW function. The application circuit should follow the guide below:

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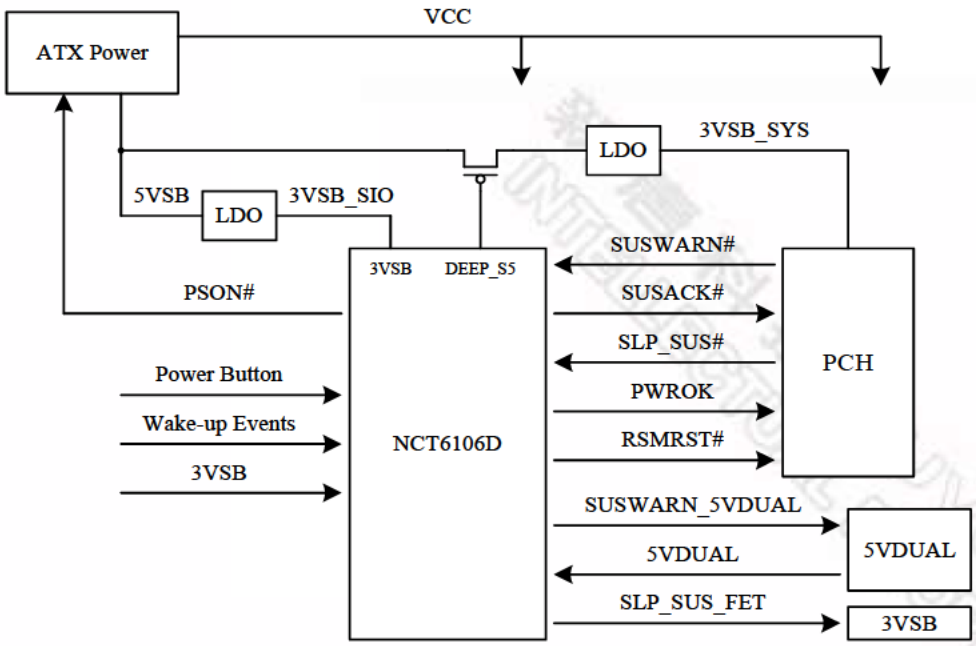

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7. CONFIGURATION REGISTER ACCESS PROTOCOL

The NCT6102D / NCT6106D uses a special protocol to access configuration registers to set up different types of configurations. The NCT6102D / NCT6106D has a total of 17 Logical Devices (from Logical Device 0 to Logical Device 16 with the exception of Logical Device 4 & C for backward compatibility) corresponding to fourteen individual functions: FDC (Logical Device 0), PRT (Logical Device 1), UARTA (Logical Device 2), UARTB (Logical Device 3), KBC (Logical Device 5), CIR (Logical Device 6), GPIO (Logical Device 7), GPIO & WDT1 (Logical Device 8), GPIO (Logical Device 9), ACPI (Logical Device A), HM & LED (Logical Device B), WDT2 (Logical Device D), CIR WAKE-UP (Logical Device E), GPIO (Logical Device F), UARTC (Logical Device 10), UARTD (Logical Device 11), UARTE (Logical Device 12), UARTF (Logical Device 13), PORT80 & IR (Logical Device 14), FADING LED (Logical Device 15) and DEEP SLEEP (Logical Device 16).

It would require a large address space to access all of the logical device configuration registers if they were mapped into the normal PC address space. The NCT6102D / NCT6106D, then, maps all the configuration registers through two I/O addresses (2Eh/2Fh or 4Eh/4Fh) set at power on by the strap pin 2E_4E_SEL. The two I/O addresses act as an index/data pair to read or write data to the Super I/O. One must write an index to the first I/O address which points to the register and read or write to the second address which acts as a data register.

An extra level of security is added by only allowing data updates when the Super I/O is in a special mode, called the Extended Function Mode. This mode is entered by two successive writes of 87h data to the first I/O address. This special mode ensures no false data can corrupt the Super I/O configuration during a program runaway.

There are a set of global registers located at index 0h – 2Fh, containing information and configuration for the entire chip.

The method to access the control registers of the individual logical devices is straightforward. Simply write the desired logical device number into the global register 07h. Subsequent accesses with indexes of 30h or higher are directly to the logical device registers.

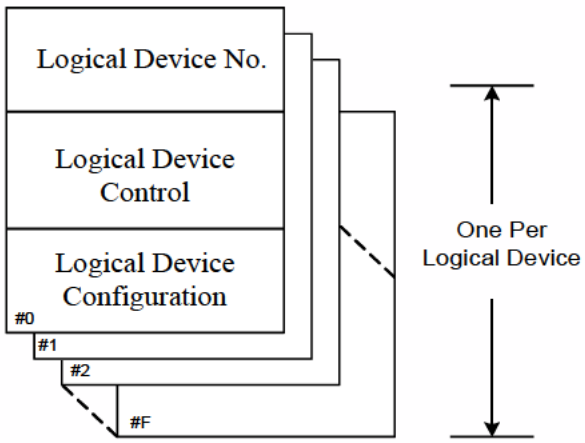

Figure 7-1 Structure of the Configuration Register

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Table 7-1 Devices of I/O Base Address

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
0	FDC	100h ~ FF8h
1	PRT	100h ~ FF8h
2	UARTA	100h ~ FF8h
3	UARTB	100h ~ FF8h
4	Reserved	
5	KBC	100h ~ FFFh
6	CIR	100h ~ FF8h
7	GPIO	Reserved
8	GPIO, WDT1	Reserved
9	GPIO	Reserved
A	ACPI	Reserved
B	HM, LED	100h ~ FFEh
C	Reserved	
D	WDT2	Reserved
E	CIR WAKE-UP	100h ~ FF8h
F	GPIO	Reserved
10	UARTC	100h ~ FF8h
11	UARTD	100h ~ FF8h
12	UARTE	100h ~ FF8h
13	UARTF	100h ~ FF8h
14	PORT80, IR	100h ~ FF8h
15	FADING LED	Reserved
16	DEEP SLEEP	Reserved

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7.1 Configuration Sequence

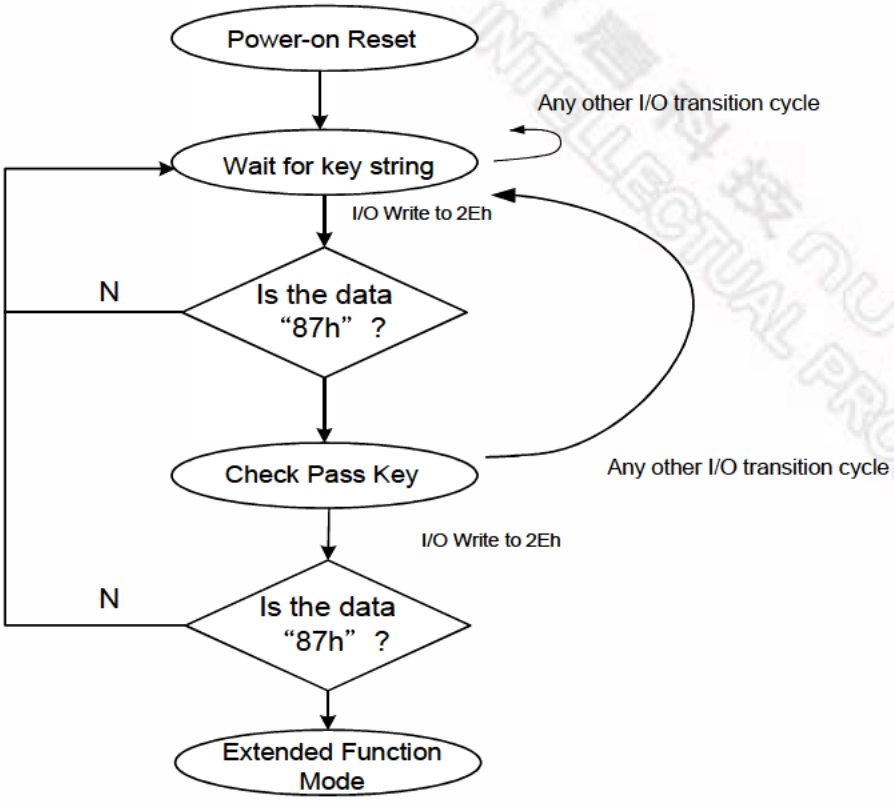

Figure 7-2 Configuration Register

To program the NCT6102D / NCT6106D configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

(3). Exit the Extended Function Mode.

7.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

7.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

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Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

7.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

7.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR [26h] bit 6 showing the value of the strap pin at power on) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

This example programs the configuration register F0h (clock source) of logical device 1 (UART A) to the value of 3Ch (24MHz). First, one must enter the Extended Function Mode, then setting the Logical Device Number (Index 07h) to 01h. Then program index F0h to 3Ch. Finally, exit the Extended Function Mode.

```
;-----------------------------------------------
; Enter the Extended Function Mode
;-----------------------------------------------
MOV    DX, 2EH
MOV    AL, 87H
OUT    DX, AL
OUT    DX, AL
;-------------------------------------------------------------------------
; Configure Logical Device 1, Configuration Register CRF0
;-------------------------------------------------------------------------
MOV    DX, 2EH
MOV    AL, 07H
OUT    DX, AL          ; point to Logical Device Number Reg.
MOV    DX, 2FH
MOV    AL, 01H
OUT    DX, AL          ; select Logical Device 1
;
MOV    DX, 2EH
MOV    AL, F0H
OUT    DX, AL          ; select CRF0
MOV    DX, 2FH
MOV    AL, 3CH
OUT    DX, AL          ; update CRF0 with value 3CH
;-------------------------------------------
; Exit the Extended Function Mode
;-------------------------------------------
MOV    DX, 2EH
MOV    AL, AAH
OUT    DX, AL
```


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8. HARDWARE MONITOR

8.1 General Description

The NCT6102D / NCT6106D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures, all of which are very important for a high-end computer system to work stably and properly. In addition, proprietary hardware reduces the amount of programming and processor intervention to control cooling fan speeds, minimizing ambient noise and maximizing system temperature and reliability.

The NCT6102D / NCT6106D can simultaneously monitor all of the following inputs:

- Eight analog voltage inputs (five internal voltages CPUVCORE, VBAT, 3VSB, 3VCC and AVCC; three external voltage inputs)
- Three fan tachometer inputs
- Three remote temperatures, using either a thermistor or from the CPU thermal diode (voltage or Current Mode measurement method)
- One case-open detection signal.

These inputs are converted to digital values using the integrated, eight-bit analog-to-digital converter (ADC).

In response to these inputs, the NCT6102D / NCT6106D can generate the following outputs:

- Three PWM (pulse width modulation) or DC fan outputs for the fan speed control
- SMI#
- OVT# signals for system protection events

The NCT6102D / NCT6106D provides hardware access to all monitored parameters through the LPC or I^2C interface and software access through application software, such as Nuvoton's Hardware Doctor™, or BIOS.

The rest of this section introduces the various features of the NCT6102D / NCT6106D hardware-monitor capability. These features are divided into the following sections:

- Access Interfaces
- Analog Inputs
- Fan Speed Measurement and Control
- Smart Fan Control
- SMI# interrupt mode
- OVT# interrupt mode
- Registers and Value RAM

8.2 Access Interfaces

The NCT6102D / NCT6106D provides two interfaces, LPC and I^2C, for the microprocessor to read or write the internal registers of the hardware monitor.

8.3 LPC Interface

The internal registers of the hardware monitor block are accessible through two separate methods on the LPC bus. The first set of registers, which primarily enable the block and set its address in the CPU I/O address space are accessed by the Super I/O protocol described in Chapter 7 at address 2Eh/2Fh or 4Eh/4Fh. The bulk of the functionality and internal registers of this block are accessed form an index/data pair of CPU I/O addresses. The

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standard locations are usually 295h/296h and are set by CR[60h]&CR[61h] accessed using the Super I/O protocol as described in Chapter 7.

Due to the number of internal register, it is necessary to separate the register sets into “banks” specified by register 4Eh. The structure of the internal registers is shown in the following figure.

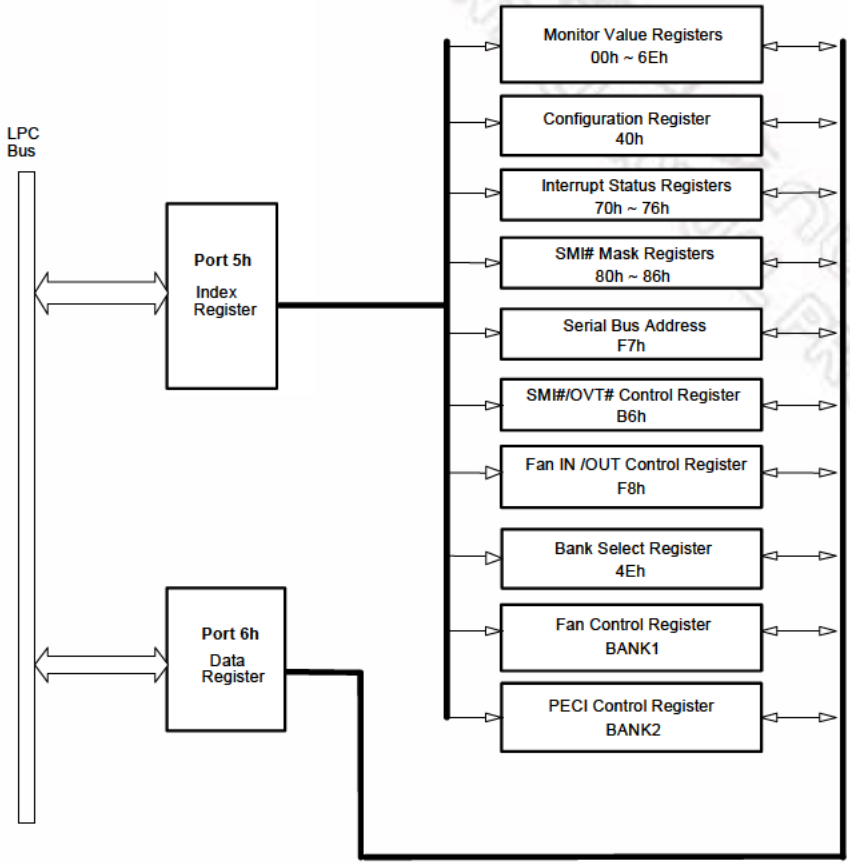

Figure 8-1 LPC Bus’ Reads from / Write to Internal Registers

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8.4 I²C interface

The I²C interface is a second, serial port into the internal registers of the hardware monitor function block. The interface is totally compatible with the industry-standard I²C specification, allowing external components that are also compatible to read the internal registers of the NCT6102D / NCT6106D hardware monitor and control fan speeds. The address of the I²C peripheral is set by the register located at index 48h (which is accessed by the index/data pair at I/O address typically at 295h/296h)

The two timing diagrams below illustrate how to use the I²C interface to write to an internal register and how to read the value in an internal register, respectively.

(a) Serial bus write to internal address register followed by the data byte

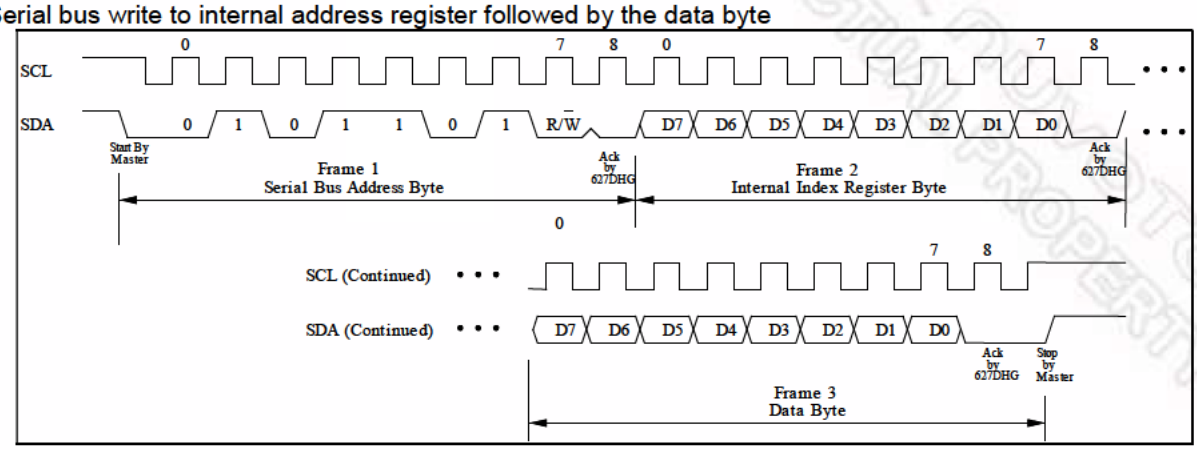

Figure 8-2 Serial Bus Write to Internal Address Register Followed by the Data Byte

(b) Serial bus read from a register

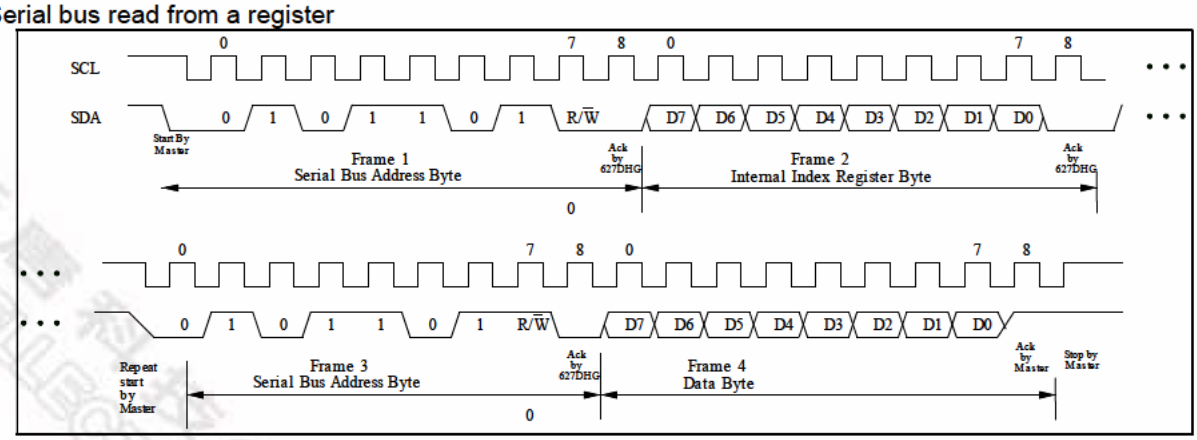

Figure 8-3 Serial Bus Read from Internal Address Register

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8.5 Analog Inputs

The nine analog inputs of the hardware monitor block connect to an 8-bit Analog to Digital Converter (ADC) and consist of 4 general-purpose inputs connected to external device pins (VIN0 – VIN2) and five internal signals connected to the power supplies (CPUVCORE, AVCC, VBAT, 3VSB and 3VCC). All inputs are limited to a maximum voltage of 2.048V due to an internal setting of 8mV LSB (256 steps x 8mV = 2.048V). All inputs to the ADC must limit the maximum voltage by using a voltage divider. The power supplies have internal resistors, while the external pins require outside limiting resistors as described below.

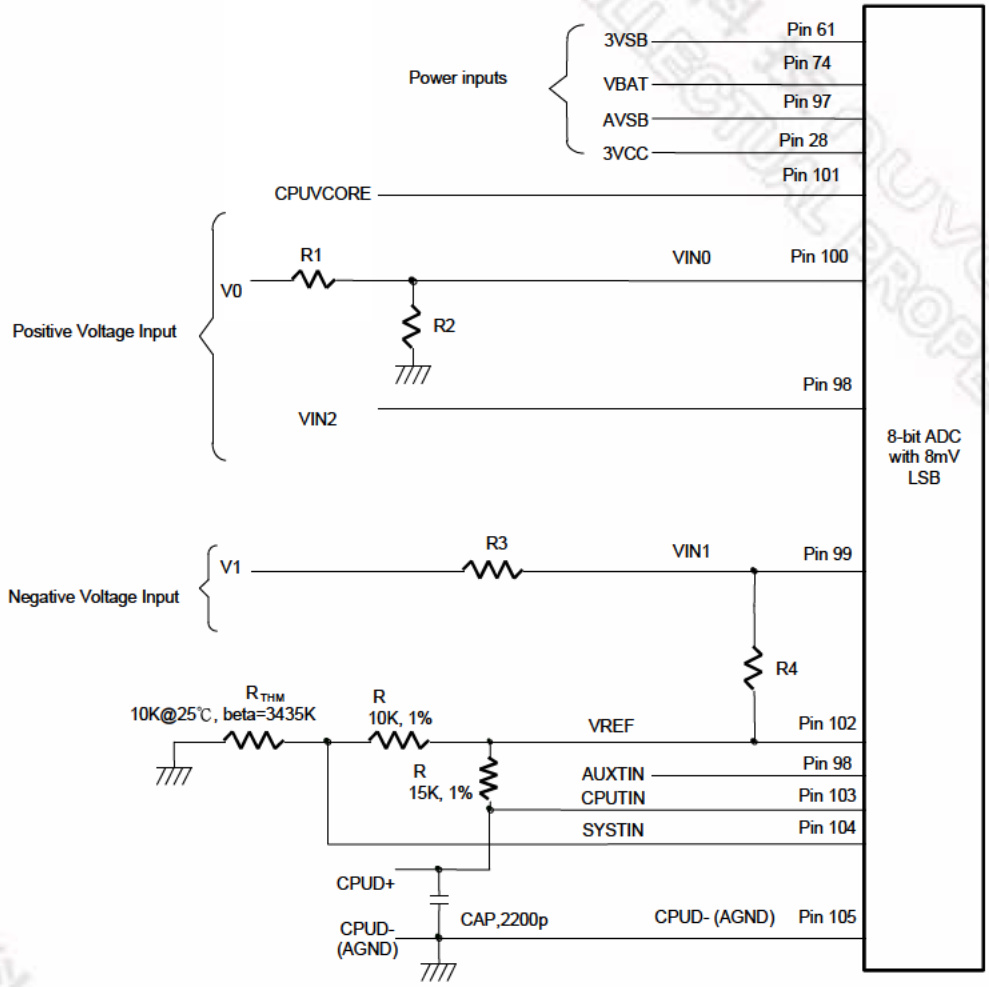

Figure 8-4 Analog Inputs and Application Circuit of the NCT6102D / NCT6106D

As illustrated in the figure above, other connections may require some external circuits. The rest of this section provides more information about voltages outside the range of the 8-bit ADC, CPU Vcore voltage detection, and temperature sensing.

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8.5.1 Voltages Over 2.048 V or Less Than 0 V

Input voltages greater than 2.048 V should be reduced by an external resistor divider to keep the input voltages in the proper range. For example, input voltage V_0 (+12 V) should be reduced before it is connected to VIN0 according to the following equation:

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

R1 and R2 can be set to 56 KΩ and 10 KΩ, respectively, to reduce V_0 from +12 V to less than 2.048 V.

All the internal inputs of the ADC, AVCC, VBAT, 3VSB and 3VCC utilize an integrated voltage divider with both resistors equal to 34KΩ, yielding a voltage one half of the power supply. Since one would expect a worst-case 10% variation or a 3.63V maximum voltage, the input to the ADC will be 1.815V, well within the maximum range.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \cong 1.65V$$, where VCC is set to 3.3V

The CPUVCORE pin feeds directly into the ADC with no voltage divider since the nominal voltage on this pin is only 1.2V.

Negative voltages are handled similarly, though the equation looks a little more complicated. For example, negative voltage V1 (-12V) can be reduced according to the following equation:

$$VIN1 = (V_1 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, where V_1 = -12$$

R3 and R4 can be set to 232 KΩ and 10 KΩ, respectively, to reduce negative input voltage V_1 from –12 V to less than 2.048 V. Note that R4 is referenced to VREF, or 2.048V instead of 0V to allow for more dynamic range. This is simply good analog practice to yield the most precise measurements.

Both of these solutions are illustrated in the figure above.

8.5.2 Voltage Data Format

The data format for voltage detection is an eight-bit value, and each unit represents an interval of 8 mV.

Detected Voltage = Reading * 0.008 V

If the source voltage was reduced by a voltage divider, the detected voltage value must be scaled accordingly.

8.5.2.1. Voltage Reading

NCT6102D / NCT6106D has 8 voltage reading:

	3VCC	AVCC	3VSB	VBAT	
Voltage reading	Bank0, Index03	Bank0, Index02	Bank0, Index07	Bank0, Index08	
	CPUVCORE	**VIN0**	**VIN1**	**VIN2**	
Voltage reading	Bank0, Index00	Bank0, Index01	Bank0, Index04	Bank0, Index05	

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8.5.3 Temperature Data Format

The data format for sensors SYSTIN, CPUTIN and AUXTIN is 9-bit, two's-complement. This is illustrated in the table below. There are two sources of temperature data: external thermistors or thermal diodes.

Table 8-1 Temperature Data Format

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1Ceh
-55°C	1100,1001	C9h	1,1001,0010	192h

8.5.3.1. Monitor Temperature from Thermistor

External thermistors should have a β value of 3435K and a resistance of 10 KΩ at 25°C. As illustrated in the schematic above, the thermistor is connected in series with a 10-KΩ resistor and then connects to VREF. The configuration registers to select a thermistor temperature sensor and the measurement method are found at Bank 3, 18h, and 19h.

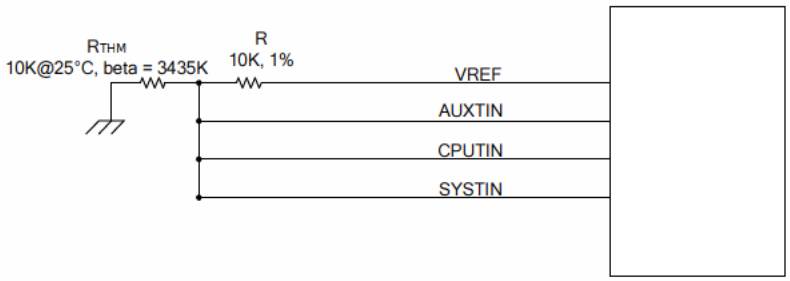

Figure 8-5 Monitoring Temperature from Thermistor

8.5.3.2. Monitor Temperature from Thermal Diode (Voltage Mode)

The thermal diode D- pin is connected to AGND, and the D+ pin is connected to the temperature sensor pin in the NCT6102D / NCT6106D. A 15-KΩ resistor is connected to VREF to supply the bias current for the diode, and the 2200-pF, bypass capacitor is added to filter high-frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 3, index 18h, and 19h.

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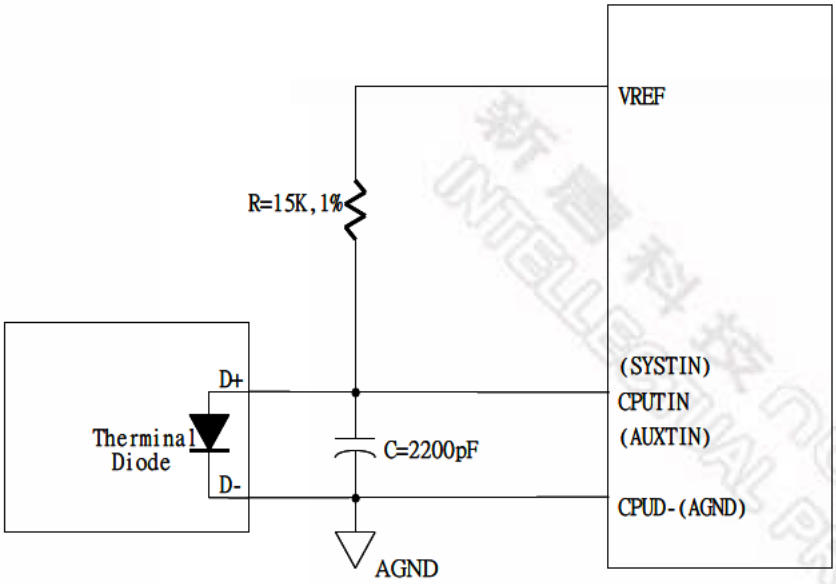

Figure 8-6 Monitoring Temperature from Thermal Diode (Voltage Mode)

8.5.3.3. Monitor Temperature from Thermal Diode (Current Mode)

The NCT6102D / NCT6106D can also sense the diode temperature through Current Mode and the circuit is shown in the following figure.

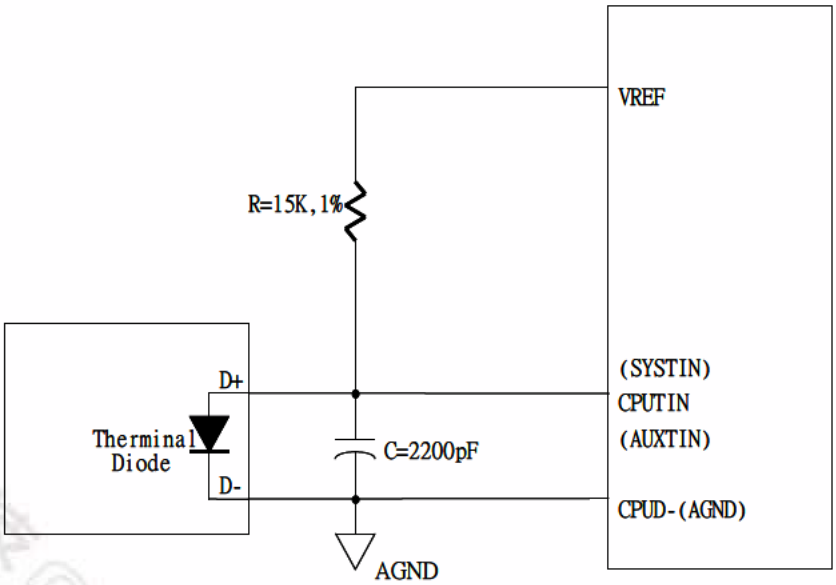

Figure 8-7 Monitoring Temperature from Thermal Diode (Current Mode)

The pin of processor D- is connected to CPUD- and the pin D+ is connected to temperature sensor pin in the NCT6102D / NCT6106D. A bypass capacitor C=2200pF should be added to filter the high frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 3, 18h, and 19h.

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8.5.3.4. Temperature Reading

NCT6102D / NCT6106D has 6 temperature reading can monitor different temperature sources (ex. SYSTIN, CPUTIN, AUXTIN, PECI…etc).

	SMIOVT1	SMIOVT2	SMIOVT3	SMIOVT4	SMIOVT5	SMIOVT6
Temperature source select	Bank0, indexB0 bit[4:0] default: SYSTIN	Bank0, indexB1 bit[4:0] default: CPUTIN	Bank0, indexB2 bit[4:0] default: AUXTIN	Bank0, indexB3 bit[4:0] default: SYSTIN	Bank0, indexB4 bit[4:0] default: SYSTIN	Bank0, indexB5 bit[4:0] default: SYSTIN
Temperature reading (2's complement)	Bank0, index10 & index16 bit0	Bank0, index11 & index16 bit1	Bank0, index12 & index16 bit2	Bank0, index13 & index16 bit3	Bank0, index14 & index16 bit4	Bank0, index15 & index16 bit5

8.6 PECI

PECI (Platform Environment Control Interface) is a new digital interface to read the CPU temperature of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECI uses a single wire for self-clocking and data transfer. By interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECI reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

PECI is one of the temperature sensing methods that the NCT6102D / NCT6106D supports. The NCT6102D / NCT6106D contains a PECI master and reads the CPU PECI temperature. The CPU is a PECI client.

The PECI temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECI temperatures. For further information, refer to the PECI specification. All references to "temperature" in this section are in "counts" instead of "°C".

Figure 8-8 PECI Temperature shows a typical fan speed (PWM duty cycle) and PECI temperature relationship.

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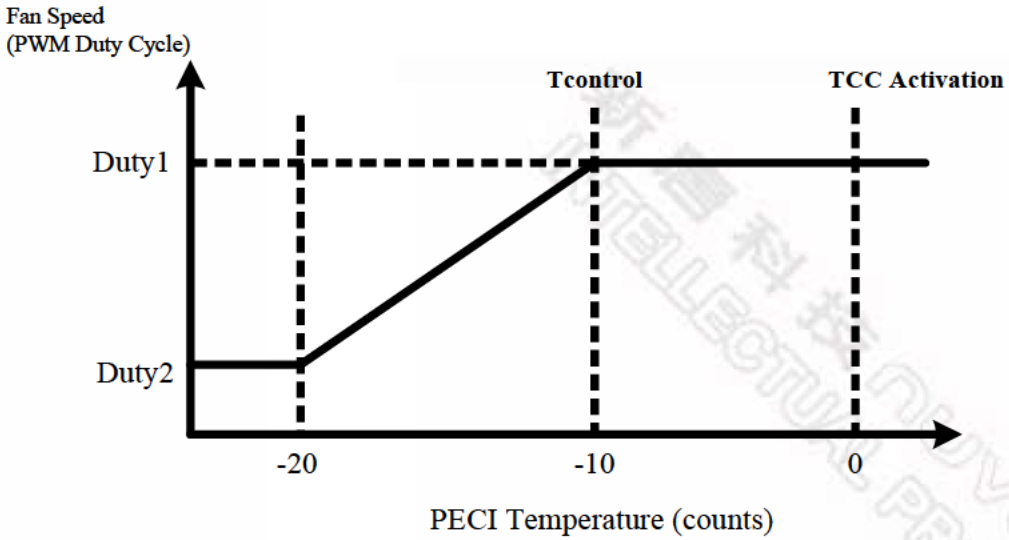

Figure 8-8 PECI Temperature

In this illustration, when PECI temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECI temperature is -10, the PWM duty cycle is at Duty1.

At Tcontrol PECI temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore Duty1 is 100% if this recommendation is followed. The value of Tcontrol can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The Tcontrol MSR address is usually in the BIOS Writer's guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, Tcontrol is -10.

When the PECI temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

NCT6102D / NCT6106D's fan control circuit can only accept positive real-time temperature inputs and limits setting (in Smart Fan ™ mode). The device provides offset registers to 'shift' the negative PECI readings to positive values otherwise the fan control circuit will not function properly. The offset registers are the Tbase registers located at Bank2, Index04h for PECI_BASE0; Bank2, Index05h for PECI_BASE1; separately. All default values of these Tbase registers are 8'h00.These registers should be programmed with (positive) values so that the resultant value (Tbase + PECI) is always positive. The unit of the Tbase register contents is "count" to match that of PECI values. The resultant value (Tbase + PECI) should not be interpreted as the "temperature" (whether in count or °C) of the PECI client (CPU).

Figure 8-9 Temperature and Fan Speed Relation after Tbase Offsetsshows the temperature/fan speed relationship after Tbase offsets are applied (based on Figure 8-8 PECI Temperature). This view is from the perspective of the NCT6102D / NCT6106D fan control circuit.

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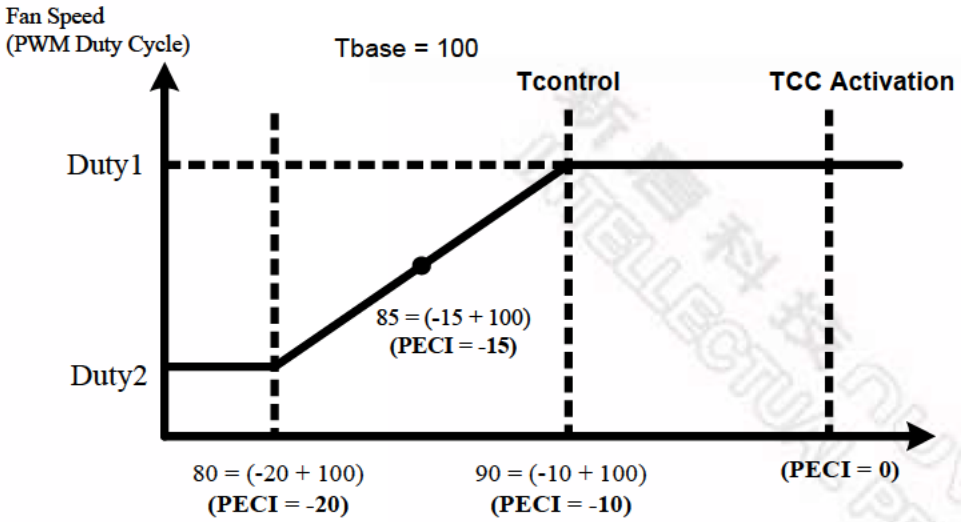

Figure 8-9 Temperature and Fan Speed Relation after Tbase Offsets

Assuming Tbase is set to 100 and the PECI temperature is -15 , the real-time temperature value to the fan control circuit will be 85 (-15 + 100). The value of 55 (hex) will appear in the relevant real-time temperature register.

While using Smart Fan control function of NCT6102D / NCT6106D, BIOS/software must include Tbase in determining the thresholds (limits). In this example, assuming Tcontrol is -10 and Tbase is set to 100 (1), the threshold temperature value corresponding to the "100% fan duty cycle" event is 90 (-10+100). The value of 5A (hex) should be written to the relevant threshold register.

Tcontrol is typically -10 to -20 for PECI-enabled CPUs. Base on that, a value of 85 ~100 for Tbase could be set for proper operation of the fan control circuit. This recommendation is applicable for most designs. In general, the concept presented in this section could be used to determine the optimum value of Tcontrol to match the specific application.

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8.7 Fan Speed Measurement and Control

This section is divided into two parts, one to measure the speed and one to control the speed.

8.7.1 Fan Speed Reading

The fan speed reading is at

	FAN COUNT READING		FAN RPM READING	
	13-bit		16-bit	
	[12:5]	[4:0]	[15:8]	[7:0]
SYSFANIN	Bank0, Index20	Bank0, Index21	Bank0, Index30	Bank0, Index31
CPUFANIN	Bank0, Index22	Bank0, Index23	Bank0, Index32	Bank0, Index33
AUXFANIN	Bank0, Index24	Bank0, Index25	Bank0, Index34	Bank0, Index35

8.7.2 Fan Speed Calculation by Fan Count Reading

In 13-bit fan count reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by the following equation:

$$RPM = \frac{1.35 \times 10^6}{Count}$$

8.7.3 Fan Speed Calculation by Fan RPM Reading

In 16-bit fan RPM reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by translating 16-bit RPM reading from hexadecimal to decimal.

Register reading 0x09C4h = 2500 RPM

8.7.4 Fan Speed Control

The NCT6102D / NCT6106D has three output pins for fan control, each of which offers PWM duty cycle and DC voltage to control the fan speed. The output type (PWM or DC) of each pin is configured by Bank0 index F3h, bits 0 for SYSFANOUT, bits 1 for CPUFANOUT and bit 2 for AUXFANOUT.

Pin14 AUXFANOUT Function Output Enable controls by CR24 bit3 default disable.

	SYSFANOUT	CPUFANOUT	AUXFANOUT
Output Type Select	Bank0, IndexF3 bit0 0: PWM output(default) 1: DC output	Bank0, IndexF3 bit1 0: PWM output (default) 1: DC output	Bank0, IndexF3 bit2 0: PWM output (default) 1: DC output
Output Type Select (in PWM output)	CR24 bit6 0: open-drain (default)	CR24 bit5 0: open-drain (default)	CR24 bit4 0: open-drain (default)

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		1: push-pull	1: push-pull	1: push-pull
PWM Output Freqency		Bank0, IndexF0	Bank0, IndexF1	Bank0, IndexF2
Fan Control Mode Select		Bank1, Index13, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank1, Index23, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank1, Index33, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV
Output Value (write)	**PWM output (Duty)**	Bank1, Index19 bit[7:0]	Bank1, Index29 bit[7:0]	Bank1, Index39 bit[7:0]
	DC output (Voltage)	Bank1, Index19 bit[7:2]	Bank1, Index29 bit[7:2]	Bank1, Index39 bit[7:2]
Current Output Value (read)		Bank0, Index4A	Bank0, Index4B	Bank0, Index4C

For PWM, the duty cycle is programmed by eight-bit registers at Bank1 Index 19h for SYSFANOUT, Bank1 Index 29h for CPUFANOUT and Bank1 Index 39h for AUXFANOUT. The duty cycle can be calculated using the following equation:

$$\text{Duty cycle}(\%) = \frac{\text{Programmed 8-bit Register Value}}{255} \times 100\%$$

The default duty cycle is FFh, or 100%. The PWM clock frequency is programmed at Bank0 Index 4Ah, Index 4Bh, and Index 4Ch.

For DC, the NCT6102D / NCT6106D has a six bit digital-to-analog converter (DAC) that produces 0 to 2.048 Volts DC. The analog output is programmed at Bank1 Index 19h bit[7:2] for SYSFANOUT, Bank1 Index 29h bit[7:2] for CPUFANOUT and Bank1 Index 39h bit[7:2] for AUXFANOUT. The analog output can be calculated using the following equation:

$$\text{OUTPUT Voltage (V)} = Vref \times \frac{\text{Programmed 6-bit Register Value}}{64}$$

The default value is 111111YY, or nearly 2.048 V, and Y is a reserved bit.

8.7.5 SMART FAN™ Control

The NCT6102D / NCT6106D supports various different fan control features:

- SMART FAN™ I (Thermal Cruise & Speed Cruise)
- SMART FAN™ IV
- Close-Loop Fan Control RPM mode

	SYSFANOUT	CPUFANOUT	AUXFANOUT
Fan Control Mode Select	Bank1, Index13, bit[7:4] 0h: Manual mode (def.)	Bank1, Index23, bit[7:4] 0h: Manual mode(def.)	Bank1, Index33, bit[7:4] 0h: Manual mode (def.)

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	1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN™ IV	1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN™ IV	1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN™ IV

8.7.6 Temperature Source & Reading for Fan Control

Select temperature source for each fan control output:

	SYSFANOUT	CPUFANOUT	AUXFANOUT
Fan Control Temperature Source Select	Bank1, Index10 bit[4:0] Default: SYSTIN	Bank1, Index20 bit[4:0] Default: CPUTIN	Bank1, Index30 bit[4:0] Default: AUXTIN
Fan Control Temperature Reading	Bank0, Index18 & Bank0, Index1B bit0	Bank0, Index19 & Bank0, Index1B bit1	Bank0, Index1A & Bank0, Index1B bit2
Close-Loop Fan Control RPM mode	Bank1, Index1E bit0	Bank1, Index2E bit0	Bank1, Index3E bit0

8.8 SMART FAN™ I

8.8.1 Thermal Cruise Mode

Thermal Cruise mode controls the fan speed to keep the temperature in a specified range. First, this range is defined in BIOS by a temperature and the interval (e.g., 55 °C ± 3 °C). As long as the current temperature remains below the low end of this range (i.e., 52 °C), the fan is off. Once the temperature exceeds the low end, the fan turns on at a speed defined in BIOS (e.g., 20% output). Thermal Cruise mode then controls the fan output according to the current temperature. Three conditions may occur:

(1) If the temperature still exceeds the high end, fan output increases slowly. If the fan is operating at full speed but the temperature still exceeds the high end, a warning message is issued to protect the system.

(2) If the temperature falls below the high end (e.g., 58°C) but remains above the low end (e.g., 52 °C), fan output remains the same.

(3) If the temperature falls below the low end (e.g., 52 °C), fan output decreases slowly to zero or to a specified "stop value".

This "stop value enable" is enabled by the Bank1, Index10h, Bit7 for SYSFANOUT; Bank1, Index20h, Bit7 for CPUFANOUT and Bank1, Index30h, Bit7 for AUXFANOUT.

The "stop value" itself is separately specified in Bank1 Index16h, Bank1 Index26h and Bank1 Index36h.

The "stop time" means fan remains at the stop value for the period of time also separately defined in Bank1 Index18h, Bank1 Index28h and Bank1 Index38h.

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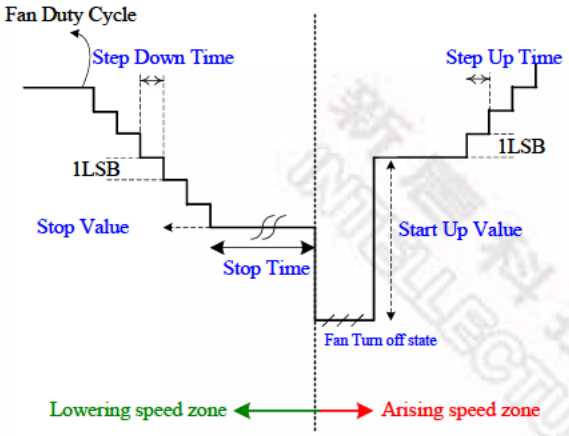

Figure 8-10 Thermal Cruise™ Mode Parameters Figure

In general, Thermal Cruise mode means

- If the current temperature is higher than the high end, increase the fan speed.
- If the current temperature is lower than the low end, decrease the fan speed.
- Otherwise, keep the fan speed the same.

The following figures illustrate two examples of Thermal Cruise mode.

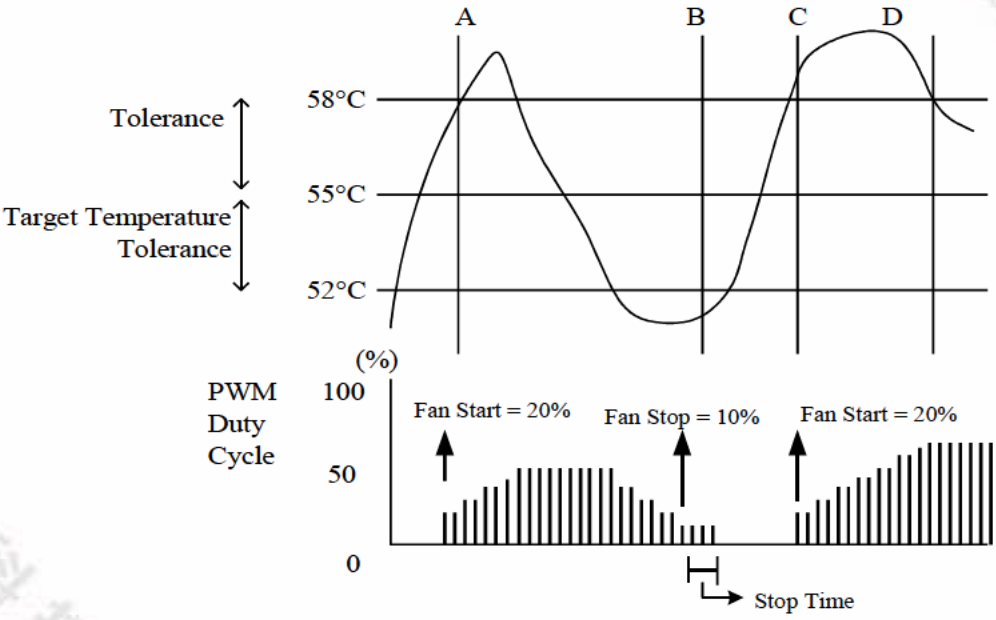

Figure 8-11 Mechanism of Thermal Cruise™ Mode (PWN Duty Cycle)

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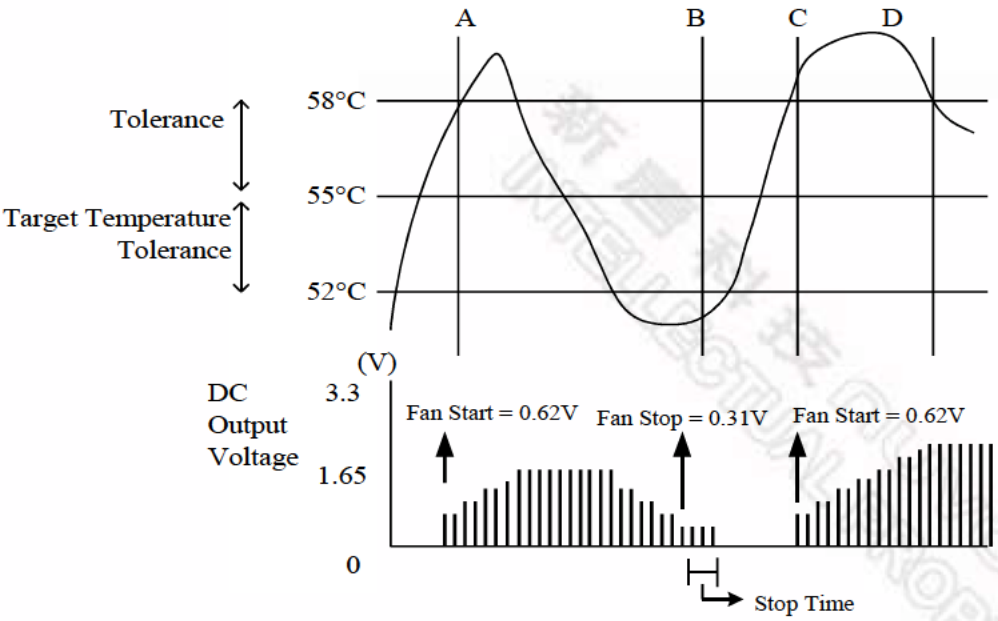

Figure 8-12 Mechanism of Thermal Cruise™ Mode (DC Output Voltage)

8.8.2 Speed Cruise Mode

Speed Cruise mode keeps the fan speed in a specified range. First, this range is defined in BIOS by a fan speed count (the amount of time between clock input signals, not the number of clock input signals in a period of time) and an interval (e.g., 160 ± 10). As long as the fan speed count is in the specified range, fan output remains the same. If the fan speed count is higher than the high end (e.g., 170), fan output increases to make the count lower. If the fan speed count is lower than the low end (e.g., 150), fan output decreases to make the count higher. One example is illustrated in this figure.

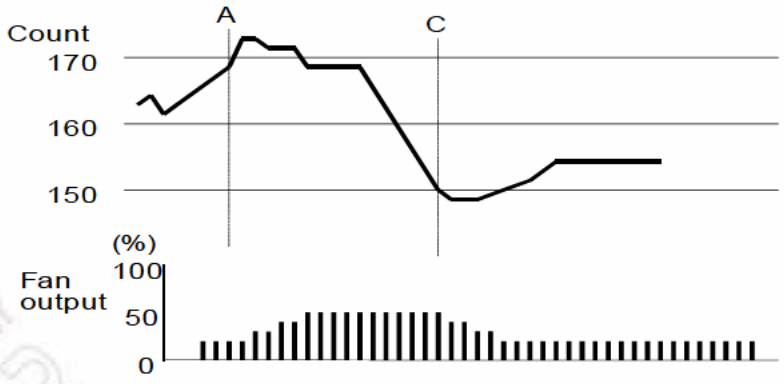

Figure 8-13 Mechanism of Fan Speed Cruise™ Mode

The following tables show current temperatures, fan output values and the relative control registers at Thermal Cruise and Fan Speed mode.

Table 8-2 Display Registers – at SMART FAN™ I Mode

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DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Current SYSFANOUT Temperature	Bank0, Index18h, Index1Bh bit0	SYSFAN MUX Temperature Sensor (default: SYSTIN)	Read only	Index 18h, unit 1°C Index 1Bh, bit 0, unit 0.5 °C
Current CPUFANOUT Temperature	Bank0, Index19h, Index1Bh bit1	CPUFAN MUX Temperature Sensor (default: CPUTIN)	Read only	Index 19h, unit 1°C Index 1Bh, bit 1, unit 0.5 °C
Current AUXFANOUT Temperature	Bank0, Index1Ah, Index1Bh bit2	AUXFAN MUX Temperature Sensor (default: AUXTIN)	Read only	Index 1Ah, unit 1°C Index 1Bh, bit 2, unit 0.5 °C
Current SYSFANOUT Output Value	Bank0, Index 4Ah	SYSFANOUT Output Value Select	Read only	
Current CPUFANOUT Output Value	Bank0, Index 4Bh	CPUFANOUT Output Value Select	Read only	
Current AUXFANOUT Output Value	Bank0, Index 4Ch	AUXFANOUT Output Value Select	Read only	

Table 8-3 Relative Registers – at Thermal Cruise™ Mode

THERMAL CRUISE MODE	CRITICAL TEMPERATURE	STEP- UP TIME	STEP- DOWN TIME	ENABLE THERMAL CRUISE MODE	ENABLE CRITICAL DUTY	CRITICAL DUTY
SYSFANOUT	Bank 1, Index 1Ah	Bank 1, Index 14h	Bank 1, Index 15h	Bank 1, Index 13h,bit[7:4] = 01h	Bank 1, Index 1Ch, bit4	Bank 1, Index 1Dh
CPUFANOUT	Bank 1, Index 2Ah	Bank 1, Index 24h	Bank 1, Index 25h	Bank 1, Index 23h,bit[7:4] = 01h	Bank 1, Index 2Ch, bit4	Bank 1, Index 2Dh
AUXFANOUT	Bank 1, Index 3Ah	Bank 1, Index 34h	Bank 1, Index 35h	Bank 1, Index 33h,bit[7:4] = 01h	Bank 1, Index 3Ch, bit4	Bank 1, Index 3Dh

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THERMAL CRUISE MODE	TARGET TEMPERATURE	TOLERANCE	KEEP MIN. FAN OUTPUT VALUE	STOP VALUE	START-UP VALUE	STOP TIME
SYSFANOUT	Bank 1, Index 11h	Bank 1, Index 13h,Bit[2:0]	Bank 1, Index 10h, bit7	Bank 1, index 16h	Bank 1, index 17h	Bank 1, index 18h
CPUFANOUT	Bank 1, Index 21h	Bank 1, Index 23h,Bit[2:0]	Bank 1, Index 20h, bit7	Bank 1, index 26h	Bank 1, index 27h	Bank 1, index 28h
AUXFANOUT	Bank 1, Index 31h	Bank 1, Index 33h,Bit[2:0]	Bank 1, Index 30h, bit7	Bank 1, index 36h	Bank 1, index 37h	Bank 1, index 38h

Table 8-4 Relative Registers – at Speed Cruise™ Mode

SPEED CRUISE MODE	CRITICAL TEMPERATURE	STEP- UP TIME	STEP- DOWN TIME	ENABLE THERMAL CRUISE MODE	ENABLE CRITICAL DUTY	CRITICAL DUTY
SYSFANOUT	Bank 1, Index 1Ah	Bank 1, Index 14h	Bank 1, Index 15h	Bank 1, Index 13h,bit[7:4] = 02h	Bank 1, Index 1Ch, bit4	Bank 1, Index 1Dh
CPUFANOUT	Bank 1, Index 2Ah	Bank 1, Index 24h	Bank 1, Index 25h	Bank 1, Index 23h,bit[7:4] = 02h	Bank 1, Index 2Ch, bit4	Bank 1, Index 2Dh
AUXFANOUT	Bank 1, Index 3Ah	Bank 1, Index 34h	Bank 1, Index 35h	Bank 1, Index 33h,bit[7:4] = 02h	Bank 1, Index 3Ch, bit4	Bank 1, Index 3Dh

SPEED CRUISE MODE	TARGET-SPEED COUNT_L	TARGET-SPEED COUNT_H	TOLERANCE_L	TOLERANCE_H
SYSFANOUT	Bank 1, Index 11h	Bank 1, Index 12,bit[3:0]	Bank 1, Index 13h,Bit[2:0]	Bank 1, Index 12,bit[6:4]
CPUFANOUT	Bank 1, Index 21h	Bank 1, Index 22,bit[3:0]	Bank 1, Index 23h,Bit[2:0]	Bank 1, Index 22,bit[6:4]
AUXFANOUT	Bank 1, Index 31h	Bank 1, Index 32,bit[3:0]	Bank 1, Index 33h,Bit[2:0]	Bank 1, Index 32,bit[6:4]

8.9 SMART FAN™ IV & Close Loop Fan Control RPM Mode

SMART FAN™ IV and Close Loop Fan Control RPM Mode offer 3 slopes to control the fan speed.

Set **Critical Temperature, Bank1 Address $1A_{HEX}$, Bank1 Address $2A_{HEX}$, Bank1 Address $3A_{HEX}$**

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- Set the **Relative Register-at SMART FAN™ IV Control Mode Table**
  If fan control mode is set as Close Loop Fan Control, the unit step is 50 RPM. So the maximum controllable RPM is 50*255=12,750 rpm.
  If for High Speed Fan Control at RPM Mode, Set **RPM_High of Bank1 Address $1F_{HEX}$ bit[7]. Address $2F_{HEX}$ bit[7]. Address $3F_{HEX}$ bit[7].**
  the unit is 100 RPM, Support 100 rpm ~ 25500 rpm.
- Set **Hysteresis of Temperature, Bank1 Address 13_{HEX} bit[2:0] . Bank1 Address 23_{HEX} bit[2:0]. Bank1 Address 33_{HEX} bit[2:0].**

The 3 slopes can be obtained by setting FanDuty1/RPM1~FanDuty4/RPM4 and T1~T4 through the registers. When the temperature rises, FAN Output will calculate the target FanDuty/RPM based on the current slope. For example, assuming Tx is the current temperature and Ty is the target, then

The slope:

$$X2 = \frac{(FanDuty3 / RPM3) - (FanDuty2 / RPM2)}{(T3 - T2)}$$

Fan Output:

$$Target\ FanDuty\ or\ RPM = (FanDuty2\ or\ RPM2) + (Tx - T2) \cdot X2$$

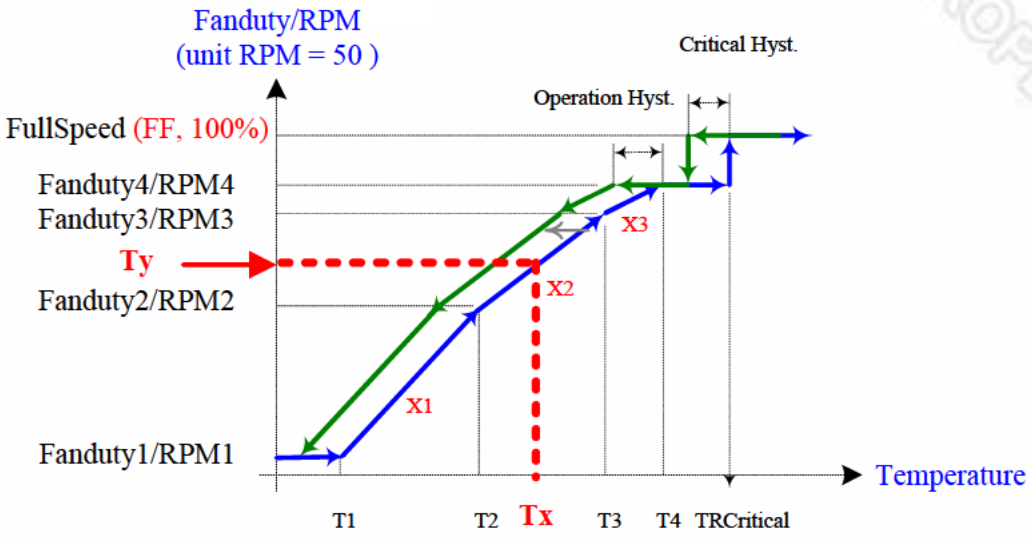

Figure 8-14 SMART FAN™ IV & Close Loop Fan Control Mechanism

Table 8-5 Relative Register-at SMART FAN™ IV Control Mode

DESCRIPTION	T1	T2	T3	T4
SYSFANOUT	Bank 1, Index 60h	Bank 1, Index 61h	Bank 1, Index 62h	Bank 1, Index 63h
CPUFANOUT	Bank 1, Index 70h	Bank 1, Index 71h	Bank 1, Index 72h	Bank 1, Index 73h
AUXFANOUT	Bank 1, Index 80h	Bank 1, Index 81h	Bank 1, Index 82h	Bank 1, Index 83h

DESCRIPTION	FD1/RPM1	FD2/RPM2	FD3/RPM3	FD4/RPM4
SYSFANOUT	Bank 1,	Bank 1,	Bank 1,	Bank 1,

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	Index 64h	Index 65h	Index 66h	Index 67h
CPUFANOUT	Bank 1, Index 74h	Bank 1, Index 75h	Bank 1, Index 76h	Bank 1, Index 77h
AUXFANOUT	Bank 1, Index 84h	Bank 1, Index 85h	Bank 1, Index 86h	Bank 1, Index 87h

DESCRIPTION	STEP- UP TIME	STEP-DOWN TIME	ENABLE SMART IV MODE	ENABLE FANOUT STEP	ENABLE CRITICAL DUTY	CRITICAL DUTY
SYSFANOUT	Bank 1, Index 14h	Bank 1, Index 15h	Bank 1, Index 13h,bit[7:4] = 04h	Bank 1, Index 1Ch, bit0	Bank 1, Index 1Ch, bit4	Bank 1, Index 1Dh
CPUFANOUT	Bank 1, Index 24h	Bank 1, Index 25h	Bank 1, Index 23h,bit[7:4] = 04h	Bank 1, Index 2Ch, bit0	Bank 1, Index 2Ch, bit4	Bank 1, Index 2Dh
AUXFANOUT	Bank 1, Index 34h	Bank 1, Index 35h	Bank 1, Index 33h,bit[7:4] = 04h	Bank 1, Index 3Ch, bit0	Bank 1, Index 3Ch, bit4	Bank 1, Index 3Dh

DESCRIPTION	CRITICAL TEMPERATURE	CRITICAL TOLERANCE	TEMPERATURE TOLERANCE	ENABLE RPM MODE	RPM TOLERANCE	ENABLE RPM HIGH MODE
SYSFANOUT	Bank 1, Index 1Ah	Bank 1, Index 1Bh, bit[2:0]	Bank1, Index 13h, bit[2:0]	Bank 1, Index 1Eh, bit0	Bank1, Index 1Fh, bit[3:0]	Bank 1, Index 1Fh, bit7
CPUFANOUT	Bank 1, Index 2Ah	Bank 1, Index 2Bh, bit[2:0]	Bank1, Index 23h, bit[2:0]	Bank 1, Index 2Eh, bit0	Bank1, Index 2Fh, bit[3:0]	Bank 1, Index 2Fh, bit7
AUXFANOUT	Bank 1, Index 3Ah	Bank 1, Index 3Bh, bit[2:0]	Bank1, Index 33h, bit[2:0]	Bank 1, Index 3Eh, bit0	Bank1, Index 3Fh, bit[3:0]	Bank 1, Index 3Fh, bit7

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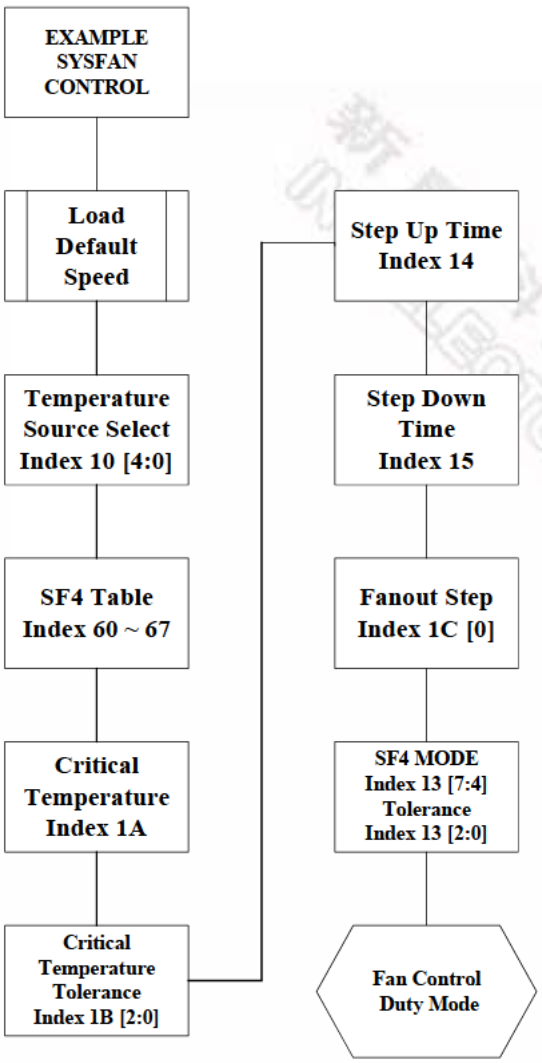

Figure 8-15 Fan Control Duty Mode Programming Flow

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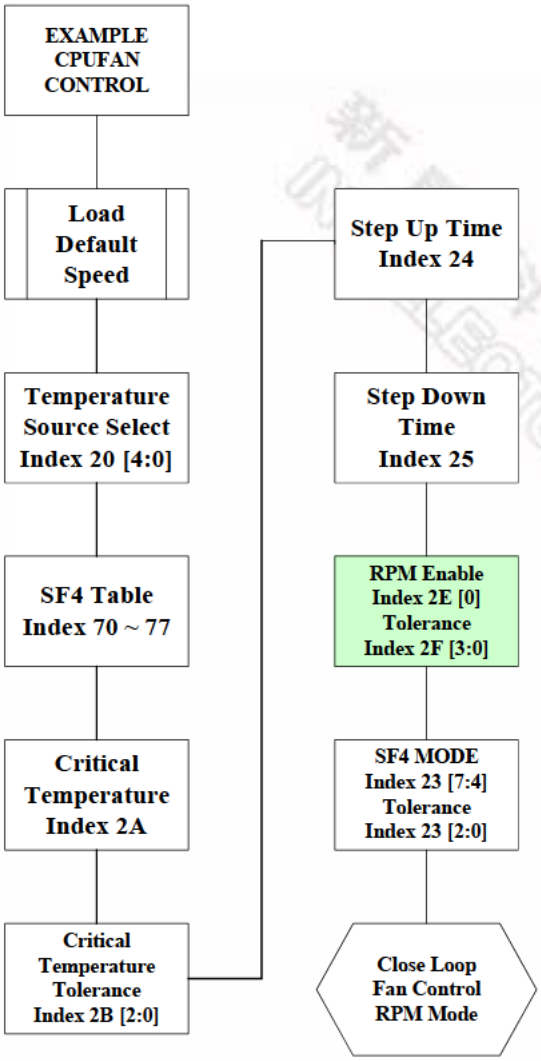

Figure 8-16 Close-Loop Fan Control RPM Mode Programming Flow

8.9.1 Step Up Time / Step Down Time

SMART FAN™ IV is designed for the smooth operation of the fan. The Up Time / Down Time register defines the time interval between successive duty increases or decreases. If this value is set too small, the fan will not have enough time to speed up after tuning the duty and sometimes may result in unstable fan speed.
On the otherhand, if Up Time / Down Time is set too large, the fan may not work fast enough to dissipate the heat. This register should never be set to 0, otherwise, the fan duty will be abnormal.

8.9.2 Fan Output Step

The "Fanout Step" itself is separately specified in Bank1 Index1Ch bit0 for SYSFANOUT, Index2Ch bit0 for CPUFANOUT and Index3Ch bit0 for AUXFANOUT.

This example for Fanout Step exposition:

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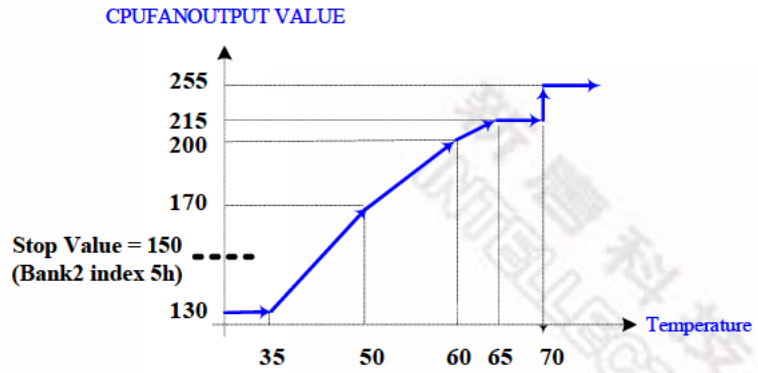

Figure 8-17 CPUFAN SMART FAN™ IV Table Parameters Figure

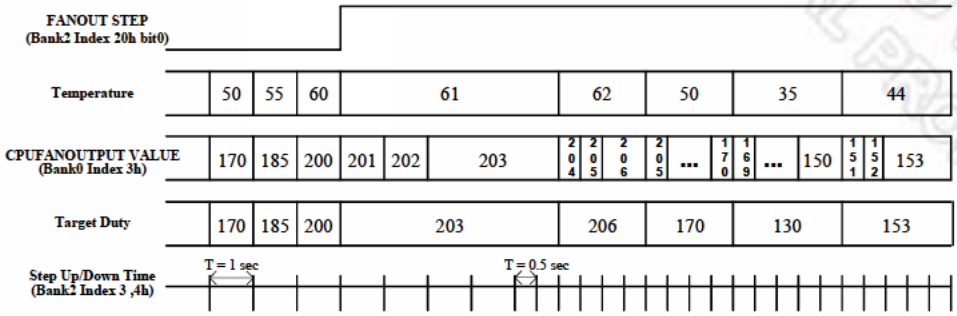

Figure 8-18 Fanout Step Relation of CPUFANOUT

8.9.3 Revolution Pulse Selection

The NCT6102D / NCT6106D supports four RPM output of the pulses selection function for different type of FAN which has the character of different pulses per revolution.The others could be set by HM register at Bank0, IndexF6, Bit1-0 for SYSFANIN; Bank0, IndexF6, Bit3-2 for CPUFANIN and Bank0, IndexF6, Bit5-4 for AUXFANIN. All default value of pulse selection registers are 2 pulses of one revolution.

Setting description for "Pulse Selections Bits":

00: 4 pulses per revolution
01: 1 pulse per revolution
10: 2 pulses per revolution (default)
11: 3 pulses per revolution

8.9.4 Weight Value Control

The NCT6102D / NCT6106D supports weight value control for fan duty output. By register configuration, the results of weight value circuit can be added to the fan duty of Thermal Cruise Mode or SMART FAN™ IV Duty Mode and output to the fan. Take CPUFANOUT for example, if SMART FAN™ IV is selected, CPUTIN is the temperature source, and weight value control is enabled, SMART FAN™ IV will calculate the output duty, and weight value circuit will calculate the corresponding weight value based on SYSTIN. As the SYSTIN temperature rises, its corresponding weight value increases. Then, the two values will be summed up and output to CPU fan. In other words, the CPU fan duty is affected not only by the CPUTIN but also the SYSTIN temperature.

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Figure 8-19 SYS TEMP and Weight Value Relations shows the relation between the SYSTIN temperature and the weight value. Tolerance setup is offered on each change point to avoid weight value fluctuation resulted from SYSTIN temperature change. The weight value will increase by one weight value step only when the SYSTIN temperature is higher than the point value plus tolerance. Likewise, the weight value decreases by one weight value step only when the SYSTIN temperature is lower than the point value minus tolerance.

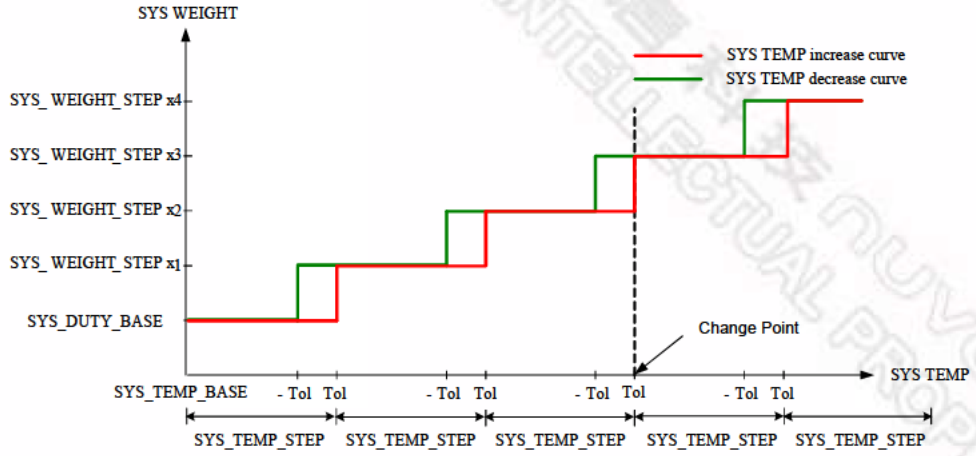

Figure 8-19 SYS TEMP and Weight Value Relations

Table 8-6 Relative Register-at Weight Value Control

DESCRIPTION	ENABLE WEIGHT MODE	WEIGHT TEMPERATURE SOURCE SELECT
SYSFANOUT	Bank 1, Index 68h, bit7	Bank 1, Index 68h, bit[4:0]
CPUFANOUT	Bank 1, Index 78h, bit7	Bank 1, Index 78h, bit[4:0]
AUXFANOUT	Bank 1, Index 88h, bit7	Bank 1, Index 88h, bit[4:0]

DESCRIPTION	TEMP STEP	TEMP STEP TOLERANCE	WEIGHT STEP	TEMP BASE	DUTY BASE
SYSFANOUT	Bank 1, Index 69h	Bank 1, Index 6Ah	Bank 1, Index 6Bh	Bank 1, Index 6Ch	Bank 1, Index 6Dh
CPUFANOUT	Bank 1, Index 79h	Bank 1, Index 7Ah	Bank 1, Index 7Bh	Bank 1, Index 7Ch	Bank 1, Index 7Dh
AUXFANOUT	Bank 1, Index 89h	Bank 1, Index 8Ah	Bank 1, Index 8Bh	Bank 1, Index 8Ch	Bank 1, Index 8Dh

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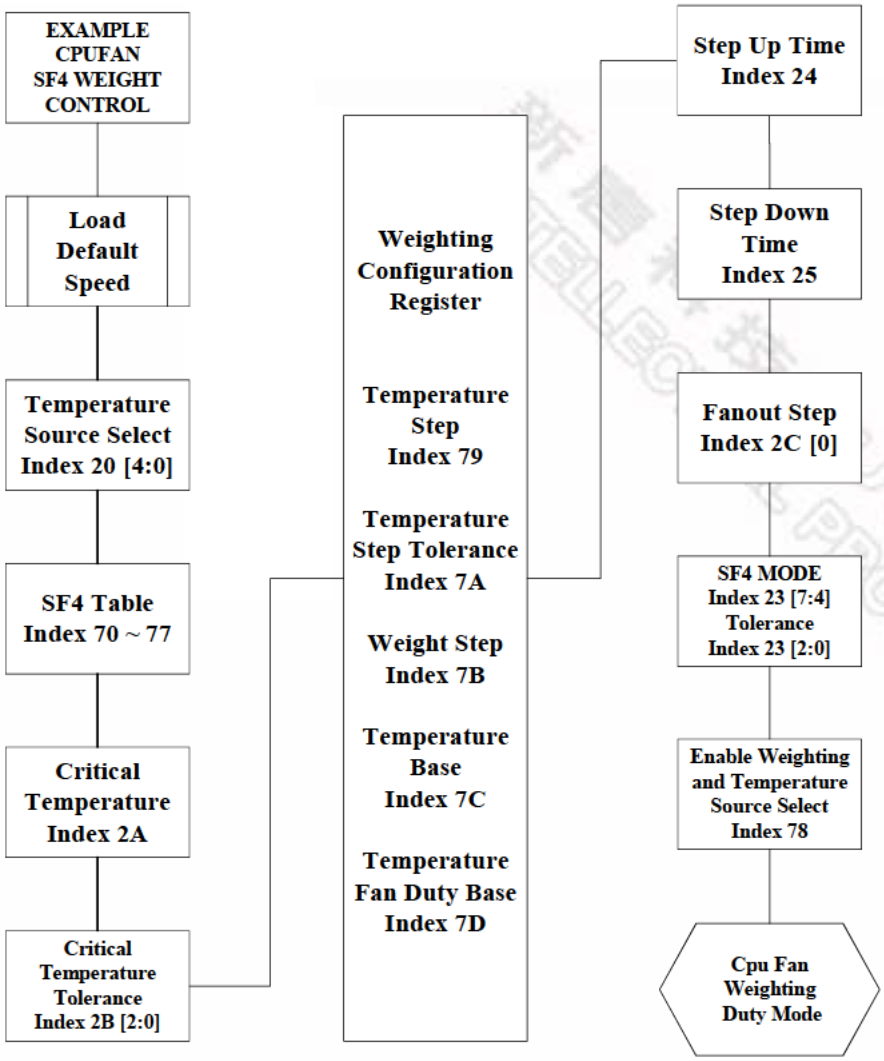

Figure 8-20 Weighting Duty Mode Programming Flow

8.10 Alert and Interrupt

NCT6102D / NCT6106D supports 6 Temperature Sensors for interrupt detection depending on selective monitor temperature source.

	SMIOVT1	SMIOVT2	SMIOVT3	SMIOVT4	SMIOVT5	SMIOVT6
Temperature source select	Bank0, indexB0 bit[4:0] default: SYSTIN	Bank0 indexB1 bit[4:0] default: CPUTIN	Bank0, indexB2 bit[4:0] default: AUXTIN	Bank0, indexB3 bit[4:0] default: SYSTIN	Bank0, indexB4 bit[4:0] default: SYSTIN	Bank0, indexB5 bit[4:0] default: SYSTIN
Temperature reading (2's	Bank0, index10 &	Bank0, index11 &	Bank0, index12 &	Bank0, index13 &	Bank0, index14 &	Bank0, index15 &

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complement)	index16 bit0	index16 bit1	index16 bit2	index16 bit3	index16 bit4	index16 bit5
Temperature High Limit	Bank0, indexC2 & indexB7 bit6	Bank0, indexC6 & indexB8 bit6	Bank0, indexCA & indexB9 bit6	Bank0, indexCE & indexBA bit6	Bank0, indexD2 & indexBB bit6	Bank0, indexD6 & indexBC bit6
Temperature Low Limit	Bank0, indexB7 & index56 bit7	Bank1, indexC7 & indexB8 bit7	Bank2, indexCB & indexB9 bit7	Bank6, indexCF & indexBA bit0	Bank6, indexD3 & indexBB bit0	Bank6, indexD7 & indexBC bit0

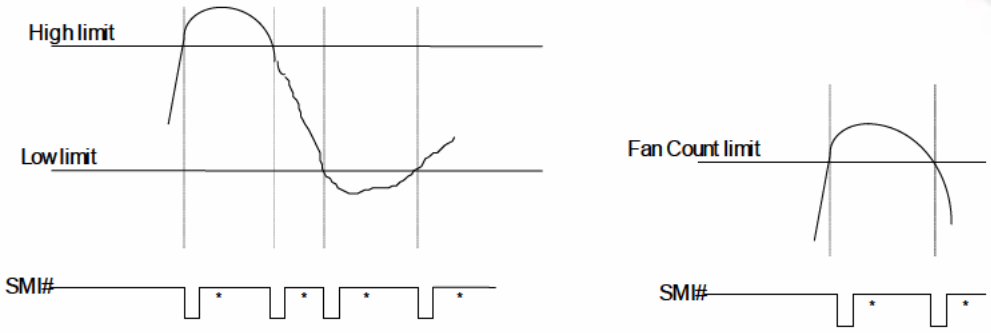
SMIOVT Relative Temperature Registers

8.10.1 SMI# Interrupt Mode

The SMI#/OVT# pin (pin.95) is a multi-function pin. It can be in HM_SMI# mode or in OVT# mode by setting Configuration Register CR29h, bit 6 to one or zero, respectively. In HM_SMI# mode, it can monitor voltages, fan counts, or temperatures.

8.10.2 Voltage SMI# Mode

The SMI# pin can create an interrupt if a voltage exceeds a specified high limit or falls below a specified low limit. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

Figure 8-21 SMI Mode of Voltage and Fan Inputs

8.10.3 Fan SMI# Mode

The SMI# pin can create an interrupt if a fan count crosses a specified fan limit (rises above it or falls below it). This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the figure above.

8.10.4 Temperature SMI# Mode

The SMI# pin can create interrupts that depend on the temperatures measured by SYSTIN, CPUTIN, and AUXTIN. These interrupts are divided into two parts, one for SYSTIN and the other for CPUTIN / AUXTIN.

8.10.4.1. Temperature Sensor 1 SMI# Interrupt (Default: SYSTIN)

The SMI# pin has five interrupt modes with Temperature Sensor 1.

(1) Shut-down Interrupt Mode

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This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_{OL} and setting Bank0 Index 40h, bit 4 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

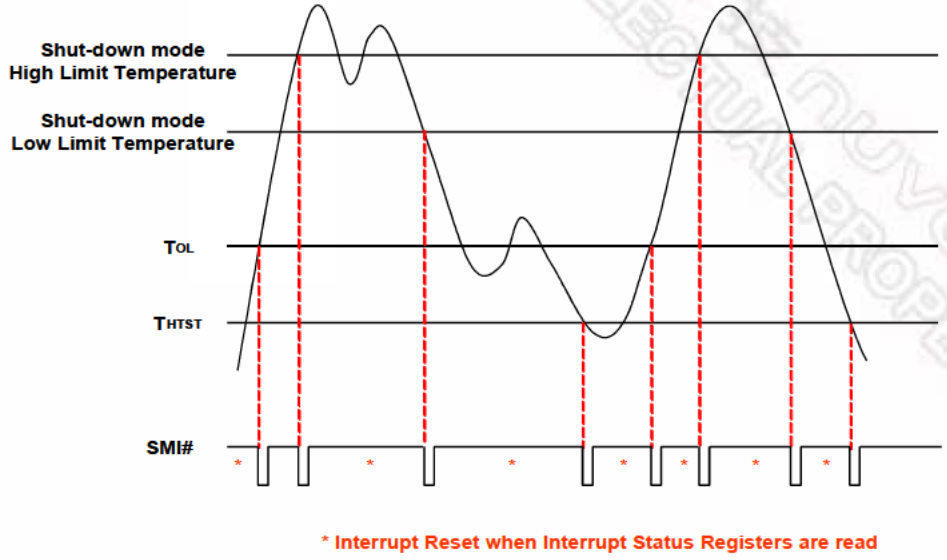
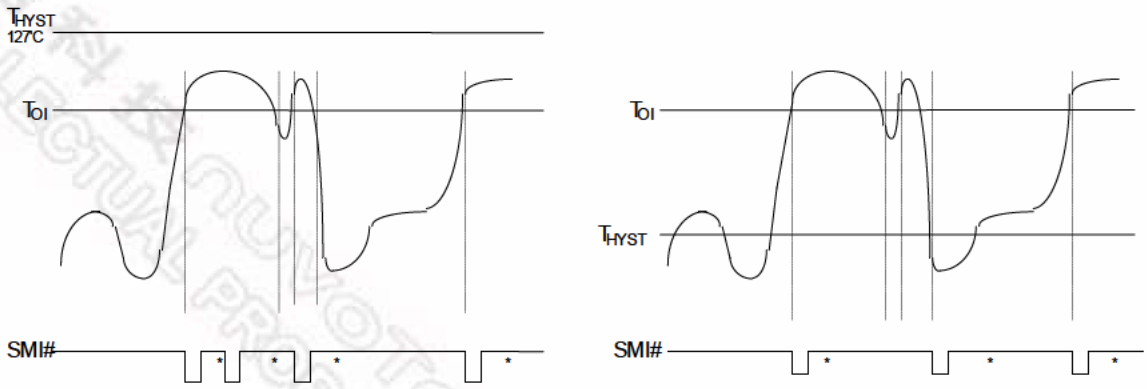


Figure 8-22 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) to 127°C.

In this mode, the SMI# pin can create an interrupt as long as the current temperature exceeds T_O (Over Temperature). This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. If the interrupt is reset, the SMI# pin continues to create interrupts until the temperature goes below T_O. This is illustrated in the figure below.



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Comparator Interrupt Mode Two-Times Interrupt Mode

Figure 8-23 SMI Mode of SYSTIN I

(3) Two-Times Interrupt Mode

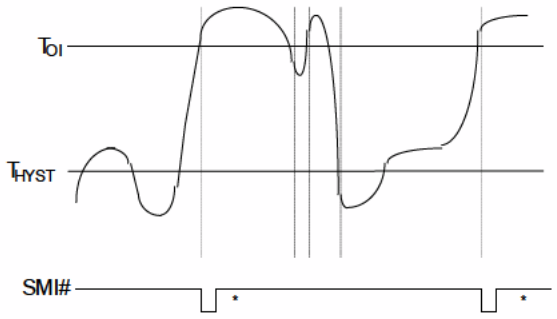
This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index B6h, bit1 to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

(4) One-Time Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index B6h, bit1 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

One-Time Interrupt Mode

Figure 8-24 SMI Mode of SYSTIN II

8.10.4.2. SMI# Interrupt of Temperature Sensor 2 (Default: CPUTIN) and Temperature Sensor 3 (Default: AUXTIN) and Temperature Sensor 4 (Default: SYSTIN) and Temperature Sensor 5 (Default: SYSTIN) and Temperature Sensor 6 (Default: SYSTIN)

The SMI# pin has 5 interrupt modes with Temperature Sensor 2~6.

(1) Shut-down Interrupt Mode

This mode is enabled by setting Bank0 Index B6h, bit 2 to zero and Bank0 Index B8h, bit2 to one for Temperature Sensor 2; Bank0 Index B9h, bit2 to one for Temperature Sensor 3; Bank0 Index BAh, bit2 to one for Temperature Sensor 4; Bank0 Index BBh, bit2 to one for Temperature Sensor 5 and Bank0 Index BCh, bit2 to one for Temperature Sensor 6.

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In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

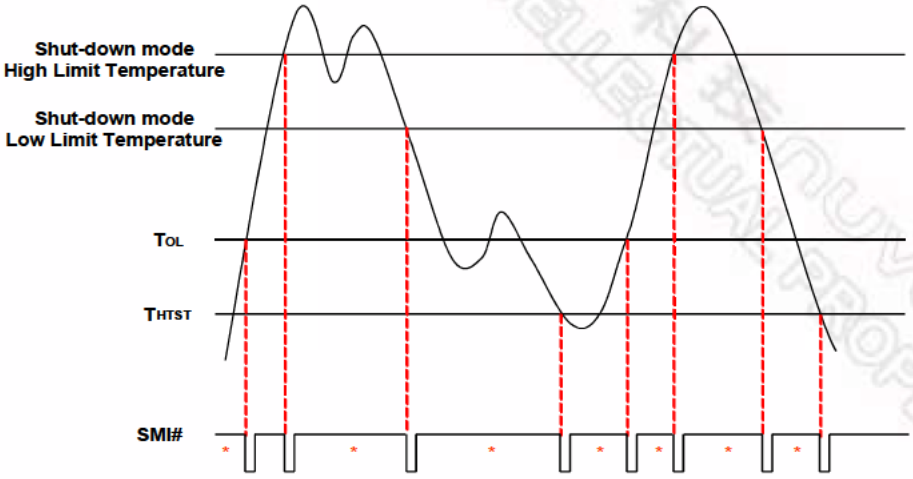
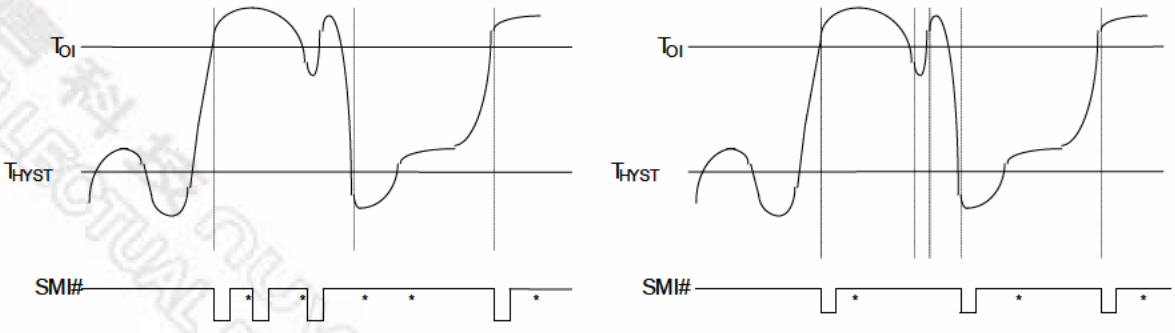


Figure 8-25 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting Bank0 Index B6h, bit 2, to one.

In this mode, the SMI# pin can create an interrupt when the current temperature exceeds T_O (Over Temperature) and continues to create interrupts until the temperature falls below T_{HYST}. This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure below.



Comparator Interrupt Mode Two-Times Interrupt Mode

Figure 8-26 SMI Mode of CPUTIN

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(3) Two-Times Interrupt Mode

This mode is enabled by setting Bank0 Index B6h, bit 2, to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

Table 8-7 Relative Register of SMI functions

	SHUTDOWN MODE	COMPARATOR MODE	TWO-TIME INTERRUPT MODE	ONE-TIME INTERRUPT MODE
SMIOVT1	Bank0,IndexB7_Bit2 (EN_WS=1) Bank0,Index82 _Bit0(TIN=0) Bank0,Index83 _Bit0 (Shut = 0)	Bank0,Index82_Bit0 (TIN=0) Bank0,IndexC3 (Thyst = 8'h7F)	Bank0,Index82_Bit0 (TIN=0) Bank0,IndexB6_Bit1 (EN_T1_One = 0)	Bank0,Index82_ Bit0 (TIN=0) Bank0,IndexB6_ Bit1 (EN_T1_One= 1)
SMIOVT2	Bank0,IndexB8_Bit2 (EN_WS=1) Bank0,Index82_ Bit1(TIN=0) Bank0,Index83_ Bit1 (Shut = 0)	Bank0,Index82_Bit1 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=1)	Bank0,Index82_Bit1 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=0)	
SMIOVT3	Bank0,IndxB9_Bit2 (EN_WS=1) Bank0,Indx82_ Bit2(TIN=0) Bank0,Index83_ Bit2 (Shut = 0)	Bank0,Indx82_Bit2 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=1)	Bank0,Index82_Bit1 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=0)	
SMIOVT4	Bank0,IndexBA_Bit 2(EN_WS=1) Bank4,Indx82_ Bit3(TIN=0) Bank4,Inex83_ Bit3 (Shut = 0)	Bank4,Index82_Bit3 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=1)	Bank0,Index82_Bit1 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=0)	
SMIOVT5	Bank0,IndexBB_Bit 2(EN_WS=1) Bank4,Index82 _Bit4(TIN=0) Bank4,Index83 _Bit4 (Shut = 0)	Bank4,Index82_Bit4 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=1)	Bank0,Index82_Bit1 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=0)	
SMIOVT6	Bank0,IndexBC_Bit 2(EN_WS=1) Bank4,Inex82_Bit5 (TIN=0)	Bank4,Inex82_Bit5 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=1)	Bank0,Index82_Bit1 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=0)	

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	Bank4,Index83_Bit5 (Shut = 0)			

Table 8-8 Relative Register of OVT functions

SMIOVT1	SMIOVT2	SMIOVT3
Bank0, IndexB7_Bit0 **0:** Start to monitor the source of SMIOVT1 temperature. **1:** Stop to monitor the source of SMIOVT1 temperature. **Bank 0, IndexB7_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 0, InedexB7_Bit 3** **0:** Enable SMIOVT1 temperature sensor over temperature output **1:** Disable SMIOVT1 temperature sensor over temperature output	**Bank0, IndexB8_Bit0** **0:** Start to monitor the source of SMIOVT2 temperature. **1:** Stop to monitor the source of SMIOVT2 temperature. **Bank 0, IndexB8_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 0, InedexB8_Bit 3** **0:** Enable SMIOVT2 temperature sensor over temperature output **1:** Disable SMIOVT2 temperature sensor over temperature output	**Bank0, IndexB9_Bit0** **0:** Start to monitor the source of SMIOVT3 temperature. **1:** Stop to monitor the source of SMIOVT3 temperature. **Bank 0, IndexB9_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 0, InedexB9_Bit 3** **0:** Enable SMIOVT3 temperature sensor over temperature output **1:** Disable SMIOVT3 temperature sensor over temperature output
SMIOVT4	**SMIOVT5**	**SMIOVT6**
Bank0, IndexBA_Bit0 **0:** Start to monitor the source of SMIOVT4 temperature. **1:** Stop to monitor the source of SMIOVT4 temperature. **Bank 0, IndexBA_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 0, InedexBA_Bit 3** **0:** Enable SMIOVT4 temperature sensor over temperature output **1:** Disable SMIOVT4 temperature sensor over temperature output	**Bank0, IndexBB_Bit0** **0:** Start to monitor the source of SMIOVT5 temperature. **1:** Stop to monitor the source of SMIOVT5 temperature. **Bank 0, IndexBB_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 0, InedexBB_Bit 3** **0:** Enable SMIOVT5 temperature sensor over temperature output **1:** Disable SMIOVT5 temperature sensor over temperature output	**Bank0, IndexBC_Bit0** **0:** Start to monitor the source of SMIOVT6 temperature. **1:** Stop to monitor the source of SMIOVT6 temperature. **Bank 0, IndexBC_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 0, InedexBC_Bit 3** **0:** Enable SMIOVT6 temperature sensor over temperature output **1:** Disable SMIOVT6 temperature sensor over temperature output

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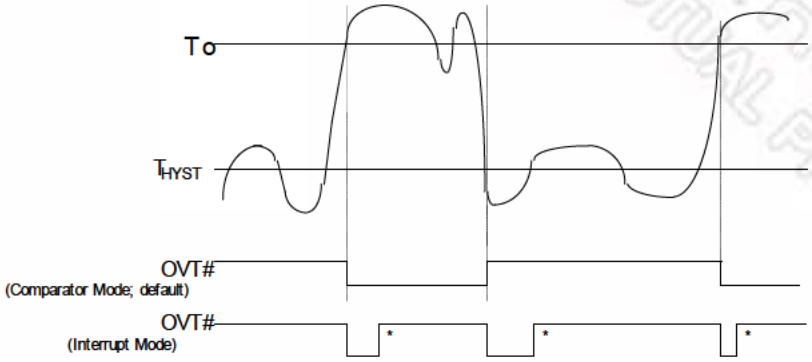
8.10.5 OVT# Interrupt Mode

The SMI#/OVT# pin is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register CR[29h], bit 6 to one or zero, respectively. In OVT# mode, it can monitor temperatures, and OVT pin could be enabled to OVT output by Bank0 Index B7h, bit 3 for Temperature Sensor 1(default: SYSTIN); Bank0 Index B8h, bit 3 for Temperature Sensor 2(default: CPUTIN); Bank0 Index B9h, bit3 for Temperature Sensor 3(default: AUXTIN); Bank0 Index BAh, bit3 for Temperature Sensor 4(default: SYSTIN); Bank0 Index BBh, bit3 for Temperature Sensor 5(default: SYSTIN)and Bank0 Index BCh, bit3 for Temperature Sensor 6(default: SYSTIN).

The OVT# pin has two interrupt modes, comparator and interrupt. The modes are illustrated in this figure.



*Interrupt Reset when Temperature sensor registers are read

Figure 8-27 OVT# Modes of Temperature Inputs

If Bank0 Index B7h, bit 1, is set to zero, the OVT# pin is in comparator mode. In comparator mode, the OVT# pin can create an interrupt once the current temperature exceeds T_O and continues to create interrupts until the temperature falls below T_{HYST}. The OVT# pin is asserted once the temperature has exceeded T_O and has not yet fallen below T_{HYST}.

If Bank0 Index B7h, bit 1, is set to one, the OVT# pin is in interrupt mode. In interrupt mode, the OVT# pin can create an interrupt once the current temperature rises above T_O or when the temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers. The OVT# pin is asserted when an interrupt is generated and remains asserted until the interrupt is reset.

8.10.6 Caseopen Detection

The purpose of Caseopen function is used to detect whether the computer case has been opened and possible tampered with. This feature must function even when there is no 3VSB power. Consequently, the power source for the circuit is from either Pin 74 (VBAT) or Pin 61 (3VSB). 3VSB is the default power source. If there is no 3VSB power, the power source is VBAT. This is designed to save power consumption of the battery.

When the case is closed, CASEOPEN# (pin 76) must be pulled high by an externally pulled-up 2MΩ resistor that is connected to VBAT (pin 74). When the case is opened, CASEOPEN# will be switched from high to low. Meanwhile, the detection circuit inside the IC latches the signal. As a result, the interrupt status and the real-time status can be

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read at the registers next time when the computer is powered. The CASEOPEN# status will not be cleared unless CR[46h], bit 7, or CR[E6h] bit 5 at Logical Device A is set to "1" first and then to "0".

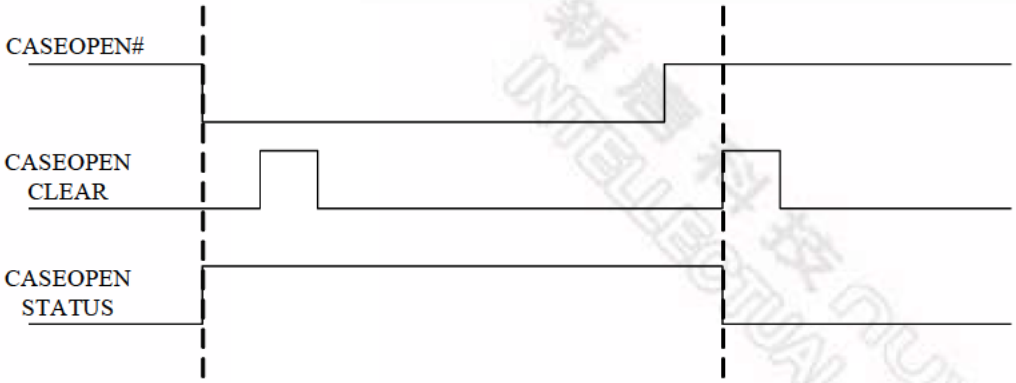

Figure 8-28 Caseopen Mechanism

8.11 Power Measurement

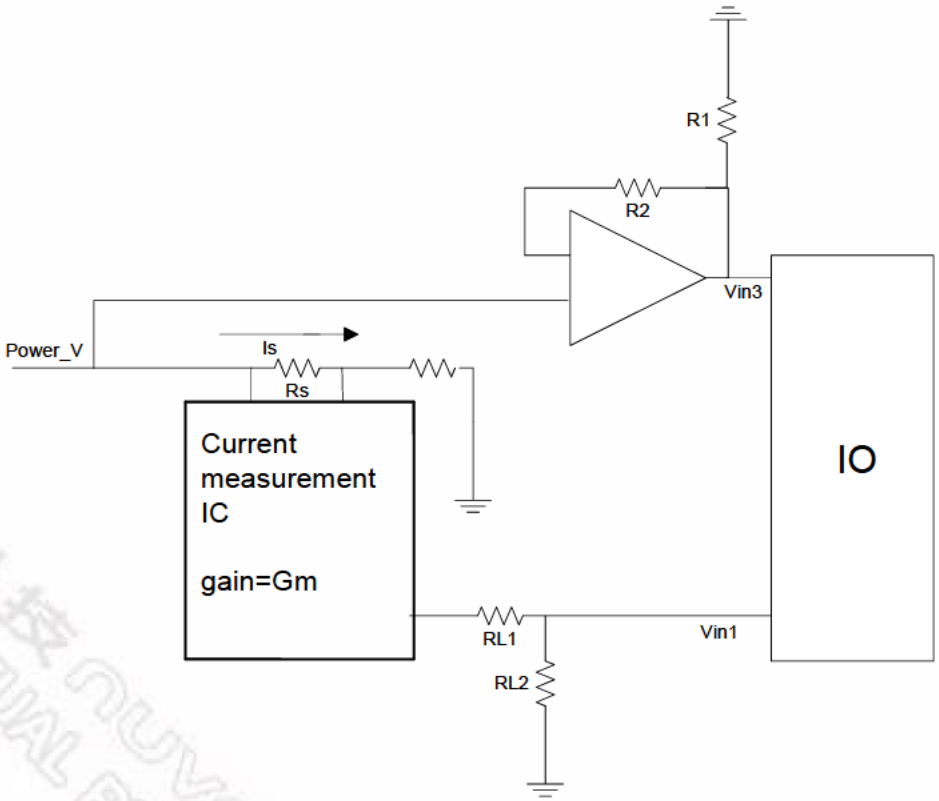

Figure 8-29 Power measurement architecture

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This function will detect the voltage from current measurement IC on board and calculate the current and power. Fig 8.29 is the architecture. Vin3 ($Vin3 = Power_V \times \frac{R1}{R1+R2}$) and Vin1 ($Vin1 = Is \times Rs \times Gm \times RL2$) could not over 2.048. We suggest the ratio $\frac{R1}{R1+R2} = \frac{1}{15}$.

	HM Register	Note
Is	Bank3 Index D0h & Index D1h	Calculate by IO
POWER	Bank3 Index D2h & Index D3h	Calculate by IO
VIN	Bank3 Index D4h	Given by user
Rre	Bank3 Index D5h	Given by user Rreg=Rs*RL2*Gm
Reg_Ration_K	Bank3 Index D6h	Given by user Reg_Ration_K = (R1+R2)/(R1)
Power_Volt_En	Bank3 Index D6h	Given by user
POWER_V	Bank3 Index D7h	Calculate by IO or given by user depend on Power_Volt_En
Vin1	Bank0 Index 04h	Measure by IO

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9. HARDWARE MONITOR REGISTER SET

The base address of the Address Port and Data Port is specified in registers CR[60h] and CR[61h] of Logical Device B, the hardware monitor device. CR[60h] is the high byte, and CR[61h] is the low byte. The Address Port and Data Port are located at the base address, plus 5h and 6h, respectively. For example, if CR[60h] is 02h and CR[61h] is 90h, the Address Port is at 0x295h, and the Data Port is at 0x296h.

Remember that this access is from the host CPU I/O address range. To conserve space in the crowded CPU I/O addresses, many of the hardware monitor registers are "banked" with the bank number located at index 04Eh. Indexes from 000h to 04Fh are "global" or accessible from all banks, while indexes 050h to 0FFh are specific to each bank.

9.1 Address Port (Port x5h)

Attribute: Bit 6:0 Read/Write , Bit 7: Reserved

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED.
6-0	READ/WRITE.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved (Power On default 0)	Address Pointer (Power On default 00h)						
	A6	A5	A4	A3	A2	A1	A0

9.2 Data Port (Port x6h)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Data to be read from or to be written to Value RAM and Register.

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9.3 Value RAM — Index 00h ~ 6Fh (Bank 0)

ADDRESS 00-6F	DESCRIPTION
00h	CPUVCORE reading
01h	VIN0 reading
02h	AVSB reading
03h	3VCC reading
04h	VIN1 reading
05h	VIN2 reading
06h	**RESERVED**
07h	3VSB reading.
08h	VBAT reading
09h	V10 reading
0Ah	**RESERVED**
0Bh	**RESERVED**
0Ch	**RESERVED**
0Dh	**RESERVED**
0Eh	**RESERVED**
0Fh	**RESERVED**
10h	SMIOVT1 temperature reading
11h	SMIOVT2 temperature reading
12h	SMIOVT3 temperature reading
13h	SMIOVT4 temperature reading
14h	SMIOVT5 temperature reading
15h	SMIOVT6 temperature reading
16h	SMIOVT1~6 temperature reading LSB
17h	**RESERVED**
18h	System fan control temperature reading
19h	CPU fan control temperature reading
1Ah	AUX fan control temperature reading
1Bh	Fan control temperature reading LSB
1Ch	System fan weighting temperature reading
1Dh	CPU fan weighting temperature reading
1Eh	AUX fan weighting temperature reading
1Fh	fan weighting temperature reading LSB
20h	SYS fan count reading [12:5]
21h	SYS fan count reading [4:0]

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ADDRESS 00-6F	DESCRIPTION
22h	CPU fan count reading [12:5]
23h	CPU fan count reading [4:0]
24h	AUX fan count reading [12:5]
25h	AUX fan count reading [4:0]
26h	**RESERVED**
27h	**RESERVED**
28h	**RESERVED**
29h	**RESERVED**
2Ah	SYS fan target
2Bh	CPU fan target
2Ch	AUX fan target
2Dh	**RESERVED**
2Eh	**RESERVED**
2Fh	**RESERVED**
30h	Syatem fan RPM value reading high byte
31h	Syatem fan RPM value reading low byte
32h	CPU fan RPM value reading high byte
33h	CPU fan RPM value reading low byte
34h	AUX fan RPM value reading high byte
35h	AUX fan RPM value reading low byte
36h	**RESERVED**
37h	**RESERVED**
38h	**RESERVED**
39h	**RESERVED**
3Ah	System FANIN RPM target (unit is 50 RPM)
3Bh	CPU FANIN RPM target (unit is 50 RPM)
3Ch	AUX FANIN RPM target (unit is 50 RPM)
3Dh	**RESERVED**
3Eh	**RESERVED**
3Fh	**RESERVED**
40h	**RESERVED**
41h	**RESERVED**
42h	**RESERVED**
43h	**RESERVED**
44h	**RESERVED**
45h	**RESERVED**

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ADDRESS 00-6F	DESCRIPTION
46h	RESERVED
47h	RESERVED
48h	RESERVED
49h	RESERVED
4Ah	System fan duty
4Bh	CPU fan duty
4Ch	AUX fan duty
4Dh	RESERVED
4Eh	Bank select register
4Fh	Port 80 data input
50h	PCH_CHIP_CPU_MAX_Temperature
51h	PCH_CHIP_Temperature
52h	PCH_CPU_TEMP_H
53h	PCH_CPU_TEMP_L
54h	PCH_MCH_TEMP
55h	PCH_DIM0_TEMP
56h	PCH_DIM1_TEMP
57h	PCH_DIM2_TEMP
58h	PCH_DIM3_TEMP
59h	TSI Agent 0 temperature high byte
5Ah	TSI Agent 0 temperature low byte
5Bh	TSI Agent 1 temperature high byte
5Ch	TSI Agent 1 temperature low byte
5Dh	TSI Agent 2 temperature high byte
5Eh	TSI Agent 2 temperature low byte
5Fh	TSI Agent 3 temperature high byte
60h	TSI Agent 3 temperature low byte
61h	TSI Agent 4 temperature high byte
62h	TSI Agent 4 temperature low byte
63h	TSI Agent 5 temperature high byte
64h	TSI Agent 5 temperature low byte
65h	TSI Agent 6 temperature high byte
66h	TSI Agent 6 temperature low byte
67h	TSI Agent 7 temperature high byte
68h	TSI Agent 7 temperature low byte
69h	Byte Temperature high byte

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ADDRESS 00-6F	DESCRIPTION
6Ah	Byte Temperature low byte
6Bh	RESERVED
6Ch	RESERVED
6Dh	RESERVED
6Eh	RESERVED
6Fh	RESERVED

9.4 SMIOVT1 Temperature Source (High Byte) Register – Index 10h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**Temperature <8:1> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5℃.

9.5 SMIOVT2 Temperature Source (High Byte) Register – Index 11h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**Temperature <8:1> (default: CPUTIN temperature source).** The nine-bit value is in units of 0.5℃.

9.6 SMIOVT3 Temperature Source (High Byte) Register – Index 12h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**Temperature <8:1> (default: AUXTIN temperature source).** The nine-bit value is in units of 0.5℃.

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9.7 SMIOVT4 Temperature Source (High Byte) Register – Index 13h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**Temperature <8:1> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5℃.

9.8 SMIOVT5 Temperature Source (High Byte) Register – Index 14h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**Temperature <8:1> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5℃.

9.9 SMIOVT6 Temperature Source (High Byte) Register – Index 15h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**Temperature <8:1> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5℃.

9.10 SMIOVT1-6 Temperature Source (Low Byte) Register – Index 16h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.		SMIOVT6_ TEMP<0>	SMIOVT5_ TEMP<0>	SMIOVT4_ TEMP<0>	SMIOVT3_ TEMP<0>	SMIOVT2_ TEMP<0>	SMIOVT1_ TEMP<0>

BIT	DESCRIPTION
7-6	**Reserved.**
5	**SMIOVT6 Temperature <0> (default: SYSTIN temperature source).** The nine-bit value

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BIT	DESCRIPTION
	is in units of 0.5°C.
4	**SMIOVT5 Temperature <0> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5°C.
3	**SMIOVT4 Temperature <0> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5°C.
2	**SMIOVT3 Temperature <0> (default: AUXTIN temperature source).** The nine-bit value is in units of 0.5°C.
1	**SMIOVT2 Temperature <0> (default: CPUTIN temperature source).** The nine-bit value is in units of 0.5°C.
0	**SMIOVT1 Temperature <0> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5°C.

9.11 System Fan Control Temperature Register (Integer Value)- Index 18h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SysFanControlTemp [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SysFanControlTemp [8:1]** SYSFANOUT fan control temperature reading.

9.12 Cpu Fan Control Temperature Register (Integer Value)- Index 19h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CpuFanControlTemp [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CpuFanControlTemp [8:1]** CPUFANOUT fan control temperature reading.

9.13 Aux Fan Control Temperature Register (Integer Value)- Index 1Ah (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AuxFanControlTemp [8:1]							

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DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AuxFanControlTemp [8:1]** AUXFANOUT fan control temperature reading.

9.14 Fan Temperature Register (Fractional Value)- Index 1Bh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7-3	2	1	0
NAME	Reserved	AuxFan ControlTemp[0]	CpuFan ControlTemp[0]	SysFan ControlTemp[0]
DEFAULT	0	0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2	**AuxFanControlTemp[0]** AuxFANOUT fan control temperature reading
1	**CpuFanControlTemp[0]** CpuFANOUT fan control temperature reading
0	**SysFanControlTemp[0]** SYSFANOUT fan control temperature reading

9.15 (SYSFANIN) FANIN1 COUNT High-byte Register – Index 20h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT1 [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANCNT1_H:** 13-bit SYSFANIN Fan Count, High Byte

9.16 (SYSFANIN) FANIN1 COUNT Low-byte Register – Index 21h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT1 [4:0]				

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DEFAULT	0	0

9.17 (CPUFANIN) FANIN2 COUNT High-byte Register – Index 22h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT2 [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANCNT2_H:** 13-bit CPUFANIN Fan Count, High Byte

9.18 (CPUFANIN) FANIN2 COUNT Low-byte Register – Index 23h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT2[4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT2_L:** 13-bit CPUFANIN Fan Count, Low Byte

9.19 (AUXFANIN) FANIN3 COUNT High-byte Register – Index 24h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT3 [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANCNT3_H:** 13-bit AUXFANIN Fan Count, High Byte

9.20 (AUXFANIN) FANIN3 COUNT Low-byte Register – Index 25h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT3 [4:0]				

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DEFAULT	0	0

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT3_L:** 13-bit AUXFANIN Fan Count, Low Byte

9.21 Bank Select Register – Index 4Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	HBACS	Reserved					BANK SEL1	BANK SEL0
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**HBACS. HBACS – High Byte Access.** 1: Access Index 4Fh high-byte register. (Default) 0: Access Index 4Fh low-byte register.	
6-2	**RESERVED**	
1	**BANKSEL1.**	Bank Select for Bank0 to Bank3. The Two - bit binary value corresponds to the bank number. For example, "01" selects bank1.
0	**BANKSEL0.**	

9.22 PORT 80 DATA INPUT Register – Index 4F (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	P80_IN							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PORT 80 DATA INPUT**

9.23 PCH_CHIP_CPU_MAX_TEMP Register – Index 50h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CHIP_CPU_MAX_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

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BIT	DESCRIPTION
7-0	**PCH_CHIP_CPU_MAX_TEMP:** The maximum temperature in absolute degree C, of the CPU and MCH.

9.24 PCH_CHIP_TEMP Register – Index 51h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CHIP_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CHIP_TEMP** The IBX_CHIP temperature in degree C.

9.25 PCH_CPU_TEMP_H Register – Index 52h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CPU_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CPU_TEMP_H** The CPU temperature in degree C. (Integer Part)

9.26 PCH_CPU_TEMP_L Register – Index 53h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CPU_TEMP_L						Reserved	Reading _Flag
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**PCH_CPU_TEMP_L** The CPU temperature in degree C. (Fractional Part)
1	**Reserved**
0	**Reading_Flag:** If there is an error when the IBX read the data from the CPU, then Bit0 is set to '1'.

9.27 PCH_MCH_TEMP Register – Index 54h (Bank 0)

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Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_MCH_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7-0	PCH_MCH_TEMP	The MCH temperature in degree C.

9.28 PCH_DIM0_TEMP Register – Index 55h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_DIM0_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7-0	PCH_DIM0_TEMP	The DIM0 temperature in degree C.

9.29 PCH_DIM1_TEMP Register – Index 56h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_DIM1_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7-0	PCH_DIM1_TEMP	The DIM1 temperature in degree C.

9.30 PCH_DIM2_TEMP Register – Index 57h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_DIM2_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7-0	PCH_DIM2_TEMP	The DIM2 temperature in degree C.

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9.31 PCH_DIM3_TEMP Register – Index 58h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_DIM3_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_DIM3_TEMP** The DIM3 temperature in degree C.

9.32 PCH_TSI0_TEMP_H Register – Index 59h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI0_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI0_TEMP_H** The TSI High-Byte temperature in degree C.

9.33 PCH_TSI0_TEMP_L Register – Index 5Ah (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI0_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI0_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.34 PCH_TSI1_TEMP_H Register – Index 5Bh (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI1_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

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BIT	DESCRIPTION
7-0	**PCH_TSI1_TEMP_H** The TSI High-Byte temperature in degree C.

9.35 PCH_TSI1_TEMP_L Register – Index 5Ch (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI1_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI1_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.36 PCH_TSI2_TEMP_H Register – Index 5Dh (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI2_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI2_TEMP_H** The TSI High-Byte temperature in degree C.

9.37 PCH_TSI2_TEMP_L Register – Index 5Eh (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI2_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI2_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.38 PCH_TSI3_TEMP_H Register – Index 5Fh (Bank 0)

Attribute: Read
Size: 8 bits

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BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI3_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI3_TEMP_H** The TSI High-Byte temperature in degree C.

9.39 PCH_TSI3_TEMP_L Register – Index 60h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI3_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI3_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.40 PCH_TSI4_TEMP_H Register – Index 61h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI4_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI4_TEMP_H** The TSI High-Byte temperature in degree C.

9.41 PCH_TSI4_TEMP_L Register – Index 62h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI4_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI4_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

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9.42 PCH_TSI5_TEMP_H Register – Index 63h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI5_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI5_TEMP_H** The TSI High-Byte temperature in degree C.

9.43 PCH_TSI5_TEMP_L Register – Index 64h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI5_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI5_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.44 PCH_TSI6_TEMP_H Register – Index 65h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI6_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI6_TEMP_H** The TSI High-Byte temperature in degree C.

9.45 PCH_TSI6_TEMP_L Register – Index 66h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI6_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

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BIT	DESCRIPTION
7-5	**PCH_TSI6_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.46 PCH_TSI7_TEMP_H Register – Index 67h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI7_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI7_TEMP_H** The TSI High-Byte temperature in degree C.

9.47 PCH_TSI7_TEMP_L Register – Index 68h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI7_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI7_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.48 ByteTemp_H Register – Index 69h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	ByteTemp_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**ByteTemp_H** The TSI Byte format High-Byte temperature in degree C.

9.49 ByteTemp_L Register – Index 6Ah (Bank 0)

Attribute: Read
Size: 8 bits

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BIT	7	6	5	4	3	2	1	0
NAME	ByteTemp_L							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**ByteTemp_L** The TSI Byte format Low-Byte temperature in degree C.

9.50 Peci Temp Register – Index 6Bh (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Peci Temp							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**ByteTemp_L** The TSI Byte format Low-Byte temperature in degree C.

9.51 Interrupt Status Register 1 – Index 70h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VSB	RESERVED	VIN2	VIN1	3VCC	AVCC	VIN0	CPUVCORE
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**3VSB.** A one indicates the high or low limit of 3VSB has been exceeded.
6	**RESERVED**
5	**VIN2.** A one indicates the high or low limit of VIN2 has been exceeded
4	**VIN1.** A one indicates the high or low limit of VIN1 has been exceeded
3	**3VCC.** A one indicates the high or low limit of 3VCC has been exceeded.
2	**AVCC .** A one indicates the high or low limit of AVCC has been exceeded.
1	**VIN0.** A one indicates the high or low limit of VIN0 has been exceeded.
0	**CPUVCORE.** A one indicates the high or low limit of CPUVCORE has been exceeded.

9.52 Interrupt Status Register 2 – Index 71h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

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NAME	RESERVED						V10	VBAT
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED
6	RESERVED
5	RESERVED
4	RESERVED
3	RESERVED
2	RESERVED
1	**V10.** A one indicates the high or low limit of V10 has been exceeded.
0	**VBAT**one indicates the high or low limit of VBAT has been exceeded.

9.53 Interrupt Status Register 3 – Index 72h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	SOURCE6_SMI	SOURCE5_SMI	SOURCE4_SMI	SOURCE3_SMI	SOURCE2_SMI	SOURCE1_SMI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED
6	RESERVED
5	**SOURCE6_SMI.** A one indicates the high limit of SMIOVT SOURCE6 temperature has been exceeded. (SYSTIN is default temperature)
4	**SOURCE5_SMI.** A one indicates the high limit of SMIOVT SOURCE5 temperature has been exceeded. (SYSTIN is default temperature)
3	**SOURCE4_SMI.** A one indicates the high limit of SMIOVT SOURCE4 temperature has been exceeded. (SYSTIN is default temperature)
2	**SOURCE3_SMI.** A one indicates the high limit of SMIOVT SOURCE3 temperature has been exceeded. (AUXTIN is default temperature)
1	**SOURCE2_SMI.** A one indicates the high limit of SMIOVT SOURCE2 temperature has been exceeded. (CPUTIN is default temperature)
0	**SOURCE1_SMI.** A one indicates the high limit of SMIOVT SOURCE1 temperature has been exceeded. (SYSTIN is default temperature)

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9.54 Interrupt Status Register 4 – Index 73h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	Shut_SOURCE6_SMI	Shut_SOURCE5_SMI	Shut_SOURCE4_SMI	Shut_SOURCE3_SMI	Shut_SOURCE2_SMI	Shut_SOURCE1_SMI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED
6	RESERVED
5	**Shut_SOURCE6_SMI.** "1" indicates the high limit of SMIOVT _SOURCE6 temperature of SMI# Shut-down mode has been exceeded. (SYSTIN is default temperature)
4	**Shut_SOURCE5_SMI.** "1" indicates the high limit of SMIOVT _SOURCE5 temperature of SMI# Shut-down mode has been exceeded. (SYSTIN is default temperature)
3	**Shut_SOURCE4_SMI.** "1" indicates the high limit of SMIOVT _SOURCE4 temperature of SMI# Shut-down mode has been exceeded. (SYSTIN is default temperature)
2	**Shut_SOURCE3_SMI.** "1" indicates the high limit of SMIOVT _SOURCE3 temperature of SMI# Shut-down mode has been exceeded. (AUXTIN is default temperature)
1	**Shut_SOURCE2_SMI.** "1" indicates the high limit of SMIOVT _SOURCE2 temperature of SMI# Shut-down mode has been exceeded. (CPUTIN is default temperature)
0	**Shut_SOURCE1_SMI.** "1" indicates the high limit of SMIOVT _SOURCE1 temperature of SMI# Shut-down mode has been exceeded. (SYSTIN is default temperature)

9.55 Interrupt Status Register 5 – Index 74h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	AUXFANIN	CPUFANIN	SYSFANIN
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED
6	RESERVED
5	RESERVED
4	RESERVED
3	RESERVED
2	**AUXFANIN.** A one indicates the fan count limit of AUXFANIN has been exceeded.
1	**CPUFANIN.** A one indicates the fan count limit of CPUFANIN has been exceeded.
0	**SYSFANIN.** A one indicates the fan count limit of SYSFANIN has been exceeded.

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9.56 Interrupt Status Register 6 – Index 75h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	AUX FANOUT	CPU FANOUT	SYS FANOUT
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED
6	RESERVED
5	RESERVED
4	RESERVED
3	RESERVED
2	**AUXFANOUT.** "1" indicates that AUXFANOUT works for three minutes at the full fan speed.
1	**CPUFANOUT.** "1" indicates that CPUFANOUT works for three minutes at the full fan speed.
0	**SYSFANOUT.** "1" indicates that SYSFANOUT works for three minutes at the full fan speed.

9.57 Interrupt Status Register 7 – Index 76h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CASEOPEN1
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED
6	RESERVED
5	RESERVED
4	RESERVED
3	RESERVED
2	RESERVED
1	RESERVED
0	**CASEOPEN1.** A one indicates the case has been opened.

9.58 Real Time Status Register 1 – Index 77h (Bank 0)

Attribute: Read Only
Size: 8 bits

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BIT	7	6	5	4	3	2	1	0
NAME	3VSB _STS	RESERVED	VIN2 _STS	VIN1 _STS	3VCC _STS	AVCC _STS	VIN0 _STS	CPUVCORE _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**3VSB_STS.** 1: 3VSB voltage is over or under the allowed range. 0: 3VSB voltage is in the allowed range.
6	RESERVED
5	**VIN2_STS.** 1: VIN2 voltage is over or under the allowed range. 0: VIN2 voltage is in the allowed range.
4	**VIN1_STS.** 1: VIN1 voltage is over or under the allowed range. 0: VIN1 voltage is in the allowed range.
3	**3VCC_STS.** 1: 3VCC voltage is over or under the allowed range. 0: 3VCC voltage is in the allowed range.
2	**AVCC_STS.** 1: AVCC voltage is over or under the allowed range. 0: AVCC voltage is in the allowed range.
1	**VIN0_STS.** 1: VIN0 voltage is over or under the allowed range. 0: VIN0 voltage is in the allowed range.
0	**CPUVCORE_STS.** 1: CPUVCORE voltage is over or under the allowed range. 0: CPUVCORE voltage is in the allowed range.

9.59 Real Time Status Register 2 – Index 78h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	V10 _STS	VBAT _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED
6	RESERVED
5	RESERVED
4	RESERVED
3	RESERVED

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BIT	DESCRIPTION
2	RESERVED.
1	**V10_STS.** 1: V10 voltage is over or under the allowed range. 0: V10 voltage is in the allowed range.
0	**VBAT_STS.** 1: VBAT voltage is over or under the allowed range. 0: VBAT voltage is in the allowed range.

9.60 Real Time Status Register 3 – Index 79h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	SMIOVT6_STS	SMIOVT5_STS	SMIOVT4_STS	SMIOVT3_STS	SMIOVT2_STS	SMIOVT1_STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED
6	RESERVED
5	**SMIOVT6_STS.** 1: SMIOVT6 Temperature exceeds the over-temperature value. 0: SMIOVT6 Temperature is under the hysteresis value.
4	**SMIOVT5_STS.** 1: SMIOVT5 Temperature exceeds the over-temperature value. 0: SMIOVT5 Temperature is under the hysteresis value.
3	**SMIOVT4_STS.** 1: SMIOVT4 Temperature exceeds the over-temperature value. 0: SMIOVT4 Temperature is under the hysteresis value.
2	**SMIOVT3_STS.** 1: SMIOVT3 Temperature exceeds the over-temperature value. 0: SMIOVT3 Temperature is under the hysteresis value.
1	**SMIOVT2_STS.** 1: SMIOVT2 Temperature exceeds the over-temperature value. 0: SMIOVT2 Temperature is under the hysteresis value.
0	**SMIOVT1_STS.** 1: SMIOVT1 Temperature exceeds the over-temperature value. 0: SMIOVT1 Temperature is under the hysteresis value.

9.61 Real Time Status Register 4 – Index 7Ah (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

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NAME	RESERVED	RESERVED	Shut_ SMIOVT6 _STS	Shut_ SMIOVT5 _STS	Shut_ SMIOVT4 _STS	Shut_ SMIOVT3 _STS	Shut_ SMIOVT2 _STS	Shut_ SMIOVT1 _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED
6	RESERVED
5	**Shut_SMIOVT6_STS.** 1: SMIOVT6 Temperature exceeds the Shut -temperature value. 0: SMIOVT6 Temperature is under the Shut-hysteresis value.
4	**Shut_SMIOVT5_STS.** 1: SMIOVT5 Temperature exceeds the Shut -temperature value. 0: SMIOVT5 Temperature is under the Shut-hysteresis value.
3	**Shut_SMIOVT4_STS.** 1: SMIOVT4 Temperature exceeds the Shut -temperature value. 0: SMIOVT4 Temperature is under the Shut-hysteresis value.
2	**Shut_SMIOVT3_STS.** 1: SMIOVT3 Temperature exceeds the Shut -temperature value. 0: SMIOVT3 Temperature is under the Shut-hysteresis value.
1	**Shut_SMIOVT2_STS.** 1: SMIOVT2 Temperature exceeds the Shut -temperature value. 0: SMIOVT2 Temperature is under the Shut-hysteresis value.
0	**Shut_SMIOVT1_STS.** 1: SMIOVT1 Temperature exceeds the Shut -temperature value. 0: SMIOVT1 Temperature is under the Shut-hysteresis value.

9.62 Real Time Status Register 5 – Index 7Bh (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	AUX FANIN _STS	CPU FANIN _STS	SYS FANIN _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED
6	RESERVED
5	RESERVED
4	RESERVED
3	RESERVED
2	**AUXFANIN_STS.**

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BIT	DESCRIPTION
	1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
1	**CPUFANIN_STS.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
0	**SYSFANIN_STS.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.

9.63 Real Time Status Register 6 – Index 7Ch (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	AUX FANOUT _STS	CPU FANOUT _STS	SYS FANOUT _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED
6	RESERVED
5	RESERVED
4	RESERVED
3	RESERVED
2	**AUXFANOUT_STS.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode. 0: The selected temperature has not reached the warning range.
1	**CPUFANOUT_STS.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode. 0: The selected temperature has not reached the warning range.
0	**SYSFANOUT_STS.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode. 0: The selected temperature has not reached the warning range.

9.64 Real Time Status Register 7 – Index 7Dh (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED							Caseopen_STS

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DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED
6	RESERVED
5	RESERVED
4	RESERVED
3	RESERVED
2	RESERVED
1	RESERVED
0	**CASEOPEN_STS.** 1: Caseopen is detected and latched. 0: Caseopen is not latched.

9.65 Reserved Register – Index 7Eh ~ 7Fh (Bank 0)

9.66 SMI# Mask Register 1 – Index 80h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VSB	RESERVED	VIN2	VIN1	3VCC	AVCC	VIN0	CPUVCORE
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	3VSB.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 1 – Index 70h (Bank0))
6	RESERVED	
5	VIN2.	
4	VIN1.	
3	3VCC.	
2	AVCC.	
1	VIN0.	
0	CPUVCORE.	

9.67 SMI# Mask Register 2 – Index 81h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	V10	VBAT
DEFAULT	0	0	0	0	0	0	1	1

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BIT	DESCRIPTION	
7	RESERVED.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 2 – Index 71h (Bank0))
6	RESERVED.	
5	RESERVED.	
4	RESERVED.	
3	RESERVED.	
2	RESERVED.	
1	V10.	
0	VBAT.	

9.68 SMI# Mask Register 3 – Index 82h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	SMIOVT6	SMIOVT5	SMIOVT4	SMIOVT3	SMIOVT2	SMIOVT1
DEFAULT	0	0	1	1	1	1	1	1

BIT	DESCRIPTION	
7	RESERVED.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 3 – Index 72h (Bank0))
6	RESERVED.	
5	SMIOVT6.	
4	SMIOVT5.	
3	SMIOVT4.	
2	SMIOVT3.	
1	SMIOVT2.	
0	SMIOVT1.	

9.69 SMI# Mask Register 4 – Index 83h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	Shut_ SMIOVT6	Shut_ SMIOVT5	Shut_ SMIOVT4	Shut_ SMIOVT3	Shut_ SMIOVT2	Shut_ SMIOVT1
DEFAULT	0	0	1	1	1	1	1	1

BIT	DESCRIPTION	
7	RESERVED.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 4 – Index 73h (Bank0))
6	RESERVED.	
5	Shut_SMIOVT6.	
4	Shut_SMIOVT5.	

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BIT	DESCRIPTION
3	Shut_SMIOVT4.
2	Shut_SMIOVT3.
1	Shut_SMIOVT2.
0	Shut_SMIOVT1.

9.70 SMI# Mask Register 5 – Index 84h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	AUX FANIN	CPU FANIN	SYS FANIN
DEFAULT	0	0	1	1	1	1	1	1

BIT	DESCRIPTION	
7	RESERVED.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 5 – Index 74h (Bank0))
6	RESERVED.	
5	RESERVED.	
4	RESERVED.	
3	RESERVED.	
2	AUXFANIN.	
1	CPUFANIN.	
0	SYSFANIN.	

9.71 SMI# Mask Register 6 – Index 85h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					AUX FANOUT	CPU FANOUT	SYS FANOUT
DEFAULT	0	0	0	0	0	1	1	1

BIT	DESCRIPTION	
7	RESERVED.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 6 – Index 75h (Bank0))
6	RESERVED.	
5	RESERVED.	
4	RESERVED.	
3	RESERVED.	
2	AUXFANOUT.	
1	CPUFANOUT.	

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BIT	DESCRIPTION	
0	SYSFANOUT.	

9.72 SMI# Mask Register 7 – Index 86h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					Caseopen_clr	RESERVED	Caseopen
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION	
7	RESERVED.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 7 – Index 76h (Bank0))
6	RESERVED.	
5	RESERVED.	
4	RESERVED.	
3	RESERVED.	
2	Caseopen_clr.	
1	RESERVED.	
0	Caseopen.	

9.73 CPUVCORE High Limit Voltage Register – Index 90h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUVCORE High Limit Voltage							
DEFAULT	1	1	0	1	1	0	1	0

BIT	DESCRIPTION
7-0	**CPUVCORE High Limit Voltage.** Default: 0xDAh

9.74 CPUVCORE Low Limit Voltage Register – Index 91h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUVCORE High Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION

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7-0	**CPUVCORE Low Limit Voltage.** Default: 0x00h

9.75 VIN0 High Limit Voltage Register – Index 92h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN0 High Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**VIN0 High Limit Voltage.** Default: 0xFFh

9.76 VIN1 Low Limit Voltage Register – Index 93h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN1 Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**VIN0 Low Limit Voltage.** Default: 0x00h

9.77 AVCC High Limit Voltage Register – Index 94h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AVCC High Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**AVCC High Limit Voltage.** Default: 0xFFh

9.78 AVCC Low Limit Voltage Register – Index 95h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AVCC Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

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BIT	DESCRIPTION
7-0	**AVCC Low Limit Voltage.** Default: 0x00h

9.79 3VCC High Limit Voltage Register – Index 96h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VCC High Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**3VCC High Limit Voltage.** Default: 0xFFh

9.80 3VCC Low Limit Voltage Register – Index 97h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VCC Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**3VCC Low Limit Voltage.** Default: 0x00h

9.81 VIN1 High Limit Voltage Register – Index 98h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN1 High Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**VIN1 High Limit Voltage.** Default: 0xFFh

9.82 VIN1 Low Limit Voltage Register – Index 99h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

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NAME	VIN1 Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**VIN1 Low Limit Voltage.** Default: 0x00h

9.83 VIN2 High Limit Voltage Register – Index 9Ah (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN2 High Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**VIN2 High Limit Voltage.** Default: 0xFFh

9.84 VIN2 Low Limit Voltage Register – Index 9Bh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN2 Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**VIN2 Low Limit Voltage.** Default: 0x00h

9.85 Reserved Register – Index 9Ch ~ 9Dh (Bank 0)

9.86 3VSB High Limit Voltage Register – Index 9Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VSB High Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**3VSB High Limit Voltage.** Default: 0xFFh

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9.87 3VSB Low Limit Voltage Register – Index 9Fh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VSB Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**3VSB Low Limit Voltage.** Default: 0x00h

9.88 VBAT High Limit Voltage Register – Index A0h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VBAT High Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**VBAT High Limit Voltage.** Default: 0xFFh

9.89 VBAT Low Limit Voltage Register – Index A1h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VBAT Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**VBAT Low Limit Voltage.** Default: 0x00h

9.90 V10 High Limit Voltage Register – Index A2h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	V10 High Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION

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7-0	**VBAT High Limit Voltage.** Default: 0xFFh

9.91 V10 Low Limit Voltage Register – Index A3h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	V10 Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**V10 Low Limit Voltage.** Default: 0x00h

9.92 Reserved Register – Index A4h ~ AFh (Bank 0)

9.93 SMIOVT1 Temperature Source Select Register – Index B0 (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC1				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT1 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT1 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT1 monitoring source. 0 0 0 1 1: Select **AUXTIN** as SMIOVT1 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT1 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT1 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT1 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT1 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT1 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT1 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT1 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT1 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT1 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT1 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT1 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT1 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT1monitoring source.

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	1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT1 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT1 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT1 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT1 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT1 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT1 monitoring source.

9.94 SMIOVT2 Temperature Source Select Register – Index B1 (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC2				
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT2 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT2 monitoring source. 0 0 0 1 0: Select **CPUTIN** as SMIOVT2 monitoring source. (Default) 0 0 0 1 1: Select **AUXTIN** as SMIOVT2 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT2 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT2 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT2 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT2 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT2 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT2 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT2 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT2 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT2 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT2 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT2 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT2 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT2monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT2 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT2 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT2 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT2 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT2 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT2 monitoring source.

9.95 SMIOVT3 Temperature Source Select Register – Index B2 (Bank 0)

Attribute: Read/Write
Size: 8 bits

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BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT3 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT3 monitoring source. 0 0 0 1 0: Select **CPUTIN** as SMIOVT3 monitoring source. 0 0 0 1 1: Select **AUXTIN** as SMIOVT3 monitoring source. (Default) 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT3 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT3 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT3 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT3 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT3 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT3 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT3 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT3 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT3 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT3 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT3 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT3 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT3monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT3 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT3 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT3 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT3 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT3 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT3 monitoring source.

9.96 SMIOVT4 Temperature Source Select Register – Index B3 (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC4				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT4 Temperature selection.** **Bits**

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	4 3 2 1 0 0 0 0 0 1: Select **SYSTIN** as SMIOVT4 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT4 monitoring source. 0 0 0 1 1: Select **AUXTIN** as SMIOVT4 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT4 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT4 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT4 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT4 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT4 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT4 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT4 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT4 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT4 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT4 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT4 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT4 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT4monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT4 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT4 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT4 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT4 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT4 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT4 monitoring source.

9.97 SMIOVT5 Temperature Source Select Register – Index B4 (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC5				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT5 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT5 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT5 monitoring source. 0 0 0 1 1: Select **AUXTIN** as SMIOVT5 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT5 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT5 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT5 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT5 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT5 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT5 monitoring source.

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	0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT5 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT5 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT5 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT5 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT5 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT5 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT5monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT5 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT5 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT5 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT5 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT5 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT5 monitoring source.

9.98 SMIOVT6 Temperature Source Select Register – Index B5 (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC6				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT6 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT6 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT6 monitoring source. 0 0 0 1 1: Select **AUXTIN** as SMIOVT6 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT6 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT6 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT6 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT6 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT6 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT6 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT6 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT6 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT6 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT6 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT6 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT6 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT6monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT6 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT6 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT6 monitoring source.

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	1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT6 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT6 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT6 monitoring source.

9.99 SMI/OVT Control Register – Index B6h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	OVTPOL	Reserved	T2ToT6 _INTMODE	EN_T1 _ONE	SMI# ENABLE
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7	**Reserved**
6	**Reserved**
5	**Reserved**
4	**OVTPOL (Over-temperature polarity).** 1: OVT# is active high. 0: OVT# is active low (Default).
3	**Reserved**
2	**T2ToT6_INTMode.** 1: SMI# output type of Temperature SMIOVT2, SMIOVT3, SMIOVT4, SMIOVT5 and SMIOVT6 temperature source is in Comparator Interrupt mode. 0: SMI# output type of Temperature SMIOVT2, SMIOVT3, SMIOVT4, SMIOVT5 and SMIOVT6 temperature source is in Two-Times Interrupt mode. (Default)
1	**EN_T1_ONE.** 1: SMI# output type of SMIOVT Source1 temperature (Default: SYSTIN) is One-Time Interrupt Mode. 0: SMI# output type is in Two-Times Interrupt Mode. (Default)
0	**SMI#Enable.** A one enables the SMI# Interrupt output.

9.100 SMIOVT1 Control Register – Index B7h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST1<0>	TOVF1<0>	FAULT1		DIS_ OVT1	EN_ WS1	OVT1_ Mode	SOPT1
DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION
7	**THYST1<0>:** Hysteresis temperature bit0.

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BIT	DESCRIPTION
6	**TOVF1<0>:** Over-temperature bits0.
5-4	**Fault1.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
3	**DIS_OVT1.** 0: Enable SMIOVT1 OVT# output. (Default) 1: Disable temperature sensor SMIOVT1 over-temperature (OVT#) output.
2	**EN_WS1.** 1: SMI# output type of SMIOVT Source1 temperature (Default: SYSTIN) is Shut-down Interrupt Mode. 0: SMI# output type is in Interrupt Mode. (Default)
1	**OVT1_Mode. SMIOVT1 Mode Select.** 0: Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP1.** **0: Monitor SMIOVT1 temperature source.** **1: Stop monitoring SMIOVT1 temperature source.**

9.101 SMIOVT2 Control Register – Index B8h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST2<0>	TOVF2<0>	FAULT2		DIS_ OVT2	EN_ WS2	OVT2_ Mode	SOPT2
DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION
7	**THYST2<0>:** Hysteresis temperature bit0.
6	**TOVF2<0>:** Over-temperature bits0.
5-4	**Fault2.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
3	**DIS_OVT2.** 0: Enable SMIOVT2 OVT# output. (Default) 1: Disable temperature sensor SMIOVT2 over-temperature (OVT#) output.
2	**EN_WS2.** 1: SMI# output type of SMIOVT Source2 temperature (Default: CPUTIN) is Shut-down Interrupt Mode. 0: SMI# output type is in Interrupt Mode. (Default)
1	**OVT2_Mode. SMIOVT2 Mode Select.** 0: Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP2.** **0: Monitor SMIOVT2 temperature source.** **1: Stop monitoring SMIOVT2 temperature source.**

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9.102 SMIOVT3 Control Register – Index B9h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST3<0>	TOVF3<0>	FAULT3		DIS_ OVT3	EN_ WS3	OVT3_ Mode	SOPT3
DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION
7	**THYST3<0>:** Hysteresis temperature bit0.
6	**TOVF3<0>:** Over-temperature bits0.
5-4	**Fault3.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
3	**DIS_OVT3.** 0: Enable SMIOVT3 OVT# output. (Default) 1: Disable temperature sensor SMIOVT3 over-temperature (OVT#) output.
2	**EN_WS3.** 1: SMI# output type of SMIOVT Source3 temperature (Default: AUXTIN) is Shut-down Interrupt Mode. 0: SMI# output type is in Interrupt Mode. (Default)
1	**OVT3_Mode. SMIOVT3 Mode Select.** 0: Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP3.** **0: Monitor SMIOVT3 temperature source.** **1: Stop monitoring SMIOVT3 temperature source.**

9.103 SMIOVT4 Control Register – Index BAh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST4<0>	TOVF4<0>	FAULT4		DIS_ OVT4	EN_ WS4	OVT4_ Mode	SOPT4
DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION
7	**THYST4<0>:** Hysteresis temperature bit0.
6	**TOVF4<0>:** Over-temperature bits0.
5-4	**Fault4.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
3	**DIS_OVT4.** 0: Enable SMIOVT4 OVT# output. (Default) 1: Disable temperature sensor SMIOVT4 over-temperature (OVT#) output.

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BIT	DESCRIPTION
2	**EN_WS4.** 1: SMI# output type of SMIOVT Source4 temperature (Default: SYSTIN) is Shut-down Interrupt Mode. 0: SMI# output type is in Interrupt Mode. (Default)
1	**OVT4_Mode. SMIOVT4 Mode Select.** 0: Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP4.** **0: Monitor SMIOVT4 temperature source.** **1: Stop monitoring SMIOVT4 temperature source.**

9.104 SMIOVT5 Control Register – Index BBh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST5<0>	TOVF5<0>	FAULT5		DIS_ OVT5	EN_ WS5	OVT5_ Mode	SOPT5
DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION
7	**THYST5<0>:** Hysteresis temperature bit0.
6	**TOVF5<0>:** Over-temperature bits0.
5-4	**Fault5.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
3	**DIS_OVT5.** 0: Enable SMIOVT5 OVT# output. (Default) 1: Disable temperature sensor SMIOVT5 over-temperature (OVT#) output.
2	**EN_WS5.** 1: SMI# output type of SMIOVT Source5 temperature (Default: SYSTIN) is Shut-down Interrupt Mode. 0: SMI# output type is in Interrupt Mode. (Default)
1	**OVT5_Mode. SMIOVT5 Mode Select.** 0: Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP5.** **0: Monitor SMIOVT5 temperature source.** **1: Stop monitoring SMIOVT5 temperature source.**

9.105 SMIOVT6 Control Register – Index BCh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

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NAME	THYST6<0>	TOVF6<0>	FAULT6		DIS_ OVT6	EN_ WS6	OVT6_ Mode	SOPT6
DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION
7	**THYST6<0>:** Hysteresis temperature bit0.
6	**TOVF6<0>:** Over-temperature bits0.
5-4	**Fault6.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
3	**DIS_OVT6.** 0: Enable SMIOVT6 OVT# output. (Default) 1: Disable temperature sensor SMIOVT6 over-temperature (OVT#) output.
2	**EN_WS6.** 1: SMI# output type of SMIOVT Source6 temperature (Default: SYSTIN) is Shut-down Interrupt Mode. 0: SMI# output type is in Interrupt Mode. (Default)
1	**OVT6_Mode. SMIOVT6 Mode Select.** 0: Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP6.** **0: Monitor SMIOVT6 temperature source.** **1: Stop monitoring SMIOVT6 temperature source.**

9.106 Reserved Register – Index BDh ~ BFh (Bank 0)

9.107 SMIOVT1 Shut-down mode High Limit Temperature Register – Index C0h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT1 Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT1 Shut-down mode High Limit Temperature.**

9.108 SMIOVT1 Shut-down mode Low Limit Temperature Register – Index C1h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT1 Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

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BIT	DESCRIPTION
7-0	SMIOVT1 Shut-down mode Low Limit Temperature.

9.109 SMIOVT1 Temperature Source Over-temperature (High Byte) Register – Index C2h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF1<8:1>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF1<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.110 SMIOVT1 Temperature Source Hysteresis (High Byte) Register – Index C3h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST1<8:1>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**THYST1<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 0°C.

9.111 SMIOVT2 Shut-down mode High Limit Temperature Register – Index C4h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT2 Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	SMIOVT2 Shut-down mode High Limit Temperature.

9.112 SMIOVT2 Shut-down mode Low Limit Temperature Register – Index C5h (Bank 0)

Attribute: Read/Write
Size: 8 bits

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BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT2 Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT2 Shut-down mode Low Limit Temperature.**

9.113 SMIOVT2 Temperature Source Over-temperature (High Byte) Register – Index C6h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF2<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF2<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.114 SMIOVT2 Temperature Source Hysteresis (High Byte) Register – Index C7h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST2<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST2<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.115 SMIOVT3 Shut-down mode High Limit Temperature Register – Index C8h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT3 Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT3 Shut-down mode High Limit Temperature.**

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9.116 SMIOVT3 Shut-down mode Low Limit Temperature Register – Index C9h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT3 Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT3 Shut-down mode Low Limit Temperature.**

9.117 SMIOVT3 Temperature Source Over-temperature (High Byte) Register – Index CAh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF3<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF3<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.118 SMIOVT3 Temperature Source Hysteresis (High Byte) Register – Index CBh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST3<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST3<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.119 SMIOVT4 Shut-down mode High Limit Temperature Register – Index CCh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT4 Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

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BIT	DESCRIPTION
7-0	SMIOVT4 Shut-down mode High Limit Temperature.

9.120 SMIOVT4 Shut-down mode Low Limit Temperature Register – Index CDh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT4 Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	SMIOVT4 Shut-down mode Low Limit Temperature.

9.121 SMIOVT4 Temperature Source Over-temperature (High Byte) Register – Index CEh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF4<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF4<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.122 SMIOVT4 Temperature Source Hysteresis (High Byte) Register – Index CFh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST4<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST4<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.123 SMIOVT5 Shut-down mode High Limit Temperature Register – Index D0h (Bank 0)

Attribute: Read/Write

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Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT5 Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT5 Shut-down mode High Limit Temperature.**

9.124 SMIOVT5 Shut-down mode Low Limit Temperature Register – Index D1h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT5 Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT5 Shut-down mode Low Limit Temperature.**

9.125 SMIOVT5 Temperature Source Over-temperature (High Byte) Register – Index D2h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF5<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF5<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.126 SMIOVT5 Temperature Source Hysteresis (High Byte) Register – Index D3h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST5<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION

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BIT	DESCRIPTION
7-0	**THYST5<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.127 SMIOVT6 Shut-down mode High Limit Temperature Register – Index D4h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT6 Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT6 Shut-down mode High Limit Temperature.**

9.128 SMIOVT6 Shut-down mode Low Limit Temperature Register – Index D5h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT6 Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT6 Shut-down mode Low Limit Temperature.**

9.129 SMIOVT6 Temperature Source Over-temperature (High Byte) Register – Index D6h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF6<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF6<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.130 SMIOVT6 Temperature Source Hysteresis (High Byte) Register – Index D7h (Bank 0)

Attribute: Read/Write
Size: 8 bits

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BIT	7	6	5	4	3	2	1	0
NAME	THYST6<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST6<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.131 Reserved Register – Index D8h ~ DFh (Bank 0)

9.132 (SYSFANIN) Fan Count Limit High-byte Register – Index E0h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN1_HL [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANIN1_HL:** 13-bit SYSFANIN Fan Count Limit, High Byte

9.133 (SYSFANIN) Fan Count Limit Low-byte Register – Index E1h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN1_HL [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN1_HL:** 13-bit SYSFANIN Fan Count Limit, Low Byte

9.134 (CPUFANIN) Fan Count Limit High-byte Register – Index E2h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN2_HL [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

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BIT	DESCRIPTION
7-0	**FANIN2_HL:** 13-bit CPUFANIN Fan Count Limit, High Byte

9.135 (CPUFANIN) Fan Count Limit Low-byte Register – Index E3h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN2_HL [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN2_HL:** 13-bit CPUFANIN Fan Count Limit, Low Byte

9.136 (AUXFANIN) Fan Count Limit High-byte Register – Index E4h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN3_HL [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANIN3_HL:** 13-bit AUXFANIN Fan Count Limit, High Byte

9.137 (AUXFANIN) Fan Count Limit Low-byte Register – Index E5h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN3_HL [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN3_HL:** 13-bit AUXFANIN Fan Count Limit, Low Byte

9.138 Reserved Register – Index E6h ~ EFh (Bank 0)

9.139 SYSFAN PWM Output Frequency Configuration Register – Index F0h (Bank 0)

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Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL1	PWM_SCALE1						
DEFAULT	0	3						

The register is meaningful only when SYSFANOUT is progarmmed for PWM output (i.e., Bank0, Index F3h, bit 0 is 0).

BIT	DESCRIPTION
7	**PWM_CLK_SEL1. SYSFANOUT PWM Input Clock Source Select.** This bit selects the clock source for PWM output frequency. Refer the Divisor table.
6-0	**PWM_SCALE1. SYSFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

9.140 CPUFAN PWM Output Frequency Configuration Register – Index F1h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL2	PWM_SCALE2						
DEFAULT	0	3						

The register is meaningful only when CPUFANOUT is progarmmed for PWM output (i.e., Bank0, Index F3h, bit 1 is 0).

BIT	DESCRIPTION
7	**PWM_CLK_SEL2. CPUFANOUT PWM Input Clock Source Select.** This bit selects the clock source for the PWM output. Refer the Divisor table.
6-0	**PWM_SCALE2. CPUFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

9.141 AUXFAN PWM Output Frequency Configuration Register – Index F2h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL3	PWM_SCALE3						
DEFAULT	0	3						

This register is only meaningful when AUXFANOUT is programmed for PWM output (i.e. Bank0, Index F3h, bit 2 is 0)

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BIT	DESCRIPTION
7	**PWM_CLK_SEL3. AUXFANOUT PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE3. AUXFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency. If CKSEL equals **0**, then the output clock is simply equal to **92.5/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	92.5KHz	.....		
0000001	2	46.3KHz			
0000010	3	31.2KHz			
0000011	4	23.3KHz			
0000100	5	18.5KHz	0001111	16	5.8KHz
0000101	6	15.6KHz	0011111	32	2.9KHz
0000110	7	13.3KHz	0111111	64	1.4KHz
0000111	8	11.6KHz	1111111	128	724Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1000Hz	1000	12	83Hz
0001	2	500Hz	1001	16	62.5Hz
0010	3	333Hz	1010	32	31.25Hz
0011	4	250Hz	1011	64	15.62Hz
0100	5	200Hz	1100	128	7.81Hz
0101	6	166Hz	1101	256	3.9Hz
0110	7	142Hz	1110	512	2Hz
0111	8	125Hz	1111	1024	0.98Hz

9.142 FAN Output Mode Configuration – Index F3h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					AUXFANOUT_SEL	CPUFANOUT_SEL	SYSFANOUT_SEL
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	Reserved.

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BIT	DESCRIPTION
2	**AUXFANOUT Output Mode Selection.** 0: AUXFANAOUT pin produces a PWM output duty cycle. (Default) 1: AUXFANOUT pin produces DC output.
1	**CPUFANOUT Output Mode Selection.** 0: CPUFANOUT pin produces a PWM output duty cycle. (Default) 1: CPUFANOUT pin produces DC output.
0	**SYSFANOUT Output Mode Selection.** 0: SYSFANOUT pin produces a PWM duty cycle output. (Default) 1: SYSFANOUT pin produces DC output.

9.143 Reserved Register – Index F4h ~ F5h (Bank 0)

9.144 FANIN Revolution Pulses Selection Register – Index F6h (Bank 0)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		HM_Rev_Pulse_Fan3_Sel		HM_Rev_Pulse_Fan2_Sel		HM_Rev_Pulse_Fan1_Sel	
DEFAULT	0		0		0		0	

BIT	DESCRIPTION
7-6	**Reserved**
5-4	**AUXFANIN Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.
3-2	**CPUFANIN Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.
1-0	**SYSFANIN Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.145 Serial Bus Address Register – Index F7h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

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NAME	RESERVED	SERIAL BUS ADDRESS						
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7	**Reserved (Read Only).**
6-0	**Serial Bus Address <7:1>**

9.146 FAN IN/OUT Control Register – Index F8h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				FANOPV2	FANINC2	FANOPV1	FANINC1
DEFAULT	0	0	0	0	0	1	0	1

BIT	DESCRIPTION
7-4	**Reserved.**
3	**FANOPV2. CPUFANIN output value**, only if bit 2 is set to zero. 1: Pin 124 (CPUFANIN) generates a logic-high signal. 0: Pin 124 generates a logic-low signal. (Default)
2	**FANINC2. CPUFANIN Input Control.** 1: Pin 124 (CPUFANIN) acts as a fan tachometer input. (Default) 0: Pin 124 acts as a fan control signal, and the output value is set by bit 3.
1	**FANOPV1. SYSFANIN output value**, only if bit 0 is set to zero. 1: Pin 126 (SYSFANIN) generates a logic-high signal. 0: Pin 126 generates a logic-low signal. (Default)
0	**FANINC1. SYSFANIN Input Control.** 1: Pin 126 (SYSFANIN) acts as a fan tachometer input. (Default) 0: Pin 126 acts as a fan control signal, and the output value is set by bit 1.

9.147 Reserved Register – Index F9h ~ FCh (Bank 0)

9.148 Nuvoton Vendor ID Register by I2C Interface – Index FDh (Bank 0)

Attribute: Read Only
Size: 16 bits

BIT	15	14	13	12	11	10	9	8
NAME	VIDH							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDL							

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DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	**Vendor ID High-Byte**, if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	**Vendor ID Low-Byte**, if Index 4Eh, bit 7 is 0. Default A3h.

9.149 Nuvoton Vendor ID Register by LPC Interface – Index FEh (Bank 0)

Attribute: Read Only
Size: 16 bits

BIT	15	14	13	12	11	10	9	8
NAME	VIDH							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDL							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	**Vendor ID High-Byte**, if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	**Vendor ID Low-Byte**, if Index 4Eh, bit 7 is 0. Default A3h.

9.150 Chip ID – Index FFh (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CHIPID							
DEFAULT	1	1	0	0	0	0	0	1

BIT	DESCRIPTION
7-0	Nuvoton Chip ID number. Default C1h.

9.151 SYSFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 10h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		SYSFAN SOURCE[4:0]				
DEFAULT	0	0		1				

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BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to SYSFANOUT Stop Value (Bank1, index16h) at most if necessary.
6-5	**Reserved**
4-0	**SYSFAN Temperature Source Select:** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as SYSFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

9.152 SYSFAN Target Temperature Register / SYSFANIN Target Speed_L Register – Index 11h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSTIN Target Temperature / SYSFANIN Target Speed_L							
DEFAULT	0							

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	SYSFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	SYSFANIN Target Speed [7:0], [11:8] associate index 12 [3:0]							

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9.153 SYSFANIN Tolerance_H / Target Speed_H Register – Index 12h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	SYSFANIN TOL_H			SYSFANIN Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	SYSFANIN Tolerance_H [5:3]
3-0	SYSFANIN Target Speed_H [11:8]

9.154 SYSFAN MODE Register / SYSFAN TOLERRANCE Register – Index 13h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN MODE				Reserved	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L		
DEFAULT	0				0	0		

BIT	DESCRIPTION
7-4	**SYSFANOUT Mode Select.** 0000: SYSFANOUT is in Manual Mode. (Default) 0001: SYSFANOUT is in Thermal Cruise Mode. 0010: SYSFANOUT is in Speed Cruise Mode. 0100: SYSFANOUT is in SMART FAN™ IV Mode.
3	**Reserved**
2-0	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L.

9.155 SYSFAN Step Up Time Register – Index 14h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Step Up Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to increase its value by one step.
(1) For PWM output:

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The units are intervals of 0.1 second. The default time is 1 second.

9.156 SYSFAN Step Down Time Register – Index 15h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Step Down Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.157 SYSFAN Stop Value Register – Index 16h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Stop Value							
DEFAULT	1							

In Thermal Cruise mode, the SYSFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.158 SYSFAN Start-up Value Register – Index 17h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Start-Up Value							
DEFAULT	1							

In Thermal Cruise mode, SYSFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.159 SYSFAN Stop Time Register – Index 18h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Stop Time							

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DEFAULT	3C

In Thermal Cruise mode, Define the retention time to the fan stop. It is required by Fan Stop Function.
The time unit is 0.1sec.

9.160 SYSFAN Output Value Select Register – Index 19h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	7F							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index F3h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index F3h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation. **OUTPUT Voltage =** $Vref * \frac{FANOUT}{64}$ Note. VREF is approx 2.048V.						Reserved	

9.161 SYSFAN Temperature Critical Register – Index 1Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Temperature Critical							
DEFAULT	3C							

BIT	DESCRIPTION
7-0	SYSFAN Temperature Critical Register.

9.162 SYSFAN Critical Temperature Tolerance Register – Index 1Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					SYSFANOUT Critical Temperature Tolerance		
DEFAULT	0					0		

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BIT	DESCRIPTION
7-3	**Reserved**
2-0	SYSFAN Critical Temperature Tolerance

9.163 SYSFAN Enable Critical Duty / Fanout Step Register – Index 1Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En_SYS_3WFAN	Reserved		En_SYS_CRITICAL_DUTY	Reserved			En_SYSFANOUT_STEP
DEFAULT	0	0		0	0			0

BIT	DESCRIPTION
7	**En_SYS_3WFAN** 0: 4-wire fan 1: 3-wire fan
6-5	**Reserved**
4	**En_SYS_CRITICAL_DUTY** 0: Load default Full Speed 8'hFF for SYSFANOUT. 1: Used Index 1D CRITICAL_DUTY Value for SYSFANOUT.
3-1	**Reserved**
0	**En_SYSFANOUT_STEP** 0: Disable SMART FAN™ IV has Stepping SYSFANOUT. 1: Enable SMART FAN™ IV has Stepping SYSFANOUT.

9.164 SYSFAN Critical Duty Register – Index 1Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	SYSFAN Critical Duty.

9.165 SYSFAN Enable Close Loop Fan Control RPM Mode Register – Index 1Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_SYS_RPM

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DEFAULT	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_SYS_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.

9.166 SYSFAN Enable RPM High Mode / RPM Mode Tolerance Register – Index 1Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En_SYS_RPM_High	Reserved			Generic_Tol_RPM			
DEFAULT	0	0			2			

BIT	DESCRIPTION
7	**En_SYS_RPM_High** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
6-4	**Reserved**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode, unit is 100 RPM.

9.167 CPUFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 20h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		CPUFAN SOURCE[4:0]				
DEFAULT	0	0		2				

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to CPUFANOUT Stop Value (Bank1, index26h) at most if necessary.
6-5	**Reserved**
4-0	**CPUFAN Temperature Source Select:**

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BIT	DESCRIPTION
	Bits **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as CPUFAN monitoring source. 0 0 0 1 0: Select **CPUTIN** as CPUFAN monitoring source. (Default) 0 0 0 1 1: Select **AUXTIN** as CPUFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as CPUFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as CPUFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as CPUFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as CPUFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as CPUFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as CPUFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as CPUFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as CPUFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as CPUFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as CPUFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as CPUFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as CPUFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as CPUFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as CPUFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as CPUFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as CPUFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as CPUFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as CPUFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as CPUFAN monitoring source.

9.168 CPUFAN Target Temperature Register / CPUFANIN Target Speed_L Register – Index 21h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN Target Temperature / CPUFANIN Target Speed_L							
DEFAULT	0							

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	CPUFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	CPUFANIN Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.169 CPUFANIN Tolerance_H / Target Speed_H Register – Index 22h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	CPUFANIN TOL_H			CPUFANIN Target Speed_H			

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DEFAULT	0	0	0

BIT	DESCRIPTION
7	**Reserved**
6-4	CPUFANIN Tolerance_H [5:3]
3-0	CPUFANIN Target Speed_H [11:8]

9.170 CPUFAN MODE Register / CPUFAN TOLERRANCE Register – Index 23h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN MODE				Reserved	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L		
DEFAULT	0				0	0		

BIT	DESCRIPTION
7-4	**CPUFANOUT Mode Select.** 0000: CPUFANOUT is in Manual Mode. (Default) 0001: CPUFANOUT is in Thermal Cruise Mode. 0010: CPUFANOUT is in Speed Cruise Mode. 0100: CPUFANOUT is in SMART FAN™ IV Mode.
3	**Reserved**
2-0	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L.

9.171 CPUFAN Step Up Time Register – Index 24h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Step Up Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.172 CPUFAN Step Down Time Register – Index 25h (Bank 1)

Attribute: Read/Write

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Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Step Down Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.173 CPUFAN Stop Value Register – Index 26h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Stop Value							
DEFAULT	1							

In Thermal Cruise mode, the CPUFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.174 CPUFANOUT Start-up Value Register – Index 27h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Start-Up Value							
DEFAULT	1							

In Thermal Cruise mode, CPUFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.175 CPUFAN Stop Time Register – Index 28h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Stop Time							
DEFAULT	3C							

In Thermal Cruise mode, Define the retention time to the fan stop. It is required by Fan Stop Function.
The time unit is 0.1sec.

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9.176 CPUFANOUT Output Value Select Register – Index 29h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value							
DEFAULT	7F							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index F3h, bit 1 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index F3h, bit 1 is 1)	DESCRIPTION	CPUFANOUT voltage control. The output voltage is calculated according to this equation. **OUTPUT Voltage =** $Vref * \frac{FANOUT}{64}$ Note. VREF is approx 2.048V.							Reserved

9.177 CPUFAN Temperature Critical Register – Index 2Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Temperature Critical							
DEFAULT	4B							

BIT	DESCRIPTION
7-0	CPUFAN Temperature Critical Register.

9.178 CPUFAN Critical Temperature Tolerance Register – Index 2Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					CPUFANOUT Critical Temperature Tolerance		
DEFAULT	0					0		

BIT	DESCRIPTION
7-3	**Reserved**
2-0	CPUFAN Critical Temperature Tolerance

9.179 CPUFAN Enable Critical Duty / Fanout Step Register – Index 2Ch (Bank 1)

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Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En_CPU_3WFAN	Reserved		En_CPU_CRITICAL_DUTY	Reserved			En_CPUFANOUT_STEP
DEFAULT	0	0		0	0			0

BIT	DESCRIPTION
7	**En_CPU_3WFAN** 0: 4-wire fan 1: 3-wire fan
6-5	**Reserved**
4	**En_CPU_CRITICAL_DUTY** 0: Load default Full Speed 8'hFF for CPUFANOUT. 1: Used Index 1D CRITICAL_DUTY Value for CPUFANOUT.
3-1	**Reserved**
0	**En_CPUFANOUT_STEP** 0: Disable SMART FAN™ IV has Stepping CPUFANOUT. 1: Enable SMART FAN™ IV has Stepping CPUFANOUT.

9.180 CPUFAN Critical Duty Register – Index 2Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	CPUFAN Critical Duty.

9.181 CPUFAN Enable Close Loop Fan Control RPM Mode Register – Index 2Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_CPU_RPM
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_CPU_RPM**

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	0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.

9.182 CPUFAN Enable RPM High Mode / RPM Mode Tolerance Register – Index 2Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En_CPU_RPM_High	Reserved			Generic_Tol_RPM			
DEFAULT	0	0			2			

BIT	DESCRIPTION
7	**En_CPU_RPM_High** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
6-4	**Reserved**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode, unit is 100 RPM.

9.183 AUXFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 30h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN SOURCE[4:0]				
DEFAULT	0	0		3				

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT Stop Value (Bank1, index36h) at most if necessary.
6-5	**Reserved**
4-0	**AUXFAN Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN monitoring source. 0 0 0 1 0: Select **CPUTIN** as AUXFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as AUXFAN monitoring source. (Default) 0 0 1 0 0: Select **SMBUSMASTER 0** as AUXFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as AUXFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as AUXFAN monitoring source.

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BIT	DESCRIPTION
	0 0 1 1 1: Select **SMBUSMASTER 3** as AUXFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as AUXFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as AUXFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as AUXFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as AUXFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as AUXFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as AUXFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as AUXFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as AUXFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as AUXFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as AUXFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as AUXFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as AUXFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as AUXFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as AUXFAN monitoring source.

9.184 AUXFAN Target Temperature Register / AUXFANIN Target Speed_L Register – Index 31h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN Target Temperature / AUXFANIN Target Speed_L							
DEFAULT	0							

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.185 AUXFANIN Tolerance_H / Target Speed_H Register – Index 32h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	AUXFANIN TOL_H			AUXFANIN Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	AUXFANIN Tolerance_H [5:3]
3-0	AUXFANIN Target Speed_H [11:8]

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9.186 AUXFAN MODE Register / AUXFAN TOLERRANCE Register – Index 33h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN MODE				Reseved	Tolerance of AUXFAN Target Temperature or AUXFANIN Target Speed_L		
DEFAULT	0				0	0		

BIT	DESCRIPTION
7-4	**AUXFANOUT Mode Select.** 0000: AUXFANOUT is in Manual Mode. (Default) 0001: AUXFANOUT is in Thermal Cruise Mode. 0010: AUXFANOUT is as Fan Speed Cruise Mode. 0100: AUXFANOUT is in SMART FAN™ IV Mode.
3	**Reseved**
2-0	Tolerance of AUXFAN Target Temperature or AUXFANIN Target Speed_L.

9.187 AUXFAN Step Up Time Register – Index 34h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Step Up Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT takes to increase its value by one step.
(1) For PWM output:
The units are intervals of 0.1 second. The default time is 1 second.

9.188 AUXFAN Step Down Time Register – Index 35h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Step Down Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT takes to decrease its value by one step.
(1) For PWM output:

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The units are intervals of 0.1 second. The default time is 1 second.

9.189 AUXFAN Stop Value Register – Index 36h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Stop Value							
DEFAULT	1							

In Thermal Cruise mode, the AUXFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.190 AUXFAN Start-up Value Register – Index 37h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Start-Up Value							
DEFAULT	1							

In Thermal Cruise mode, AUXFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.191 AUXFAN Stop Time Register – Index 38h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Stop Time							
DEFAULT	3C							

In Thermal Cruise mode, Define the retention time to the fan stop. It is required by Fan Stop Function.
The time unit is 0.1sec.

9.192 AUXFAN Output Value Select Register – Index 39h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Value							
DEFAULT	FF							

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FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index F3h, bit 2 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index F3h, bit 2 is 1)	DESCRIPTION	AUXFANOUT voltage control. The output voltage is calculated according to this equation. **OUTPUT Voltage =** $Vref * \frac{FANOUT}{64}$ Note. VREF is approx 2.048V.							Reserved

9.193 AUXFAN Temperature Critical Register – Index 3Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN Temperature Critical							
DEFAULT	3C							

BIT	DESCRIPTION
7-0	AUXFAN Temperature Critical Register.

9.194 AUXFAN Critical Temperature Tolerance Register – Index 3Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT Critical Temperature Tolerance		
DEFAULT	0					0		

BIT	DESCRIPTION
7-3	**Reserved**
2-0	AUXFAN Critical Temperature Tolerance

9.195 AUXFAN Enable Critical Duty / Fanout Step Register – Index 3Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En_AUX_3WFAN	Reserved		En_AUX_CRITICAL_DUTY	Reserved			En_AUXFANOUT_STEP
DEFAULT	0	0		0	0			0

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BIT	DESCRIPTION
7	**En_AUX_3WFAN** 0: 4-wire fan 1: 3-wire fan
6-5	**Reserved**
4	**En_AUX_CRITICAL_DUTY** 0: Load default Full Speed 8'hFF for AUXFANOUT. 1: Used Index 1D CRITICAL_DUTY Value for AUXFANOUT.
3-1	**Reserved**
0	**En_AUXFANOUT_STEP** 0: Disable SMART FAN™ IV has Stepping AUXFANOUT. 1: Enable SMART FAN™ IV has Stepping AUXFANOUT.

9.196 AUXFAN Critical Duty Register – Index 3Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	AUXFAN Critical Duty.

9.197 AUXFAN Enable Close Loop Fan Control RPM Mode Register – Index 3Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX_RPM
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUX_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.

9.198 AUXFAN Enable RPM High Mode / RPM Mode Tolerance Register – Index 3Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

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NAME	En_AUX_RPM_High	Reserved	Generic_Tol_RPM
DEFAULT	0	0	2

BIT	DESCRIPTION
7	**En_AUX_RPM_High** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
6-4	**Reserved**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode, unit is 100 RPM.

9.199 SYSFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 60h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	19							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.200 SYSFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 61h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 2							
DEFAULT	23							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.201 SYSFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 62h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	2D							

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BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.202 SYSFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 63h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 4							
DEFAULT	37							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.203 SYSFAN (SMART FAN™ IV) FD1/RPM1 Register – Index 64h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) FD1/RPM1							
DEFAULT	8C							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) FD1/RPM1 Register.

9.204 SYSFAN (SMART FAN™ IV) FD2/RPM2 Register – Index 65h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) FD2/RPM2							
DEFAULT	AA							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) FD2/RPM2 Register.

9.205 SYSFAN (SMART FAN™ IV) FD3/RPM3 Register – Index 66h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

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NAME	SYSFAN (SMART FAN™ IV) FD3/RPM3
DEFAULT	C8

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) FD3/RPM3 Register.

9.206 SYSFAN (SMART FAN™ IV) FD4/RPM4 Register – Index 67h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) FD4/RPM4							
DEFAULT	E6							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) FD4/RPM4 Register.

9.207 SYSFAN Weight value Configuration Register – Index 68h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_SYSFAN_WEIGHT	Reserved		SYS_WEIGHT_SEL				
DEFAULT	0	0		1				

BIT	DESCRIPTION
7	**EN_SYSFAN_WEIGHT.** 0: Disable Weight Value Control for SYSFAN. 1: Enable Weight Value Control for SYSFAN.
6-5	**Reserved**
4-0	**SYSFAN Weighting Temperature Source Select:** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as SYSFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source.

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BIT	DESCRIPTION
	0 1 0 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

9.208 SYSFAN Weight Temperature Step Register – Index 69h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Step (SYS_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**SYSFANOUT Temperature Step**

9.209 SYSFAN Weight Temperature Step Tolerance Register – Index 6Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Step Tolerance (SYS_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**SYSFANOUT Temperature Step Tolerance**

9.210 SYSFAN Weight Step Register – Index 6Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Weight Step (SYS_WEIGHT_STEP)							
DEFAULT	0							

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BIT	DESCRIPTION
7-0	SYSFANOUT Weight Step

9.211 SYSFAN Weight Temperature Base Register – Index 6Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Base (SYS_TEMP_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	SYSFANOUT Temperature Base

9.212 SYSFAN Weight Fan Duty Base Register – index 6Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Base (SYS_DUTY_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	SYSFANOUT Start point of Fan Duty increasing

9.213 SYSFAN Enable PECIERR DUTY Register – Index 6Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_SYS_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	Reserved
1-0	EN_SYS_PECIERR_DUTY 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT 10,11: Keep Full Speed

9.214 SYSFAN Pre-Configured Register For PECI Error – Index 6Fh (Bank 1)

Attribute: Read/Write

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Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT pre-configured register for PECI error (PECI_ERR_SYSOUT)							
DEFAULT	FF							

BIT	DESCRIPTION
7-0	SYSFANOUT pre-configured register for PECI error.

9.215 CPUFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 70h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	28							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.216 CPUFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 71h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 2							
DEFAULT	32							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.217 CPUFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 72h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	3C							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 3 Register (T3).

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9.218 CPUFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 73h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 4							
DEFAULT	46							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.219 CPUFAN (SMART FAN™ IV) FD1/RPM1 Register – Index 74h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) FD1/RPM1							
DEFAULT	8C							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) FD1/RPM1 Register.

9.220 CPUFAN (SMART FAN™ IV) FD2/RPM2 Register – Index 75h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) FD2/RPM2							
DEFAULT	AA							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) FD2/RPM2 Register.

9.221 CPUFAN (SMART FAN™ IV) FD3/RPM3 Register – Index 76h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) FD3/RPM3							
DEFAULT	C8							

BIT	DESCRIPTION

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7-0	CPUFAN (SMART FAN™ IV) FD3/RPM3 Register.

9.222 CPUFAN (SMART FAN™ IV) FD4/RPM4 Register – Index 77h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) FD4/RPM4							
DEFAULT	E6							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) FD4/RPM4 Register.

9.223 CPUFAN Weight value Configuration Register – Index 78h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_CPUFAN_WEIGHT	Reserved		CPU_WEIGHT_SEL				
DEFAULT	0	0		1				

BIT	DESCRIPTION
7	**EN_CPUFAN_WEIGHT.** 0: Disable Weight Value Control for CPUFAN. 1: Enable Weight Value Control for CPUFAN.
6-5	**Reserved**
4-0	**CPUFAN Weighting Temperature Source Select:** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as CPUFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as CPUFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as CPUFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER** as CPUFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as CPUFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as CPUFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as CPUFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as CPUFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as CPUFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as CPUFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as CPUFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as CPUFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as CPUFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as CPUFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as CPUFAN monitoring source.

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BIT	DESCRIPTION
	0 1 1 1 1: Select **PCH_CHIP_TEMP** as CPUFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as CPUFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as CPUFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as CPUFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as CPUFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as CPUFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as CPUFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as CPUFAN monitoring source.

9.224 CPUFAN Weight Temperature Step Register – Index 79h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Temperature Step (CPU_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Step**

9.225 CPUFAN Weight Temperature Step Tolerance Register – Index 7Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Temperature Step Tolerance (CPU_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Step Tolerance**

9.226 CPUFAN Weight Step Register – Index 7Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Weight Step (CPU_WEIGHT_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Weight Step**

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9.227 CPUFAN Weight Temperature Base Register – Index 7Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_TEMP_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	CPUFANOUT Temperature Base

9.228 CPUFAN Weight Fan Duty Base Register – Index 7Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_DUTY_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	CPUFANOUT Start point of Fan Duty increasing

9.229 CPUFAN Enable PECIERR DUTY Register – Index 7Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	Reserved						EN_CPU_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	Reserved
1-0	EN_CPU_PECIERR_DUTY 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT 10,11: Keep Full Speed

9.230 CPUFAN Pre-Configured Register For PECI Error – Index 7Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT pre-configured register for PECI error (PECI_ERR_CPUOUT)							
DEFAULT	FF							

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BIT	DESCRIPTION
7-0	CPUFANOUT pre-configured register for PECI error.

9.231 AUXFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 80h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	19							

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.232 AUXFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 81h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) Temperature 2							
DEFAULT	23							

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.233 AUXFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 82h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	2D							

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.234 AUXFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 83h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

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NAME	AUXFAN (SMART FAN™ IV) Temperature 4
DEFAULT	37

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.235 AUXFAN (SMART FAN™ IV) FD1/RPM1 Register – Index 84h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) FD1/RPM1							
DEFAULT	8C							

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) FD1/RPM1 Register.

9.236 AUXFAN (SMART FAN™ IV) FD2/RPM2 Register – Index 85h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) FD2/RPM2							
DEFAULT	AA							

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) FD2/RPM2 Register.

9.237 AUXFAN (SMART FAN™ IV) FD3/RPM3 Register – Index 86h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) FD3/RPM3							
DEFAULT	C8							

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) FD3/RPM3 Register.

9.238 AUXFAN (SMART FAN™ IV) FD4/RPM4 Register – Index 87h (Bank 1)

Attribute: Read/Write

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Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) FD4/RPM4							
DEFAULT	E6							

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) FD4/RPM4 Register.

9.239 AUXFAN Weight value Configuration Register – Index 88h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_AUXFAN_WEIGHT	Reserved		AUX_WEIGHT_SEL				
DEFAULT	0	0		1				

BIT	DESCRIPTION
7	**EN_AUXFAN_WEIGHT.** 0: Disable Weight Value Control for AUXFAN. 1: Enable Weight Value Control for AUXFAN.
6-5	**Reserved**
4-0	**AUXFAN Weighting Temperature Source Select:** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as AUXFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as AUXFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as AUXFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as AUXFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as AUXFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as AUXFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as AUXFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as AUXFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as AUXFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as AUXFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as AUXFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as AUXFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as AUXFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as AUXFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as AUXFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as AUXFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as AUXFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as AUXFAN monitoring source.

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BIT	DESCRIPTION
	1 0 1 0 1: Select **PCH_DIM3_TEMP** as AUXFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as AUXFAN monitoring source.

9.240 AUXFAN Weight Temperature Step Register – Index 89h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Temperature Step (AUX_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT Temperature Step**

9.241 AUXFAN Weight Temperature Step Tolerance Register – Index 8Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Temperature Step Tolerance (AUX_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT Temperature Step Tolerance**

9.242 AUXFAN Weight Step Register – Index 8Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Weight Step (AUX_WEIGHT_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT Weight Step**

9.243 AUXFAN Weight Temperature Base Register – Index 8Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

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NAME	AUXFANOUT Temperature Base (AUX_TEMP_BASE)
DEFAULT	0

BIT	DESCRIPTION
7-0	AUXFANOUT Temperature Base

9.244 AUXFAN Weight Fan Duty Base Register – Index 8Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Temperature Base (AUX_DUTY_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	AUXFANOUT Start point of Fan Duty increasing

9.245 AUXFAN Enable PECIERR DUTY Register – Index 8Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_AUX_PECIERR_DUTY	
DEFAULT	0						0	

BIT	DESCRIPTION
7-2	Reserved
1-0	EN_AUX_PECIERR_DUTY 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT 10,11: Keep Full Speed

9.246 AUXFAN Pre-Configured Register For PECI Error – Index 8Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT pre-configured register for PECI error (PECI_ERR_AUXOUT)							
DEFAULT	FF							

BIT	DESCRIPTION
7-0	AUXFANOUT pre-configured register for PECI error.

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9.247 Reserved Register – Index 90h~FF (Bank 1)

9.248 PECI Function Control Registers – Index 00 ~ 03h (Bank 2)

9.249 PECI Enable Function Register – Index 00h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI_En	Reserved				Is_PECI30	Manual_En	Routine_En
DEFAULT	0	0	0	0	0	1	0	1

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable PECI Function.(**PECI_En**)
6 ~ 3	R / W	Reserved
2	R / W	Enable PECI 3.0 Command function (**Is_PECI30**)
1	R / W	Enable PECI Manual Function(**Manual_En**)
0	R / W	Enable PECI Routine Function(**Routine_En**)

9.250 PECI Timing Config Register – Index 01h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		TN_Extend		Adj[2 :0]			PECI_DC
DEFAULT	0	0	0	0	0	0	1	0

BIT	READ / WRITE	DESCRIPTION
7 ~ 6	R / W	Reserve
5	R / W	**TN_Extend[1:0]** Adjust Transaction Rate. 00_{BIN} = 1.5 MHz 01_{BIN} = 750 KHz 10_{BIN} = 375 KHz 11_{BIN} = 187.5 KHz
4	R / W	
3	R / W	**Adj[2:0]** Compensate the effect of rising time on physical bus Default Value = 001
2	R / W	
1	R / W	
0	R / W	Adjust PECI Tbit Duty cycle selection. **(PECI_DC)** 0 = 75% Tbit high duty cycle time. (Default) 1 = 68% Tbit high duty cycle time.

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9.251 PECI Agent Config Register – Index 02h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		En_Agt[1:0]		Reserved		Dmn1_Agt[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	READ / WRITE	DESCRIPTION
7 ~ 6	R / W	Reserved
5	R / W	PECI host to process related agent 31 Enable or Disable. 0 = Agent Disable 1 = Agent Enable
4	R / W	PECI host to process related agent 30 Enable or Disable. 0 = Agent Disable 1 = Agent Enable
3 ~ 2	R / W	Reserved
1	R / W	Indicate agent 31 domain1. 0 = Agent does not have domain 1. 1 = Agent has domain 1.
0	R / W	Indicate agent 30 domain1. 0 = Agent does not have domain 1. 1 = Agent has domain 1.

9.252 PECI Temperature Config Register – Index 03h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Virtual_En	Reserved		Clamp	Reserved	RtDmn_Agt[1 :0]		RtHigher
DEFAULT	0	0	0	0	0	0	0	0

BIT	READ / WRITE	DESCRIPTION
7	R / W	Virtual Temp Function Enable.(**Virtual_En)** When enable this function, the temperature raw data can use LPC to write raw data to Bank7 CR 17_{HEX} ~ CR $1E_{HEX}$
6 ~ 5	R / W	Reserved
4	R / W	When temperature data reading is positive or less than -128, can enable this function to clamp temperature data.(**Clamp**)
3	R / W	Reserved

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BIT	READ / WRITE	DESCRIPTION
2	R / W	Agent 31 always return the relative domain Temperature. 0 = Agent always returns the relative temperature from domain 0. 1 = Agent always returns the relative temperature from domain 1.
1	R / W	Agent 30 always return the relative domain Temperature. 0 = Agent always returns the relative temperature from domain 0. 1 = Agent always returns the relative temperature from domain 1.
0	R / W	Return High Temperature of doamin0 or domain1.(**RtHigher**) 0 = The temperature of each agent is returned from domain 0 or domain 1, which is controlled by (CR 04_{HEX}) 1 = Return the highest temperature in domain 0 and domain 1 of individual Agent.

9.253 PECI Command Tbase0 Register – Index 04h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Tbase 0						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Agent0 base temperature for calculating agent0 absolute temperature.

9.254 PECI Command Tbase1 Register – Index 05h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Tbase 1						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Agent1 base temperature for calculating agent1 absolute temperature.

9.255 PECI Agent Relative Temperature Register – Index 06h-0Dh (Bank 2)

These registers return the raw data retrieved from PECI GetTemp(). The data may be the error code (range: 8000H~81FFH) or relative temperatures to process the defined **Tbase**. The error code will only be update in **ARTR** and absolute Temperature will not be updated when the error code is received. If the **RtHigher** mechanism is activated, the normal temperature will always be returned first. In case both 2 domains return errors, the return priority will be Overflow Error > Underflow Error > Missing Diode > General Error. The reset value is 8001_{HEX}, in that PECI is defaulted to be off. In PECI, 8001_{HEX} means the diode is missing.

Attribute: Read / Write(When Virtual_En enable)

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ADDRESS 17-1E	DESCRIPTION
06h[15:8],07h[7:0]	Domain0 Relative Temperature Agent0 [15:0]
08h[15:8],09h[7:0]	Domain1 Relative Temperature Agent0 [15:0]
0Ah[15:8],0Bh[7:0]	Domain0 Relative Temperature Agent1 [15:0]
0Ch[15:8],0Dh[7:0]	Domain1 Relative Temperature Agent1 [15:0]

GetTemp() PECI Temperature format:

BIT	DESCRIPTION
15	Sign Bit. **(Sign)** In PECI Protocol, this bit should always be 1 to represent a negative temperature.
14-6	The integer part of the relative temperature. (**Temperature[8:0]**)
5	**TEMP_2**. 0.5℃ unit.
4	**TEMP_4**. 0.25℃ unit.
3	**TEMP_8**. 0.125℃ unit.
2	**TEMP_16**. 0.0625℃ unit.
1	**TEMP_32**. 0.03125℃ unit.
0	**TEMP_64**. 0.015625℃ unit.

GetTemp() Response Definition:

RESPONSE	MEANING
General Sensor Error (GSE)	Thermal scan did not complete in time. Retry is appropriate.
0x0000	Processor is running at its maximum temperature or is currently being reset.
All other data	Valid temperature reading, reported as a negative offset from the TCC activation temperature. The valide temperature reading is referred to GetTemp() PECI Temperature format

Error Code	Description	Host operation
8000_{HEX}	General Sensor Error	No further processing.
8001_{HEX}	Sensing Device Missing	
8002_{HEX}	Operational, but the temperature is lower than the sensor operation range.	Compulsorily write 0℃ back to the temperature readouts.
8003_{HEX}	Operational, but the temperature is higher than the sensor operation range.	Compulsorily write 127℃ back to the temperature readouts.
8004_{HEX}	Reserved.	No further operation.

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Error Code	Description	Host operation
$81FF_{HEX}$		

9.256 PECI Command Write Date Registers – Index 10 ~ 1Fh (Bank 2)

9.257 PECI Command Address Register – Index 10h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Address							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.258 PECI Command Write Length Register – Index 11h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Write Length							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.259 PECI Command Read Length Register – Index 12h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Read Length							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.260 ECI Command Code Register – Index 13h (Bank 2)

Attribute: Read/Write

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Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Code							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.261 PECI Command Write Data 1 Register – Index 14h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.262 PECI Command Write Data 2 Register – Index 15h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.263 PECI Command Write Data 3 Register – Index 16h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

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9.264 PECI Command Write Data 4 Register – Index 17h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.265 PECI Command Write Data 5 Register – Index 18h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.266 PECI Command Write Data 6 Register – Index 19h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.267 PECI Command Write Data 7 Register – Index 1Ah (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

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NAME	PECI Write Data 7							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.268 PECI Command Write Data 8 Register – Index 1Bh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.269 PECI Command Write Data 9 Register – Index 1Ch (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.270 PECI Command Write Data 10 Register – Index 1Dh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 10							
DEFAULT	0	0	0	0	0	0	0	0

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BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.271 PECI Command Write Data 11 Register – Index 1Eh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 11							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.272 PECI Command Write Data 12 Register – Index 1Fh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 12							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client through issuing Manual Command.

9.273 PECI Command Read Date Registers – Index 20 ~ 24h (Bank 2)

9.274 PECI Absolute Temperature value Register – Index 20h-21h (Bank 2)

[ATH_Agent [8:2] +ATL_Agent[1:0]]] = Tbase + [RTH_Agent + RTL_Agent]

9.275 PECI Absolute Temperature value Register – Index 20h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Absolute Temperature Vaule[9:2]							
DEFAULT	0	0	1	0	1	0	0	0

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BIT	DESCRIPTION
7~0	Absolute Temperature value of all Agent [9](Sign bit) Absolute Temperature value of all Agent [8:2](Integer bits) Absolute Temperature value of all Agent [1:0](Fraction bits)

9.276 PECI Absolute Temperature value Register – Index 21h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECI Absolute Temperature Vaule[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Absolute Temperature value of all Agent [9](Sign bit) Absolute Temperature value of all Agent [8:2](Integer bits) Absolute Temperature value of all Agent [1:0](Fraction bits)

9.277 PECI Command Alive Agent and Warning Flag Register – Index 24h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Alive Agent[1:0]		Reserved		Alert Value[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
5	Agent 31 Alive Bit 1: agent31 is able to respond to Ping() command. Agent alive 0: agent31 isn't able to respond to Ping() command. Agent is not alive
4	Agent 30 Alive Bit 1: agent30 is able to respond to Ping() command. Agent alive 0: agent30 isn't able to respond to Ping() command. Agent is not alive
1	Agent31 Alert Bit (Default value is 0) 0: Agent has valid FCS. 1: Agent has invalid FCS in the previous 3 transactions.
0	Agent30 Alert Bit (Default value is 0) 0: Agent has valid FCS. 1: Agent has invalid FCS in the previous 3 transactions.

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9.278 PECI Command Read Data Register – Index 30 ~ 38h (Bank 2)

9.279 PECI Command Read Data 1 Register – Index 30h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.280 PECI Command Read Data 2 Register – Index 31h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.281 PECI Command Read Data 3 Register – Index 32h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.282 PECI Command Read Data 4 Register – Index 33h (Bank 2)

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Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.283 PECI Command Read Data 5 Register – Index 34h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.284 PECI Command Read Data 6 Register – Index 35h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.285 PECI Command Read Data 7 Register – Index 36h (Bank 2)

Attribute: Read only
Size: 8 bits

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BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 7							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.286 PECI Command Read Data 8 Register – Index 37h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.287 PECI Command Read Data 9 Register – Index 38h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

PECI Manual Command Address Table

Command Bank 2	Address CR 10_{HEX}	WriteLength CR 11_{HEX}	Read Length CR 12_{HEX}	Command Code CR 13_{HEX}
Ping	Addr	00	00	
GetDIB		01	08	F7

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Command Bank 2	Address CR 10_{HEX}	WriteLength CR 11_{HEX}	Read Length CR 12_{HEX}	Command Code CR 13_{HEX}
GetTemp		01	02	01
PCIRd30		06	02 / 03 / 05	61
PCIWr30		08 / 09 / 0B	01	65
PCIRdLocal30		05	02 / 03 / 05	E1
PCIWrLocal30		07 / 08 / 0A	01	E5
PKGRd30		05	02 / 03 / 05	A1
PKGWr30		07 / 08 / 0A	01	A5
IAMSRRd30		05	02 / 03 / 05 / 09	B1
IAMSRWr30		07 / 08 / 0A / 0E	01	B5

PECI Manual Command Read Data Table

Command	PCI Rd30	PCI Wr30	PCIRd Local30	PCIWr Local30	PKG Rd30	PKG Wr30	IAMSR Rd30	IAMSR Wr30	GetDIB	GetTemp
Command Code	61	65	E1	E5	A1	A5	B1	B5	F7	01
RdData 1 CR 30_{HEX}	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	X	X
RdData 2 CR 31_{HEX}	X	X	X	X	X	X	Data LSB_1	X	Device Info	X
RdData 3 CR 32_{HEX}	X	X	X	X	X	X	Data LSB_2	X	Revision Number	X
RdData 4 CR 33_{HEX}	X	X	X	X	X	X	Data LSB_3	X	Reserved 1	X
RdData 5 CR 34_{HEX}	X	X	x	X	X	X	Data LSB_4	X	Reserved 2	X
RdData 6 CR 35_{HEX}	Data LSB_1	X	Data LSB_1	X	Data LSB_1	X	Data LSB_5	X	Reserved 3	X
RdData 7 CR 36_{HEX}	Data LSB_2	X	Data LSB_2	X	Data LSB_2	X	Data LSB_6	X	Reserved 4	X
RdData 8 CR 37_{HEX}	Data LSB_3	X	Data LSB_3	X	Data LSB_3	X	Data LSB_7	X	Reserved 5	Temp_LB
RdData 9 CR 38_{HEX}	Data MSB	X	Data MSB	X	Data MSB	X	Data MSB	X	Reserved 6	Temp_HB

Note: X mean don't care

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PECI Manual Command Write Data Table

Command	PCI Rd30	PCI Wr30	PCIRd Local30	PCIWr Local30	PKG Rd30	PKG Wr30	IAMSR Rd30	IAMSR Wr30
Command Code	61	65	E1	E5	A1	A5	B1	B5
WrData 1 CR 14_{HEX}	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID
WrData 2 CR 15_{HEX}	Addr LSB_1	Addr LSB_1	Addr LSB_1	Addr LSB_1	Index	Index	Processor ID	Processor ID
WrData 3 CR 16_{HEX}	Addr LSB_2	Addr LSB_2	Addr LSB_2	Addr LSB_2	Param LSB	Param LSB	Addr LSB	Addr LSB
WrData 4 CR 17_{HEX}	Addr LSB_3	Addr LSB_3	Addr MSB	Addr MSB	Param MSB	Param MSB	Addr MSB	Addr MSB
WrData 5 CR 18_{HEX}	Addr MSB	Addr MSB	X	Data LSB_1	X	Data LSB_1	X	Data LSB_1
WrData 6 CR 19_{HEX}	X	Data LSB_1	X	Data LSB_2	X	Data LSB_2	X	Data LSB_2
WrData 7 CR $1A_{HEX}$	X	Data LSB_2	X	Data LSB_3	X	Data LSB_3	X	Data LSB_3
WrData 8 CR $1B_{HEX}$	X	Data LSB_3	X	Data MSB	X	Data MSB	X	Data LSB_4
WrData 9 CR $1C_{HEX}$	X	Data MSB	X	X	X	X	X	Data LSB_5
WrData10 CR $1D_{HEX}$	X	X	X	X	X	X	X	Data LSB_6
WrData11 CR $1E_{HEX}$	X	X	X	X	X	X	X	Data LSB_7
WrData12 CR $1F_{HEX}$	X	X	X	X	X	X	X	Data MSB

Note: X mean don't care

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9.288 Voltage and Temperature Read Register – Index 00h~0Fh (Bank 3)

Attribute: Read only at VSB domain
Size: 8 bits

ADDRESS 00-0F	DESCRIPTION
00h	CPUVCORE reading
01h	VIN0 reading
02h	AVCC reading
03h	3VCC reading
04h	VIN1 reading
05h	VIN2 reading
06h	RESERVED
07h	3VSB reading.
08h	VBAT reading
09h	V10 reading
0Ah	RESERVED
0Bh	RESERVED
0Ch	SYSTIN
0Dh	CPUTIN
0Eh	AUXTIN
0Fh	RESERVED

9.289 SYSTIN Temperature Sensor Offset Register – Index 11h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSTIN Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.290 CPUTIN Temperature Sensor Offset Register – Index 12h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							

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DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUTIN Temperature Offset Value.** The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.291 AUXTIN Temperature Sensor Offset Register – Index13h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN Temperature Offset Value.** The value in this register is added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.292 Reserved Register – Index 14h ~ 16h (Bank 3)

9.293 Configuration Register – Index 17h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	INITIALIZATION	RESERVED	RESERVED	RESERVED	INT_CLEAR	RESERVED	RESERVED	START
DEFAULT	0				0	0	1	1

BIT	DESCRIPTION
7	**Initialization.** A one restores the power-on default values to some registers. This bit clears itself since the power-on default of this bit is zero.
6	RESERVED
5	RESERVED
4	RESERVED
3	**INT_Clear.** A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
2	**Reserved.**
1	RESERVED
0	**Start.** A one enables startup of monitoring operations. A zero puts the part in standby mode. **Note:** Unlike the "INT_Clear" bit, the outputs of interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred.

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9.294 VBAT Monitor Control Register – Index 18h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				DIODES3	DIODES2	DIODES1	EN_VBAT_MNT
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7-4	**Reserved**
3	**DIODES 3. Sensor type selection for AUXTIN.** 1: Diode sensor. 0: Thermistor sensor. (default)
2	**DIODES 2. Sensor type selection for CPUTIN.** 1: Diode sensor. (default) 0: Thermistor sensor.
1	**DIODES 1. Sensor type selection for SYSTIN.** 1: Diode sensor. 0: Thermistor sensor. (default)
0	**EN_VBAT_MNT.** 1: Enable battery voltage monitor. When this bit changes from zero to one, it takes one monitor cycle time to update the VBAT reading value register. 0: Disable battery voltage monitor.

9.295 Current Mode Enable Register – Index 19h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					EN_AUXTIN CURRENT MODE	EN_CPUTIN CURRENT MODE	EN_SYSTIN CURRENT MODE
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-3	**Reserved.**
2	**Enable AUXTIN Current Mode.** With AUXTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 3 = 1). 1: Temperature sensing of AUXTIN by Current Mode. 0: Temperature sensing of AUXTIN depends on the setting of Index 5Dh and 59h. (Default)
1	**Enable CPUTIN Current Mode.** With CPUTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 2 = 1).

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BIT	DESCRIPTION
	1: Temperature sensing of CPUTIN by Current mode. (Default) 0: Temperature sensing of CPUTIN depends on the setting of Index 5Dh and 59h.
0	**Enable SYSTIN Current Mode.** With SYSTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 1 = 1). 1: Temperature sensing of SYSTIN by Current Mode. 0: Temperature sensing of SYSTIN depends on the setting of Index 5Dh and 59h. (Default)

9.296 Reserved Register – Index 1Ah ~ 8Fh (Bank 3)

9.297 PECI Agent Enable Register – Index 90h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_PECI1	EN_PECI0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**Reserved.**
1	**Enable PECI Agent1 Mode.**
0	**Enable PECI Agent0 Mode.**

9.298 Reserved Register – Index 91h ~ CFh (Bank 3)

9.299 Is<8:1> Current Register – Index D0h (Bank 3)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Is<8:1>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Is<8:1>.** Current measure by current measure IC (1LSB=31.25mA)

9.300 Is<0> Current Register – Index D1h (Bank 3)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

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NAME	Reserved							Is<0>
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	Reserved
0	**Is<0>.** Current measure by current measure IC (1LSB=31.25mA)

9.301 POWER <9:2> Register – Index D2h (Bank 3)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	POWER <9:2>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**POWER <9:2>.** Power calculate by IO (1LSB=0.25W)

9.302 POWER<1:0> Register – Index D3h (Bank 3)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						POWER<1:0>	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	Reserved
1:0	**POWER<1:0>.** Power calculate by IO (1LSB=0.25W)

9.303 VIN Register – Index D4h (Bank 3)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**VIN.** Power voltage given by customer. (1LSB=128mV)

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9.304 Rreg Setting Register – Index D5h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Rreg							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Rreg.** Equivalent electric impedance in order to calculate Is. (1LSB=1m ohm)

9.305 Reg_Ratio_K and POWER_Voltage Enable Register – Index D6h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reg_Ration_K				Reserved			Power_ Volt_En
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**Reg_Ration_K:** The ration in order to make power voltage input to IO is below 2.048. Reg_Ration_K=(R1+R2)/(R1)
3-1	**Reserved**
0	**Power_Volt_En** 0:Power voltage is monitored by IO 1:Power voltage is given by customer

9.306 POWER_V Register – Index D7h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	POWER_V							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**POWER_V:** Power voltage (1LSB=128mV)

9.307 Reserved Register Index D8~FF (Bank3)

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10. FLOPPY DISK CONTROLLER

10.1 FDC Functional Description

The floppy disk controller (FDC) of the NCT6102D / NCT6106D integrates all of the logic required for floppy disk control. The FDC implements a FIFO which provides better system performance in multi-master systems, and the digital data separator supports data rates up to 2 M bits/sec.

The FDC includes the following blocks: Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core. The rest of this section discusses these blocks through the following topics: FIFO, Data Separator, Write Precompensation, Perpendicular Recording mode, FDC core, FDC commands, and FDC registers.

10.1.1 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM (Request fro Master) and DIO (Data Input / Output) bits in the Main Status Register.

The FIFO is defaulted to disabled mode after any form of reset, which maintains PC/AT hardware compatibility. The default values can be changed through the configure command. The advantage of the FIFO is that it lets the system have a larger DMA latency without causing disk errors. The following tables give several examples of the delays with the FIFO. The data are based upon the following formula:

DELAY = THRESHOLD # x (1 / DATA RATE) * 8 – 1.5 μs

Table 10-1 The Delays of the FIFO

FIFO THRESHOLD	MAXIMUM DELAY UNTIL SERVICING AT 500K BPS
	Data Rate
1 Byte	1 x 16 μs – 1.5 μs = 14.5 μs
2 Byte	2 x 16 μs – 1.5 μs = 30.5 μs
8 Byte	8 x 16 μs – 1.5 μs = 6.5 μs
15 Byte	15 x 16 μs – 1.5 μs = 238.5 μs
FIFO THRESHOLD	**MAXIMUM DELAY UNTIL SERVICING AT 1M BPS**
	Data Rate
1 Byte	1 x 8 μs – 1.5 μs = 6.5 μs
2 Byte	2 x 8 μs – 1.5 μs = 14.5 μs
8 Byte	8 x 8 μs – 1.5 μs = 62.5 μs
15 Byte	15 x 8 μs – 1.5 μs = 118.5 μs

At the start of a command, the FIFO is always disabled, and command parameters must be sent based upon the RQM and DIO bit settings in the Main Status Register. When the FDC enters the command execution phase, it clears the FIFO off any data to ensure that invalid data are not transferred.

An overrun or underrun terminates the current command and data transfer. Disk writes complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled by the specify command and are initiated by the FDC when the LDRQ pin is activated during a data transfer command.

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10.1.2 Data Separator

The function of the data separator is to lock onto incoming serial read data. When a lock is achieved, the serial front-end logic in the chip is provided with a clock that is synchronized with the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial-to-parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The control logic generates RDD and RWD for every pulse input, and any data pulse input is synchronized and then adjusted immediately by error adjustment. A digital integrator keeps track of the speed changes in the input data stream.

10.1.3 Write Precompensation

The write precompensation logic minimizes bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and depends on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known, so, depending on the pattern, the bit is shifted either early or late, relative to the surrounding bits.

10.1.4 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. Perpendicular mode requires a 1 Mbps data rate for the FDC, and, at this data rate, the FIFO manages the host interface bottleneck due to the high speed of data transfer to and from the disk.

10.1.5 FDC Core

The NCT6102D / NCT6106D FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor, and the result may be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information are provided to the microprocessor.

The next section introduces each of the commands.

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10.1.6 FDC Commands

Command Symbol Descriptions:

C:	Cylinder Number 0 – 256
D:	Data Pattern
DIR:	Step Direction
	DIR = 0: step out
	DIR = 1: step in
DS0:	Disk Drive Select 0
DS1:	Disk Drive Select 1
DTL:	Data Length
EC:	Enable Count
EFIFO:	Enable FIFO
EIS:	Enable Implied Seek
EOT:	End of Track
FIFOTHR:	FIFO Threshold
GAP:	Gap Length Selection
GPL:	Gap Length
H:	Head Number
HDS:	Head Number Select
HLT:	Head Load Time
HUT:	Head Unload Time
LOCK:	Lock EFIFO, FIFOTHR, and PTRTRK bits to prevent being affected by software reset
MFM:	MFM or FM Mode
MT:	Multitrack
N:	The number of data bytes written in a sector
NCN:	New Cylinder Number
ND:	Non-DMA Mode
OW:	Overwritten
PCN:	Present Cylinder Number
POLL:	Polling Disable
PRETRK:	Precompensation Start Track Number
R:	Record
RCN:	Relative Cylinder Number
R/W:	Read/Write
SC:	Sectors per Cylinder
SK:	Skip deleted data address mark
SRT:	Step Rate Time
ST0:	Status Register 0
ST1:	Status Register 1
ST2:	Status Register 2
ST3:	Status Register 3
WG:	Write gate alters timing of WE

(1) Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command codes

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PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(2) Read Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

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(3) Read A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(4) Read ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in the Data Register
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Disk status after the command has been completed
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

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(5) Verify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
		---------- DTL/SC ----------								
Execution										No data transfer takes place
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(6) Version

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command code
Result	R	1	0	0	1	0	0	0	0	Enhanced controller

(7) Write Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to Command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and the system

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PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Result	R	---------- ST0 ----------								Status information after Command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after Command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(8) Write Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and the system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(9) Format A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- N ----------								Bytes per Sector
	W	---------- SC ----------								Sectors per Cylinder
	W	---------- GPL ----------								Gap 3
	W	---------- D ----------								Filler Byte

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PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Execution for Each Sector: (Repeat)	W	---------- C ----------	Input Sector Parameters
	W	---------- H ----------	
	W	---------- R ----------	
	W	---------- N ----------	
Result	R	---------- ST0 ----------	Status information after command execution
	R	---------- ST1 ----------	
	R	---------- ST2 ----------	
	R	---------- Undefined ----------	
	R	---------- Undefined ----------	
	R	---------- Undefined ----------	
	R	---------- Undefined ----------	

(10) Recalibrate

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt

(11) Sense Interrupt Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	---------- ST0 ----------								Status information at the end of each seek operation
	R	---------- PCN ----------								

(12) Specify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	| ---------SRT ---------- | -------- HUT ---------- |								
	W	|---------- HLT ----------| ND								

(13) Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- NCN ----------								
Execution	R									Head positioned over proper cylinder on the diskette

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(14) Configure

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	------ FIFOTHR ----				
	W		----------PRETRK ----------							
Execution										Internal registers written

(15) Relative Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W		---------- RCN ----------							

(16) Dumpreg

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	Registers placed in FIFO
Result	R	---------- PCN-Drive 0----------								
	R	---------- PCN-Drive 1 ----------								
	R	---------- PCN-Drive 2----------								
	R	---------- PCN-Drive 3 ----------								
	R	--------SRT ---------- | --------- HUT --------								
	R	---------- HLT ----------| ND							
	R	---------- SC/EOT ----------								
	R	LOCK	0	D3	D2	D1	D0	GAP	WG	
	R	0	EIS	EFIFO	POLL	------ FIFOTHR --------				
	R	----------PRETRK ----------								

(17) Perpendicular Mode

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Code
	W	OW	0	D3	D2	D1	D0	GAP	WG	

(18) Lock

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Code
Result	R	0	0	0	LOCK	0	0	0	0	

(19) Sense Drive Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Code

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PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	---------- ST3 ----------								Status information about the disk drive

(20) Invalid

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	---------- Invalid Codes ----------								Invalid codes (no operation-FDC goes to standby state)
Result	R	---------- ST0 ----------								ST0 = 80h

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10.2 Register Descriptions

There are several status, data, and control registers in the NCT6102D / NCT6106D. These registers are defined below, and the rest of this section provides more details about each one of them.

Table 10-2 FDC Registers

ADDRESS OFFSET	REGISTER	
	READ	WRITE
base address + 0	SA REGISTER	
base address + 1	SB REGISTER	
base address + 2		DO REGISTER
base address + 3	TD REGISTER	TD REGISTER
base address + 4	MS REGISTER	DR REGISTER
base address + 5	DT (FIFO) REGISTER	DT (FIFO) REGISTER
base address + 7	DI REGISTER	CC REGISTER

10.2.1 Status Register A (SA Register) (Read base address + 0)

Along with the SB register, the SA register is used to monitor several disk-interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	INIT PENDING	DRV 2#	STEP	TRAK0#	HEAD	INDEX#	WP#	DIR
DEFAULT	0	0	NA	1	NA	1	1	NA

BIT	DESCRIPTION
7	**INIT PENDING**. Indicates the value of the floppy disk interrupt output.
6	**DRV2#.** 0: A second drive has been installed. 1: A second drive has not been installed.
5	**STEP.** Indicates the complement of the STEP# output.
4	**TRAK0#.** Indicates the value of the TRAK# input.
3	**HEAD.** Indicates the complement of the HEAD# output. 0: Side 0. 1: Side 1.
2	**INDEX#.** Indicates the value of the INDEX# output.
1	**WP#.** 0: The disk is write-protected. 1: The disk is not write-protected.
0	**DIR.** Indicates the direction of head movement. 0: Outward direction. 1: Inward direction.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:

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BIT	7	6	5	4	3	2	1	0
NAME	INIT PENDING	DRQ	STEP F/F	TRAK0	HEAD#	INDEX	WP	DIR#
DEFAULT	0	0	NA	0	NA	0	0	NA

BIT	DESCRIPTION
7	**INIT PENDING.** Indicates the value of the floppy disk interrupt output.
6	**DRQ.** Indicates the value of the DRQ output pin.
5	**SETP F/F.** indicates the complement of latched STEP# output.
4	**TRAK0.** Indicates the complement of the TRAK0# input.
3	**HEAD#.** Indicates the value of the HEAD# output. 0: Side 1. 1: Side 0.
2	**INDEX.** Indicates the complement of the INDEX# output.
1	**WP.** 0: The disk is not write-protected. 1: The disk is write-protected.
0	**DIR#.** Indicates the direction of the head movement. 0: Inward direction. 1: Outward direction.

10.2.2 Status Register B (SB Register) (Read base address + 1)

Along with the SA register, the SB register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Drive SEL0	WDTA Toggle	RDTA Toggle	WE	Reserved	MOT EN A
DEFAULT	1	1	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Reserved.**
5	**Drive SEL0.** Indicates the status of the DO Register, bit 0 (drive-select bit 0).
4	**WDATA Toggle.** Changes state on every rising edge of the WD# output pin.
3	**RDATA Toggle.** Changes state on every rising edge of the RDATA# output pin.
2	**WE.** Indicates the complement of the WE# output pin.
1	**Reserved.**
0	**MOT EN A.** Indicates the complement of the MOA# output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DSA#	WD F/F	RDATA	WE F/F	DSD#	DSC#

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					F/F			
DEFAULT	0	1	1	0	0	0	1	1

BIT	DESCRIPTION
7-6	**Reserved.**
5	**DSA#.** This bit indicates the status of the DSA# output pin.
4	**WD F/F.** Indicates the complement of the WD# output pin, which is latched on every rising edge of the WD# output pin.
3	**RDATA F/F.** Indicates the complement of the latched RDATA# output pin.
2	**WE F/F.** Indicates the complement of the latched WE# output pin.
1	**DSD#.** 0: Drive D has been selected. 1: Drive D has not been selected.
0	**Reserved.**

10.2.3 Digital Output Register (DO Register) (Write base address + 2)

The Digital Output Register is a write-only register that controls drive motors, drive selection, DRQ/IRQ enable, and FDC reset. All the bits in this register are cleared by the MR pin. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			MOTOR ENABLE A	DMA&INT ENABLE	FDC RESET	DRIVE SELECT	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.**
4	**MOTOR ENABLE A.** A logical 1 enables Motor A.
3	**DMA & INT ENABLE.** A logical 1 enables DRQ/IRQ.
2	**FDC RESET.** Floppy Disk Controller Reset. A logical 0 resets the FDC.
1-0	**DRIVE SELECT.** **Bits** **1 0** 0 0: Select Drive A. 0 1: Select Drive B. 1 0: Select Drive C. 1 1: Select Drive D.

10.2.4 Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information for the floppy disk drive.

In normal floppy mode, this register only has bits 0 and 1, and the bit definitions are as follows:

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BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						Tape sel 1	Tape sel 0
DEFAULT	NA	NA	NA	NA	NA	NA	0	0

BIT	DESCRIPTION
7-2	**RESERVED.**
1	**Tape sel 1.**
0	**Tape sel 0.**

If the three-mode FDD function is enabled (EN3MODE = 1 in LD0 CRF0, Bit 0), the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Media ID1	Media ID0	Drive Type ID1	Drive Type ID0	Floppy Boot Drive 1	Floppy Boot Drive 0	Tape Sel 1	Tape Sel 0
DEFAULT	0	0	1	1	0	0	0	0

BIT	DESCRIPTION	
7	**Media ID1.** Read only. Reflects the value of LD0, CRF1, bit 5.	
6	**Media ID0.** Read only. Reflects the value of LD0, CRF1, bit 4.	
5	**Drive Type ID1.**	Reflect the bit in LD0, CR[F2h]. Which bit is reflected depends on the last drive selected in the PO register.
4	**Drive Type ID0.**	
3	**Floppy Boot Drive 1.** Reflects the value of LD0, CRF1, bit 7.	
2	**Floppy Boot Drive 0.** Reflects the value of LD0, CRF1, bit 6.	
1	**Tape Sel 1.**	Assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved for the floppy disk boot drive.
0	**Tape Sel 0.**	

TAPE SEL 1	TAPE SEL 0	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

10.2.5 Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RQM	DIO	Non-DMA	FDC Busy	RESRVED			FDD 0

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			mode					Busy
DEFAULT	0	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**Request for Master (RQM).** A high on this bit indicates Data Register is ready to send or receive data to or from the processor.
6	**DATA INPUT/OUTPUT (DIO).** If DIO = HIGH, then the transfer is from Data Register to the processor. If DIO = LOW, the transfer is from processor to Data Register.
5	**Non-DMA mode.** The FDC is in the non-DMA mode, this bit is set only during the execution phase in non-DMA mode.
4	**FDC Busy** (CB). A read or write command is in the process when CB = HIGH.
3-1	**Reserved.**
0	**FDD 0 Busy.** (D0B = 1) FDD number 0 is in the SEEK mode.

10.2.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. However, in PC-AT and PS/2 Model 30 and PS/2 modes, the data rate is controlled by the CC register, not by the DR register. As a result, the real data rate is determined by the most recent write to either the DR or CC register. The bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	S/W RESET	POWER DOWN	RESERVED	PRECOMP2	PRECOMP1	PRECOMP0	DRATE1	DRATE0
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION	
7	**S/W RESET.** The software reset bit.	
6	**POWER DOWN.** 0: FDC in normal mode. 1: FDC in power-down mode.	
5	**RESERVED.**	
4	**PRECOMP 2.**	Selects the value of write precompensation. The following tables show the precompensation values for every combination of these bits. Please see the tables below.
3	**PRECOMP 1.**	
2	**PRECOMP 0.**	
1	**DRATE 1.**	Select the data rate of the FDC and reduced write-current control. **Bits** **1 0** 0 0: 500 KB/S (MFM), 250 KB/S (FM),

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BIT	DESCRIPTION	
0	**DRATE 0.**	RWC# = 1 0 1: 300 KB/S (MFM), 150 KB/S (FM), RWC# = 0 1 0: 250 KB/S (MFM), 125 KB/S (FM), RWC# = 0 1 1: 1 MB/S (MFM), Illegal (FM), RWC# = 1

The 2 MB/S data rate for the tape drive is only supported by setting DRATE1 and DRATE0 to 01, as well as setting DRT1 and DRT0 (CRF4 and CRF5 for logical device 0) to 10. Please see the functional description of CRF4 or CRF5 and the data rate table for individual data-rate settings.

PRECOMP	PRECOMPENSATION DELAY	
2 1 0	250K – 1 Mbps	2 Mbps Tape drive
0 0 0	Default Delays	Default Delays
0 0 1	41.67 ns	20.8 ns
0 1 0	83.34 ns	41.17 ns
0 1 1	125.00 ns	62.5ns
1 0 0	166.67 ns	83.3 ns
1 0 1	208.33 ns	104.2 ns
1 1 0	250.00 ns	125.00 ns
1 1 1	0.00 ns (disabled)	0.00 ns (disabled)

DATA RATE	DEFAULT PRECOMPENSATION DELAYS
250 KB/S	125 ns
300 KB/S	125 ns
500 KB/S	125 ns
1 MB/S	41.67ns
2 MB/S	20.8 ns

10.2.7 FIFO Register (R/W base address + 5)

The FIFO register consists of four status registers in a stack, and only one register is presented to the data bus at a time. The FIFO register stores data, commands, and parameters, and it provides disk-drive status information. In addition, data bytes pass through the data register to program or obtain results after a command. In the NCT6102D / NCT6106D, this register is disabled after reset. The FIFO can enable it and change its values through the CONFIGURE command.

BIT	7	6	5	4	3	2	1	0
NAME	IC		SE	EC	NR	HD	US1, US0 Drive Select	

Status Register 0 (ST0)

BIT	DESCRIPTION
7-6	**IC (Interrupt Code).** **Bits** **7 6**

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BIT	DESCRIPTION
	0 0: Normal termination of the command. 0 1: Abnormal termination of the command. 1 0: Invalid command issue. 1 1: Abnormal termination because the ready signal from FDD changed state during command execution.
5	**SE (Seek End).** 1: Seek end. 0: Seek error.
4	**EC (Equipment Check).** 1: When a fault signal is received from the FDD or the track. Signal fails to occur after 77 step pulses. 0: No error.
3	**NR (Not Ready).** 1: Drive is not ready. 0: Drive is ready.
2	**HD Head Address. (The current head address)** 1: Head selected. 0: Head selected.
1-0	**US 1, US0 Drive Select.** **Bits** **1 0** 0 0: Drive A selected. 0 1: Drive B selected. 1 0: Drive C selected. 1 1: Drive D selected.

Status Register 1 (ST1)

BIT	7	6	5	4	3	2	1	0
NAME	EN	Reserved	OE	OR	Reserved	ND	NW	MAM

BIT	DESCRIPTION
7	**EN (End of Track).** 1 will be written to this bit if the FDC tries to access a sector beyond the final sector or a cylinder.
6	Reserved. This bit is always 0.
5	**DE (Data Error).** 1 will be written to this bit if the FDC detects a CRC error in either the ID field or the data field.
4	**OR (Over Run).** 1 will be written to this bit if the FDC is not served by the host system within a certain time interval during data transfer.
3	Reserved. This bit is always 0.
2	**ND (No Data).** 1 will be written to this bit if the specified sector cannot be found during execution of a read, write or verity data.
1	**NW (Not Writable).** 1 will be written to this bit if a write protect signal is detected from the diskette drive during execution of write data.
0	**MAM (Missing Address Mark).** 1 will be written to this bit if the FDC cannot detect the data address mark or the data address mark has been deleted.

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Status Register 2 (ST2)

BIT	7	6	5	4	3	2	1	0
NAME	NOT USED	CM	DD	WC	SH	SN	BC	MD

BIT	DESCRIPTION
7	Not used. This bit is always 0.
6	**CM (Control Mark).** 1: During execution of the read data or scan command. 0: No error.
5	**DD (Data error in the Data field).** 1: If the FDC detects a CRC error in the data field. 0: No error.
4	**WC (Wrong Cylinder).** 1: Indicates wrong cylinder.
3	**SH (Scan Equal Hit).** 1: During execution of the Scan command, if the equal condition is satisfied. 0: No error.
2	**SN (Scan Not Satisfied).** 1: During execution of the Scan command. 0: No error.
1	**BC (Bad Cylinder).** 1: Bad Cylinder. 0: No error.
0	**MD (Missing Address Mark in Data Field).** 1: If FDC cannot find a data address mark (or the address mark has been deleted) when reading data from the media. 0: No error.

Status Register 3 (ST3)

BIT	7	6	5	4	3	2	1	0
NAME	FT	WP	RY	T0	TS	HD	US1	US0

BIT	DESCRIPTION
7	**FT.** Fault.
6	**WP.** Write protected.
5	**RY.** Ready.
4	**T0.** Track 0.
3	**TS.** Two-side.
2	**HD.** Head Address.
1	**US1.** Unit Select 1.
0	**US0.** Unit Select 0.

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10.2.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit, read-only register used for diagnostic purposes. In PC/XT or PC/AT mode, only bit 7 is checked by the BIOS. When the register is read, bit 7 shows the complement of DSKCHG#, while the other bits remain in tri-state. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG	RESERVED						
DEFAULT	0	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DSKCHG.**
6-0	**RESERVED.** Reserved for the hard disk controller. During a read of this register, these bits are in tri-state.

In PS/2 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG	RESERVED				DRATE1	DRATE0	HIGH DENS#
DEFAULT	0	1	1	1	1	1	0	1

BIT	DESCRIPTION	
7	**DSKCHG.** Indicates the complement of the DSKCHG# input.	
6-3	**RESERVED.** Always 1 during a read.	
2	**DRATE 1.**	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.
1	**DRATE 0.**	
0	**HIGHDENS#.** 0: 500 KB/S or 1 MB/S data rate (high-density FDD). 1: 250 KB/S or 300 KB/S data rate.	

In PS/2 Model 30 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG#	RESERVED			DMAEN	NOPREC	DRATE1	DRATE0
DEFAULT	1	0	0	0	0	0	1	0

BIT	DESCRIPTION
7	**DSKCHG.** Indicates the status of the DSKCHG# input.
6-4	**RESERVED.** Always 0 during a read.
3	**DMAEN.** Indicates the value of DO register, bit 3.

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2	**NOPREC.** Indicates the value of the NOPREC bit in the CC REGISTER.	
1	**DRATE 1.**	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address +4)) for how the settings correspond to individual data rates.
0	**DRATE 0.**	

10.2.9 Configuration Control Register (CC Register) (Write base address + 7)

This register is used to control the data rate. In PC/AT and PS/2 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						DRATE1	DRATE0
DEFAULT	NA	NA	NA	NAN	NA	NA	1	0

BIT	DESCRIPTION	
7-2	**RESERVED.** Should be set to 0.	
1	**DRATE 1.**	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address +4)) for how the settings correspond to individual data rates.
0	**DRATE 0.**	

In the PS/2 Model 30 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					NOPREC	DRATE1	DRATE0
DEFAULT	NA	NA	NA	NA	NA	0	1	0

BIT	DESCRIPTION	
7-3	**RESERVED.** Should be set to 0.	
2	**NOPREC.** Disables the precompensation function. This bit can be set by the software.	
1	**DRATE1.**	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.
0	**DRATE0.**	

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11. UART PORT

NCT6102D supports 2 UART – UART A and UART B.
NCT6106D supports 6 UART – UART A, UART B, UART C, UART D, UART E and UART F.

11.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.

BIT	7	6	5	4	3	2	1	0
NAME	BDLAB	SSE	PBFE	EPE	PBE	MSBE	DLS1	DLS0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**BDLAB (Baud Rate Divisor Latch Access Bit).** When this bit is set to logic 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logic 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.
6	**SSE (Set Silence Enable).** A logic 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.
5	**PBFE (Parity Bit Fixed Enable).** When PBE and PBFE of UCR are both set to logic 1, (1) if EPE is logic 1, the parity bit is logical 0 when transmitting and checking; (2) if EPE is logic 0, the parity bit is logical 1 when transmitting and checking.
4	**EPE (Even Parity Enable).** When PBE is set to logic 1, this bit counts the number of logic 1's in the data word bits and determines the parity bit. When this bit is set to logic 1, the parity bit is set to logic 1 if an even number of logic 1's are sent or checked. When the bit is set to logic 0, the parity bit is logic 1, if an odd number of logic 1's are sent or checked.
3	**PBE (Parity Bit Enable).** When this bit is set to logic 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.
2	**MSBE (Multiple Stop Bit Enable).** Defines the number of stop bits in each serial character that is transmitted or received. (1) If MSBE is set to logic 0, one stop bit is sent and checked. (2) If MSBE is set to logic 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked. (3) If MSBE is set to logic 1 and the data length is 6, 7, or 8 bits, two stop bits are sent and checked.
1	**DLS1 (Data Length Select Bit 1).** Defines the number of data bits that are sent or checked in each serial character.
0	**DLS0 (Data Length Select Bit 0).** Defines the number of data bits that are sent or checked in each serial character.

DLS1	DLS0	DATA LENGTH
0	0	5 bits

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DLS1	DLS0	DATA LENGTH
0	1	6 bits
1	0	7 bits
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Table 11-1 Register Summary for UART

Register Address Base			Bit Number							
			0	1	2	3	4	5	6	7
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 Mode.

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11.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.

BIT	7	6	5	4	3	2	1	0
NAME	RF EI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
DEFAULT	0	1	1	0	0	0	0	0

BIT	DESCRIPTION
7	**RF EI (RX FIFO Error Indication).** In 16450 mode, this bit is always set to logical 0. in 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop0bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.
6	**TSRE (Transmitter Shift Register Empty).** In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.
5	**TBRE (Transmitter Buffer Register Empty).** In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI of ICR is high, and interrupt is generated to notify the CPU to write next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.
4	**SBD (Silent Byte Detected).** This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
3	**NSER (No Stop Bit Error).** This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
2	**PBER (Parity Bit Error).** This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
1	**OER (Overrun Error).** This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.
0	**RDR (RBR Data Ready).** This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

11.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			INTERNAL LOOPBACK ENABLE	IRQ ENABLE	LOOPBACK RI INPUT	RTS	DTR
DEFAULT	0	0	0	0	0	0	0	0

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BIT	DESCRIPTION
7-5	**Reserved.**
4	**Internal Loopback Enable.** When this bit is set to logic 1, the UART enters diagnostic mode, as follows: (1) SOUT is forced to logic 1, and SIN is isolated from the communication link. (2) The modem output pins are set to their inactive state. (3) The modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) →DSR#, RTS (bit 1 of HCR) →CTS#, Loopback RI input (bit 2 of HCR) → RI# and IRQ enable (bit 3 of HCR) →DCD#. Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.
3	**IRQ Enable.** The UART interrupt output is enabled by setting this bit to logic 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.
2	**Loopback RI Input.** This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.
1	**RTS (Request to Send).** This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.
0	**DTR (Data Terminal Ready).** This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

11.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins used with handshake peripherals such as modems and records changes on these pins.

BIT	7	6	5	4	3	2	1	0
NAME	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
DEFAULT	NA	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DCD (Data Carrier Detect).** This bit is the inverse of the DCD# input and is equivalent to bit 3 of HCR in Loopback mode.
6	**RI (Ring Indicator).** This bit is the inverse of the RI# input and is equivalent to bit 2 of HCR in Loopback mode.
5	**DSR (Data Set Ready).** This bit is the inverse of the DSR# input and is equivalent to bit 0 of HCR in Loopback mode.
4	**CTS (Clear to Send).** This bit is the inverse of the CTS# input and is equivalent to bit 1 of HCR in Loopback mode.
3	**TDCD (DCD# Toggling).** This bit indicates that the state of the DCD# pin has changed after HSR is read by the CPU.
2	**FERI (RI Falling Edge).** This bit indicates that the RI# pin has changed from low to high after HSR is read by the CPU.
1	**TDSR (DSR# Toggling).** This bit indicates that the state of the DSR# pin has changed after HSR is read by the CPU.
0	**TCTS (CTS# Toggling).** This bit indicates that the state of the CTS# pin has changed

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BIT	DESCRIPTION
	after HSR is read by the CPU.

11.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	MSB	LSB	RESERVED		DMA MODE SELECT	TRANSMITTER FIFO RESET	RECEIVER FIFO RESET	FIFO ENABLE
DEFAULT	0	0	NA	NA	0	0	0	0

BIT	DESCRIPTION	
7	**MSB (RX Interrupt Active Level).**	These two bits are used to set the active level of the receiver FIFO interrupt. The active level is the number of bytes that must be in the receiver FIFO to generate an interrupt.
6	**LSB (RX Interrupt Active Level).**	
5-4	**RESERVED.**	
3	**DMS MODE SELECT.** When this bit is set to logic 1, DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.	
2	**TRANSMITTER FIFO RESET.** Setting this bit to logic 1 resets the TX FIFO counter logic to its initial state.	
1	**RECEIVER FIFO RESET.** Setting this bit to logic 1 resets the RX FIFO counter logic to its initial state.	
0	**FIFO ENABLE.** This bit enables 16550 (FIFO) mode. This bit should be set to logic 1 before other UFR bits are programmed.	

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

11.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status.

BIT	7	6	5	4	3	2	1	0
NAME	FIFOS ENABLED		RESERVED		INTERRUPT STATUS BIT 2	INTERRUPT STATUS BIT 1	INTERRUPT STATUS BIT 0	0 IF INTERRUPT PENDING

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DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION	
7-6	**FIFOS ENABLED.** Set to logical 1 when UFR, bit 0 = 1.	
5-4	**RESERVED.**	
3	**INTERRUPT STATUS BIT 2.** In 16450 mode, this bit is logical 0. In 16550 mode, bits 3 and 2 are set to logical 1 when a time-out interrupt is pending. Please see the table below.	
2	**INTERRUPT STATUS BIT 1.**	These two bits identify the priority level of the pending interrupt, as shown in the table below.
1	**INTERRUPT STATUS BIT 0.**	
0	**0 IF INTERRUPT PENDING.** This bit is logic 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.	

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

11.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.

BIT	7	6	5	4	3	2	1	0
NAME	En_address_byte	RX_ctrl	RESERVED		EHSRI	EUSRI	ETBREI	ERDRI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En_address_byte.** 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1)

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BIT	DESCRIPTION
	1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	**RX_ctrl.** 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)
5-4	**RESERVED.**
3	**EHSRI (Handshake Status Interrupt Enable).** Set this bit to logical 1 to enable the handshake status register interrupt.
2	**EUSRI (UART Receive Status Interrupt Enable).** Set this bit to logical 1 to enable the UART status register interrupt.
1	**ETBREI (TBR Empty Interrupt Enable).** Set this bit to logical 1 to enable the TBR empty interrupt.
0	**ERDRI (RBR Data Ready Interrupt Enable).** Set this bit to logical 1 to enable the RBR data ready interrupt.

11.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divide it by a divisor from 1 to (2^{16} –1). The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (CR0C, bits 7 and 6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. As a result, in high-speed mode, the data transmission rate can be as high as 1.5M bps.

BAUD RATE FROM DIFFERENT PRE-DIVIDER			
Pre-Div: 13 1.8461M Hz	Pre-Div: 1.0 24M Hz	Decimal divisor used to generate 16X clock	Error Percentage
50	650	**2304**	**
75	975	**1536**	**
110	1430	**1047**	0.18%
134.5	1478.5	**857**	0.099%
150	1950	**768**	**
300	3900	**384**	**
600	7800	**192**	**
1200	15600	**96**	**
1800	23400	**64**	**
2000	26000	**58**	0.53%
2400	31200	**48**	**
3600	46800	**32**	**
4800	62400	**24**	**
7200	93600	**16**	**
9600	124800	**12**	**
19200	249600	**6**	**

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BAUD RATE FROM DIFFERENT PRE-DIVIDER			
38400	499200	3	**
57600	748800	2	**
115200	1497600	1	**

** Unless specified, the error percentage for all of the baud rates is 0.16%.
Note: Pre-Divisor is determined by CRF0 of UART A.

11.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

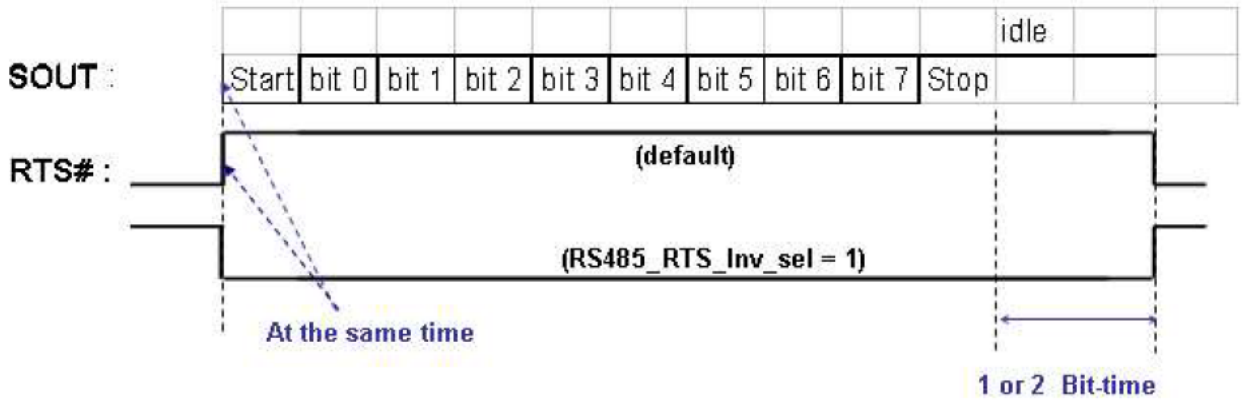
11.10 Extendding FIFO

We support FIFO size extending to 32bytes for RX and TX block. (Enable bit: CRF8, Bit0)

11.11 UART RS485 Auto Flow Control

NCT6102D / NCT6106D supports RS485 auto flow control function for UARTA ~ UARTF. When enabling the RS485 auto control function, it will automatically drive RTS# pin to logic high or low for UARTA ~ UARTF when UART TX block transmits the data.

The diagram shown below illustrates the RS485 auto flow control function for UARTA ~ UARTF.



The default behavior of RTS# pin will drive logic high the time edge between **Start bit** and **bit0** when the UART TX Block start to transmits the data on SOUT pin. Then the RTS# pin will drive logic low later than **Stop bit** about 1 or 2 Bit-Time when UART TX Block completes the data transmission. The driving behavior of RTS# will be inverted when we set RS485_RTS_inv_sel bit = 1'b1. (Bit-time: Depends on the baud rate of transmission)

The bellowing control register table relates to the RS485 auto flow control function for UARTA ~ UARTF.

	UARTA	UARTB	UARTC	UARTD	UARTE	UARTF
RTS485_enable	Logic Device 2, CRF2_Bit1	Logic Device 3, CRF2_Bit1	Logic Device 10, CRF2_Bit1	Logic Device 11, CRF2_Bit1	Logic Device 12, CRF2_Bit1	Logic Device 13, CRF2_Bit1

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RTS485_inv_sel	Logic Device 2, CRF2_Bit4	Logic Device 3, CRF2_Bit4	Logic Device 10, CRF2_Bit4	Logic Device 11, CRF2_Bit4	Logic Device 12, CRF2_Bit4	Logic Device 13, CRF2_Bit4
RST_low_time_sel	Logic Device 2, CRF2_Bit5	Logic Device 3, CRF2_Bit5	Logic Device 10, CRF2_Bit5	Logic Device 11, CRF2_Bit5	Logic Device 12, CRF2_Bit5	Logic Device 13, CRF2_Bit5

11.12 UART 9BIT-MODE

11.12.1 Function Dscription

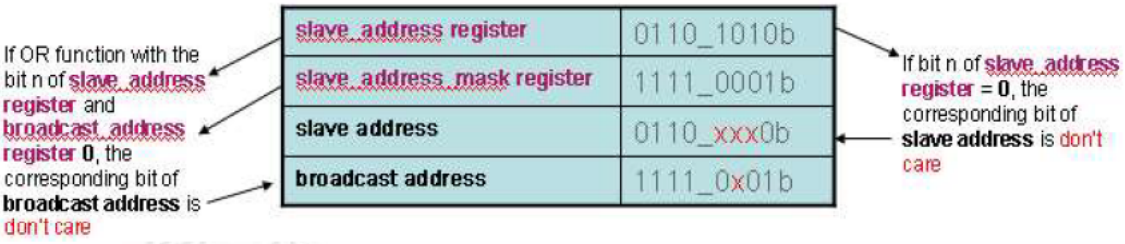
► **Tx function block:**

1. 9bit-TX block supports 9bit-mode or original RS232 mode TX signal output.
2. 9bit-TX block supports sending address byte
   (Setting **En_9bit_mode =1** and **En_address_byte =1** will force parity bit turned to high bit)
3. 9bit-TX block supports 9bit-mode RS485 RTS or original RS232 mode RTS signal output.
4. 9bit-TX block supports 9bit-mode inverted and time selected for the RS485 RTS signal.
   (RS485 RTS time selected: one or two TXC period)
5. 9bit-TX block supports clear "en_address_byte" bit automatic.

	Register location (UART A) Logic Device 2	**Register location (UART B) Logic Device 3**	**Register location (UART C) Logic Device 10**	**Register location (UART D) Logic Device 11**	**Register location (UART E) Logic Device 12**	**Register location (UART F) Logic Device 13**
En_address_byte	03f9, Bit7 (default)	02f9, Bit7 (default)	03f9, Bit7 (default)	03f9, Bit7 (default)	03f9, Bit7 (default)	03f9, Bit7 (default)

► **Rx function block:**

1. 9bit-RX block supports 9bit-mode or original RS232 mode RX signal output.
2. 9bit-RX block supports comparison between with the slave address and broadcast address byte determined by the two registers. (see blow: slave_address and slave_address_mask registers)



3. 9bit-RX block supports received address byte pass into RX block FIFO.
4. 9bit-RX block supports UART 9bit-mode IRQ output and could select to be issued only when receiving any address bytes or only received address matched.
5. 9bit-RX block will automatic modify parity bit of address/data byte to meet parity check from UART receiver block when using 9bit-bit mode.
6. 9bit-RX block supports different mode that have different functions by setting RX_ctrl_set[2:0].

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(default: RX_ctrl_set[2:0] = 000)

	Register location (UART A) Logic Device 2	Register location (UART B) Logic Device 3	Register location (UART C) Logic Device 10	Register location (UART D) Logic Device 11	Register location (UART E) Logic Device 12	Register location (UART F) Logic Device 13
RX_ctrl_set[2]: (en_auto_only_addr_comp)	CRF2_B6	CRF2_B6	CRF2_B6	CRF2_B6	CRF2_B6	CRF2_B6
RX_ctrl_set[1]: (en_auto_RX_ctrl)	CRF2_B7	CRF2_B7	CRF2_B7	CRF2_B7	CRF2_B7	CRF2_B7
RX_ctrl_set[0]: (RX_ctrl)	03f9, Bit6 (default)	02f9, Bit6 (default)	03f9, Bit6 (default)	03f9, Bit6 (default)	03f9, Bit6 (default)	03f9, Bit6 (default)

RX_ctrl_set[2:0]	Function Description
000	1. 9bitmode RX block function will pass all data or address bytes to UART receiver block directly. 2. 9bitmode RX block function will not compare any address byte. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
001	1. 9bitmode RX block function will only pass address bytes to UART receiver block. 2. 9bitmode RX block function will not compare any address byte. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
010	1. 9bitmode RX block function will update RX_ctrl Bit automatically. When RX_ctrl = 0: If receive address byte, 9bitmode RX block function will update RX_ctrl=1 automatically. In order to receive address byte at next byte cycle. (RX block function will ignore the current address byte. Then the transmitter needs to resend this address byte again.) 2. 9bitmode RX block function will compare the address byte automatically and will pass the matched address or not depending on CRF2_B2 setting. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
011	1. 9bitmode RX block function will update RX_ctrl Bit automatically. When RX_ctrl = 1: If address byte matched, 9bitmode RX block function will update RX_ctrl=0 automatically. In order to receive data byte at next byte cycle.

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RX_ctrl_set[2:0]	Function Description
	2. 9bitmode RX block function will compare the address byte automatically and will pass the matched address or not depending on CRF2_B2 setting. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
100 (The same as 000)	1 9bitmode RX block function will pass all data or address bytes to UART receiver block directly. 2 9bitmode RX block function will not compare any address byte. 3 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
101 (The same as 001)	1. 9bitmode RX block function will only pass address bytes to UART receiver block. 2. 9bitmode RX block function will not compare any address byte. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
110	1. 9bitmode RX block function will not update RX_ctrl Bit automatically. When RX_ctrl = 0: If receive address byte, in order to receive the address byte, we need set RX_ctrl = 1 manually. 2. 9bitmode RX block function will compare the address byte automatically and will pass the matched address or not depending on CRF2_B2 setting. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
111	1. 9bitmode RX block function will not update RX_ctrl Bit automatically. When RX_ctrl = 1: If address byte matched, in order to receive the proceeding data bytes, we need set RX_ctrl = 0 manually. 2. 9bitmode RX block function will compare the address byte automatically and will pass the matched address or not depending on CRF2_B2 setting. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)

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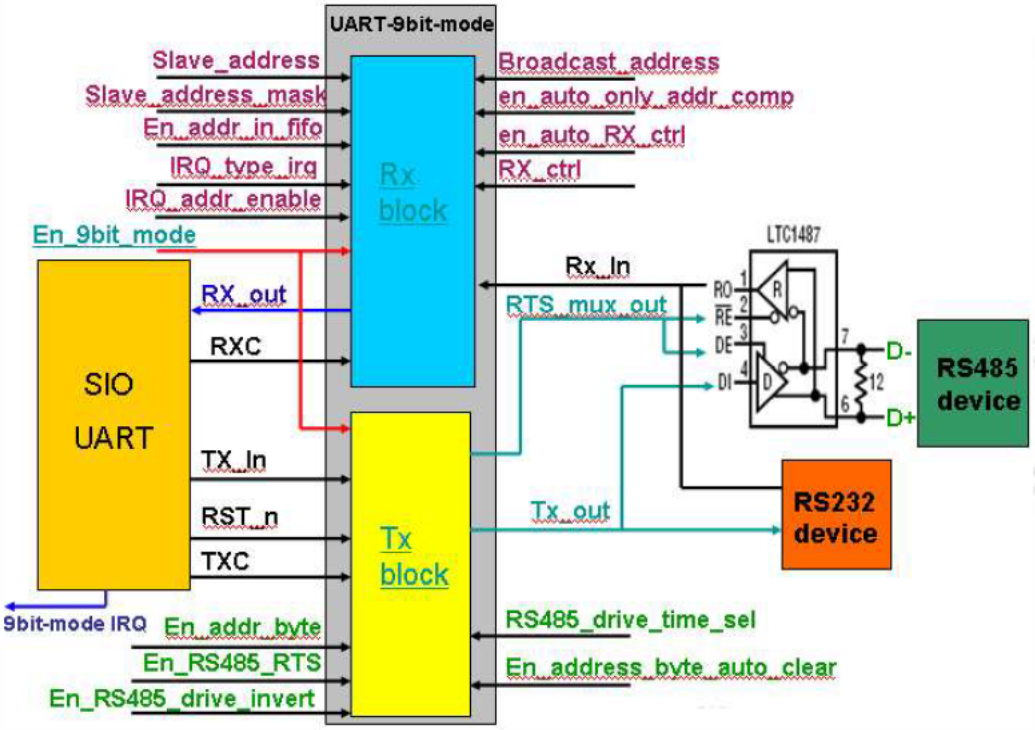
11.12.2 Function Block



11.13 UART switch

Due to the limitation length of the cable for the communication of UART,

We support 3 sets of switches to fix this limitation. They are UARTAB, UARTCD and UARTEF switches.

Switch Name	Switch Enable Bit	Description
UARTAB switch	Logic Device 02, IndexF8_Bit4	Conection with UARTA and UARTB
UARTCD switch	Logic Device 10, IndexF8_Bit4	Conection with UARTC and UARTD
UARTEF switch	Logic Device 12, IndexF8_Bit4	Conection with UARTE and UARTF

For example, if computer A and computer B will transfer data to each other with UART, but the distance between computer A and B is over the limitation length of the cable. See the figure11.13.1, the cable 1 is over the limitation.

And we could use uart switch to fix this limitation. If the switch of computer1 is enabled, computer A could transfer data to computer 1 and computer 1 would bypass the data to computer B. In the same method, computer B also could achieve the goal to transfer data to computer A.

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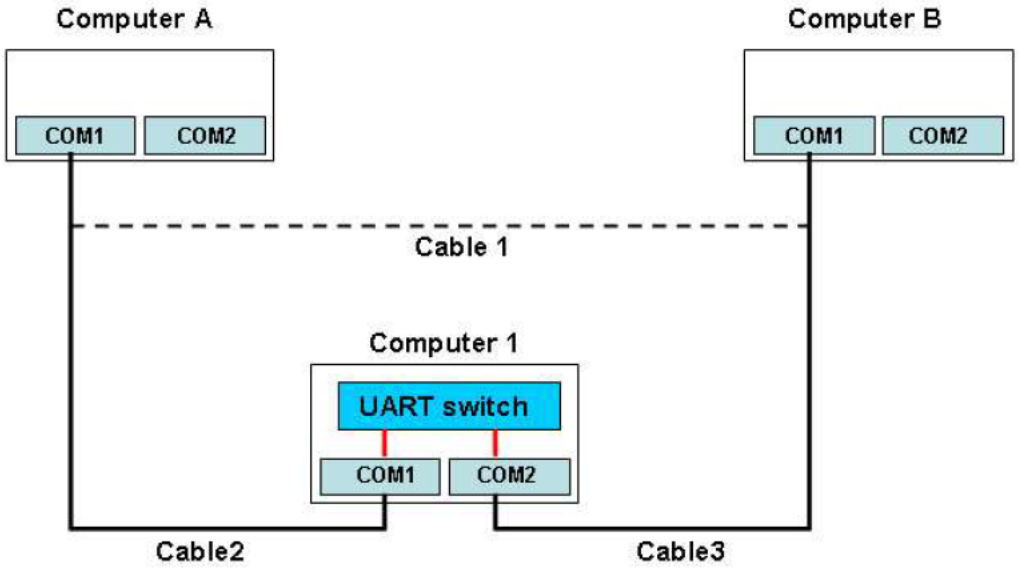
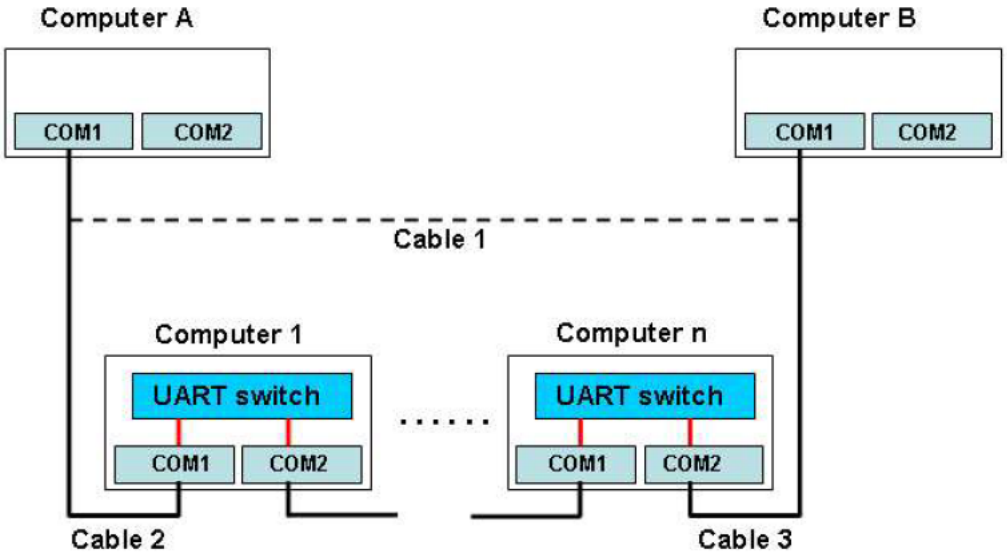


The connection of UART switch with single computer

We also could connect mult-switch to fix the limitataion length of the cable, if the distance between computer A and computer B is too far. Figure 11.13.2 shows the connection method of multi-switch.



The connection of UART switch with multi-computer

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12. PARALLEL PORT

12.1 Printer Interface Logic

The NCT6102D / NCT6106D parallel port can be attached to devices that accept eight bits of parallel data at standard TTL level. The NCT6102D / NCT6106D supports the IBM XT/AT compatible parallel port (SPP), the bi-directional parallel port (BPP), the Enhanced Parallel Port (EPP), and the Extended Capabilities Parallel Port (ECP).

The following tables show the pin definitions for different modes of the parallel port.

Table 12-1 Pin Descriptions for SPP, EPP, and ECP Modes

HOST CONNECTOR	PIN NUMBER OF NCT6102D / NCT6106D	PIN ATTRIBUTE	SPP	EPP	ECP
1	47	O	Nstb	nWrite	nSTB, HostClk[2]
2-9	35-42	I/O	PD<7:0>	PD<7:0>	PD<7:0>
10	34	I	nACK	Intr	nACK, PeriphClk[2]
11	33	I	BUSY	nWait	BUSY, PeriphAck[2]
12	32	I	PE	PE	Peerror, nAckReverse[2]
13	31	I	SLCT	Select	SLCT, Xflag[2]
14	46	O	Nafd	nDStrb	nAFD, HostAck[2]
15	45	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	44	O	Ninit	nInit	nINIT[1], nReverseRqst[2]
17	43	O	nSLIN	nAStrb	nSLIN[1], ECPMode[2]

Notes:
n<name > : Active Low
1. Compatible Mode
2. High Speed Mode
3. For more information, please refer to the IEEE 1284 standard.

HOST CONNECTOR	PIN NUMBER OF NCT6102D / NCT6106D	PIN ATTRIBUTE	SPP
1	47	O	nSTB
2	42	I/O	PD0
3	41	I/O	PD1
4	40	I/O	PD2
5	39	I/O	PD3
6	38	I/O	PD4
7	37	I/O	PD5
8	36	I/O	PD6
9	35	I/O	PD7
10	34	I	nACK
11	33	I	BUSY
12	32	I	PE
13	31	I	SLCT
14	46	O	nAFD

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HOST CONNECTOR	PIN NUMBER OF NCT6102D / NCT6106D	PIN ATTRIBUTE	SPP
15	45	I	nERR
16	44	O	nINIT
17	43	O	nSLIN

12.2 Enhanced Parallel Port (EPP)

The following table lists the registers used in the EPP mode and identifies the bit map of the parallel port and EPP registers. Some of the registers are used in other modes as well.

Table 12-2 EPP Register Addresses

A2	A1	A0	REGISTER	NOTE
0	0	0	Data pot (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:
1. These registers are available in all modes.
2. These registers are available only in EPP mode.

Table 12-3 Address and Bit Map for SPP and EPP Modes

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	BUSY#	ACK#	PE	SLCT	ERROR#	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	INIT#	AUTOFD#	STROBE#
Control Latch (Write)	1	1	DIR	IRQ	SLIN	INIT#	AUTOFD#	STROBE#
EPP Address Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Each register (or pair of registers, in some cases) is discussed below.

12.2.1 Data Port (Data Swapper)

The CPU reads the contents of the printer's data latch by reading the data port.

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12.2.2 Printer Status Buffer

The CPU reads the printer status by reading the printer status buffer. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	BUSY#	ACK#	PE	SLCT	ERROR#	RESERVED		TMOUT
DEFAULT	NA	NA	NA	NA	NA	1	1	0

BIT	DESCRIPTION
7	**BUSY#.** This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.
6	**ACK#.** This bit represents the current state of the printer's ACK# signal. A logical 0 means the printer has received a character and is ready to accept another. Normally, this signal is active for approximately 5 μs before BUSY# stops.
5	**PE.** A logical 1 means the printer has detected the end of paper.
4	**SLCT.** A logical 1 means the printer is selected.
3	**ERROR#.** A logical 0 means the printer has encountered an error condition.
2-1	**RESERVED.**
0	**TMOUT.** This bit is only valid in EPP mode. A logical 1 indicates that a 10-μs time-out has occurred on the EPP bus; a logical 0 means hat no time-out error has occurred. Writing a logical 1 to this bit clears the time-out status bit; writing a logical 0 has no effect.

12.2.3 Printer Control Latch and Printer Control Swapper

The CPU reads the contents of the printer control latch by reading the printer control swapper. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DIR	IRQ ENABLE	SLCT IN	INIT#	AUTO FD	STROBE
DEFAULT	1	1	NA	0	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	**RESERVED.** These two bits are always read as logical 1 and can be written.
5	**DIR (Direction Control Bit).** When this bit is logical 1, the parallel port is in the input mode (read). When it is logical 0, the parallel port is in the output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.
4	**IRQ ENABLE.** A logical 1 allows an interrupt to occur when ACK# changes from low to high.
3	**SLCT IN.** a logical 1 selects the printer.
2	**INIT#.** A logical 0 starts the printer (50 microsecond pulse, minimum).
1	**AUTO FD.** A logical 1 causes the printer to line-feed after a line is printed.
0	**STROBE.** A logical 1 generates an active-high pulse for a minimum of 0.5 μs to clock data into the printer. Valid data must be presented for a minimum of 0.5 μs before and after the strobe pulse.

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12.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP address write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR# causes an EPP address read cycle to be performed and the data to be output to the host CPU.

12.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. The bit definitions for each data port are the same and as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

When any EPP data port is accessed, the contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP data write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of IOR# causes an EPP read cycle to be performed and the data to be output to the host CPU.

12.2.6 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
Nwrite	O	Denotes read or write operation for address or data.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
Nwait	I	Inactivated to acknowledge that data transfer is complete. Activated to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer-select status; same as SPP mode.
NDStrb	O	This signal is active low. It denotes a data read or write operation.
Nerror	I	Error; same as SPP mode.
Ninits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
NAStrb	O	This signal is active low. It denotes an address read or write operation.

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12.2.7 EPP Operation

When EPP mode is selected, the PDx bus is in standard or bi-directional mode when no EPP read, write, or address cycle is being executed. In this situation, all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μS have elapsed from the start of the EPP cycle to the time WAIT# is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in status bit 0.

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

12.2.8 EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If nWait is active low, the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, proceeds normally, and is completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle cannot start. It must wait until nWait changes to active low, at which time it starts as described above.

12.2.9 EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it does not finish until nWait changes from active low to inactive high.

12.3 Extended Capabilities Parallel (ECP) Port

This port is software- and hardware-compatible with existing parallel ports, so the NCT6102D / NCT6106D parallel port may be used in standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host-to-peripheral) and reverse (peripheral-to-host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port hardware supports run-length-encoded (RLE) decompression. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. RLE compression is required; the hardware support is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

The NCT6102D / NCT6106D ECP supports the following modes.

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Table 12-4 ECP Mode Description

MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CRF0h to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

The mode selection bits are bits 7-5 of the Extended Control Register.

12.3.1 ECP Register and Bit Map

The next two tables list the registers used in ECP mode and provide a bit map of the parallel port and ECP registers.

Table 12-5 ECP Register Addresses

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR60 and 61, which are determined by configuration register or hardware setting.

Table 12-6 Bit Map of the ECP Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
Dsr	nBusy	nAck	Perror	Select	nFault	1	1	1	1
Dcr	1	1	Directio	ackIntEn	SelectIn	nInit	Autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
Ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

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Notes:
1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

Each register (or pair of registers, in some cases) is discussed below.

12.3.2 Data and ecpAFifo Port

Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input, and the contents of this register are output to PD0-PD7. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. This operation is defined only for the forward direction. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Address/RLE	Address or RLE						

12.3.3 Device Status Register (DSR)

These bits are logical 0 during a read of the Printer Status Register. The bits of this status register are defined as follows:

BIT	7	6	5	4	3	2	1	0
NAME	nBusy	nAck	Perror	Select	nFault	1	1	1

BIT	DESCRIPTION
7	**nBusy.** This bit reflects the complement of the Busy input.
6	**nAck.** This bit reflects the nAck input.
5	**Perror.** This bit reflects the Perror input.
4	**Select.** This bit reflects the Select input.
3	**nFault.** This bit reflects the nFault input.
2-0	These three bits are not implemented and are always logical 1 during a read.

12.3.4 Device Control Register (DCR)

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Director	ackInEn	SelectIn	nInit	Autofd	Strobe
DEFAULT	1	1	NA	NA	NA	NA	NA	NA

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BIT	DESCRIPTION
7-6	**Reserved.** These two bits are always read as logical 1 and cannot be written.
5	**Director.** If the mode is 000 or 010, this bit has no effect and the direction is always out. In other modes, 0: The parallel port is in the output mode. 1: The parallel port is in the input mode.
4	**ackInEn** (Interrupt Request Enable). When this bit is set to logical 1, it enables interrupt requests from the parallel port to the CPU on the low-to-high transition on ACK#.
3	**SelectIn.** This bit is inverted and output to the SLIN# output. 0: The printer is not selected. 1: The printer is selected.
2	**nInit.** This bit is output to the INIT# output.
1	**Autofd.** This bit is inverted and output to the AFD# output.
0	**Strobe.** This bit is inverted and output to the STB# output.

12.3.5 CFIFO (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. Bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte-aligned.

12.3.6 ECPDFIFO (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte-aligned.

When the direction bit is 1, data bytes from the peripheral are read via automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO return bytes of ECP data to the system.

12.3.7 TFIFO (Test FIFO Mode) Mode = 110

Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO is not transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

12.3.8 CNFGA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates that this is an 8-bit implementation.

12.3.9 CNFGB (Configuration Register B) Mode = 111

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	COMPRESS	intrVALUE	IRQx2	IRQx1	IRQx0	RESERVED		
DEFAULT	0	0	0	0	0	1	1	1

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BIT	DESCRIPTION
7	**Compress.** This bit is read-only. It is logical 0 during a read, which means that this chip does not support hardware RLE compression.
6	**intrValue.** Returns the value on the ISA IRQ line to determine possible conflicts.
5	**IRQx2.** Reflects the IRQ resource assigned for ECP port.
4	**IRQx1.**
3	**IRQx0.**
2-0	**Reserved.** These three bits are logical 1 during a read and can be written.

cnfgB[5:3]	IRQ resource
000	Reflects other IRQ resources selected by PnP register (default)
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	IRQ14
110	IRQ15
111	IRQ5

12.3.10ECR (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:

BIT	7	6	5	4	3	2	1	0
NAME	MODE			nErrIntrEn	dmaEn	ServiceIntr	Full	Empty
DEFAULT	0	0	0	1	0	1	0	1

BIT	DESCRIPTION
7-5	**Mode.** Read/Write. These bits select the mode.

000	Standard Parallel Port (SPP) mode. The FIFO is reset in this mode.
001	PS/2 Parallel Port mode. This is the same as SPP mode except that direction may be used to tri-state the data lines. Furthermore, reading the data register returns the value on the data lines, not the value in the data register.
010	Parallel Port FIFO mode. This is the same as SPP mode except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.
011	ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral using the ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.
100	EPP Mode. EPP mode is activated if the EPP mode is selected.

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BIT	DESCRIPTION
	101 Reserved. 110 Test Mode. The FIFO may be written and read in this mode, but the data is not transmitted on the parallel port. 111 Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.
4	**nErrIntrEn.** Read/Write (Valid only in ECP Mode) 0: Enables the interrupt generated on the falling edge of nFault. This prevents interrupts from being lost in the time between the read of the ECR and the write of the ECR. 1: Disables the interrupt generated on the asserting edge of nFault.
3	**dmaEn.** Read/Write. 0: Disable DMA unconditionally. 1: Enable DMA.
2	**serviceIntr.** Read/Write. 0: Enable one of the following cases of interrupts. When one of the serviced interrupts occurs, this bit is set to logical 1 by the hardware. This bit must be rest to logical 0 to re-enable the interrupts. (a) dmaEn = 1: During DMA, this bit is set to logical 1 when terminal count is reached. (b) dmaEn = 0, direction = 0: This bit is set to logical 1 whenever there are writeIntr threshold or more bytes free in the FIFO. (c) dmaEn = 0, direction = 1: This bit is set to logical 1 whenever there are readIntr threshold or more valid bytes to be read from the FIFO. 1: Disable DMA and all of the service interrupts. Writing a logical 1 to this bit does not cause an interrupt.
1	**Full.** Read Only. 0: The FIFO has at least one free byte. 1: The FIFO is completely full; it cannot accept another byte.
0	**Empty.** Read Only. 0: The FIFO contains at least one byte of data. 1: The FIFO is completely empty.

12.3.11 ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
Nstrobe (HostClk)	O	This pin loads data or address into the slave on its asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contain address, data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. In the reverse direction, it indicates whether the data lines contain ECP command information or data. Normal data are transferred when Busy (PeriphAck) is high, and an 8-bit command is transferred when it is low.

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NAME	TYPE	DESCRIPTION
Perror (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on-line.
NautoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. In the forward direction, this signal indicates whether the data lines contain ECP address or data. Normal data are transferred when nAutoFd (HostAck) is high, and an 8-bit command is transferred when it is low.
nFault (nPeriphReuqest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

12.3.12 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits.

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

I Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

12.3.12.1. Mode Switching

The software must handle P1284 negotiation and all operations prior to a data transfer in SPP or PS/2 modes (000 or 001). The hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port, only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

In extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode, the software should wait for all the data to be read from the FIFO before changing back to mode 000 or 001.

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12.3.12.2. Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high, and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high, and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

12.3.12.3. Data Compression

The NCT6102D / NCT6106D hardware supports RLE decompression and can transfer compressed data to a peripheral. Odd (RLE) compression is not supported in the hardware, however. In order to transfer data in ECP mode, the compression count is written to ecpAFifo and the data byte is written to ecpDFifo.

12.3.13FIFO Operation

The FIFO threshold is set in CR5. All data transferred to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used in Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

12.3.14DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or Cfifo. DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA empties or fills the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated, and serviceIntr is asserted, which will disable the DMA.

12.3.15Programmed I/O (NON-DMA) Mode

The ECP and parallel port FIFOs can also be operated using interrupt-driven, programmed I/O. Programmed I/O transfers are

1. To the ecpDFifo at 400H and ecpAFifo at 000H
2. From the ecpDFifo located at 400H
3. To / from the tFifo at 400H.

The host must set dmaEn and serviceIntr to 0 and also must set the direction and state accordingly in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O empties or fills the FIFO using the appropriate direction and mode.

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13. KEYBOARD CONTROLLER

The NCT6102D / NCT6106D KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.

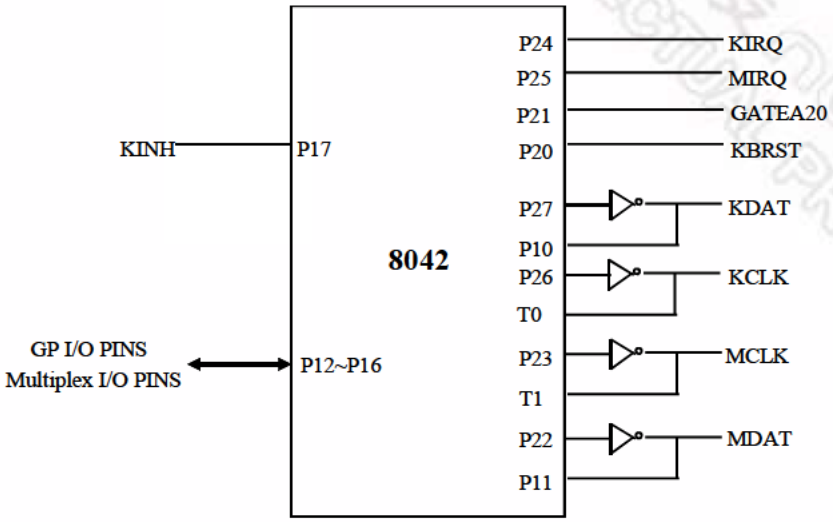

Figure 13-1 Keyboard and Mouse Interface

13.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60H (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

13.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

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13.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64h (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

Table 13-1 Bit Map of Status Register

BIT	BUT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

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13.4 Commands

Table 13-2 KBC Command Sets

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte of Keyboard Controller</td></tr>
<tr><td>60h</td><td>Write Command Byte of Keyboard Controller
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>7</td><td>Reserved</td></tr>
<tr><td>6</td><td>IBM Keyboard Translate Mode</td></tr>
<tr><td>5</td><td>Disable Auxiliary Device</td></tr>
<tr><td>4</td><td>Disable Keyboard</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>2</td><td>System Flag</td></tr>
<tr><td>1</td><td>Enable Auxiliary Interrupt</td></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
</table></td></tr>
<tr><td>A4h</td><td>Test Password
Returns 0Fah if Password is loaded
Returns 0F1h if Password is not loaded</td></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a logical 0 is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>Aah</td><td>Self-test
Returns 055h if self-test succeeds</td></tr>
<tr><td>Abh</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Keyboard "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Keyboard "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Keyboard "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Keyboard "Data" line is stuck high</td></tr>
</table></td></tr>
</table>

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COMMAND	FUNCTION
Adh	Disable Keyboard Interface
Aeh	Enable Keyboard Interface
C0h	Read Input Port (P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into the STATUS register
C2h	Continuously puts the upper four bits of Port1 into the STATUS register
D0h	Send Port 2 value to the system
D1h	Only set / reset GateA20 line based on system data bit 1
D2h	Send data back to the system as if it came from the Keyboard
D3h	Send data back to the system as if it came from Auxiliary Device
D4h	Output next received byte of data from system to Auxiliary Device
E0h	Reports the status of the test inputs
FXh	Pulse only RC (the reset line) low for 6μs if the Command byte is even

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13.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

13.5.1 KB Control Register (Logic Device 5, CR-F0)

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	RESERVED			P92EN	HGA20	HKBRST#
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**KCLKS1.**	Select the KBC clock rate. **Bits** **7 6** 0 0: Reserved 0 1: Reserved 1 0: KBC clock input is 12 MHz. 1 1: Reserved
6	**KCLKS0.**	
5-3	**RESERVED.**	
2	**P92EN (Port 92 Enable).** 1: Enables Port 92 to control GATEA20 and KBRESET. 0: Disables Port 92 functions.	
1	**HGA20 (Hardware GATEA 20).** 1: Selects hardware GATE A20 control logic to control GATE A20 signal. 0: Disables GATEA20 control logic functions.	
0	**HKBRST# (Hardware Keyboard Reset).** 1: Selects hardware KB RESET control logic to control KBRESET signal. 0: Disables hardware KB RESET control logic function.	

When the KBC receives data that follows a "D1" command, the hardware control logic sets or clears GATE A20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an "FE" command, the KBRESET is pulse low for 6 μs (Min.) with a 14 μs (Min.) delay.

GATE A20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATE A20 and KBRESET are merged with Port92 when the P92EN bit is set.

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13.5.2 Port 92 Control Register (Default Value = 0x24)

BIT	7	6	5	4	3	2	1	0
NAME	RES. (0)		RES. (1)	RES. (0)		RES. (1)	SGA20	PLKBRST#
DEFAULT	0	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-6	**RES. (0)**
5	**RES. (1)**
4-3	**RES. (0)**
2	**RES. (1)**
1	**SGA20 (Special GATE A20 Control)** 1: Drives GATE A20 signal to high. 0: Drives GATE A20 signal to low.
0	**PLKBRST# (Pulled-low KBRESET).** A logical 1 on this bit causes KBRESET to drive low for 6 µS(Min.) with a 14 µS(Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

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14. CONSUMER INFRARED REMOTE (CIR)

Regarding the receiving of IR Block, the hardware uses the sampling rates of 1us, 25us, 50us and 100us to calculate the widths of H Level and L Level. The results are saved/stored in 32*8 RX FIFO. The max widths of H Level and L Level will be determined by Sample Limit Count Register. During the receiving, the hardware will reflect the FIFO status in RX FIFO Status Register. In addition, the hardware also generates status, such as Data Ready, Trigger Level Reach, FIFO Overrun and FIFO underrun, in RC Status Register.

As for the transmission, the user has to set up the Carrier frequency and the transmission mode first and then writes the widths of H Level and L Level via TX FIFO. The hardware will add Carrier to H Level according to the transmission mode.

14.1 CIR Register Table

Table 14-1 CIR Register Table

RC Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
base+0	IRCON	R	WIREN	TXEN	RXEN	WRXINV	RXINV	Sample Period Select	
base+1	IRSTS	RDR	RTR	PE	RFO	TE	TTR	TFU	GH
base+2	IREN	RDR	RTR	PE	RFO	TE	TTR	TFU	GH
base+3	RXFCONT	RXFIFO Count							
base+4	CP	MODE	Reserved						Carrier Prescalar
base+5	CC	Carrier Period							
base+6	SLCH	Sample Limit Count High Byte							
base+7	SLCL	Sample Limit Count Low Byte							
base+8	FIFOCON	TXFIFOCLR	R	Tx Trigger Level		RXFIFOCLR	R	Rx Trigger Level	
base+9	IRFIFOSTS	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	TX_FTA	TX_Empty	TX_Full
base+A	SRXFIFO	Sample RX FIFO							
base+B	TXFCONT	TX FIFO Count							
base+C	STXFIFO	Sample TX FIFO							
base+D	FCCH	Frame Carrier Count High Byte							
base+E	FCCL	Frame Carrier Count Low Byte							
base+F	IRFSM	R	Decoder FSM			R	Encoder FSM		

14.1.1 IR Configuration Register – Base Address + 0

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Resevered	WIREN	TXEN	RXEN	WRXINV	RXINV	Sample Period Select	
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	Resevered.

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6	**Wide-band IR Enable**
5	**TX Enable** 1: Transmission Enable. After confirming that FIFO is not empty, the transmission starts (the hardware will wait until TX FIFO data are written). If TX Enable is set to 0 during the transmission, the transmission stops when the transmission of FIFO data is completed. 0: Transmission Disable.
4	**RX Enable**
3	**Wide-band IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
2	**IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1~0	**Sample Period Select** 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

14.1.2 IR Status Register – Base Address + 1

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
Name	**RDR**	**RTR**	**PE**	**RFO**	**TE**	**TTR**	**TFU**	**GH**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RX Data Ready** (Writing 1 will clear the bit).
6	**RX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
5	**Packet End** (Writing 1 will clear the bit).
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3	**TX FIFO Empty** (Writing 1 will clear the bit).
2	**TX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
1	**TX FIFO Underrun** (Writing 1 will clear the bit).
0	**Min Length Detected** (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.

14.1.3 IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write
Size: 8 bits

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BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	TE	TTR	TFU	GH
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

BIT	DESCRIPTION
7	**RX Data Ready**
6	**RX FIFO Trigger Level Reach**
5	**Packet End**
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated).
3	**TX FIFO Empty**
2	**TX FIFO Trigger Level Reach**
1	**TX FIFO Underrun**
0	**Min Length Detected**

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

14.1.4 RX FIFO Count– Base Address + 5

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7~0	**RX FIFO Count**

14.1.5 IR TX Carrier Prescalar Configuration Register (CP) – Base Address + 4

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Mode	Reserved						CP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Mode** 0 : DC Mode

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	1 : Pulse Mode
6~1	**Reserved.**
0	**Carrier Prescalar** (CP). This bit is set for the Prescalar value of the IR TX carrier frequency.

14.1.6 IR TX Carrier Period Configuration Register (CC) – Base Address + 5

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Carrier Period (CC)							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is set for IR TX carrier period. The actual carrier period will be: Period = 2 * (2 ^ (CP*2)) * (CC+1) / (System Clock), where the frequency = 1 / period, and System Clock = 24MHz. Setting CP and CC to 0 will cause stop the device to from use using anyno carrier at all (that is, no light modulation, just constant on and off periods). The period count value CC can be any number from 0 to 255.

14.1.7 IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is defined as the high byte of the limited count in the IR RX mode.

14.1.8 IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

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14.1.9 IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TXFIFOCLR	Reserved	TX Trigger Level		RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TX FIFO Cleared.**
6	**Reserved.**
5~4	**TX Trigger Level** **Bits** **5 4** 0 0: 31 0 1: 24 1 0: 16 1 1: 8
3	**RX FIFO Cleared.**
2	**Reserved.**
1~0	**RX Trigger Level** **Bits** **1 0** 0 0: 1 0 1: 8 1 0: 16 1 1: 24

14.1.10 IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	TX_FTA	TX_Empty	TX_Full
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**IR Pending** 1: No Interrupt 0: Interrupt issue
6	**Minimum Length Detect Status**. This bit will be cleared when Packet End appears.

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BIT	DESCRIPTION
5	RX FIFO Trigger Level Active.
4	RX FIFO Empty Flag.
3	RX FIFO Full Flag.
2	TX FIFO Trigger Level Active.
1	TX FIFO Empty Flag.
0	TX FIFO Full Flag.

14.1.11IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7	**Voltage Level** 0: Low, 1: High
6~0	**RX data length** (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

14.1.12TX FIFO Count– Base Address + 5

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TX FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7~0	TX FIFO Count

14.1.13IR Sample TX FIFO Register – Base Address + C

Attribute: Read Only
Size: 8 bits

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BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample TX FIFO						

BIT	DESCRIPTION
7	**Voltage Level** 0: Low, 1: High
6~0	**TX data length** (Unit : Sample Period)

14.1.14IR Carrier Count High Byte Register – Base Address + D

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Carrier Count High Byte							

BIT	DESCRIPTION
7~0	**Carrier Count High Byte**. This byte records the total amount of the total rising edges until time-out event appears.

14.1.15IR Carrier Count Low Byte Register – Base Address + E

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Carrier Count Low Byte							

BIT	DESCRIPTION
7~0	**Carrier Count Low Byte**. This byte records the total amount of the the rising edges until time-out event appears.

After a time-out of reception on the learning receiver, this response is sent to tell the host the carrier frequency of the previous sample. The Carrier Count High Byte (ch) and Carrier Count Low Byte (cl) specify the cycle counts of cycles of the carrier. Carrier counts can also be thought ofregarded as the number of leading edges in the previous sample.

This is used toe calculation of the calculate carrier frequency is as followsfollowed:

$lastCarrierCount_{(decimal)} = ch*256+cl;$

Thus,

Carrier frequency = (lastCarrierCount) / (irPacketOnDuration);

The **irPacketOnDuration** value is the total amount of time that the envelope of the signal was is high. The IR receiver should keep track of the time that of the high envelope is high and return it using this response.

This response is unsolicited. It is returned by the receiver when IR arrives but is never explicitly requested.

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14.1.16IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Decoder FSM			Reserved	Encoder FSM		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**Decoder over status**
5	**Decoder continuing status**
4	**Decoder wait H status** 1: idle, 0: RX busy
3	**Reserved.**
2	**Encoder Idle Status.** 1: idle, 0: TX busy
1	**Encoder Read Status**
0	**Encoder Level Output Status**

14.1.17IR Minimum Length Register – Base Address + F

Attribute: Write Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Min Length Register							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	**Min Length Register**. Set up the shortest expected length of each carrier on the RX receiver (Unit: Sample Clock).

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15. CONSUMER INFRARED REMOTE (CIR) WAKE-UP

One of the features of the NCT6102D / NCT6106D is system boot-up by a remote controller. The hardware will store a specifically appointed key command from the IR remote controller in the FIFO of 67Byte.

The same key is required to re-boot the system after the computer shut-down. Such way can be applied to any remote controllers. Learning is necessary only at the first time.

15.1 CIR WAKE-UP Register Table

RC Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
base+0	IRCON	DEC_RST	Mode[1]	Mode[0]	RXEN	IgnoreEN	RXINV	Sample Period Select	
base+1	IRSTS	RDR	RTR	PE	RFO	GH	R	R	IR Pending
base+2	IREN	RDR	RTR	PE	RFO	GH	R		
Base+3		FIFO_COMPARE_DEEP							
base+4		FIFO_COMPARE_TOLERANCE							
base+5		FIFO_Count							
Base+6	SLCH	Sample Limit Count High Byte							
base+7	SLCL	Sample Limit Count Low Byte							
base+8	FIFOCON	R				RXFIFOCLR	R	Rx Trigger Level	
base+9	SRXFSTS	GS	FTA	Empty	Full	R			
base+A		Sample RX FIFO							
base+B		WR_FIFO_DATA							
Base+C		Read FIFO Only							
Base+D		Read FIFO Only Index							
Base+E		FIFO_Ignore							
Base+F	IRFSM	R	Decoder FSM			R			Wakeup Event

15.1.1 IR Configuration Register – Base Address + 0

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**DEC_RST**	**Mode[1]**	**Mode[0]**	**RXEN**	**Received**	**RXINV**	**Sample Period Select**	
DEFAULT	0	0	1	0	0	1	1	0

BIT	DESCRIPTION
7	**Reset CIR DECODER** (Write 1 to clear)
6	**Mode[1]** : 0: FIFO can't be written 1: FIFO can be written
5	**Mode[0]**

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BIT	DESCRIPTION
	0: Learning Mode 1: Wake up Mode (Before enter in Power S3 state, this bit should be set) This bit reset by VCC.
4	**RX Enable**
3	**Ignore Bit Enable**
2	**IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1~0	**Sample Period Select** 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

15.1.2 IR Status Register – Base Address + 1

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	GH	Received		IR_Pending
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RX Data Ready** (Writing 1 will clear the bit).
6	**RX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
5	**Packet End** (Writing 1 will clear the bit).
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3	**Min Length Detected** (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.
2~1	**Reserved.**
0	**IR Pending** 1: No Interrupt 0: Interrupt issue

15.1.3 IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	GH	Reserved		
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

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BIT	DESCRIPTION
7	**RX Data Ready**
6	**RX FIFO Trigger Level Reach**
5	**Packet End**
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated).
3	**Min Length Detected**
2~0	**Reserved**

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

15.1.4 IR TX Configuration Register – Base Address + 3

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Compare Deep							
DEFAULT	0	1	0	0	0	0	1	1

1: Enable; 0: Disable

BIT	DESCRIPTION
7~0	When in S3 state, how many bytes need to compare. Default is 67 bytes.

15.1.5 IR FIFO Compare Tolerance Configuration Register – Base Address + 4

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Compare Tolerance							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	**FIFO Data Tolerance between Learning mode and Wakeup mode**. (Every byte) FIFO Date Tolerance = (Learning mode data) – (Wakeup mode data)

15.1.6 RX FIFO Count– Base Address + 5

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

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1: Enable; 0: Disable

BIT	DESCRIPTION
7~0	RX FIFO Count

15.1.7 IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is defined as the high byte of the limited count in the IR RX mode.

15.1.8 IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

15.1.9 IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~4	**Reserved**
3	**RX FIFO Cleared.**
2	**Reserved.**
1~0	**RX Trigger Level** **Bits** **1 0**

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	0 0: 67 0 1: 66 1 0: 65 1 1: 64

15.1.10IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GS	FTA	Empty	Full	Reserved			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Minimum Length Detect Status**. This bit will be cleared when Packet End appears.
6	**RX FIFO Trigger Level Active.**
5	**RX FIFO Empty Flag.**
4	**RX FIFO Full Flag.**
3~0	**Reserved**

15.1.11IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7~6	**Voltage Level** 0: Low, 1: High
0	**RX data length** (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

15.1.12Write FIFO – Base Address + B

Attribute: Write Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Write Sample RX FIFO						

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BIT	DESCRIPTION
7~6	**Voltage Level** 0: Low, 1: High
0	**RX data length** (Unit : Sample Period)

Note. Before writing FIFO Data, mode[1] register should be set.

15.1.13Read FIFO Only – Base Address + C

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7~6	**Voltage Level** 0: Low, 1: High
0	RX data length (Unit : Sample Period)

Note. Only Read FIFO Data.

15.1.14Read FIFO Index – Base Address + D

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Index							

BIT	DESCRIPTION
7~0	Indicate that FIFO Index when only read FIFO data(Base Address + C)

Note. Only Read FIFO Data.

15.1.15Reserved – Base Address + E

15.1.16IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Decoder FSM			Reserved			Wakeup event
DEFAULT	0	0	0	0	0	0	0	0

15.1.17IR Minimum Length Register – Base Address + F

Attribute: Write Only
Size: 8 bits

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BIT	7	6	5	4	3	2	1	0
NAME	Min Length Register							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Min Length Register. Set up the shortest expected length of each carrier on the RX receiver (Unit: Sample Clock).

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16. POWER MANAGEMENT EVENT

The PME# (pin 86) signal is connected to the South Bridge and is used to wake up the system from S1 ~ S5 sleeping states.

One control bit and four registers in the NCT6102D / NCT6106D are associated with the PME function. The control bit is at Logical Device A, CR[F2h], bit[0] and is for enabling or disabling the PME function. If this bit is set to "0", the NCT6102D / NCT6106D won't output any PME signal when any of the wake-up events has occurred and is enabled. The four registers are divided into PME status registers and PME interrupt registers of wake-up events Note.1.

1) The PME status registers of wake-up event:
   - At Logical Device A, CR[F3h] and CR[F4h]
   - Each wake-up event has its own status
   - The PME status should be cleared by writing a "1" before enabling its corresponding bit in the PME interrupt registers
2) The PME interrupt registers of wake-up event:
   - At Logical Device A, CR[F6h] and CR[F7h]
   - Each wake-up event can be enabled / disabled individually to generate a PME# signal

Note.1 PME wake-up events that the NCT6102D / NCT6106D supports include:

- Mouse IRQ event
- Keyboard IRQ event
- Printer IRQ event
- Floppy IRQ event
- UART A IRQ event
- IR IRQ event
- Hardware Monitor IRQ event
- WDT1 event

Note.2 All the above support both S0 and S1 states.

16.1 Power Control Logic

This chapter describes how the NCT6102D / NCT6106D implements its ACPI function via these power control pins: PSIN# (Pin 68), PSOUT# (Pin 67), SLP_S3# (Pin 73) and PSON# (Pin 72). The following figure illustrates the relationships.

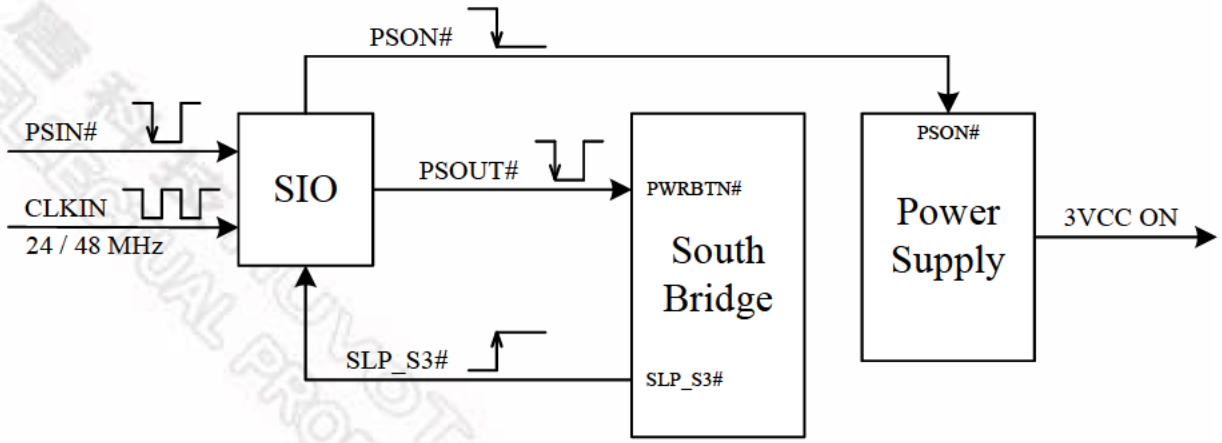

Figure 16-1 Power Control Mechanism

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16.1.1 PSON# Logic

16.1.1.1. Normal Operation

The PSOUT# signal will be asserted low if the PSIN# signal is asserted low. The PSOUT# signal is held low for as long as the PSIN# is held low. The South Bridge controls the SLP_S3# signal through the PSOUT# signal. The PSON# is directly connected to the power supply to turn on or off the power.

Figure 16-2 shows the power on and off sequences.

The ACPI state changes from S5 to S0, then to S5

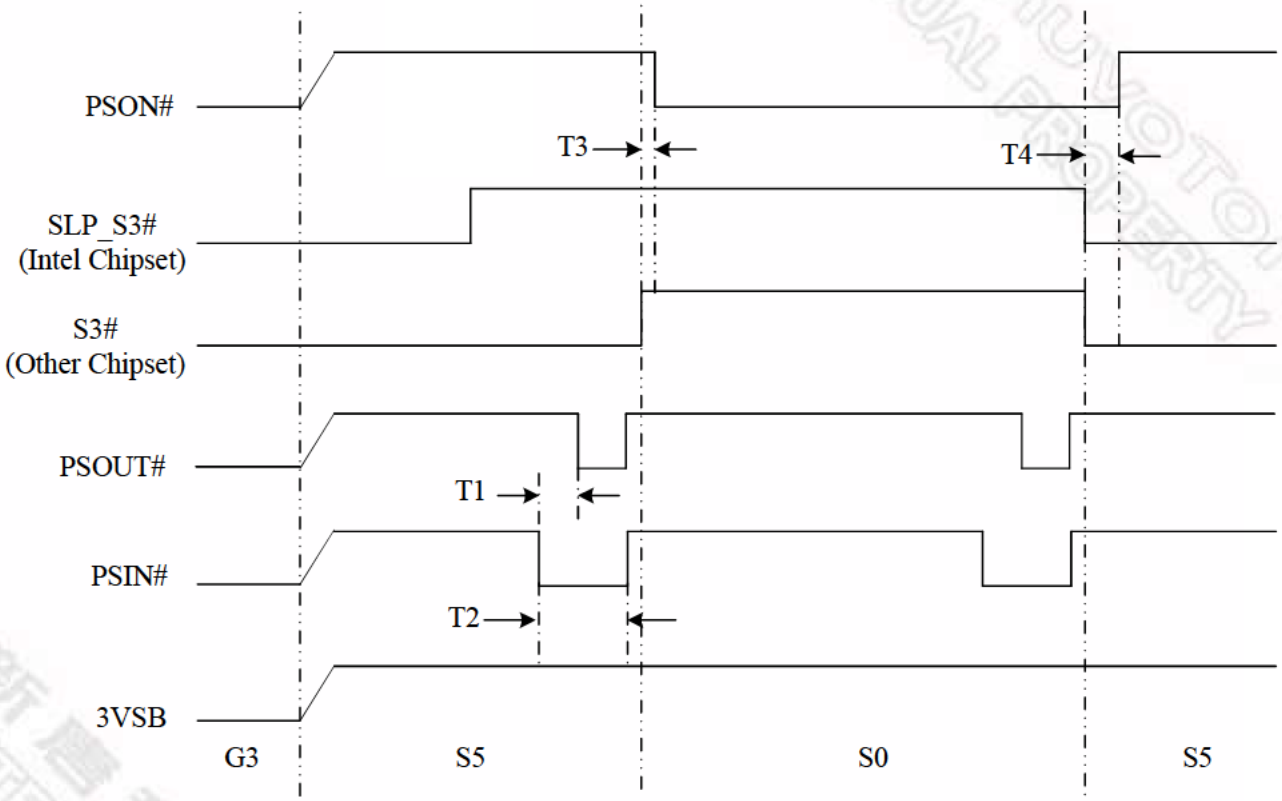

Figure 16-2 Power Sequence from S5 to S0, then Back to S5

16.1.2 AC Power Failure Resume

By definition, AC power failure means that the standby power is removed. The power failure resume control logic of the NCT6102D / NCT6106D is used to recover the system to a pre-defined state after AC power failure. Two control bits at Logical Device A, CR[E4h], bits[6:5] indicate the pre-defined state. The definition of these two bits is listed in the following table:

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Table 16-1 Bit Map of Logical Device A, CR[E4h], Bits[6:5]

LOGICAL DEVICE A, CR[E4H], BITS[6 :5]	DEFINITION
00	System always turns off when it returns from AC power failure
01	System always turns on when it returns from AC power failure
10	System turns off / on when it returns from power failure depending on the state before the power failure. (Please see Note 1)
11	User defines the state before the power failure. (The previous state is set at CRE6[4]. Please see Note 2)

Note1. The NCT6102D / NCT6106D detects the state before power failure (on or off) through the SLP_S3# signal and the 3VCC power. The relation is illustrated in the following two figures.

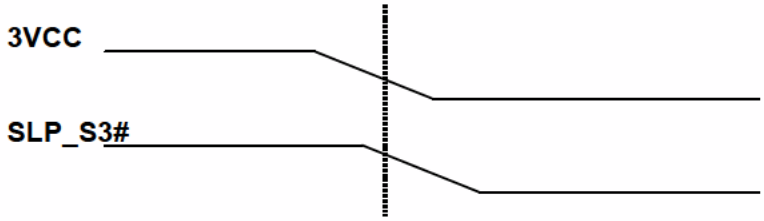

Figure 16-3 The previous state is "on"

3VCC falls to 2.6V and SLP_S3# keeps at 2.0V.

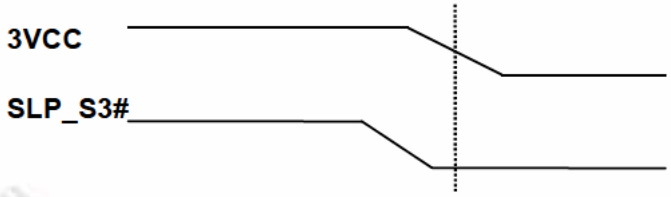

Figure 16-4 The previous state is "off".

3VCC falls to 2.6V and SLP_S3# keeps at 0.8V.

Note 2.

Logical Device A, CR[E6h] bit [4]	Definition
0	User defines the state to be "on"
1	User defines the state to be "off"

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To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT6102D / NCT6106D adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be "On" or "Off". According to this setting, the system is returned to the pre-defined state after the AC power recovery.

16.2 Wake Up the System by Keyboard and Mouse

The NCT6102D / NCT6106D generates a low pulse through the PSOUT# pin to wake up the system when it detects a key code pressed or mouse button clicked. The following sections describe how the NCT6102D / NCT6106D works.

16.2.1 Waken up by Keyboard events

The keyboard Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 6 to "1".

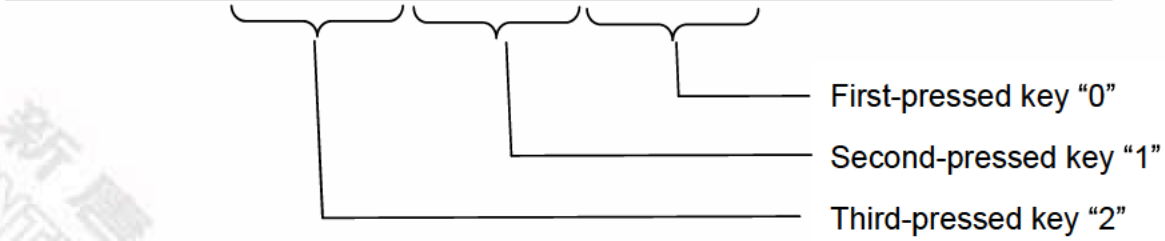
There are two keyboard events can be used for the wake-up

1) Any key – Set bit 0 at Logical Device A, CR[E0h] to "1" (Default).
2) Specific keys (Password) – Set bit 0 at Logical Device A, CR[E0h] to "0".

Three sets of specific key combinations are stored at Logical Device A. CR[E1h] is an index register to indicate which byte of key code storage (0x00h ~ 0x0Eh, 0x30h ~ 0x3Eh, 0x40h ~ 0x4Eh) is going to be read or written through CR[E2h]. According to IBM 101/102 keyboard specification, a complete key code contains a 1-byte make code and a 2-byte break code. For example, the make code of "0" is 0x45h, and the corresponding break code is 0xF0h, 0x45h.

The approach to implement Keyboard Password Wake-Up Function is to fill key codes into the password storage. Assume that we want to set "012" as the password. The storage should be filled as below. Please note that index 0x09h ~ 0x0Eh must be filled as 0x00h since the password has only three numbers.

Index(CRE1)→	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Data(CRE2)→	1E	F0	1E	16	F0	16	45	F0	45	00	00	00	00	00	00



16.2.2 Waken up by Mouse events

The mouse Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 5 to "1".

The following specific mouse events can be used for the wake-up:

- Any button clicked or any movement
- One click of the left or the right button
- One click of the left button
- One click of the right button
- Two clicks of the left button
- Two clicks of the right button.

Three control bits (ENMDAT_UP, MSRKEY, MSXKEY) define the combinations of the mouse wake-up events. Please see the following table for the details.

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Table 16-2 Definitions of Mouse Wake-Up Events

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
1	x	1	Any button clicked or any movement.
1	x	0	One click of the left or right button.
0	0	1	One click of the left button.
0	1	1	One click of the right button.
0	0	0	Two clicks of the left button.
0	1	0	Two clicks of the right button.

16.3 Resume Reset Logic

The RSMRST# (Pin 75) signal is a reset output and is used as the VSB power on reset signal for the South Bridge.

When the NCT6102D / NCT6106D detects the 3VSB voltage rises to "V1", it then starts a delay – "t1" before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below "V2", the RSMRST# de-asserts immediately.

Timing and voltage parameters are shown in Figure 16-5 and Table 16-3.

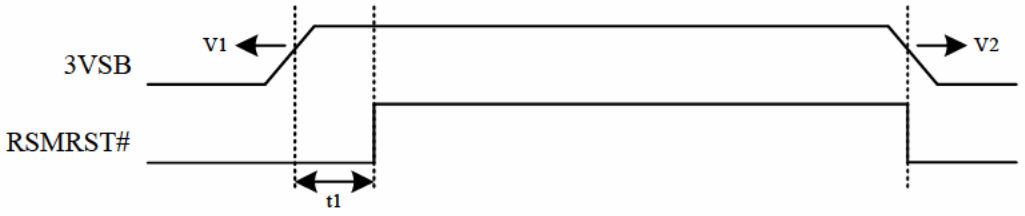

Figure 16-5 Mechanism of Resume Reset Logic

Table 16-3 Timing and Voltage Parameters of RSMRST#

NAME	PARAMETER	MIN.	MAX.	UNIT
V1	3VSB Valid Voltage	-	3.033	V
V2	3VSB Ineffective Voltage	2.882	-	V
t1	Valid 3VSB to RSMRST# inactive	200	300	mS

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17. SERIALIZED IRQ

The NCT6102D / NCT6106D supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

17.1 Start Frame

There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the NCT6102D / NCT6106D drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the NCT6102D / NCT6106D from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.

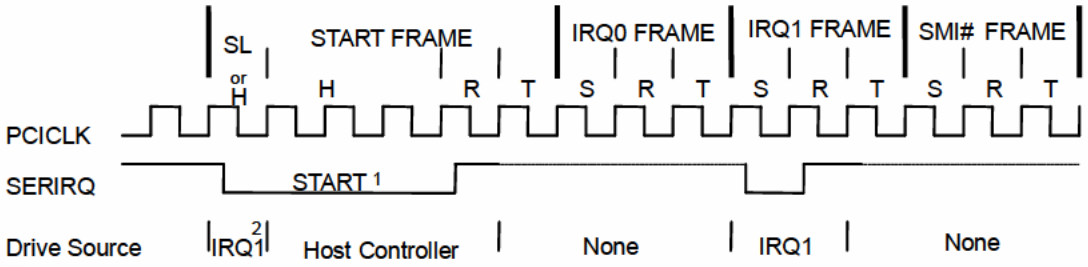

Figure 17-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1

H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the NCT6102D / NCT6106D because IRQ1 of the NCT6102D / NCT6106D needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

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17.2 IRQ/Data Frame

Once the Start Frame has been initiated, the NCT6102D / NCT6106D must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the NCT6102D / NCT6106D drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the NCT6102D / NCT6106D device drives the SERIRQ high. During the Turn-around phase, the NCT6102D / NCT6106D device leaves the SERIRQ tri-stated. The NCT6102D / NCT6106D starts to drive the SERIRQ line from the beginning of "IRQ0 FRAME" based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 17-1.

Table 17-1 SERIRQ Sampling Periods

SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	**SIGNAL SAMPLED**	**# OF CLOCKS PAST START**	**EMPLOYED BY**
1	IRQ0	2	Reserved
2	IRQ1	5	Keyboard
3	SMI#	8	H/W Monitor & SMI
4	IRQ3	11	IR
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	FDC
8	IRQ7	23	LPT
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	Reserved
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

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17.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminates SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.

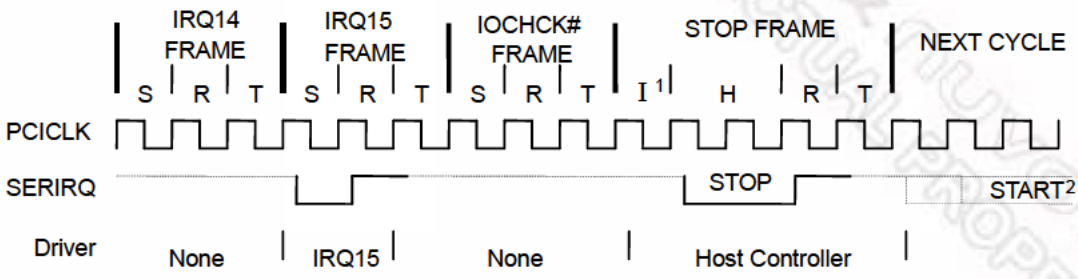

Figure 17-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period

H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

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18. WATCHDOG TIMER

The Watchdog Timer of the NCT6102D / NCT6106D consists of an 8-bit programmable time-out counter and a control and status register. GPIO0, GPIO2, GPIO3, GPIO5, GPIO6, GPIO7 provides an alternative WDT1 function. This function can be configured by the relative GPIO control register. The units of Watchdog Timer counter can be selected at Logical Device 8, CR[F0h], bit[3]. The time-out value is set at Logical Device 8, CR[F1h], default is 4. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

When Watchdog Timer 1 time-out event is occurring, GPIO0 bit[1], [5], GPIO2, bit[3], [7], GPIO3 bit[1], [5], GPIO5 bit[0], [4], GPIO6 bit[7], GPIO7 bit[0], will trigger a low pluse apporx 100mS. Also the event could go to pin77 WDTO#. In other words, when the value is counted down to zero, the timer stops, and the NCT6102D / NCT6106D sets the WDT1 status bit in Logical Device 8, CR[F2h], bit[4]. Writing a zero will clear the status bit. it. This bit will also be cleared if LRESET# or PWROK# signal is asserted.

The Watchdog Timer 2 of the NCT6102D / NCT6106D consists of an 8-bit programmable time-out counter register (Logic Device D, CR[E2h]) and status register (Logic Device D, CR[E4h] bit7). The timeout event will trigger PWROK pin to gerenate a low pulse when Logic Device D, CRE3[bit0] is timer count down start bit. When Logic Device D, CRE3[bit0] set to one, the timer will start count down, until this bit is written to zero.

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19. GENERAL PURPOSE I/O

19.1 GPIO ARCHITECTURE

The NCT6102D / NCT6106D provides 57 input/output ports that can be individually configured to perform a simple basic I/O function or alternative, pre-defined function. GPIO port 0 ~ 7 is configured through control registers in logical device 7. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 = output, 1 = input). Invert port value by setting inversion register (0 = non–inverse, 1 = inverse). Port value is read/written through data register.

In addition, only GP44, GP45, GP46 and GP47 are designed to be able to assert PSOUT# or PME# signal to wake up the system if any of them has any transitions. There are about 16ms debounced circuit inside these 4 GPIOs and it can be disabled by programming respective bit (LD9, CRE0h bit 4-7). Users can set what kind of event type, level or edge, and polarity, rising or falling, to perform the wake-up function. The following table gives more detailed register map on GP44, GP45, GP46 and GP47.

Table 19-1 Relative Control Registers of GPIO 44, 45, 46 and 47 that Support Wake-Up Function

	EVENTROUTE I (PSOUT#) 0: DISABLE 1: ENABLE	EVENTROUTE II (PME#) 0: DISABLE 1: ENABLE	EVENT DEBOUNCED 0 : ENABLE 1 : DISABLE	EVENT TYPE 0 : EDGE 1: LEVEL	EVENT POLARITY 0 : RISING 1 : FALLING	EVENT STATUS
GP47	LD9, CR E1h Bit7	LD9, CR E1h Bit3	LD9, CR E0h Bit7	LD9, CR E0h Bit3	LD7, CR F2h Bit7	LD7, CR F3h Bit7
GP46	LD9, CR E1h Bit6	LD9, CR E1h Bit2	LD9, CR E0h Bit6	LD9, CR E0h Bit2	LD7, CR F2h Bit6	LD7, CR F3h Bit6
GP45	LD9, CR E1h Bit5	LD9, CR E1h Bit1	LD9, CR E0h Bit5	LD9, CR E0h Bit1	LD7, CR F2h Bit5	LD7, CR F3h Bit5
GP44	LD9, CR E1h Bit4	LD9, CR E1h Bit0	LD9, CR E0h Bit4	LD9, CR E0h Bit0	LD7, CR F2h Bit4	LD7, CR F3h Bit4

Table 19-2 GPIO Group Programming Table

Equips maximum 57-pin GPIOs.
GPIO0 Group Enable: Logic Device 7, CR30[0] Data: Logic Device 7, E0~E3 Multi-function: YLW, GRN, WDTO#, SUSLED (Logic Device 8, CRE0[7-0]) Reset: Logic Device 9, CRE2[0]

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OD/PP: Logic Device F, CRE0

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP00	109	GP00	input	3VSB	
GP01	110	GP01	input	3VSB	
GP02	111	GP02	input	3VSB	
GP03	112	GP03	input	3VSB	
GP04	113	GP04	input	3VSB	
GP05	114	GP05	input	3VSB	
GP06	115	GP06	input	3VSB	
GP07	116	GP07	input	3VSB	

GPIO1 Group

Enable: Logic Device 7, CR30[1]
Data: Logic Device 7, E4~E7
Multi-function: YLW, GRN, BEEP, SMI (Logic Device 8, CRE1[7-0])
Reset: Logic Device 9, CRE2[1]
OD/PP: Logic Device F, CRE1

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP10	117	GP10	input	3VSB	
GP11	118	GP11	input	3VSB	
GP12	119	GP12	input	3VSB	
GP13	120	GP13	input	3VSB	
GP14	121	GP14	input	3VSB	
GP15	122	GP15	input	3VSB	
GP16	123	GP16	input	3VSB	
GP17	124	GP17	input	3VSB	

GPIO2 Group

Enable: Logic Device 7, CR30[2]
Data: Logic Device 7, E8~EB
Multi-function: WDTO#, BEEP, SMI, PLED (Logic Device 8, CRE2[7-0])
Reset: Logic Device 9, CRE2[2]
OD/PP: Logic Device F, CRE2

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP20	125	GP20	input	3VCC	
GP21	126	GP21	input	3VCC	
GP22	127	GP22	input	3VCC	
GP23	128	GP23	input	3VCC	
GP24	01	GP24	input	3VCC	

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GP25	02	GP25	input	3VCC	
GP26	03	GP26	input	3VCC	
GP27	04	GP27	input	3VCC	

GPIO3 Group
Enable: Logic Device 7, CR30[3]
Data: Logic Device 7, EC~EF
Multi-function: BEEP, SMI, WDTO#, SUSLED (Logic Device 8, CRE3[7-0])
Reset: Logic Device 9, CRE2[3]
OD/PP: Logic Device F, CRE3

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP30	32	GP30	input	3VSB	
GP31	33	GP31	input	3VSB	
GP32	34	GP32	input	3VSB	
GP33	35	GP33	input	3VSB	
GP34	36	GP34	input	3VSB	
GP35	37	GP35	input	3VSB	
GP36	38	GP36	input	3VSB	
GP37	39	GP37	input	3VSB	

GPIO4 Group
Enable: Logic Device 7, CR30[4]
Data: Logic Device 7, F0~F3
Multi-function: YLW, GRN, PLED, SMI (Logic Device 8, CRE4[7-0])
Reset: Logic Device 9, CRE2[4]
OD/PP: Logic Device F, CRE4

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP40	40	GP40	input	3VSB	
GP41	41	GP41	input	3VSB	
GP42	42	GP42	input	3VSB	
GP43	43	GP43	input	3VSB	
GP44	44	GP44	input	3VSB	
GP45	45	GP45	input	3VSB	
GP46	46	GP46	input	3VSB	
GP47	47	GP47	input	3VSB	

GPIO5 Group
Enable: Logic Device 7, CR30[5]
Data: Logic Device 7, F4~F7
Multi-function: YLW, GRN, BEEP, WDTO# (Logic Device 8, CRE5[7-0])
Reset: Logic Device 9, CRE2[5]
OD/PP: Logic Device F, CRE5

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP50	62	KCLK	bi-direction	3VSB	
GP51	63	KDAT	bi-direction	3VSB	

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GP52	65	MCLK	bi-direction	3VSB	
GP53	66	MDAT	bi-direction	3VSB	
GP54	67	PSOUT#	output	3VSB	
GP55	68	PSIN#	input	3VSB	
GP56	70	SLP_S5#	input	3VSB	
GP57	71	PWROK	output (OD)	VRTC	

GPIO6 Group

Enable: Logic Device 7, CR30[6]
Data: Logic Device 7, F8~FB
Multi-function: YLW, GRN, BEEP, SMI, WDTO#, SUSLED, PLED (Logic Device 8, CRE6[7-0])
Reset: Logic Device 9, CRE2[6]
OD/PP: Logic Device F, CRE6

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP60	72	PSON#	output	3VSB	
GP61	73	SLP_S3#	input	3VSB	
GP62	75	RSMRST#	output	3VSB	
GP63	94	SDA	input	3VSB	
GP64	96	SCL	input	3VSB	
GP65	106	SUSLED	output	3VSB	
GP66	107	GP66	input	3VSB	
GP67	108	GP67	input	3VSB	

GPIO7 Group

Enable: Logic Device 7, CR30[6]
Data: Logic Device 7, FC~FF
Multi-function: YLW, GRN, BEEP, SMI, WDTO#, SUSLED, PLED (Logic Device 8, CRE7[7-0])
Reset: Logic Device 9, CRE2[7]
OD/PP: Logic Device F, CRE7

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP71	87	GP71	Input	3VSB	

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Table 19-3 GPIO Multi-Function Routing Table

GPIO Multi-Function Routing							
Bit	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6
7	0: GPIO07 1: YLW	0: GPIO17 1: YLW	0: GPIO27 1: WDTO#	0: GPIO37 1: BEEP	0: GPIO47 1: YLW	0: GPIO57 1: YLW	
6	0: GPIO06 1: GRN	0: GPIO16 1: GRN	0: GPIO26 1: BEEP	0: GPIO36 1: SMI	0: GPIO46 1: GRN	0: GPIO56 1: GRN	0: GPIO66 1: YLW
5	0: GPIO05 1: WDTO#	0: GPIO15 1: BEEP	0: GPIO25 1: SMI	0: GPIO35 1: WDTO#	0: GPIO45 1: PLED	0: GPIO55 1: BEEP	0: GPIO65 1: GRN
4	0: GPIO04 1: SUSLED	0: GPIO14 1: SMI	0: GPIO24 1: PLED	0: GPIO34 1: SUSLED	0: GPIO44 1: SMI	0: GPIO54 1: WDTO#	0: GPIO64 1: BEEP
3	0: GPIO03 1: YLW	0: GPIO13 1: YLW	0: GPIO23 1: WDTO#	0: GPIO33 1: BEEP	0: GPIO43 1: YLW	0: GPIO53 1: YLW	0: GPIO63 1: SMI
2	0: GPIO02 1: GRN	0: GPIO12 1: GRN	0: GPIO22 1: BEEP	0: GPIO32 1: SMI	0: GPIO42 1: GRN	0: GPIO52 1: GRN	0: GPIO62 1: WDTO#
1	0: GPIO01 1: WDTO#	0: GPIO11 1: BEEP	0: GPIO21 1: SMI	0: GPIO31 1: WDTO#	0: GPIO41 1: PLED	0: GPIO51 1: BEEP	0: GPIO61 1: SUSLED
0	0: GPIO00 1: SUSLED	0: GPIO10 1: SMI	0: GPIO20 1: PLED	0: GPIO30 1: SUSLED	0: GPIO40 1: SMI	0: GPIO50 1: WDTO#	0: GPIO60 1: PLED

Bit	GPIO6	GPIO7
7	000: GPIO67 001: YLW 001: GRN 001: BEEP 001: SMI 001: WDTO# 001: SUSLED 001: PLED	
1		0: GPIO71 1: WDTO#

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19.2 ACCESS CHANNELS

There are two different channels to set up/access the GPIO ports. The first one is the indirect access via register 2E/2F (4E/4F, it depends by HEFRAS trapping). The registers can be read / written only when the respective logical device ID and port number are selected.

The other is the direct access through GPIO register table that can be configured by {CR61, CR60} of logic device 8. The mapped 7 registers are defined in table 19-4. Base address plus 0 to 4 are GPIO registers, base address plus 5 and 6 are watchdog registers.Since the base address is set, the GPIO number can be selected by writing the group number to GSR [INDEX] (GPIO Select Register, #0~#7 for GPIO0 ~ GPIO7 respectively). Then the I/O register, the Data register and the Inversion register are mapped to addresses Base+0, Base+1 and Base+2 respectively. Only one GPIO can be accessed at one time.

Table 19-4 GPIO Register Addresses

ADDRESS	ABBR	BIT NUMBER							
		7	6	5	4	3	2	1	0
Base + 0	GSR	Reserved				INDEX			
Base + 1	IOR	GPIO I/O Register							
Base + 2	DAT	GPIO Data Register							
Base + 3	INV	GPIO Inversion Register							
Base + 4	DST	GPIO Status Register							
Base + 5	Wdtmod	Watchdog Timer I (WDT1) and KBC P20 Control Mode Register							
Base + 6	Wdttim	Watchdog Timer I (WDT1) Control Register							

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20. SMBUS MASTER INTERFACE

20.1 General Description

The SMBus interface module is two wire serial interface compatible to the SMBus physical layer. It is also compatible with Intel's SMBus and Philips' I^2C bus.

The rest of this section introduces the various features of the SMBus master capability. These features are divided into the following sections:

- SMBus and I^2C compliant
- AMD-TSI
- PCH
- SMBus master

20.2 Introduction to the SMBus Master

20.2.1 Data Transfer Format

Every byte transferred on the bus consists of 8 bits. After the start condition, the master places the 7-bit address to the slave device it wants to address on the bus. The address followed an eight bit indicating the direction of the data transfer (R/W#); a zero indicates a transmission for data while a one indicates a request for data. Each byte is transferred with the most significant bit first, and after each byte, an acknowledge signal must follow. A data transfer is always terminated by stop condition generated by master.

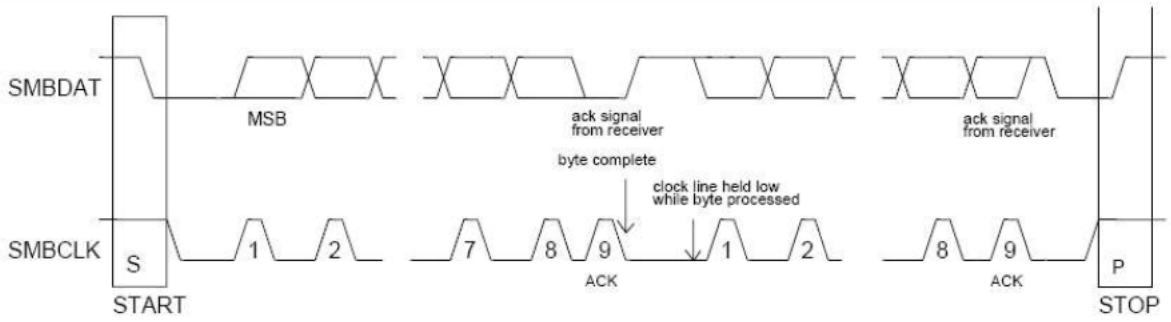

Figure 20-1 Data Transfer Format

20.2.2 Arbitration

Arbitration takes place on the SMBDAT data line while the SMBCLK line is high. Two devices may generate a start condition at the same time and enter the arbitration procedure. Arbitration continues until one master generates a HIGH level on the SMBDAT line while another competing master generates a LOW level on the SMBDAT line while SMBCLK is high. The master device which generated the HIGH level on SMBDAT loses arbitration. If a device loses arbitration during the first byte following a start condition i.e. while transmitting a slave address it becomes a slave receiver and monitors the address for a potential match. Arbitration may also be lost in the master receive mode during the acknowledge cycle.

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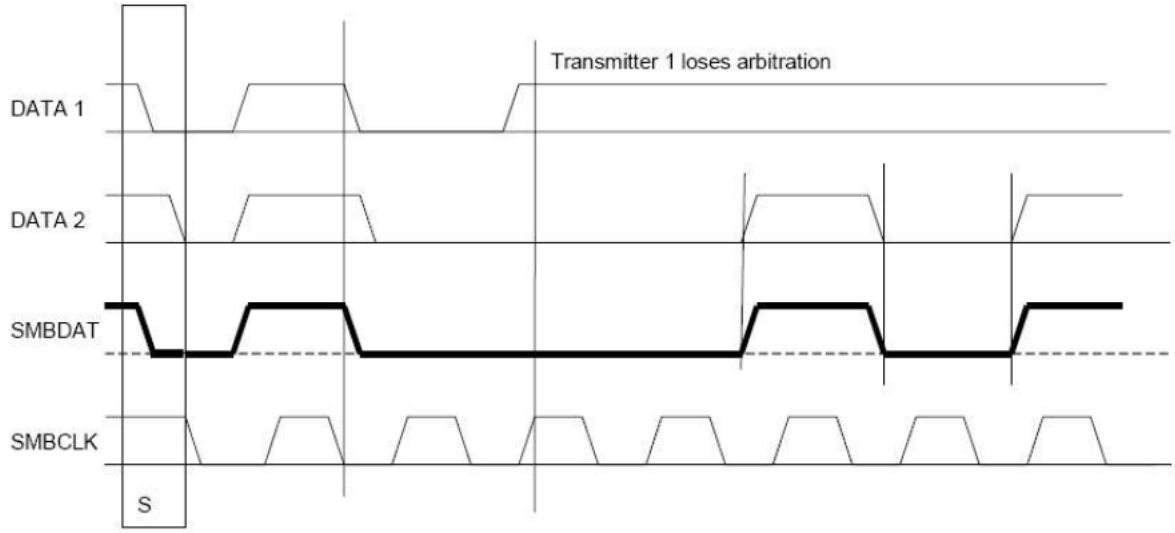

Figure 20-2 SMBus Arbitration

20.2.3 Clock Synchronization

Clock synchronization is performed while the arbitration procedure described above is in effect. Clock Synchronization takes place between two competing devices by utilizing the wired-AND nature of the SMBCLK line. The SMBCLK line will go low as soon as the master with the shortest high time pulls SMBCLK low. SMBCLK will remain low until the device with the longest SMBCLK low time relinquishes the SMBCLK line. Therefore the SMBCLK high time is determined by device with the shortest high time while the SMBCLK low time is determined by the device with the longest low time.

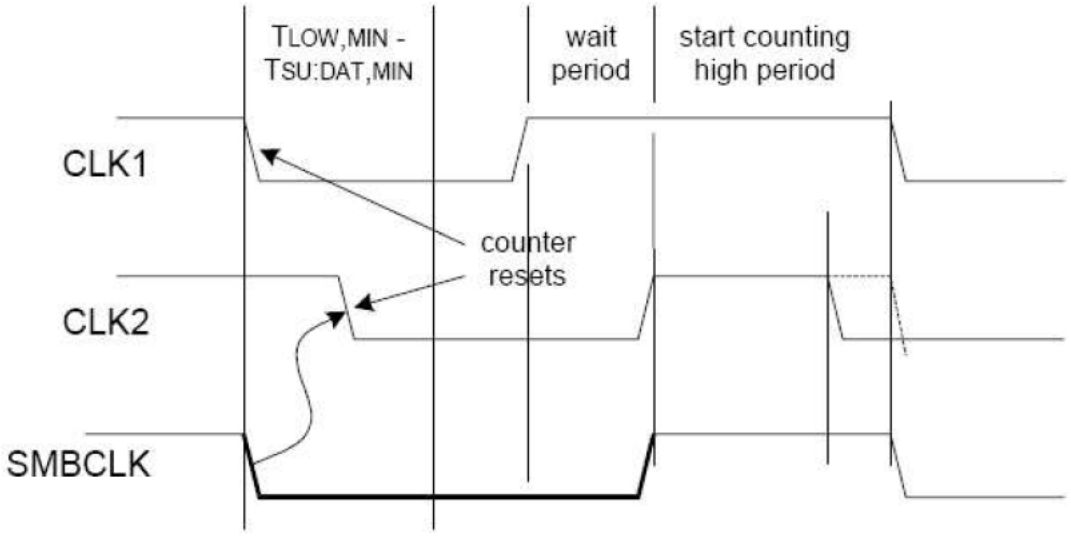

Figure 20-3 Clock synchronization

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20.3 SB-TSI

The combined-format repeated start sequence is not supported in standard-mode and fast-mode.

- Only 7-bit SMBus addresses are supported.
- SB-TSI implements the Send/Receive Byte and Read/Write Byte protocols.
- SB-TSI registers can only by written using a write byte command.
- Address Resolution Protocol (ARP) is not implemented.
- Packet Error Checking (PEC) is not supported.

20.3.1 SB-TSI Address

The SMBus address is really 7 bits. The SB-TSI address is normally 98h or 4Ch. The address could vary with address select bits.

Table 20-1 SB-TSI Address Encoding

Address Select Bits	SB-TSI Address
000b	98h
001b	9Ah
010b	9Ch
011b	9Eh
100b	90h
101b	92h
110b	94h
111b	96h

20.4 PCH

The PCH provide system thermal data to EC. The EC can manage the fans and other cooling elements based on this data. A subset of the thermal collection is that the PCH and be programmed to alert the EC when a device has gone outside of its temperature limits.

20.4.1 Command Summary

Table 20-2 PCH Command Summary

Trans-action	Slave Addr.	Data Byte 0 =Command	Data Byte 1 =Byte Count	Data Byte 2	Data Byte 3	Data Byte 4	Data Byte 5	Data Byte 6	Data Byte 7
Write STS Preferences	I2C	0x41	0x6	STS [47:40]	STS [39:32]	STS [31:24]	STS [23:16]	STS [15:8]	STS [7:0]
Write CPU Temp Limits	I2C	0x42	0x6	Lower Limit [15:8]	Lower Limit [7:0]	Upper Limit [15:8]	Upper Limit [15:8]		
Write MCH	I2C	0x43	0x2	Lower	Upper	na	na		

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Trans-action	Slave Addr.	Data Byte 0 =Com mand	Data Byte 1 =Byte Count	Data Byte 2	Data Byte 3	Data Byte 4	Data Byte 5	Data Byte 6	Data Byte 7
Temp Limits				Limit [7:0]	Limit [7:0]				
Write IBX Temp Limits	I2C	0x44	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write DIMM Temp Limits	I2C	0x45	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write MPC CPU Power Clamp	I2C	0x50	0x2	Lower Limit [7:0]	Power Clamp [7:0]				
Block Read	Block Read Address	0x40	Block Read Address	Byte Count	Data 0	Data N	PEC (optional)		

20.5 SMBus Master

20.5.1 Block Diagram

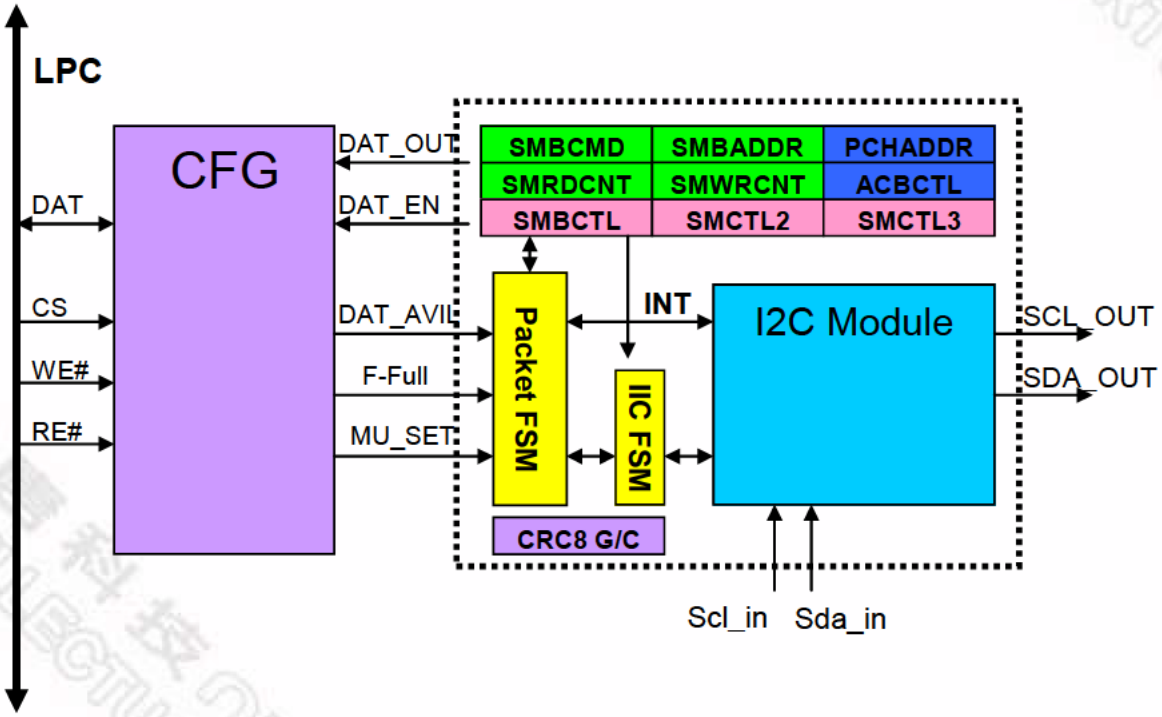

Figure 20-4 SMBus Master Block Diagram

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20.5.2 Programming Flow

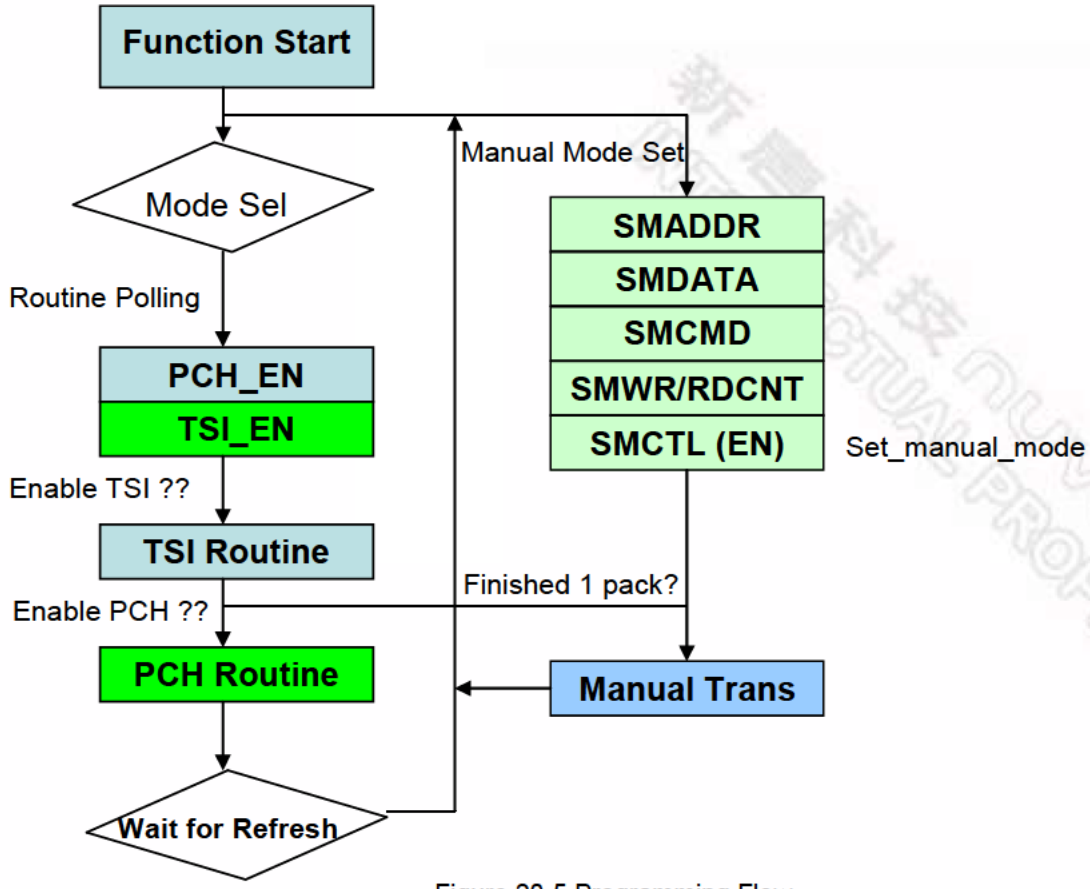

Figure 20-5 Programming Flow

20.5.3 TSI Routine

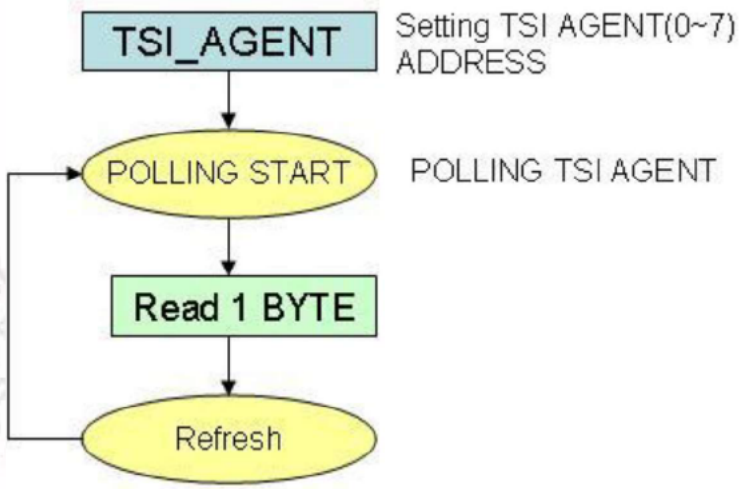

Figure 20-6 TSI Routine

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20.5.4 PCH Routine

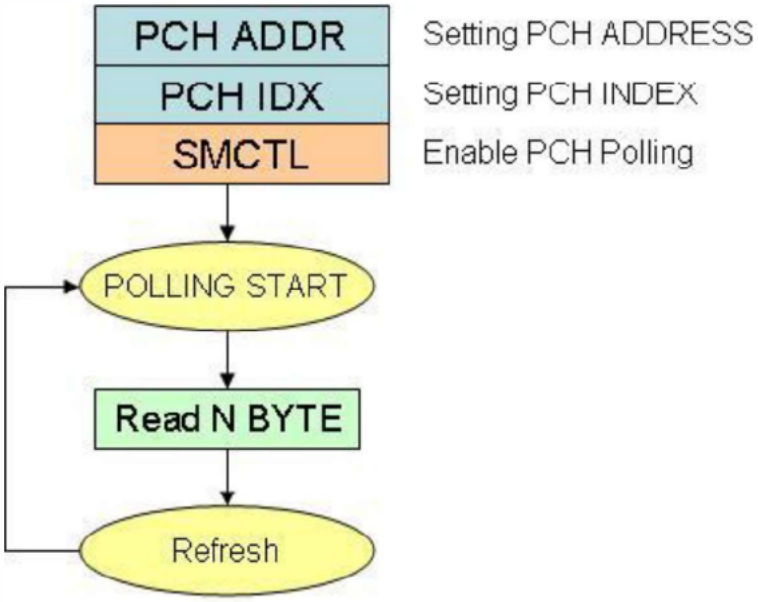

Figure 20-7 PCH Routine

20.5.5 BYTE Ruttine

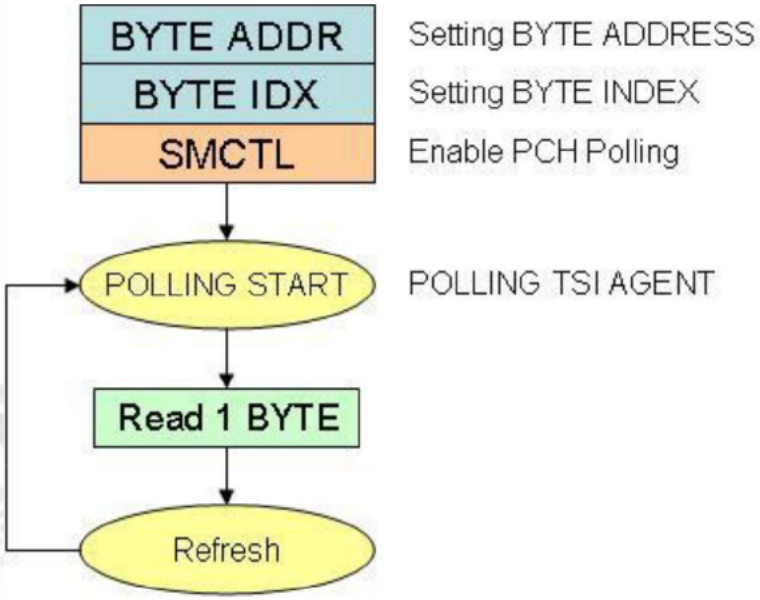

Figure 20-8 PCH Routine

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20.5.6 Manual Mode interface

The SMBus host supports Block/Word/Byte Write and Block/Word/Byte read with PEC. The SMBus host can use the interface to access the smbus slave. The timing diagrams below illustrate how to use the smbus interface to write the data or read the data to the smbus slave.

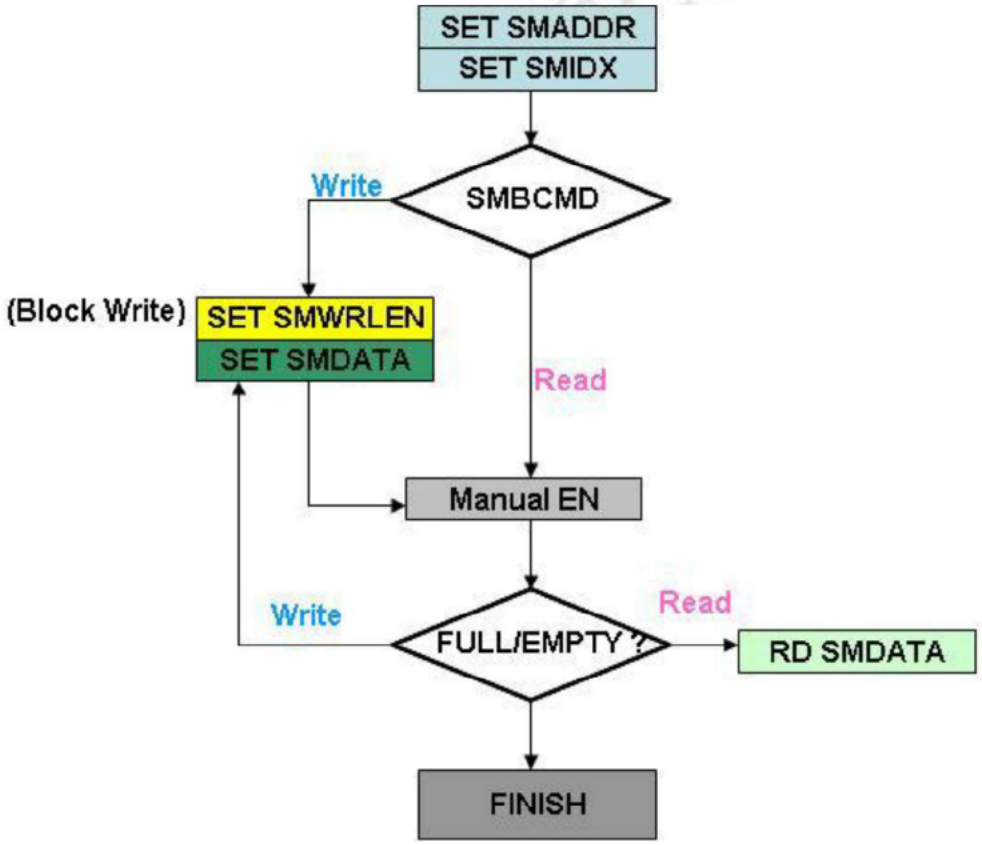

Figure 20-9 Manual Mode Programming Flow

20.6 Register Type Abbreviations

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register.
- W = Write.
- RO = Read-only.

To program the SMBus master configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

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20.6.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x26 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

20.6.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

20.7 SMBus Master Register Set

20.7.1 SMBus Register Map

SMBus Master base address in register Logic Device B CR62h(MSB), CR63h(LSB).

Table 20-3 SMBus Master Bank 0 Registers

Offset	Type	Name	Section
0	R/W	**SMDATA**	25.7.2
1	R/W	**SMWRSIZE**	25.7.3
2	R/W	**SMBCMD**	25.7.4
3	R/W	**SMIDX**	25.7.5
4	R/W	**SMCTL**	25.7.6
5	R/W	**SMADDR**	25.7.7
6	R/W	**SCLFREQ**	25.7.8
7	RO	**Reserved**	--
8	R/W	**PCHADDR**	25.7.10
9	R/W	**Error_status**	25.7.11
A	R/W	**Reserved**	--
B	R/W	**PCHCMD**	25.7.13
D	R/W	**TSI_AGENT**	--
E	R/W	**SMCTL3**	25.7.15
F	R/W	**SMCTL2**	25.7.15
10	R/W	**BYTE_ADDR**	
11	R/W	**BYTE_IDX_H**	
12	R/W	**BYTE_IDX_L**	
13	R/W	**Reserved**	
14	R/W	**Reserved**	

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20.7.2 SMBus Data (SMDATA) – Bank 0

This 32 bits register is the data in and out register of SMBus data register. Before writing to SMDATA register, this register contains the input data, after writing to SMDATA register, this register contains the output data.

Offset: 0h

Type: R/W

Byte	3	2	1	0
Name	**SMFIFO3**	**SMFIFO2**	**SMFIFO1**	**SMFIFO0**
Default	00h	00h	00h	00h

Byte	Description
3	**SMFIFO3 (SMBus FIFO 3).** This byte represents the high byte of the 32 bits SMBus data.
2	**SMFIFO2 (SMBus FIFO 2).** This byte represents the second byte of the 32 bits SMBus data.
1	**SMFIFO1 (SMBus FIFO 1).** This byte represents the first byte of the 32 bits SMBus data.
0	**SMFIFO0 (SMBus FIFO 0).** This byte represents the low byte of the 32 bits SMBus data.

20.7.3 SMBus Write Data Size (SMWRSIZE) – Bank 0

Offset: 1h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**SMWRSIZE**				
Default	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved.**
4-0	**SMWRSIZE (SMBus Write Byte Counter).** This field sets the write byte counter, the max counter size is 32 bytes, and the minimal size is 1 bytes.

20.7.4 SMBus Command (SMCMD) – Bank 0

Offset: 2h

Type: R/W

Bit	7	6	5	4	3	2	1	0
NAME	REV				SMBus CMD			
Default	0	0	0	0	0	0	0	0

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Bit	Description
7-4	**Reserved.**
3-0	**SMBCMD (SMBus Command).** This field sets SMBus Command: 0000 : Read Byte (Default) 0001 : Read Word 0010 : Read Block 0011 : Block Write and Read Process Call 0100 : Process Call 1000 : Write Byte 1001 : Write Word 1010 : Write Block

20.7.5 SMBus INDEX (SMIDX) – Bank 0

Offset: 3h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SMCMD**							
Default	0	0	0	0	0	0	0	0

Bit	Description
7-0	**SMIDX (SMBus INDEX).** This field represents the index data of the SMBus.

20.7.6 SMBus Control (SMCTL) – Bank 0

Offset: 4h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**MMODE_S**	**S_RST**	**CRC8_EN**	**REFLASH_CLK**			**BYTE_EN**	**PCH_EN**
Default	0	0	0	0	0	0	0	0

Bit	Description
7	**MMODE_S (Manual Mode Set).** 0 : Disable. 1 : Enable.
6	**S_RST (Soft Reset SMBus).** 0 : Disable. 1 : Enable.

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Bit	Description
5	**CRC8_EN (CRC8 Enable).** 0 : CRC8 function is disable. 1 : CRC8 function is enable.
4-2	**REFRASH_CLK (Refrash Clock Select).** 000, 100 – 128ms 001, 101 – 256ms 010, 110 – 512ms 011, 111 – 64ms (1KHz)
1	**BYTE_EN (BYTE Enable).** 0 : BYTE function is disable. 1 : BYTE function is enable.
0	**PCH_EN (PCH Enable).** 0 : PCH function is disable. 1 : PCH function is enable.

20.7.7 SMBus Address (SMADDR) – Bank 0

Offset: 5h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SMADDR**							**REV**
Default	0	0	0	0	0	0	0	0

Bit	Description
7-1	**SMADDR (SMBus Address).** AMD-TSI only supports 7-bit SMBus address.
0	**Reserved:** 0 : Write. If the protocol is write, the WR_SIZE can't be zero. (Default)

20.7.8 SCL FREQ (SCLFREQ) – Bank 0

Offset: 6h

Type: R/W

Bit	7	6	5	4	3	2	1	0
	Reserved:				**SCLFREQ**			
Default	0	0	0	0	0	1	1	1

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Bit	Description
7-4	Reserved
3-0	**SCLFQ (SMBCLK Frequency).** This field defines the SMBCLK period (low time and high time). The clock low time and high time ate defined as follows: 0000 : 365KHz 0001 : 261KHz 0010 : 200KHz 0011 : 162KHz 0100 : 136KHz 0101 : 117KHz 0110 : 103KHz 0111 : 91.5KHz (Default) 1000 : 83KHz 1001 : 76KHz 1010 : 70KHz 1011 : 65KHz 1100 : 61KHz 1101 : 57KHz 1110 : 53KHz 1111 : 47KHz

20.7.9 PCH Address (PCHADDR) – Bank 0

Offset: 8h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	PCHADDR							REV
Default	1	0	0	1	0	1	0	0

Bit	Description
7-1	**PCHADDR (PCH Address).** PCH supports 8-bit SMBus address. The default address is 94h. The last bit is read or write bit. It needs to set to "0".

20.7.10 SMBus Error Status (Error_status) – Bank 0

Offset: 9h

Type: RO/W1C

Bit	7	6	5	4	3	2	1	0
Name	REV		ADNACK	Timeout	Reserved	BER	NACK	Reserved
Default	1	0	0	1	0	1	0	0

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Bit	Description
7-6	**Reserved.**
5	**ADDR Non ACK.** This bit reflects SMBus occurred ADDRESS NON ACK in Manual mode..
4	**Timeout.** This bit reflects when SMBus occurs timeout.
3	**Reserved.**
2	**BER (Bus Error).** This bit reflects when a start or stop condition is detected during data transfer, or when an arbitration problem is detected.
1	**NACK (Negative acknowledge).** This bit is set by hardware when a transmission is not acknowledged on the ninth clock. While NACK is set SCL will be drive low and subsequent bus transactions are stalled until NACK is cleared.
0	**Reserved.**

20.7.11 PCH Command (PCHCMD) – Bank 0

Offset: bh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**PCHCMD**							
Default	0	1	0	0	0	0	0	0

Bit	Description
7-0	**PCHCMD (PCH Command).** This field represents the command data of the PCH. The default command is block read (40h).

20.7.12 TSI Agent Enable Register (TSI_AGENT) – Bank

Offset: dh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	AG7	AG6	AG5	AG4	AG3	AG2	AG1	AG0
Default	0	0	0	0	0	0	0	0

Bit	Description
7	**TSI AGENT7 Enable. :** This bit reflects AMD-TSI Agent enbale. 0 : Diable
6	**TSI AGENT6 Enable. :** This bit reflects AMD-TSI Agent enbale. 0 : Diable
5	**TSI AGENT5 Enable. :** This bit reflects AMD-TSI Agent enbale. 0 : Diable

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Bit	Description
4	**TSI AGENT4 Enable. :** This bit reflects AMD-TSI Agent enbale. 0 : Diable
3	**TSI AGENT3 Enable. :** This bit reflects AMD-TSI Agent enbale. 0 : Diable
2	**TSI AGENT2 Enable. :** This bit reflects AMD-TSI Agent enbale. 0 : Diable
1	**TSI AGENT1 Enable. :** This bit reflects AMD-TSI Agent enbale. 0 : Diable 1 : Full
0	**TSI AGENT0 Enable. :** This bit reflects AMD-TSI Agent enbale. 0 : Diable 1 : Empty

20.7.13SMBus Control 3 Register (SMCTL3) – Bank 0

Offset: eh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Reserved				CRC_CHK	M_MODE	F_FULL	F_EMPT
Default	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3	**CRC_CHK (CRC Check).** 0 : incorrect 1 : correct
2	**M_MODE (Manual Mode).** 0 : Non-active 1 : Active
1	**F_FULL (fifo_full). :** This bit reflects SMBus data fifo is full. 0 : Non-full 1 : Full
0	**F_EMPT (fifo empty). :** This bit reflects the SMBus data fifo is empty. 0 : Non-empty 1 : Empty

20.7.14SMBus Control 2 Register (SMCTL2) – Bank 0

Offset: fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Reserved		INT_LCH_E	Reserved		BYTE_SEL	BANKSEL	
Default	0	0	0	0	0	0	0	0

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Bit	Description
7-6	**Reserved.**
5	**INT_LCH_E (Interrupt Latch Enable). :** This bit will latch the I2CSTA register. 0 : Disable. 1 : Enable.
2	**BYTE_SEL :**This field represents byte polling 8-bit/16bit select bits. 0: BYTE_TEMP is 16 bit data 1: BYTE_TEMP is 8 bit data
1-0	**BANKSEL (Bank Select).** 00 – Bank 0. 01 – Bank 1. 10 – Bank 2.

20.7.15BYTE ADDRESS (BYTE ADDR) – Bank 0

Offset: 10h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_ADDRESS**							
Default	0	1	0	0	0	0	0	0

Bit	Description
7-0	**BYTE ADDRESS (BYTE ADDR).** This field represents the address data of the BYTE.

20.7.16BYTE INDEX_H (BYTE_IDX_H) – Bank 0

Offset: 11h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_IDX_H**							
Default	0	0	0	0	0	0	0	1

Bit	Description
7-0	**BYTE_IDX_H (High BYTE INDEX).** This field represents the high byte index of the Byte polling. The default command is byte read (01h).

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20.7.17BYTE INDEX_L (BYTE_IDX_L) – Bank 0

Offset: 12h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	BYTE_IDX_L							
Default	0	0	0	1	0	0	0	0

Bit	Description
7-0	**BYTE_IDX_L (LOW BYTE INDEX).** This field represents the low byte index of the Byte polling. The default command is byte read (10h).

The EC may read thermal information from IBX using the SMBus block read command. The IBX doesn't support byte-read or word-read SMBus commands. The read use a different address that the writes. The address must be different so that the IBX knows which target Is intended, either the I2C target or the block read buffer.

The IBX and EC are set up by BIOS with the length of the read that is supported by the platform. The EC must always do reads of the lengths set up by BIOS. There is no way to change the length of the read after BIOS has set things up.

An EC that only wants the single highest temperature among MCH, and CPU could read one byte. A 2 byte read would provide both IBX and CPU/MCH package temperature. An EC that wanted each components temperature would do a 4 byte read. An EC that also wanted DIMM information would read 9 bytes. If an EC wanted to read the HOST STS status, it must read 19 bytes. An EC can also read the energy data provided by the CPU by reading 12 bytes.

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21. FADDING LED

21.1 FADDING LED DESCRIPTION

The NCT6102D / NCT6106D provides Fadding led interface that can be changed led speed of bright or dark througt different frequency or duty cycle. Furthermore, the constrast of led bright or dark can be decided by maximum duty cycle, minimum duty cycle, and middle value.

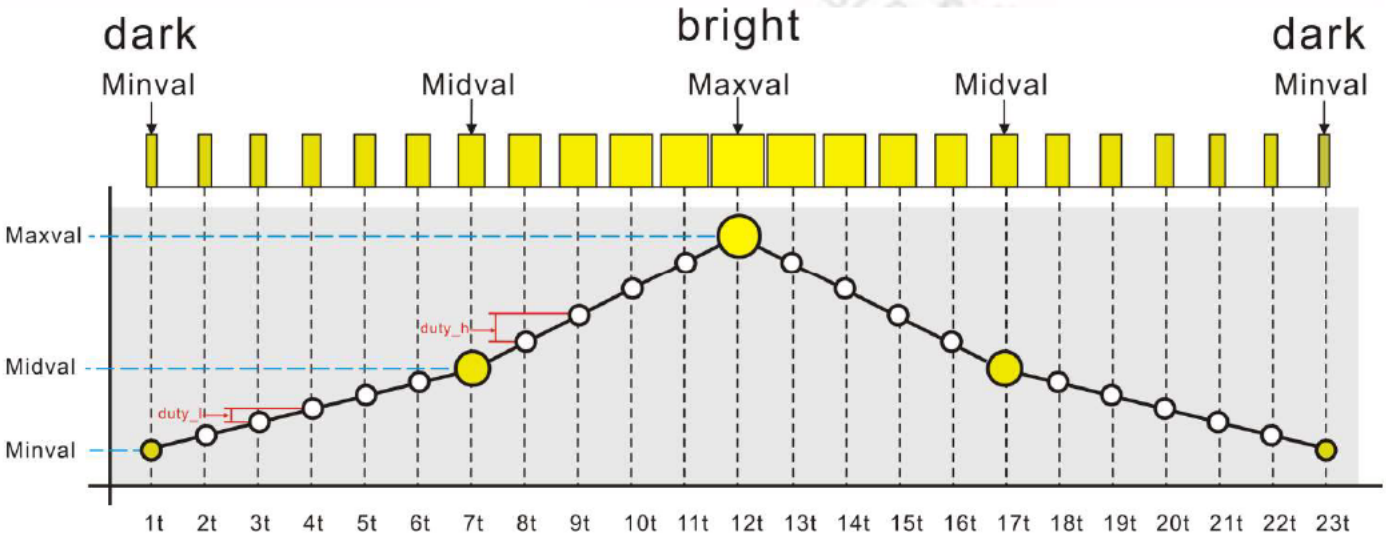

Figure 21-1 Example of Fading LED

21.2 MODULE OPERATION

MAXVAL:

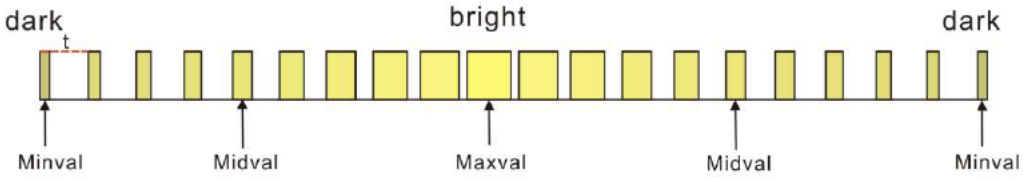

Fig1. Maxval=8'hF0

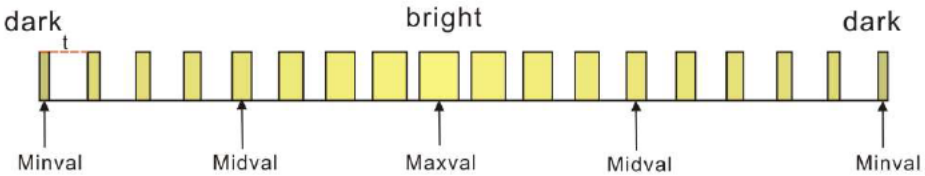

Fig2. Maxval=8'hC0

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MIDVAL:

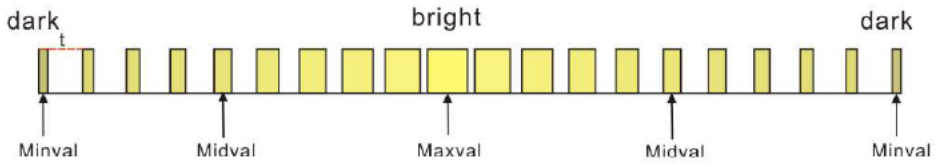

Fig1. Midval=8'h3F

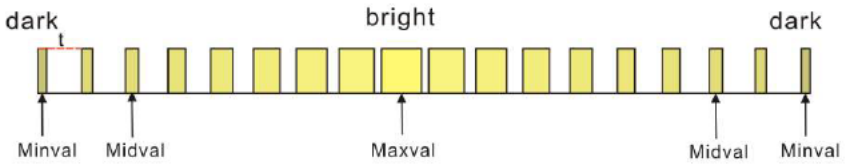

Fig2. Midval=8'h1F

MINVAL:

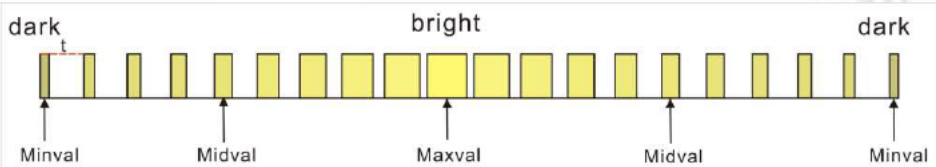

Fig1. Minval=8'h01

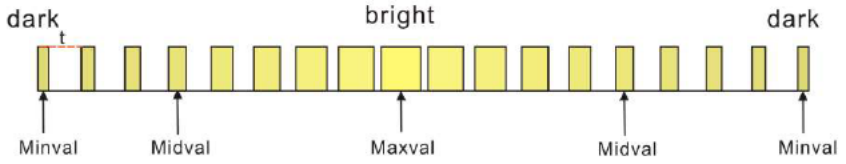

Fig2. Minval=8'h0F

DUTY HIGH, DUTY LOW:

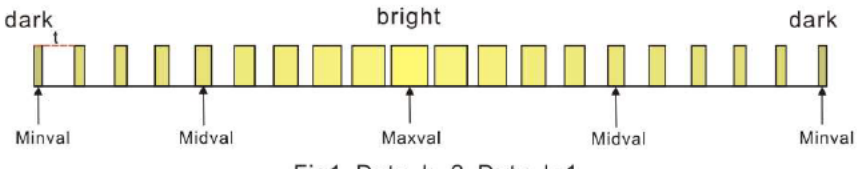

Fig1. Duty_h=2, Duty_l=1

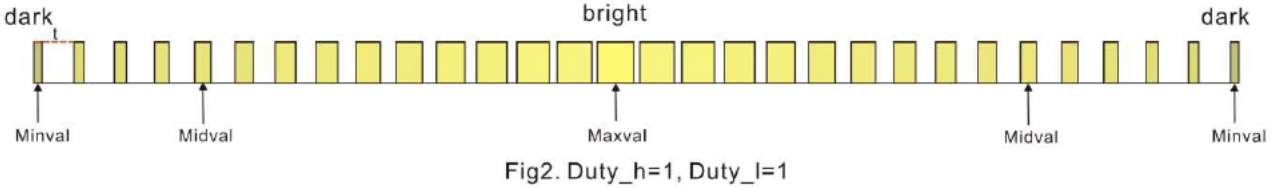

Fig2. Duty_h=1, Duty_l=1

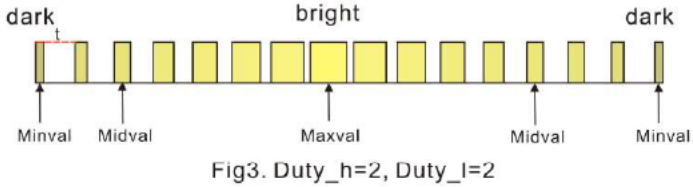

Fig3. Duty_h=2, Duty_l=2

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PRGVAL: (Repeat Duty cycle value)

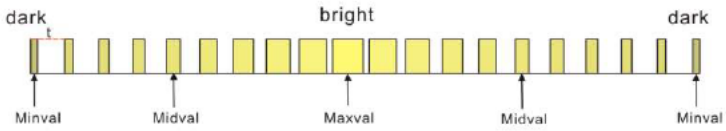

Fig1. Prgval=0

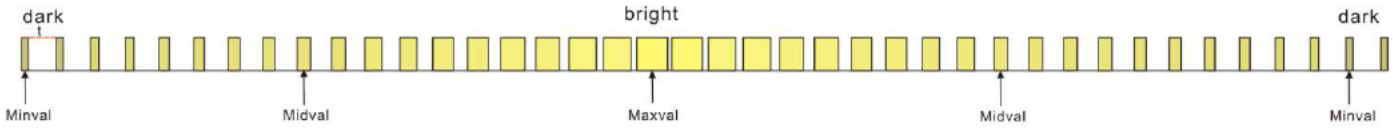

Fig2. Prgval=1

21.3 EXAMPLE ILLUSTRATION

The fading led supports three display mode, solid led, blink led, and fading led. Take pled as an example, solid led is configured through control registers logical device 15 CR[E0], CR[E5], CR[E8], shows in table 3.1, blink led is configured through control registers logical device 15 CR[E0], CR[E5], CR[E8], shows in table 3.2, fading led is configured through control registers logical device 15 CR[E0]~CR[E8] shows in table 3.3.

Table 21-1 Solid led configure mode

Logical Device 15	
Register location	**Value**
CR E0	8'h7F
CR E5	8'h02
CR E8	8'h10

Table 21-2 Blink led configure mode

Logical Device 15	
Register location	**Value**
CR E0	8'h7F
CR E5	8'h00
CR E8	8'h02

Table 21-3 Fading led configure mode

Logical Device 15	
Register location	**Value**
CR E0	8'hFF
CR E1	8'h7F
CR E2	8'h01
CR E3	8'h11

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Logical Device 15	
Register location	**Value**
CR E4	8'h11
CR E5	8'h23
CR E6	8'h00
CR E7	8'h00
CR E8	8'h10

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22. PORT80 TO UART

The NCT6102D / NCT6106D provides UART interface to transfer PORT80 information to other peripheral devices. Default baud rate is 115200Hz for universal UART protocol and it could be change by LD14 CRE2 and LD14 CRE3. When BIOS program PORT80 LED, in proportion to UART baud rate, it changes very frequently. Thus, some information might be lose. But we make sure the last one would be send.

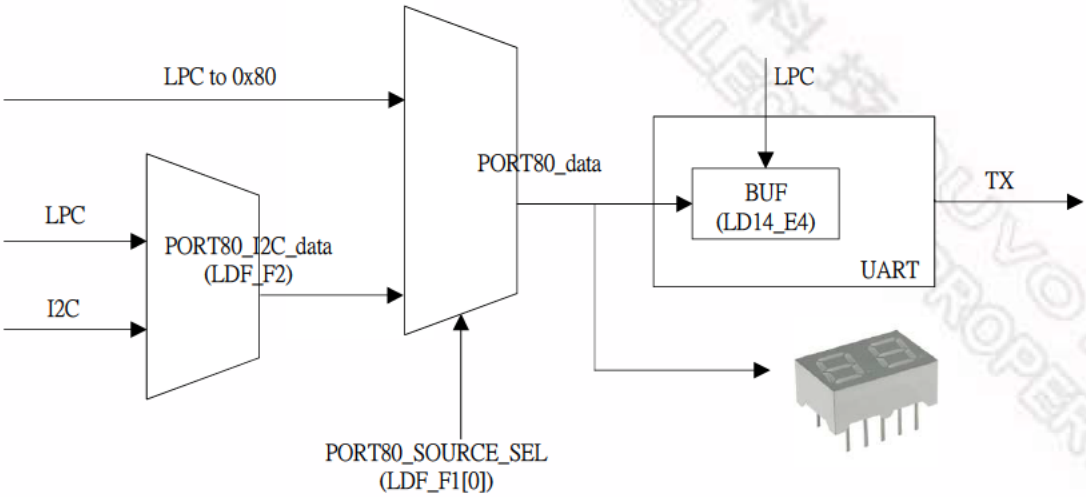

Figure 22-1 PORT80 to UART Block Diagram

After enter OS, we support other root to control PORT80 LED by write LDF CRF2 and LDF CRF1 to change other path. The UART could be control by other root, too. It is set by LD14 CRE4.

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23. CONFIGURATION REGISTER

23.1 Chip (Global) Control Register

CR 02h. Software Reset Register

Location: Address 02h
Attribute: Write Only
Power Well: VCC
Reset by: LRESET#
Default :
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	Write "1" Only	Software RESET.

CR 07h. Logical Device Selection

Location: Address 07h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Logical Device Number.

CR 10h. Device IRQ TYPE Selection

Location: Address 10h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	FDC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
6	R / W	PRT IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5	R / W	UARTA IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

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BIT	READ / WRITE	DESCRIPTION
4	R / W	UARTB IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
3	R / W	KBC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
2	R / W	MOUSE IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
1	R / W	CIR IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	R / W	CIRWAKUP IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 11h. Device IRQ TYPE Selection

Location: Address 11h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	HM IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
6	R / W	WDTO IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5	R / W	UARTC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4	R / W	UARTD IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
3	R / W	UARTE IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

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BIT	READ / WRITE	DESCRIPTION
2	R / W	UARTF IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
1	R / W	SMI IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	Reserved.	

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 13h. Device IRQ Polarity Selection

Location: Address 13h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<15:8> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 14h. Device IRQ Polarity Selection

Location: Address 14h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<7:0> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 1Ah. Multi Function Selection

Location: Address 1Ah
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : CCh
Size: 8 bits

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<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin15 function selection
<table>
<tr><th>CR24 [Bit7]</th><th>CR1A [Bit7]</th><th>Pin15</th></tr>
<tr><td>0</td><td>0</td><td>IRRX</td></tr>
<tr><td>0</td><td>1</td><td>CIRRX</td></tr>
<tr><td>1</td><td>x</td><td>WP#</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin16 function selection
<table>
<tr><th>CR24 [Bit7]</th><th>CR1A [Bit6]</th><th>Pin16</th></tr>
<tr><td>0</td><td>0</td><td>IRTX</td></tr>
<tr><td>0</td><td>1</td><td>CIRTX</td></tr>
<tr><td>1</td><td>x</td><td>RDATA#</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>R / W</td><td>Pin31 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>CR1A [Bit5-4]</th><th>CR24 [Bit7]</th><th>Pin31</th></tr>
<tr><td>1</td><td>xx</td><td>x</td><td>LED_A</td></tr>
<tr><td>0</td><td>00</td><td>x</td><td>PLED</td></tr>
<tr><td>0</td><td>01</td><td>x</td><td>SLCT</td></tr>
<tr><td>0</td><td>1x</td><td>0</td><td>DRVDEN0</td></tr>
</table>
Pin32 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>CR1A [Bit5-4]</th><th>CR24 [Bit7]</th><th>Pin32</th></tr>
<tr><td>1</td><td>xx</td><td>x</td><td>LED_B</td></tr>
<tr><td>0</td><td>00</td><td>x</td><td>GP30</td></tr>
<tr><td>0</td><td>01</td><td>x</td><td>PE</td></tr>
<tr><td>0</td><td>1x</td><td>0</td><td>INDEX#</td></tr>
</table>
Pin33 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>CR1A [Bit5-4]</th><th>CR24 [Bit7]</th><th>Pin33</th></tr>
<tr><td>1</td><td>xx</td><td>x</td><td>LED_C</td></tr>
<tr><td>0</td><td>00</td><td>x</td><td>GP31</td></tr>
<tr><td>0</td><td>01</td><td>x</td><td>BUSY</td></tr>
<tr><td>0</td><td>1x</td><td>0</td><td>MOA#</td></tr>
</table></td></tr>
</table>

Publication Release Date: January 11, 2012
Version: 1.0

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BIT	READ / WRITE	DESCRIPTION
5-4	R / W	Pin34 function selection

GPIO_PORT80_SEL	CR1A [Bit5-4]	CR24 [Bit7]	Pin34
1	xx	x	LED_D
0	00	x	GP32
0	01	x	ACK#
0	1x	0	DSA#

Pin35 function selection

GPIO_PORT80_SEL	CR1A [Bit5-4]	CR24 [Bit7]	Pin35
1	xx	x	LED_E
0	00	x	GP33
0	01	x	PD7
0	1x	0	DIR#

Pin36 function selection

GPIO_PORT80_SEL	CR1A [Bit5-4]	CR24 [Bit7]	Pin36
1	xx	x	LED_F
0	00	x	GP34
0	01	x	PD6
0	1x	0	STEP#

Pin37 function selection

GPIO_PORT80_SEL	CR1A [Bit5-4]	CR24 [Bit7]	Pin37
1	xx	x	LED_G
0	00	x	GP35
0	01	x	PD5
0	1x	0	WD#

Pin38 function selection

GPIO_PORT80_SEL	CR1A [Bit5-4]	CR24 [Bit7]	Pin38
1	xx	x	DGH#
0	00	x	GP36
0	01	x	PD4
0	1x	0	WE#

Pin39 function selection

GPIO_PORT80_SEL	CR1A [Bit5-4]	CR24 [Bit7]	Pin39
1	xx	x	DGL#
0	00	x	GP37
0	01	x	PD3
0	1x	0	TRAK0#

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BIT	READ / WRITE	DESCRIPTION
5-4	R / W	Pin40 function selection

GPIO_PORT80_SEL	CR1A [Bit5-4]	CR24 [Bit7]	Pin40
1	xx	x	GP40
0	00	x	GP40
0	01	x	PD2
0	1x	0	WP#

Pin41 function selection

GPIO_PORT80_SEL	CR1A [Bit5-4]	CR24 [Bit7]	Pin41
1	xx	x	GP41
0	00	x	GP41
0	01	x	PD1
0	1x	0	RDATA#

Pin42 function selection

GPIO_PORT80_SEL	CR1A [Bit5-4]	CR24 [Bit7]	Pin42
1	xx	x	GP42
0	00	x	GP42
0	01	x	PD0
0	1x	0	HEAD#

Pin43 function selection

GPIO_PORT80_SEL	CR1A [Bit5-4]	CR24 [Bit7]	Pin43
1	xx	x	GP43
0	00	x	GP43
0	01	x	SLIN#
0	1x	0	DSKCHG#

Pin44 function selection

GPIO_PORT80_SEL	CR1A [Bit5-4]	Pin44
1	xx	GP44
0	00	GP44
0	01	INIT#
0	1x	GP44

Pin45 function selection

GPIO_PORT80_SEL	CR1A [Bit5-4]	Pin45
1	xx	GP45
0	00	GP45
0	01	ERR#
0	1x	GP45

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<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>5-4</td><td>R / W</td><td>Pin46 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>CR1A [Bit5-4]</th><th>Pin46</th></tr>
<tr><td>1</td><td>xx</td><td>GP46</td></tr>
<tr><td>0</td><td>00</td><td>GP46</td></tr>
<tr><td>0</td><td>01</td><td>AFD#</td></tr>
<tr><td>0</td><td>1x</td><td>GP46</td></tr>
</table>
Pin47 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>CR1A [Bit5-4]</th><th>Pin47</th></tr>
<tr><td>1</td><td>xx</td><td>GP47</td></tr>
<tr><td>0</td><td>00</td><td>GP47</td></tr>
<tr><td>0</td><td>01</td><td>STB#</td></tr>
<tr><td>0</td><td>1x</td><td>GP47</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Pin62 function selection
<table>
<tr><th>CR1A [Bit3]</th><th>Pin62</th></tr>
<tr><td>0</td><td>GP50</td></tr>
<tr><td>1</td><td>KCLK</td></tr>
</table>
Pin63 function selection
<table>
<tr><th>CR1A [Bit3]</th><th>Pin63</th></tr>
<tr><td>0</td><td>GP51</td></tr>
<tr><td>1</td><td>KDAT</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin65 function selection
<table>
<tr><th>CR1A [Bit2]</th><th>Pin65</th></tr>
<tr><td>0</td><td>GP52</td></tr>
<tr><td>1</td><td>MCLK</td></tr>
</table>
Pin66 function selection
<table>
<tr><th>CR1A [Bit2]</th><th>Pin66</th></tr>
<tr><td>0</td><td>GP53</td></tr>
<tr><td>1</td><td>MDAT</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Pin67 function selection
<table>
<tr><th>CR1A [Bit1]</th><th>Pin67</th></tr>
<tr><td>0</td><td>PSOUT#</td></tr>
<tr><td>1</td><td>GP54</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin68 function selection
<table>
<tr><th>CR1A [Bit0]</th><th>Pin68</th></tr>
<tr><td>0</td><td>PSIN#</td></tr>
<tr><td>1</td><td>GP55</td></tr>
</table></td></tr>
</table>

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CR 1Bh. Multi Function Selection

Location: Address 1Bh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 03h
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin70 function selection
<table>
<tr><td>CR1B [Bit7]</td><td>Pin70</td></tr>
<tr><td>0</td><td>SLP_S5#</td></tr>
<tr><td>1</td><td>GP56</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin71 function selection
<table>
<tr><td>CR1B [Bit6]</td><td>Pin71</td></tr>
<tr><td>0</td><td>PWROK</td></tr>
<tr><td>1</td><td>GP57</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin72 function selection
<table>
<tr><td>CR1B [Bit5]</td><td>Pin72</td></tr>
<tr><td>0</td><td>PSON#</td></tr>
<tr><td>1</td><td>GP60</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td>Pin73 function selection
<table>
<tr><td>CR1B [Bit4]</td><td>Pin73</td></tr>
<tr><td>0</td><td>SLP_S3#</td></tr>
<tr><td>1</td><td>GP61</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Pin75 function selection
<table>
<tr><td>CR1B [Bit3]</td><td>Pin75</td></tr>
<tr><td>0</td><td>RSMRST#</td></tr>
<tr><td>1</td><td>GP62</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin87 function selection
<table>
<tr><td>CR27 [Bit3]</td><td>CR1B [Bit2]</td><td>Pin87</td></tr>
<tr><td>0</td><td>0</td><td>GP71</td></tr>
<tr><td>0</td><td>1</td><td>TSIC</td></tr>
<tr><td>1</td><td>x</td><td>CIRRXWB</td></tr>
</table>
Pin88 function selection
<table>
<tr><td>CR1B [Bit2]</td><td>Pin88</td></tr>
<tr><td>0</td><td>PECI</td></tr>
<tr><td>1</td><td>TSID</td></tr>
</table></td></tr>
</table>

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BIT	READ / WRITE	DESCRIPTION
1-0	R / W	Pin94 function selection CR1B [Bit1-0] / Pin94: 1x = SDA; 00 = GP63; 01 = MSDA Pin96 function selection CR1B [Bit1-0] / Pin96: 1x = SCL; 00 = GP64; 01 = MSCL

CR 1Ch. Multi Function Selection

Location: Address 1Ch
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 10h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	Pin95 function selection CR1C [Bit7] / Pin95: 0 = OVT#; 1 = SMI#
6	R / W	Pin106 function selection CR1C [Bit6] / Pin106: 0 = SUSLED; 1 = GP65
5	R / W	Pin107 function selection CR1C [Bit5] / Pin107: 0 = KEYLOCK#; 1 = GP66
4	R / W	Pin108 function selection CR27 [Bit2] / CR1C [Bit4] / Pin108: 0 / 0 = 14.7456MHZ_CLKIN; 0 / 1 = GP67; 1 / x = ATXPGD

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BIT	READ / WRITE	DESCRIPTION
3	R / W	Pin109-116 function selection SOUTC_P80_SEL / CR1C [Bit3] / Pin109-116 1 / x / GP0x, SOUTC_P80 0 / 0 / GP0x 0 / 1 / UARTC
2	R / W	Pin117-124 function selection CR1C [Bit2] / Pin117-124 0 / GP1x 1 / UARTD
1	R / W	Pin125-4 function selection SOUTE_P80_SEL / CR1C [Bit1] / Pin125-4 1 / x / GP2x, SOUTE_P80 0 / 0 / GP2x 0 / 1 / UARTE
0	Reserved.	

CR 20h. Chip ID (High Byte)

Location: Address 20h
Attribute: Read Only
Power Well: VCC
Reset by: None
Default : 10h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = 10h (high byte).

CR 21h. Chip ID (Low Byte)

Location: Address 21h
Attribute: Read Only
Power Well: VCC
Reset by: None
Default : 61h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = 61h (low byte)

CR 22h. Device Power Down

Location: Address 22h
Attribute: Read/Write

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Power Well: VCC
Reset by: LRESET#
Default : 7Fh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	DSIRLGRQ => = 0 Enable IR legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable IR legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
6	R / W	IR Power Down. 0: Powered down. 1: Not powered down.
5	R / W	UARTB Power Down. 0: Powered down. 1: Not powered down.
4	R / W	UARTA Power Down. 0: Powered down. 1: Not powered down.
3	R / W	PRT Power Down. 0: Powered down. 1: Not powered down.
2	Reserved.	
1	R / W	IPD (Immediate Power Down). When set to 0, the whole chip is put into power-down mode immediately.
0	R / W	FDC Power Down. 0: Powered down. 1: Not powered down.

CR 24h. Multi Function Selection & Global Option

Location: Address 24h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	Pin5 function selection CR24 [Bit7] / Pin5 0 / CTSF# 1 / DRVDEN0 Pin6 function selection CR24 [Bit7] / Pin6 0 / AUXFANIN 1 / INDEX# Pin7 function selection CR24 [Bit7] / Pin7 0 / DSRF# 1 / MOA#

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<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>
Pin8 function selection
<table>
<tr><td>CR24 [Bit7]</td><td>Pin8</td></tr>
<tr><td>0</td><td>RTSF#</td></tr>
<tr><td>1</td><td>DSA#</td></tr>
</table>
Pin9 function selection
<table>
<tr><td>CR24 [Bit7]</td><td>Pin9</td></tr>
<tr><td>0</td><td>DTRF#</td></tr>
<tr><td>1</td><td>DIR#</td></tr>
</table>
Pin10 function selection
<table>
<tr><td>CR24 [Bit7]</td><td>Pin10</td></tr>
<tr><td>0</td><td>SINF</td></tr>
<tr><td>1</td><td>STEP#</td></tr>
</table>
Pin11 function selection
<table>
<tr><td>CR24 [Bit7]</td><td>Pin11</td></tr>
<tr><td>0</td><td>SOUTF</td></tr>
<tr><td>1</td><td>WD#</td></tr>
</table>
Pin13 function selection
<table>
<tr><td>CR24 [Bit7]</td><td>Pin13</td></tr>
<tr><td>0</td><td>DCDF#</td></tr>
<tr><td>1</td><td>WE#</td></tr>
</table>
Pin14 function selection
<table>
<tr><td>CR24 [Bit7]</td><td>Pin14</td></tr>
<tr><td>0</td><td>AUXFANOUT</td></tr>
<tr><td>1</td><td>TRAK0#</td></tr>
</table>
Pin15 function selection
<table>
<tr><td>CR24 [Bit7]</td><td>CR1A [Bit7]</td><td>Pin15</td></tr>
<tr><td>0</td><td>0</td><td>IRRX</td></tr>
<tr><td>0</td><td>1</td><td>CIRRX</td></tr>
<tr><td>1</td><td>x</td><td>WP#</td></tr>
</table>
</td></tr>
</table>

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Version: 1.0

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<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin16 function selection
<table>
<tr><th>CR24 [Bit7]</th><th>CR1A [Bit6]</th><th>Pin16</th></tr>
<tr><td>0</td><td>0</td><td>IRTX</td></tr>
<tr><td>0</td><td>1</td><td>CIRTX</td></tr>
<tr><td>1</td><td>x</td><td>RDATA#</td></tr>
</table>
Pin17 function selection
<table>
<tr><th>CR24 [Bit7]</th><th>Pin17</th></tr>
<tr><td>0</td><td>RIF#</td></tr>
<tr><td>1</td><td>HEAD#</td></tr>
</table>
Pin18 function selection
<table>
<tr><th>CR24 [Bit7]</th><th>Pin18</th></tr>
<tr><td>0</td><td>BEEP</td></tr>
<tr><td>1</td><td>DSKCHG#</td></tr>
</table>
Pin31-43 function selection
See CR 1Ah.</td></tr>
<tr><td>6</td><td>R / W</td><td>Select output type of SYSFANOUT
=0 SYSFANOUT is Open-drain. (Default)
=1 SYSFANOUT is Push-pull.</td></tr>
<tr><td>5</td><td>R / W</td><td>Select output type of CPUFANOUT
=0 CPUFANOUT is Open-drain. (Default)
=1 CPUFANOUT is Push-pull.</td></tr>
<tr><td>4</td><td>R / W</td><td>Select output type of AUXFANOUT
=1 AUXFANOUT is Open-drain.
=0 AUXFANOUT is Push-pull. (Default)</td></tr>
<tr><td>3</td><td>R / W</td><td>Pin14 AUXFANOUT Function Output Enable
=0 Disable
=1 Enable</td></tr>
<tr><td>2</td><td>R / W</td><td>Pin16 CIRTX Function Output Enable
=0 Disable
=1 Enable</td></tr>
<tr><td>1</td><td>R / W</td><td>Pin18 BEEP Function Output Enable
=0 Disable
=1 Enable</td></tr>
<tr><td>0</td><td>R / W</td><td>PNPCVS =>
= 0 The compatible PNP address-select registers have default values.
= 1 The compatible PNP address-select registers have no default values.</td></tr>
</table>

CR 25h. Interface Tri-state Enable

Location: Address 25h

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Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	UARTFTRI
6	R / W	UARTETRI
5	R / W	UARTDTRI
4	R / W	UARTCTRI
3	R / W	UARTBTRI
2	R / W	UARTATRI
1	R / W	PRTTRI
0	R / W	FDCTRI.

CR 26h. Global Option s: value by strapping
Location: Address 26h
Attribute: Read/Write
Power Web: VCC
Reset by: LRESET#
Default : 0s000000b
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA# (Pin51).
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4	Reserved.	
3	R / W	DSFDLGRQ => = 0 Enable FDC legacy mode for IRQ and DRQ selection. Then DO register (base address + 2) bit 3 is effective when selecting IRQ. = 1 Disable FDC legacy mode for IRQ and DRQ selection. Then DO register (base address + 2) bit 3 is not effective when selecting IRQ.
2	R / W	DSPRLGRQ => = 0 Enable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is effective when selecting IRQ. = 1 Disable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is not effective when selecting IRQ.

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BIT	READ / WRITE	DESCRIPTION
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
0	R / W	DSUBLGRQ => = 0 Enable UART B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable URAT B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 27h. Global Option

Location: Address 27h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R / W	Pin87 function selection CR27 [Bit3] / CR1B [Bit2] / Pin87 0 / 0 / GP71 0 / 1 / TSIC 1 / x / CIRRXWB
2	R / W	Pin108 function selection CR27 [Bit2] / CR1C [Bit4] / Pin108 0 / 0 / 14.7456MHZ_CLKIN 0 / 1 / GP67 1 / x / ATXPGD
1	R / W	Pin16 IRTX Function Output Enable =0 Disable =1 Enable
0	R / W	Pin31 PLED Function Output Enable =0 Disable =1 Enable

CR 28h. Global Option

Location: Address 28h
Attribute: Read/Write
Power Well: VCC

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Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5-4	R / W	0 0: LPC or I2C to 80PORT switch 0 1: CPU temperature to 80PORT switch 1 0: SYS temperature to 80PORT switch 1 1: AUX temperature to 80PORT switch
3	Reserved.	
2-0	R / W	PRTMODS2 ~ 0 => **Bits** **2 1 0** = 0 x x Parallel Port Mode. = 1 x x Reserved.

CR 29h. Global Option
Location: Address 29h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : F0h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	UARTF Power Down. 0: Powered down. 1: Not powered down.
6	R / W	UARTE Power Down. 0: Powered down. 1: Not powered down.
5	R / W	UARTD Power Down. 0: Powered down. 1: Not powered down.
4	R / W	UARTC Power Down. 0: Powered down. 1: Not powered down.
3	R / W	DSUFLGRQ => = 0 Enable UART F legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART F legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
2	R / W	DSUELGRQ => = 0 Enable UART E legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART E legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
1	R / W	DSUDLGRQ => = 0 Enable UART D legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART D legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

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BIT	READ / WRITE	DESCRIPTION
0	R / W	DSUCLGRQ => = 0 Enable UART C legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART C legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 2Ah. Global Option

Location: Address 2Ah
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved.	
2	R/W	OVT# Power Down Selection =0 Disable =1 Enable
1-0	Reserved.	

CR 2Fh. Strapping Function Result

Location: Address 2Fh
Attribute: Read/Write
Power Well: VSB
Reset by: PWROK#, RSMRST# (Bit2)
Default : by 000s_ssss
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	SOUTE_P80_SEL Strapping result reading, it can output the port80 data to UARTE interface.
3	R / W	SOUTC_P80_SEL Strapping result reading, it can output the port80 data to UARTE interface.
2	R / W	COMB_DSW_SEL Strapping result reading, it can switch UARTB pad-mux to DSW function.
1	R / W	GPIO_PORT80_SEL Strapping result reading
0	R / W	24M_48M_SEL Strapping result reading

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

3) VSB Strapping result can be programming by LPC, and reset by RSMRST#
4) VCC Strapping result can be programming by LPC, and reset by PWROK
5) LRESET Strapping (2E_4E_SEL) : No change

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23.2 Logical Device 0 (FDC)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The FDC device is inactive. 1: The FDC device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, F0h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select FDC I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 06h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for FDC.

CR 74h.

Location: Address 74h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7-3	Reserved.	
2-0	R / W	These bits select DRQ resource for FDC. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 0Eh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	This bit determines the polarity of all FDD interface signals. 0: FDD interface signals are active low. 1: FDD interface signals are active high.
5	R / W	When this bit is logic 0, indicates a second drive is installed and is reflected in status register A. (PS2 mode only)
4	R / W	Swap Drive 0, 1 Mode => 0: No Swap. 1: Drive and Motor select 0 and 1 are swapped.
3-2	R / W	Interface Mode. 00: Model 30. 01: PS/2. 10: Reserved. 11: AT Mode
1	R / W	FDC DMA Mode. 0 : Burst Mode is enabled 1 : Non-Burst Mode.
0	R / W	Floppy Mode. 0 : Normal Floppy Mode. 1: Enhanced 3-mode FDD.

CR F1h.

Location: Address F1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Boot Floppy. 00: FDD A. 01: Reserved. 10: Reserved. 11: Reserved.
5-4	R / W	Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.

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BIT	READ / WRITE	DESCRIPTION
3-2	R / W	Density Select. 00: Normal. 01 Normal. 10: 1 (Forced to logic 1). 11: 0 (Forced to logic 0).
1	R / W	DISFDDWR => 0: Enable FDD write. 1: Disable FDD write (forces pins WE, WD to stay high).
0	R / W	SWWP => 0: Normal, use WP to determine whether the FDD is write protected or not. 1: FDD is always write-protected.

CR F2h.
Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1-0	R / W	FDD A Drive Type.

CR F4h.
Location: Address F4h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	0: Enable FDC Pre-compensation. 1: Disable FDC Pre-compensation.
5	Reserved.	
4-3	R / W	Data Rate Table selection (Refer to TABLE A). 00: Select regular drives and 2.88 format. 01: 3-mode drive. 10: 2 Meg Tape. 11: Reserved.
2	Reserved.	
1-0	R / W	Drive Type selection (Refer to TABLE B).

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CR F5h.

Location: Address F5h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Same as FDD0 of CR F5h.

TABLE A

DRIVE RATE TABLE SELECT		DATA RATE		SELECTED DATA RATE		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

TABLE B

DTYPE0	DTYPE1	DRVDEN0 (pin 5)	DRIVE TYPE
0	0	SELDEN	4/2/1 MB 3.5"“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	
1	0	$\overline{\text{SELDEN}}$	
1	1	DRATE0	

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23.3 Logical Device 1 (PRT)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, 78h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select PRT I/O base address. <100h: FFCh> on 4 bytes boundary (EPP not supported) or <100h: FF8h> on 8 bytes boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 07h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for PRT.

CR 74h.

Location: Address 74h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7-3	Reserved.	
2-0	R / W	These bits select DRQ resource for PRT. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 3Fh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6-3	R / W	ECP FIFO Threshold.
2-0	R / W	Parallel Port Mode selection (CR28 bit2 PRTMODS2 = 0). **Bits** **2 1 0** 0 0 0: Standard and Bi-direction (SPP) mode. 0 0 1: EPP – 1.9 and SPP mode. 0 1 0: ECP mode. 0 1 1: ECP and EPP – 1.9 mode. 1 0 0: Printer Mode. 1 0 1: EPP – 1.7 and SPP mode. 1 1 0: Reserved. 1 1 1: ECP and EPP – 1.7 mode.

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23.4 Logical Device 2 (UARTA)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, F8h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 1 I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 1.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART A clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART A clock source is 2 MHz (24 MHz / 12). 1 0: UART A clock source is 24 MHz (24 MHz / 1). 1 1: UART A clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTA 9bit-mode Config Register

Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bitmode RX block function will pass all data or address byte and not compare any address byte. 1: 9bitmode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bitmode RX block function.
5	R / W	**RST_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX blockwill keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data. 1: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data.

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BIT	READ / WRITE	DESCRIPTION
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ingored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bitmode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTA 9bit-mode Slave Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTA 9bit-mode Slave Mask Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTA 9bit-mode Broadcase Address Register

Location: Address F5h
Attribute: Read/Write

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Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcase Address**

CR F6h. UARTA 9bit-mode Interrupt Control Register
Location: Address F6h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTA 9bit-mode IRQ output. 1: Enalbe UARTA 9bit-mode IRQ output.

CR F7h. UARTA 9bit-mode IRQ Status Register
Location: Address F7h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	**UARTA 9bit-mode Status Bit** 0: UARTA 9bit-mode IRQ have not been triggered. 1: UARTA 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTA Control Register
Location: Address F8h
Attribute: Read/Write
Power Well: VCC

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Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved	uartAB_switch _enable	Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	fifo_level_mode: (Also check UFR register B7-6 definition)

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

5	Reserved.
4	uartAB_switch_enable (Bypass mode) 0: switch disable 1: switch enable
3-1	Reserved. (All should be set to 0)
0	Extending fifo enable bit: 0: Disable128bytes TX and RX FIFO. 1: Enable128bytes TX and RX FIFO.

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23.5 Logical Device 3 (UARTB)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h, F8h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 2.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART B clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART B clock source is 2 MHz (24 MHz / 12). 0 0: UART B clock source is 24 MHz (24 MHz / 1). 0 0: UART B clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTB 9bit-mode Config Register

Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bitmode RX block function will pass all data or address byte and not compare any address byte. 1: 9bitmode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bitmode RX block function.
5	R / W	**RST_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX blockwill keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data. 1: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data.

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BIT	READ / WRITE	DESCRIPTION
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ingored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bitmode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTB 9bit-mode Slave Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTB 9bit-mode Slave Mask Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTB 9bit-mode Broadcase Address Register

Location: Address F5h
Attribute: Read/Write

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Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcase Address**

CR F6h. UARTB 9bit-mode Interrupt Control Register
Location: Address F6h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTB 9bit-mode IRQ output. 1: Enalbe UARTB 9bit-mode IRQ output.

CR F7h. UARTB 9bit-mode IRQ Status Register
Location: Address F7h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	**UARTB 9bit-mode Status Bit** 0: UARTB 9bit-mode IRQ have not been triggered. 1: UARTB 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTB Control Register
Location: Address F8h
Attribute: Read/Write
Power Well: VCC

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Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved		Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	fifo_level_mode: (Also check UFR register B7-6 definition)
5-4	Reserved.
3-1	Reserved. (All should be set to 0)
0	Extending fifo enable bit: 0: Disable128bytes TX and RX FIFO. 1: Enable128bytes TX and RX FIFO.

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

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23.6 Logical Device 5 (KBC)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the first KBC I/O base address <100h: FFFh> on 1-byte boundary.

CR 62h, 63h.

Location: Address 62h, 63h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the second KBC I/O base address <100h: FFFh> on 1 byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h.
Location: Address 72h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h.
Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 83h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	KBC clock rate selection **Bits** **7 6** 0 0: Reserved 0 1: Reserved 1 0: 12MHz 1 1: Reserved
5-3	Reserved.	
2	R / W	0: Port 92 disabled. 1: Port 92 enabled.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST# software control. 1: KBRST# hardware speed up.

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23.7 Logical Device 6 (CIR)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: CIR Interface is inactive. 1: CIR Interface is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for CIR.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 08h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R/W	CIR wide band filter select 0: Low-pass filter 1: Band-pass filter
2-1	R/W	Timeout margin selection of CIR wide band band-pass filter 00: 200% recording carrier period 01: 100% recording carrier period 10: 50% recording carrier period 11: 25% recording carrier period
0	R/W	Carrier recording mode CIR wide band band-pass filter 0: Second carrier 1: Every carrier

CR F1h.
Location: Address F1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 09h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5-0	R / W	Highest input period of CIR wide band band-pass filter (unit : us)

CR F2h.
Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 32h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5-0	R / W	Lowest input period of CIR wide band band-pass filter (unit : us)

CR F3h.
Location: Address F3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

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Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5-0	R / W	Recording carrier period of CIR wide band band-pass filter (unit : us)

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23.8 Logical Device 7 (GPIO)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#, LRESET# (Bit2)
Default : DFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO7 is inactive. 1: GPIO7 is active.
6	R / W	0: GPIO6 is inactive. 1: GPIO6 is active.
5	R / W	0: GPIO5 is inactive. 1: GPIO5 is active.
4	R / W	0: GPIO4 is inactive. 1: GPIO4 is active.
3	R / W	0: GPIO3 is inactive. 1: GPIO3 is active.
2	R / W	0: GPIO2 is inactive. 1: GPIO2 is active.
1	R / W	0: GPIO1 is inactive. 1: GPIO1 is active.
0	R / W	0: GPIO0 is inactive. 1: GPIO0 is active.

CR E0h. GPIO0 I/O Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 I/O register 0: The respective GPIO0 PIN is programmed as an output port 1: The respective GPIO0 PIN is programmed as an input port.

CR E1h. GPIO0 Data Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Data register For output ports, the respective bits can be read/written and produced to pins.

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BIT	READ / WRITE	DESCRIPTION
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. GPIO0 Inversion Register

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. GPIO0 Status Register

Location: Address E3h
Attribute: Read Only
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO0 Event Status Bit 7-0 corresponds to GP07-GP00, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E4h. GPIO1 I/O Register

Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 I/O register 0: The respective GPIO1 PIN is programmed as an output port 1: The respective GPIO1 PIN is programmed as an input port.

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CR E5h. GPIO1 Data Register

Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E6h. GPIO1 Inversion Register

Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E7h. GPIO1 Status Register

Location: Address E7h
Attribute: Read Only
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO1 Event Status Bit 7-0 corresponds to GP17-GP10, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E8h. GPIO2 I/O Register

Location: Address E8h
Attribute: Read/Write

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Power Well: VCC
Reset by: GP2X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 I/O register 0: The respective GPIO2 PIN is programmed as an output port 1: The respective GPIO2 PIN is programmed as an input port.

CR E9h. GPIO2 Data Register

Location: Address E9h
Attribute: Read/Write
Power Well: VCC
Reset by: GP2X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR EAh. GPIO2 Inversion Register

Location: Address EAh
Attribute: Read/Write
Power Well: VCC
Reset by: GP2X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR EBh. GPIO2 Status Register

Location: Address EBh
Attribute: Read Only
Power Well: VCC
Reset by: GP2X_MRST
Default : 00h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO2 Event Status Bit 7-0 corresponds to GP27-GP20, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR ECh. GPIO3 I/O Register

Location: Address ECh
Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO3 I/O register 0: The respective GPIO3 PIN is programmed as an output port 1: The respective GPIO3 PIN is programmed as an input port.

CR EDh. GPIO3 Data Register

Location: Address EDh
Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO3 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR EEh. GPIO3 Inversion Register

Location: Address EEh
Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

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BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO3 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR EFh. GPIO3 Status Register

Location: Address EFh
Attribute: Read Only
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO3 Event Status Bit 7-0 corresponds to GP37-GP30, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR F0h. GPIO4 I/O Register

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 I/O register 0: The respective GPIO4 PIN is programmed as an output port 1: The respective GPIO4 PIN is programmed as an input port.

CR F1h. GPIO4 Data Register

Location: Address F1h
Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 Data register For output ports, the respective bits can be read/written and produced to pins.

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BIT	READ / WRITE	DESCRIPTION
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F2h. GPIO4 Inversion Register

Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F3h. GPIO4 Status Register

Location: Address F3h
Attribute: Read Only
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO4 Event Status Bit 7-0 corresponds to GP47-GP40, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR F4h. GPIO5 I/O Register

Location: Address F4h
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 I/O register 0: The respective GPIO5 PIN is programmed as an output port 1: The respective GPIO5 PIN is programmed as an input port.

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CR F5h. GPIO5 Data Register

Location: Address F5h
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F6h. GPIO5 Inversion Register

Location: Address F6h
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F7h. GPIO5 Status Register

Location: Address F7h
Attribute: Read Only
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO5 Event Status Bit 7-0 corresponds to GP57-GP50, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR F8h. GPIO6 I/O Register

Location: Address F8h
Attribute: Read/Write

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Power Well: VSB
Reset by: GP6X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 I/O register 0: The respective GPIO6 PIN is programmed as an output port 1: The respective GPIO6 PIN is programmed as an input port.

CR F9h. GPIO6 Data Register

Location: Address F9h
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR FAh. GPIO6 Inversion Register

Location: Address FAh
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR FBh. GPIO6 Status Register

Location: Address FBh
Attribute: Read Only
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO6 Event Status Bit 7-0 corresponds to GP67-GP60, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR FCh. GPIO7 I/O Register

Location: Address FCh
Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	GPIO7 I/O register 0: The respective GPIO7 PIN is programmed as an output port 1: The respective GPIO7 PIN is programmed as an input port.
0	Reserved.	

CR FDh. GPIO7 Data Register

Location: Address FDh
Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	GPIO7 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.
0	Reserved.	

CR FEh. GPIO7 Inversion Register

Location: Address FEh
Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST

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Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
1	R / W	GPIO7 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)
0	Reserved.	

CR FFh. GPIO7 Status Register
Location: Address FFh
Attribute: Read Only
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	Read Only Read-Clear	GPIO7 Event Status Bit 1 corresponds to GP71. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.
0	Reserved.	

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23.9 Logical Device 8 (GPIO, WDT1)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	0: GPIO Base Address mode is inactive 1: GPIO Base Address mode is active
0	R / W	0: WDT1 is inactive. 1: WDT1 is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select GPIO Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR E0h. GPIO0 Multi-function Select Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO07 1: GPIO07 → YLW
6	R / W	0: GPIO06 1: GPIO06 → GRN
5	R / W	0: GPIO05 1: GPIO05 → WDTO#
4	R / W	0: GPIO04 1: GPIO04 → SUSLED

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BIT	READ / WRITE	DESCRIPTION
3	R / W	0: GPIO03 1: GPIO03 → YLW
2	R / W	0: GPIO02 1: GPIO02 → GRN
1	R / W	0: GPIO01 1: GPIO01 → WDTO#
0	R / W	0: GPIO00 1: GPIO00 → SUSLED

CR E1h. GPIO1 Multi-function Select Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO17 1: GPIO17 → YLW
6	R / W	0: GPIO16 1: GPIO16 → GRN
5	R / W	0: GPIO15 1: GPIO15 → BEEP
4	R / W	0: GPIO14 1: GPIO14 → SMI
3	R / W	0: GPIO13 1: GPIO13 → YLW
2	R / W	0: GPIO12 1: GPIO12 → GRN
1	R / W	0: GPIO11 1: GPIO11 → BEEP
0	R / W	0: GPIO10 1: GPIO10 → SMI

CR E2h. GPIO2 Multi-function Select Register

Location: Address E2h
Attribute: Read/Write
Power Well: VCC
Reset by: GP2X_MRST
Default : 00h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO27 1: GPIO27 → WDTO#
6	R / W	0: GPIO26 1: GPIO26 → BEEP
5	R / W	0: GPIO25 1: GPIO25 → SMI
4	R / W	0: GPIO24 1: GPIO24 → PLED
3	R / W	0: GPIO23 1: GPIO23 → WDTO#
2	R / W	0: GPIO22 1: GPIO22 → BEEP
1	R / W	0: GPIO21 1: GPIO21 → SMI
0	R / W	0: GPIO20 1: GPIO20 → PLED

CR E3h. GPIO3 Multi-function Select Register

Location: Address E3h
Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO37 1: GPIO37 → BEEP
6	R / W	0: GPIO36 1: GPIO36 → SMI
5	R / W	0: GPIO35 1: GPIO35 → WDTO#
4	R / W	0: GPIO34 1: GPIO34 → SUSLED
3	R / W	0: GPIO33 1: GPIO33 → BEEP
2	R / W	0: GPIO32 1: GPIO32 → SMI
1	R / W	0: GPIO31 1: GPIO31 → WDTO#

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BIT	READ / WRITE	DESCRIPTION
0	R / W	0: GPIO30 1: GPIO30 → SUSLED

CR E4h. GPIO4 Multi-function Select Register

Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO47 1: GPIO47 → YLW
6	R / W	0: GPIO46 1: GPIO46 → GRN
5	R / W	0: GPIO45 1: GPIO45 → PLED
4	R / W	0: GPIO44 1: GPIO44 → SMI
3	R / W	0: GPIO43 1: GPIO43 → YLW
2	R / W	0: GPIO42 1: GPIO42 → GRN
1	R / W	0: GPIO41 1: GPIO41 → PLED
0	R / W	0: GPIO40 1: GPIO40 → SMI

CR E5h. GPIO5 Multi-function Select Register

Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO57 1: GPIO57 → YLW
6	R / W	0: GPIO56 1: GPIO56 → GRN

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BIT	READ / WRITE	DESCRIPTION
5	R / W	0: GPIO55 1: GPIO55 → BEEP
4	R / W	0: GPIO54 1: GPIO54 → WDTO#
3	R / W	0: GPIO53 1: GPIO53 → YLW
2	R / W	0: GPIO52 1: GPIO52 → GRN
1	R / W	0: GPIO51 1: GPIO51 → BEEP
0	R / W	0: GPIO50 1: GPIO50 → WDTO#

CR E6h. GPIO6 Multi-function Select Register

Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	0: GPIO66 1: GPIO66 → YLW
5	R / W	0: GPIO65 1: GPIO65 → GRN
4	R / W	0: GPIO64 1: GPIO64 → BEEP
3	R / W	0: GPIO63 1: GPIO63 → SMI
2	R / W	0: GPIO62 1: GPIO62 → WDTO#
1	R / W	0: GPIO61 1: GPIO61 → SUSLED
0	R / W	0: GPIO60 1: GPIO60 → PLED

CR E7h. GPIO6 & GPIO7 Multi-function Select Register

Location: Address E7h
Attribute: Read/Write

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Power Well: VSB
Reset by: GP6X_MRST (Bit7-5), GP7X_MRST(Bit3-1)
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	R / W	000: GPIO67 001: GPIO67 → YLW 010: GPIO67 → GRN 011: GPIO67 → BEEP 100: GPIO67 → SMI 101: GPIO67 → WDTO# 110: GPIO67 → SUSLED 111: GPIO67 → PLED
4-1	Reserved.	
0	R / W	0: GPIO71 1: GPIO71 → WDTO#

CR F0h. Watchdog Timer I(WDT1) and KBC P20 Control Mode Register
Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET# or PWROK
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	Watchdog Timer I count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is 0, the count mode is 1/1000 seconds mode.) (If bit-3 is 1, the count mode is 1/1000 minutes mode.)
3	R / W	Select Watchdog Timer I count mode. 0: Second Mode. 1: Minute Mode.
2	R / W	Enable the rising edge of a KBC reset (P20) to issue a time-out event. 0: Disable. 1: Enable.
1	R / W	Disable / Enable the Watchdog Timer I output low pulse to the KBRST# pin (PIN59) 0: Disable. 1: Enable.
0	Reversed	

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CR F1h. Watchdog Timer I(WDT1) Counter Register

Location: Address F1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET# or PWROK
Default : 04h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Watch Dog Timer I Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watch Dog Counter and start counting down. If CR F2h, bits 7 and 6 are set, any Mouse Interrupt or Keyboard Interrupt event causes the previously-loaded, non-zero value to be reloaded to the Watch Dog Counter and the count down resumes. Reading this register returns the current value in the Watch Dog Counter, not the Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after $5.03x10^7$ CLKIN cycle time, by analogy. ($5.03x10^7$x (1/48MHz) = 1.046s)

CR F2h. Watchdog Timer I(WDT1) Control & Status Register

Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET# or PWROK
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mouse interrupt reset enables watch-dog timer reload 0: Watchdog Timer I is not affected by mouse interrupt. 1: Watchdog Timer I is reset by mouse interrupt.
6	R / W	Keyboard interrupt reset enables watch-dog timer reload 0: Watchdog Timer I is not affected by keyboard interrupt. 1: Watchdog Timer I is reset by keyboard interrupt.
5	Write "1" Only	Trigger Watchdog Timer I event. This bit is self-clearing.
4	R / W Write "0" Clear	Watchdog Timer I status bit 0: Watchdog Timer I is running. 1: Watchdog Timer I issues time-out event.
3-0	R / W	These bits select the IRQ resource for the Watchdog Timer I

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23.10 Logical Device 9 (GPIO)

CR E0h. Input Detected Type Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB **CR 20h**
Reset by: GP4X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Enable GP47 input de-bouncer 1: Disable GP47 input de-bouncer
6	R / W	0: Enable GP46 input de-bouncer 1: Disable GP46 input de-bouncer
5	R / W	0: Enable GP45 input de-bouncer 1: Disable GP45 input de-bouncer
4	R / W	0: Enable GP44 input de-bouncer 1: Disable GP44 input de-bouncer
3	R / W	0: GP47 trigger type: edge 1: GP47 trigger type: level
2	R / W	0: GP46 trigger type: edge 1: GP46 trigger type: level
1	R / W	0: GP45 trigger type: edge 1: GP45 trigger type: level
0	R / W	0: GP44 trigger type: edge 1: GP44 trigger type: level

CR E1h. GPIO44, 45, 46 & 47 Event Route Selection Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable GP47 event route to PSOUT#. 1: Enable GP47 event route to PSOUT#.
6	R / W	0: Disable GP46 event route to PSOUT#. 1: Enable GP46 event route to PSOUT#.
5	R / W	0: Disable GP45 event route to PSOUT#. 1: Enable GP45 event route to PSOUT#.

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BIT	READ / WRITE	DESCRIPTION
4	R / W	0: Disable GP44 event route to PSOUT#. 1: Enable GP44 event route to PSOUT#.
3	R / W	0: Disable GP47 event route to PME#. 1: Enable GP47 event route to PME#.
2	R / W	0: Disable GP46 event route to PME#. 1: Enable GP46 event route to PME#.
1	R / W	0: Disable GP45 event route to PME#. 1: Enable GP45 event route to PME#.
0	R / W	0: Disable GP44 event route to PME#. 1: Enable GP44 event route to PME#.

CR E2h. GPIOs Reset Source Register

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	GP7X_MRST 0: GP7X reset by RSMRST#. 1: GP7X reset by SLPS5.
6	R / W	GP6X_MRST 0: GP6X reset by RSMRST#. 1: GP6X reset by SLPS5.
5	R / W	GP5X_MRST 0: GP5X reset by RSMRST#. 1: GP5X reset by SLPS5.
4	R / W	GP4X_MRST 0: GP4X reset by RSMRST#. 1: GP4X reset by SLPS5.
3	R / W	GP3X_MRST 0: GP3X reset by RSMRST#. 1: GP3X reset by SLPS5.
2	R / W	GP2X_MRST 0: GP2X reset by LRESET#. 1: GP2X reset by PWROK.
1	R / W	GP1X_MRST 0: GP1X reset by RSMRST#. 1: GP1X reset by SLPS5.
0	R / W	GP0X_MRST 0: GP0X reset by RSMRST#. 1: GP0X reset by SLPS5.

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23.11 Logical Device A (ACPI)

CR E0h.

Location: Address E0h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 01h
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>DIS_PSIN => Disable the panel switch input to turn on the system power supply.
0: PSIN is wire-AND and connected to PSOUT#.
1: PSIN is blocked and cannot affect PSOUT#.</td></tr>
<tr><td>6</td><td>R / W</td><td>Enable KBC wake-up
0: Disable keyboard wake-up function via PSOUT#.
1: Enable keyboard wake-up function via PSOUT#.</td></tr>
<tr><td>5</td><td>R / W</td><td>Enable Mouse wake-up
0: Disable mouse wake-up function via PSOUT#.
1: Enable mouse wake-up function via PSOUT#.</td></tr>
<tr><td>4</td><td>R / W</td><td>MSRKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the following table for the details.
<table>
<tr><th>ENMDAT_UP</th><th>MSRKEY</th><th>MSXKEY</th><th>Wake-up event</th></tr>
<tr><td>1</td><td>x</td><td>1</td><td>Any button clicked or any movement.</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>One click of left or right button.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One click of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>One click of the right button.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Two clicks of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two clicks of the right button.</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Enable CIR wake-up
0: Disable CIR wake-up function via PSOUT#.
1: Enable CIR wake-up function via PSOUT#.</td></tr>
<tr><td>2</td><td>R / W</td><td>Keyboard / Mouse swap enable
0: Normal mode.
1: Keyboard / Mouse ports are swapped.</td></tr>
<tr><td>1</td><td>R / W</td><td>MSXKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.</td></tr>
</table>

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BIT	READ / WRITE	DESCRIPTION
0	R / W	KBXKEY => 0: Only the pre-determined key combination in sequence can wake up the system. 1: Any character received from the keyboard can wake up the system.

CR E1h. KBC Wake-Up Index Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up index register. This is the index register of CRE2, which is the access window for the keyboard's pre-determined key key-combination characters. The first set of wake-up keys is in of 0x00 – 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combinations can be read through 0x10 – 0x1E.

CR E2h. KBC Wake-Up Data Register

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up data register. This is the data register for the keyboard's pre-determined key-combination characters, which is indexed by CRE1.

CR E3h. Event Status Register

Location: Address E3h
Attribute: Read Only
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	Read Only Read-Clear	This status flag indicates VSB power off/on.

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BIT	READ / WRITE	DESCRIPTION
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event issued. 1: Thermal shutdown event issued.
2	Read Only Read-Clear	PSIN_STS 0: No PSIN event issued. 1: PSIN event issued.
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event issued. 1: Mouse wake-up event issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event issued. 1: Keyboard wake-up event issued.

CR E4h.

Location: Address E4h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-5	R / W	Power-loss control bits => (VBAT) **Bits** **6 5** 0 0: System always turns off when it returns from power-loss state. 0 1: System always turns on when it returns from power-loss state. 1 0: System turns off / on when it returns from power-loss state depending on the state before the power loss. 1 1: User defines the resuming state before power loss.(refer to Logic Device A, CRE6[4])
4	R / W	VSBGATE# Enable bit => (Reset by 3VCC) 0: Disable. 1: Enable.
3	R / W	Keyboard wake-up options. 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2	R / W	Enable the hunting mode for all wake-up events set in CRE0. This bit is cleared when any wake-up events is captured. (this bit is reset by LRESET#) (Note. This bit is to generate PSOUT# via KB or MS under S1.) 0: Disable. 1: Enable.
1-0	Reserved.	

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CR E5h. PWROK Option Register

Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	PWROK source selection. 0: PSON#. 1: SLP_S3#.
0	R / W	ATXPGD signal to control PWROK 0: Enable. 1: Disable.

CR E6h.

Location: Address E6h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 1Ch
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the table in CRE0, bit 4 for the details.
6	Reserved.	
5	R / W	CASEOPEN Clear Control. Write 1 to this bit to clear CASEOPEN status. This bit will clear the status itself.
4	R / W	Power-loss Last State Flag. 0: ON 1: OFF.
3-1	R / W	PWROK_DEL Set the delay time when rising from 3VCC to PWROK **Bits** **3 2 1** 0 0 0: 300 ~ 600mS 0 0 1: 330 ~ 670mS 0 1 0: 390 ~ 730mS 0 1 1: 520 ~ 860mS 1 0 0: 200 ~ 300mS 1 0 1: 230 ~ 370mS 1 1 0: 290 ~ 430mS 1 1 1: 420 ~ 560mS
0	R / W-Clear	PWROK_TRIG => Write 1 to re-trigger the PWROK signal from low to high.

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CR E7h.

Location: Address E7h

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#, Battery reset (Bit0, 1, 4)

Default : 00h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENKD3 => Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.
6	R / W	ENKD2 => Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.
5	R / W	ENWIN98KEY => Enable Win98 keyboard dedicated key to wake-up system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.
4	R / W	EN_ONPSOUT Disable/Enable to issue a 0.5s delay PSOUT# level when system returns from power loss state and is supposed to be on as described in CRE4[6:5], logic device A. (for SiS & VIA chipsets) 0: Disable. 1: Enable.
3	R / W	Select WDT1 reset source 0: Watchdog timer is reset by LRESET#. 1: Watchdog timer is reset by PWROK.
2	Reserved.	
1	R / W	DIS_RSM2PWR 0: Enable RSMRST# to control PWROK 1: Disable RSMRST# to control PWROK
0	R / W	Hardware Monitor RESET source select 0: PWROK. 1: LRESET#.

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CR F0h.
Location: Address F0h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 80h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Pin64 function selection LDA, CRF0 [Bit7-6] / Pin64 1x / DEEP_S5_2 00 / 3VSBSW 01 / LATCH_BKFD_CUT
5-0	Reserved.	

CR F1h.
Location: Address F1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W-Clear	PME status of the RIA event. Write 1 to clear this status.
6	R / W-Clear	PME status of the RIB event. Write 1 to clear this status.
5	R / W-Clear	PME status of the RIC event. Write 1 to clear this status.
4	R / W-Clear	PME status of the RID event. Write 1 to clear this status.
3	R / W-Clear	PME status of the RIE event. Write 1 to clear this status.
2	R / W-Clear	PME status of the RIF event. Write 1 to clear this status.
1-0	Reserved.	

CR F2h.
Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#

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Default : 40h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	Block SLP_S3# to PSON# 0: Disable 1: Enable
4-1	Reserved.	
0	R / W	EN_PME => 0 : Disable PME. 1 : Enable PME.

CR F3h.
Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W-Clear	PME status of the Mouse IRQ event. Write 1 to clear this status.
4	R / W-Clear	PME status of the KBC IRQ event. Write 1 to clear this status.
3	R / W-Clear	PME status of the PRT IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the FDC IRQ event. Write 1 to clear this status.
1	R / W-Clear	PME status of the URA IRQ event. Write 1 to clear this status.
0	R / W-Clear	PME status of the URB IRQ event. Write 1 to clear this status.

CR F4h.
Location: Address F4h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W-Clear	PME status of the URC IRQ event. Write 1 to clear this status.

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BIT	READ / WRITE	DESCRIPTION
6	R / W-Clear	PME status of the URD IRQ event. Write 1 to clear this status.
5	R / W-Clear	PME status of the URE IRQ event. Write 1 to clear this status.
4	R / W-Clear	PME status of the URF IRQ event. Write 1 to clear this status.
3	R / W-Clear	PME status of the HM IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the WDT1 event. Write 1 to clear this status.
1-0	Reserved.	

CR F5h.
Location: Address F5h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable PME interrupt of the URC IRQ event. 1: Enable PME interrupt of the URC IRQ event.
6	R / W	0: Disable PME interrupt of the URD IRQ event. 1: Enable PME interrupt of the URD IRQ event.
5	R / W	0: Disable PME interrupt of the URE IRQ event. 1: Enable PME interrupt of the URE IRQ event.
4	R / W	0: Disable PME interrupt of the URF IRQ event. 1: Enable PME interrupt of the URF IRQ event.
3-0	Reserved.	

CR F6h.
Location: Address F6h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable KB, MS interrupt of the KBC password event. 1: Enable KB, MS interrupt of the KBC password event.

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BIT	READ / WRITE	DESCRIPTION
6	R / W	0: Disable PME interrupt of the RIA event. 1: Enable PME interrupt of the RIA event.
5	R / W	0: Disable PME interrupt of the Mouse IRQ event. 1: Enable PME interrupt of the Mouse IRQ event.
4	R / W	0: Disable PME interrupt of the KBC IRQ event. 1: Enable PME interrupt of the KBC IRQ event.
3	R / W	0: Disable PME interrupt of the PRT IRQ event. 1: Enable PME interrupt of the PRT IRQ event.
2	R / W	0: Disable PME interrupt of the FDC IRQ event. 1: Enable PME interrupt of the FDC IRQ event.
1	R / W	0: Disable PME interrupt of the URA IRQ event. 1: Enable PME interrupt of the URA IRQ event.
0	R / W	0: Disable PME interrupt of the URB IRQ event. 1: Enable PME interrupt of the URB IRQ event.

CR F7h.

Location: Address F7h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable PME interrupt of the RIC event. 1: Enable PME interrupt of the RIC event.
6	R / W	0: Disable PME interrupt of the RID event. 1: Enable PME interrupt of the RID event.
5	R / W	0: Disable PME interrupt of the RIE event. 1: Enable PME interrupt of the RIE event.
4	R / W	0: Disable PME interrupt of the CIRWAKEUP IRQ event. 1: Enable PME interrupt of the CIRWAKEUP IRQ event.
3	R / W	0: Disable PME interrupt of the HM IRQ event. 1: Enable PME interrupt of the HM IRQ event.
2	R / W	0: Disable PME interrupt of the WDT1 event. 1: Enable PME interrupt of the WDT1 event.
1	R / W	0: Disable PME interrupt of the RIF event. 1: Enable PME interrupt of the RIF event.
0	R / W	0: Disable PME interrupt of the RIB event. 1: Enable PME interrupt of the RIB event.

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CR F8h.

Location: Address F8h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	
3-0	R / W	

CR FAh.

Location: Address FAh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R/W	ATXPGD de-bounce for BKFD function. 0: enable 1: disable (de-bounce time depend on LDA_FA[1-0])
6-2	Reserved	
1-0	R/W	ATXPGD de-bounce time select 00: 20us ~ 26us 01: 70us ~ 100us 10: 140us ~ 200us 11: 360us ~ 560us

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23.12 Logical Device B (HM, LED)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: Hardware Monitor & SB-TSI device is inactive. 1: Hardware Monitor & SB-TSI device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the HM base address <100h : FFEh> along a two-byte boundary.

CR 62h, 63h.

Location: Address 62h, 63h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the SB-TSI base address <100h : FFEh> along a two-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select the IRQ resource for HM.

CR E0h. SYSFAN Duty Cycle Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 7Fh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	SYSFAN Duty Cycle Register

CR E1h. CPUFAN Duty Cycle Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 7Fh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	CPUFAN Duty Cycle Register

CR E2h. AUXFAN Duty Cycle Register

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN Duty Cycle Register

CR F0h. FANIN de-bouncer Register

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

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BIT	READ / WRITE	DESCRIPTION
7	R / W	1: Enable AUXFANIN input de-bouncer. 0: Disable AUXFANIN input de-bouncer.
6	R / W	1: Enable CPUFANIN input de-bouncer. 0: Disable CPUFANIN input de-bouncer.
5	R / W	1: Enable SYSFANIN input de-bouncer. 0: Disable SYSFANIN input de-bouncer.
4-0	Reserved.	

CR F1h. SMI IRQ Register

Location: Address F1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	SMI IRQ Enable
6-0	Reserved.	

CR F2h. SMBus de-bouncer Register

Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	0: Enable SCL input de-bouncer 80 ~ 120ns. 1: Disable SCL input de-bouncer.
0	R / W	0: Enable SDA input de-bouncer 80 ~ 120ns. 1: Disable SDA input de-bouncer.

CR F3h. DEEPER_SLEEPING_STATE Front panel green & yellow LED control register

Location: Address F3h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7-4	R / W	DEEPS3_YLW_BLK_FREQ bits (powered by VSB, RSMRST# reset, default 000b), when LDB CRF9 Bit 7 is set to 0 1xxx : Fading LED. 0111 : YLW_LED will drive low. 0110 : YLW_LED will output 2Hz , 50% duty-cycle signal. 0101 : YLW_LED will output 1Hz , 50% duty-cycle signal. 0100 : YLW_LED will output 0.5Hz , 50% duty-cycle signal. 0011 : YLW_LED will output 0.25Hz , 50% duty-cycle signal. 0010 : YLW_LED will output 0.125Hz , 50% duty-cycle signal. 0001 : YLW_LED will output 0.0625Hz , 50% duty-cycle signal. 0000 : YLW_LED will output High-Z. (since GRN_LED pin is open-drain).
3-0	R / W	DEEPS3_GRN_BLK_FREQ bits (powered by VSB, RSMRST# reset, default 000b), when LDB CRF9 Bit 6 is set to 0 1xxx : Fading LED. 0111 : GRN_LED will drive low. 0110 : GRN_LED will output 2Hz , 50% duty-cycle signal. 0101 : GRN_LED will output 1Hz , 50% duty-cycle signal. 0100 : GRN_LED will output 0.5Hz , 50% duty-cycle signal. 0011 : GRN_LED will output 0.25Hz , 50% duty-cycle signal. 0010 : GRN_LED will output 0.125Hz , 50% duty-cycle signal. 0001 : GRN_LED will output 0.0625Hz , 50% duty-cycle signal. 0000 : GRN_LED will output High-Z. (since GRN_LED pin is open-drain).

CR F4h. DEEPER_SLEEPING_STATE Front panel green & yellow LED control register

Location: Address F4h

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	DEEPS5_YLW_BLK_FREQ bits (powered by VSB, RSMRST# reset, default 000b), when LDB CRF9 Bit 5 is set to 0 1xxx : Fading LED. 0111 : YLW_LED will drive low. 0110 : YLW_LED will output 2Hz , 50% duty-cycle signal. 0101 : YLW_LED will output 1Hz , 50% duty-cycle signal. 0100 : YLW_LED will output 0.5Hz , 50% duty-cycle signal. 0011 : YLW_LED will output 0.25Hz , 50% duty-cycle signal. 0010 : YLW_LED will output 0.125Hz , 50% duty-cycle signal. 0001 : YLW_LED will output 0.0625Hz , 50% duty-cycle signal. 0000 : YLW_LED will output High-Z. (since GRN_LED pin is open-drain).

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BIT	READ / WRITE	DESCRIPTION
3-0	R / W	DEEPS5_GRN_BLK_FREQ bits (powered by VSB, RSMRST# reset, default 000b), when LDB CRF9 Bit 4 is set to 0 1xxx : Fading LED. 0110 : GRN_LED will output 2Hz , 50% duty-cycle signal. 0101 : GRN_LED will output 1Hz , 50% duty-cycle signal. 0100 : GRN_LED will output 0.5Hz , 50% duty-cycle signal. 0011 : GRN_LED will output 0.25Hz , 50% duty-cycle signal. 0010 : GRN_LED will output 0.125Hz , 50% duty-cycle signal. 0001 : GRN_LED will output 0.0625Hz , 50% duty-cycle signal. 0000 : GRN_LED will output High-Z. (since GRN_LED pin is open-drain).

CR F5h. Front panel green LED control register

Location: Address F5h

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 87h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	AUTO_EN bit (powered by VSB, RSMRST# reset , default 1b) Set to 0, the GRN_LED and YLW_LED are controlled by GRN_ LED_ RST, GRN_BLK_FREQ and YLW_LED_RST, YLW_BLK_FREQ bits. Set to 1, the GRN_LED and YLW_LED are controlled by SLP_S5#, SLP_S3# pins and GRN_BLK_FREQ, YLW_BLK_FREQ bits.
6	R / W	GRN_LED_RST# (powered by VSB, RSMRST# reset , default 0b) Set to 0, GRN_BLK_FREQ will be reset to 000 when (SLP_S3# & internal PWROK) = 0, which means when in S3~S5 states, GRN_LED will output High-Z. Set to 1, GRN_BLK_FREQ will be kept when (SLP_S3# & internal PWROK) = 0.
5	R / W	GRN_LED_POL (powered by VSB, RSMRST# reset , default 0b) Set to 0 , GRN_LED output is active low. Set to 1 , GRN_LED output is active high.
4	Reserved.	
3-0	R / W	GRN_BLK_FREQ bits (powered by VSB, RSMRST# reset, default 000b) 1xxx : Fading LED. 0111 : GRN_LED will drive low. 0110 : GRN_LED will output 2Hz , 50% duty-cycle signal. 0101 : GRN_LED will output 1Hz , 50% duty-cycle signal. 0100 : GRN_LED will output 0.5Hz , 50% duty-cycle signal. 0011 : GRN_LED will output 0.25Hz , 50% duty-cycle signal. 0010 : GRN_LED will output 0.125Hz , 50% duty-cycle signal. 0001 : GRN_LED will output 0.0625Hz , 50% duty-cycle signal. 0000 : GRN_LED will output High-Z. (since GRN_LED pin is open-drain).

CR F6h.Front panel yellow LED control register

Location: Address F6h

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Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 47h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	YLW_LED_RST# (powered by VSB, RSMRST# reset , default 1b) Set to 0, YLW_BLK_FREQ will be reset to 000 when (SLP_S3# & internal PWROK) = 0, which means when in S3~S5 states, YLW_LED will output High-Z. Set to 1, YLW_BLK_FREQ will be kept when (SLP_S3# & internal PWROK) = 0.
5	R / W	YLW_LED_POL (powered by VSB, RSMRST# reset , default 0b) Set to 0, YLW_LED output is active low. Set to 1, YLW_LED output is active high.
4	Reserved.	
3-0	R / W	YLW_BLK_FREQ bits (powered by VSB, RSMRST# reset, default 111b) 1xxx : Fading LED. 0111 : YLW_LED will drive low. 0110 : YLW_LED will output 2Hz , 50% duty-cycle signal. 0101 : YLW_LED will output 1Hz , 50% duty-cycle signal. 0100 : YLW_LED will output 0.5Hz , 50% duty-cycle signal. 0011 : YLW_LED will output 0.25Hz , 50% duty-cycle signal. 0010 : YLW_LED will output 0.125Hz , 50% duty-cycle signal. 0001 : YLW_LED will output 0.0625Hz , 50% duty-cycle signal. 0000 : YLW_LED will output High-Z. (since YLW_LED pin is open-drain).

CR F7h.YLW & GRN Eanble register

Location: Address F7h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	YLW_DEEPS3_SET
6	R / W	GRN_DEEPS3_SET
5	R / W	YLW_DEEPS5_SET
4	R / W	GRN_DEEPS5_SET
3-0	Reserved.	

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23.13 Logical Device D (WDT2)

CR E0h. Watchgod Timer II(WDTII) Control Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-2	R / W	Clock select of 5 second Watchdog Timer II **Bits** **3 2** **=** 0 0, clock rate 4Hz = 0 1, clock rate 1Hz = 1 0, cloak rate 1/2Hz = 1 1, clock rate 1MHz
1-0	R / W	Clock select of 100ms Watchdog Timer II **Bits** **1 0** = 0 0, clock rate 512Hz, WDT will generate 100mS low pulse after 5S = 0 1, clock rate 256Hz, WDT will generate 200mS low pulse after 5S = 1 0, clock rate 1KHz, WDT will generate 50mS low pulse after 5S = 1 1, clock rate 1MHz, WDT will generate 50uS low pulse after 5S

CR E1h. Watchdog Timer II 100ms counter Register

Location: Address E1h
Attribute: Read only
Power Well: VSB
Reset by: RSMRST#
Default : 32h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R	Setting of 100mS watch dog time out counter. Default is 8'h32. **Note. If CRE7[1:0] is 2'b00, then Watchdog Timer II 100ms counter will be 1.95ms(512Hz) * 50(8'h32) = 100m sec**

CR E2h. Watchdog Timer II 5s counter Register

Location: Address E2h
Attribute: Read only
Power Well: VSB
Reset by: RSMRST#
Default : 14h

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Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R	Setting of 5 second watch dog time out counter. Default is 8'h14. **Note. If CRE7[3:2] is 2'b00, then Watchdog Timer II counter will be 0.25s(4Hz) * 20(8'h14) = 5 sec**

CR E3h. Watchdog Timer II Software Reset Register

Location: Address E3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R/W	This bit is used to start Watchdog Timer II counter 0: Disable 1: Start the counter. When the time is up, it will clear itself to 0.

CR E4h. Watchdog Timer II Status Register

Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R/W	Watchdog Timer II status. When this bit is set to 1, it means timeout event occurs.
6-0	Reversed	

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23.14 Logical Device E (CIR WAKE-UP)

CR 30h.

Location: Address 00h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: CIR Wake-up is inactive. 1: CIR Wake-up Interface is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Wake-up Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for CIR Wake-up.

CR E0h.

Location: Address E0h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 25h

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Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5-0	R / W	Clock 1M to 40K dividor register

CR E1h.

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
2	R/W	Clock 1M to 40K dividor number flush. Write 1 then auto-clear.
1	R/W1C	CIR Wake-up clock calibration done status bit. .
0	R/W	CIR Wake-up clock calibration enable. Cleaned once calibration is done.

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23.15 Logical Device F (GPIO)

CR E0h.

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP0 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E1h.

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP1 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E2h.

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP2 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E3h.

Location: Address E3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#

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Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP3 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E4h.
Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP4 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E5h.
Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP5 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E6h.
Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP6 Push-Pull/OD select 0:Push-Pull 1:Open Drain

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CR E7h.

Location: Address E7h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 03h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	GP7 Push-Pull/OD select 0:Push-Pull 1:Open Drain
0	Reserved.	

CR F0h. I2C Control & Address Register

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 9Dh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable I2C_Slave
6-0	R / W	I2C Address

CR F1h. I2C to 80PORT Control Register

Location: Address F1h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	80PORT Display 0: Enable 1: Disable
0	R / W	LPC or I2C to 80PORT switch 0: LPC 1: I2C

CR F2h. I2C to 80PORT Data Register

Location: Address F2h

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Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	I2C to 80PORT Data

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23.16 Logical Device 10 (UARTC)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, E0h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 3.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART C clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART C clock source is 2 MHz (24 MHz / 12). 0 0: UART C clock source is 24 MHz (24 MHz / 1). 0 0: UART C clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTC 9bit-mode Config Register

Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bitmode RX block function will pass all data or address byte and not compare any address byte. 1: 9bitmode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bitmode RX block function.
5	R / W	**RST_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX blockwill keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data. 1: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data.

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BIT	READ / WRITE	DESCRIPTION
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ingored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bitmode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTC 9bit-mode Slave Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTC 9bit-mode Slave Mask Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTC 9bit-mode Broadcase Address Register

Location: Address F5h
Attribute: Read/Write

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Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcase Address**

CR F6h. UARTC 9bit-mode Interrupt Control Register
Location: Address F6h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTC 9bit-mode IRQ output. 1: Enalbe UARTC 9bit-mode IRQ output.

CR F7h. UARTC 9bit-mode IRQ Status Register
Location: Address F7h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	**UARTC 9bit-mode Status Bit** 0: UARTC 9bit-mode IRQ have not been triggered. 1: UARTC 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTC Control Register
Location: Address F8h
Attribute: Read/Write
Power Well: VCC

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Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved	uartCD_switch _enable	Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	fifo_level_mode: (Also check UFR register B7-6 definition)
5	Reserved.
4	uartCD_switch_enable (Bypass mode) 0: switch disable 1: switch enable
3-1	Reserved. (All should be set to 0)
0	Extending fifo enable bit: 0: Disable128bytes TX and RX FIFO. 1: Enable128bytes TX and RX FIFO.

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

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23.17 Logical Device 11 (UARTD)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h, E0h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 4.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART D clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART D clock source is 2 MHz (24 MHz / 12). 0 0: UART D clock source is 24 MHz (24 MHz / 1). 0 0: UART D clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTD 9bit-mode Config Register

Location: Address F1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bitmode RX block function will pass all data or address byte and not compare any address byte. 1: 9bitmode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bitmode RX block function.
5	R / W	**RST_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX blockwill keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data. 1: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data.

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BIT	READ / WRITE	DESCRIPTION
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ingored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bitmode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTD 9bit-mode Slave Address Register

Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTD 9bit-mode Slave Mask Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTD 9bit-mode Broadcase Address Register

Location: Address F4h
Attribute: Read/Write

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Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcase Address**

CR F6h. UARTD 9bit-mode Interrupt Control Register
Location: Address F5h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTD 9bit-mode IRQ output. 1: Enalbe UARTD 9bit-mode IRQ output.

CR F7h. UARTD 9bit-mode IRQ Status Register
Location: Address F6h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	**UARTD 9bit-mode Status Bit** 0: UARTD 9bit-mode IRQ have not been triggered. 1: UARTD 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTD Control Register
Location: Address F7h
Attribute: Read/Write
Power Well: VCC

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Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved		Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	fifo_level_mode: (Also check UFR register B7-6 definition)
5-4	Reserved.
3-1	Reserved. (All should be set to 0)
0	Extending fifo enable bit: 0: Disable128bytes TX and RX FIFO. 1: Enable128bytes TX and RX FIFO.

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

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23.18 Logical Device 12 (UARTE)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, E8h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 5.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART E clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART E clock source is 2 MHz (24 MHz / 12). 0 0: UART E clock source is 24 MHz (24 MHz / 1). 0 0: UART E clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTE 9bit-mode Config Register

Location: Address F1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bitmode RX block function will pass all data or address byte and not compare any address byte. 1: 9bitmode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bitmode RX block function.
5	R / W	**RST_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX blockwill keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data. 1: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data.

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BIT	READ / WRITE	DESCRIPTION
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ingored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bitmode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTE 9bit-mode Slave Address Register

Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTE 9bit-mode Slave Mask Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTE 9bit-mode Broadcase Address Register

Location: Address F4h
Attribute: Read/Write

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Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcase Address**

CR F6h. UARTE 9bit-mode Interrupt Control Register
Location: Address F5h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTE 9bit-mode IRQ output. 1: Enalbe UARTE 9bit-mode IRQ output.

CR F7h. UARTE 9bit-mode IRQ Status Register
Location: Address F6h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	**UARTE 9bit-mode Status Bit** 0: UARTE 9bit-mode IRQ have not been triggered. 1: UARTE 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTE Control Register
Location: Address F7h
Attribute: Read/Write
Power Well: VCC

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Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved	uartEF_switch _enable	Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	fifo_level_mode: (Also check UFR register B7-6 definition)

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

5	Reserved.
4	uartEF_switch_enable (Bypass mode) 0: switch disable 1: switch enable
3-1	Reserved. (All should be set to 0)
0	Extending fifo enable bit: 0: Disable128bytes TX and RX FIFO. 1: Enable128bytes TX and RX FIFO.

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23.19 Logical Device 13 (UARTF)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h, E8h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port 6.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4~2	Reserved.	
1~0	R / W	**Bits** **1 0** 0 0: UART F clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART F clock source is 2 MHz (24 MHz / 12). 0 0: UART F clock source is 24 MHz (24 MHz / 1). 0 0: UART F clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTF 9bit-mode Config Register

Location: Address F1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bitmode RX block function will pass all data or address byte and not compare any address byte. 1: 9bitmode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bitmode RX block function.
5	R / W	**RST_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX blockwill keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data. 1: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data.

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BIT	READ / WRITE	DESCRIPTION
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ingored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bitmode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTF 9bit-mode Slave Address Register

Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTF 9bit-mode Slave Mask Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTF 9bit-mode Broadcase Address Register

Location: Address F4h
Attribute: Read/Write

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Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcase Address**

CR F6h. UARTF 9bit-mode Interrupt Control Register
Location: Address F5h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTF 9bit-mode IRQ output. 1: Enalbe UARTF 9bit-mode IRQ output.

CR F7h. UARTF 9bit-mode IRQ Status Register
Location: Address F6h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	**UARTF 9bit-mode Status Bit** 0: UARTF 9bit-mode IRQ have not been triggered. 1: UARTF 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTF Control Register
Location: Address F7h
Attribute: Read/Write
Power Well: VCC

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Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved		Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	fifo_level_mode: (Also check UFR register B7-6 definition)
5-4	Reserved.
3-1	Reserved. (All should be set to 0)
0	Extending fifo enable bit: 0: Disable128bytes TX and RX FIFO. 1: Enable128bytes TX and RX FIFO.

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

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23.20 Logical Device 14 (PORT80, IR)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: IR is inactive. 1: IR is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for IR.

CR E0h. PORT80 UART Control Register

Location: Address E0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 80h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7	R / W	TxEN (Transmit enable)
6-5	Reserved.	
4	R / W	PARE (Parity enable)
3	R / W	PARS (Parity Selection) 0: odd parity 1: even parity
2	R / W	STPS (Stop bit length selecion) 0: 1 stop bit 1: 2 stop bits
1	R / W	CHAS (Character length selection) 0: 8 bits 1: 7bits
0	Reserved.	

CR E1h. PORT80 UART Status Register

Location: Address E1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R	TD (Transmit done status) When UART finish transmit, it would be 1 and auto clear by hardware
0	R	TBF (Transmit buffer full flag) 0: UART is idle 1: UART is transmitting

CR E2h. PORT80 UART Baud Rate Generator High Byte

Location: Address E2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator high byte)

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CR E3h. PORT80 UART Baud Rate Generator Low Byte

Location: Address E3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 10h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator low byte) Baud Rate = 2MHz / ({BRGH, BRGL} + 1)

CR E4h. PORT80 UART Transmit Buffer

Location: Address E4h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	UARTBUF (UART Transmit buffer)

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4~2	Reserved.	
1~0	R / W	**Bits** **1 0** 0 0: IR clock source is 1.8462 MHz (24 MHz / 13). 0 1: IR clock source is 2 MHz (24 MHz / 12). 0 0: IR clock source is 24 MHz (24 MHz / 1). 0 0: IR clock source is 14.769 MHz (24 MHz / 1.625).

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CR F1h.

Location: Address F1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5-3	R / W	IRMODE => IR function mode selection. See the table below.
2	R / W	IR half / full duplex function selection. 0: IR function is Full Duplex. 1: IR function is Half Duplex.
1	R / W	0: IRTX pin of IR function in normal condition. 1: Inverse IRTX pin of IR function.
0	R / W	0: IRRX pin of IR function in normal condition. 1: Inverse IRRX pin of IR function.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	Tri-state	High
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	Routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

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23.21 Logical Device 15 (FADING LED)

CR E0.Fading Maximun Duty Cycle Value Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_maxval Fading led ➔ Intel_led_clk_sel = 1: 250KHz and Pled_en=1 The maximum duty cycle value. Solid led ➔ Pled_clk_sel = 1: 250KHz and Pled_en=0 <duty cycle> 8'h01: 1/255 = 0.3% 8'h02: 2/255 = 0.7% … 8'h40: 64/255 = 25.1% ... 8'hFF: 255/255 = 100% Blink led ➔ Pled_clk_sel = 0: 4Hz <duty cycle> 8'h01: 1/255 = 0.3% 8'h02: 2/255 = 0.7% … 8'h40: 64/255 = 25.1% ... 8'hFF: 255/255 = 100%

CR E1. Fading Middle Duty Cycle Value Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 3Fh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_midval turning point, the duty cycle value between the minimum and maximum duty cycle value.

CR E2. Fading Minimun Duty Cycle Value Register

Location: Address E2h

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Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_minval The minimum duty cycle value.

CRE3. Fading Increase Duty Cycle Value Register

Location: Address E3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 11h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Fading_duty_inc_h The increased duty cycle value between the turning point and the maximum duty cycle value.
3-0	R / W	Fading_duty_inc_l The increased duty cycle value between the minimum duty cycle value and turning point.

CR E4. Fading Decrease Duty Cycle Value Register

Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 11h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Fading_duty_dec_h The decreased duty cycle value between the maximum duty cycle value and the turning point.
3-0	R / W	Fading_duty_dec_l The decreased duty cycle value between the turning point and the minimum duty cycle value.

CR E5. Fading Configure Register

Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 02h
Size: 8 bits

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BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Fading_prgval Repeat each duty cycle value for a few time.
3-2	R / W	Fading_extend 2'b00: No extend. 2'b01: Only extend the minimum duty cycle value for a few time. 2'b10: Only extend the maximum duty cycle value for a few time. 2'b11: Both extend the minimum and the maximum duty cycle value for a few time.
1	R / W	Fading_clk_sel 1: 250KHz 0: 4Hz
0	R / W	Fading_en 1: fading led 0: solid led

CRE6. Fading Light extend Register

Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_light_ext The time for extend the maximum duty cycle value.

CR E7. Fading Dark extend Register

Location: Address E7h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_dark_ext The time for extend the minimum duty cycle value.

CR E8. Fading Frequency Divide Register

Location: Address E8h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

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BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading freq_div led_clk_sel =1: 250KHz 8'h01: 250Khz/1=250Khz 8'h02: 250Khz/2=125Khz … 8'hFF: 250Khz/255=0.98Khz Fading_clk_sel =0: 4Hz 8'h00: always high 8'h01: always low 8'h02: 4Hz 8'h03: 2Hz 8'h04: 1Hz 8'h05: 1/2Hz 8'h06: 1/4Hz 8'h07: always high others: always low

CR E9. Suspend LED S5 Enable Register

Location: Address E9h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	**Reserved**	
0	R / W	Suspend led S5 enable (1:Enable, 0:Disbale)

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23.22 Logical Device 16 (DEEP SLEEP)

CR 30h. Deep Sleep configuration register

Location: Address 30h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 20h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	Set to 0, the RSMRST_SYS detect PSOUT# voltage. Set to 1, the RSMRST_SYS detect PCHVSB voltage.
5	R / W	deep_s3_opt Set to 0, when enter Deep S3 state, the SUS_WARN_5VDUAL will keep low. Set to 1, when enter Deep S3 state, the SUS_WARN_5VDUAL will follow DSW sequence.
4	R / W	dsw_wake_opt (test mode) Set to 0, the PSOUT# will assert until SLPS3# high when deep s5 wakeup event happened. Set to 1, the PSOUT# will assert until RSMRST_L high and SLP_SUS_L high when deep s5 wakeup event happened. **PS. This bit only active when PCH_DSW_EN & (Deep S5 Enable | Deep S3 Enable)**
3	R / W	PCH_DSW_EN Set to 0, if PCH disable DSW (Deep Sleep Well) function. Set to 1, if PCH enable DSW (Deep Sleep Well) function.
2	R / W	The pin Deep_S5#_Delay option. Set to 0, If Deep_S5 de-asserts, then Deep_S5#_DIeay will de-assert after 50ms. Set to 1, If Deep_S5 de-asserts, then Deep_S5#_DIeay will de-assert after 100ms..
1	R / W	Deep S3 Enable Set to 0, If SLP_S3# state, will not enter Deep S3 state. Set to 1, If SLP_S3# state, will enter Deep S3 state.
0	R / W	Deep S5 Enable Set to 0, If SLP_S5# state, will not enter Deep S5 state. Set to 1, If SLP_S5# state, will enter Deep S5 state.

CR E0h. Deep Sleep wake up PSOUT# delay time

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#

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Default : **20h** (Default: 512ms)
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5~0	R / W	Deep Sleep wake up PSOUT# delay time. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT# after SYS_3VSB and wait a delay time. DELAY TIME = (Setting Value) * 16ms Example : maximum delay time = $(3F)_{hex}$ * 16ms = 1008ms

CR E1h. Deep Sleep wake up PSOUT# pulse width
Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : **04h** (Default: 128 ms)
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R/W	Deep_S5_2 signal status. 0: Deep_S5_2 signal always keep low. 1: Deep_S5_2 signal follow Deep_S5_1 signal.
6	Reserved	
5	SUSLED	SUSLED Enable: 0:Disable (default and output low) 1: Enable
4	Reserved	
3~0	R / W	Deep Sleep wake up PSOUT# pulse width. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT#.. Pulse Width = (Setting Value) * **32ms** Example : maximum pulse width = $(F)_{hex}$ * **32ms** = 480ms

CR E2h. Deep Sleep Delay Time Control
Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 05h (Default: 5 sec)
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: The unit of deep sleep delay time is second. 1: The unit of deep sleep delay time is Minute.
6~0	R / W	Deep Sleep Delay Time Control. When system leaves S0 State, IO will wait a delay time before entering into Deep Sleep State. Example: maximum delay time = 127 second/minute

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24. SPECIFICATIONS

24.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	-0.3 to 3.6	V
VI	Input Voltage	-0.3 to 3VCC+0.3	V
	Input Voltage (5V tolerance)	-0.3 to 5.5	V
TA	Operating Temperature	-40 to +85	°C
TSTG	Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

24.2 DC CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V)

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Battery Quiescent Current	IBAT			2.4	µA	VBAT = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	IVSB			8.0	mA	VSB = 3.3 V, All ACPI pins are not connected.
VCC Quiescent Current	IVCC			25	mA	VSB = 3.3 V VCC (AVCC)= 3.3 V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
Vtt Quiescent Current	IVTT			1	mA	VSB = 3.3 V VCC (AVCC)= 3.3 V VTT = 1.2V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
AIN – Analog input						
AOUT – Analog output						
IN_{tp3} – 3.3V TTL-level input pin						

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PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	µA	VIN = 3.3V
Input Low Leakage	ILIL			-10	µA	VIN = 0 V
IN_{tsp3} – 3.3V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VCC = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VCC = 3.3 V
Hystersis	VTH	0.5	1.2		V	VCC = 3.3 V
Input High Leakage	ILIH			+10	µA	VIN = 3.3 V
Input Low Leakage	ILIL			-10	µA	VIN = 0 V
IN_{gp5} – 5V GTL-level input pin						
Input Low Voltage	VIL		0.72		V	
Input High Voltage	VIH		0.72		V	
Input High Leakage	ILIH			+10	µA	VIN = 3.3V
Input Low Leakage	ILIL			-10	µA	VIN = 0 V
IN_{tp5} – 5V TTL-level input pin						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	µA	VIN = 3.3V
Input Low Leakage	ILIL			-10	µA	VIN = 0 V
IN_{tscup5} – 5V TTL-level, Schmitt-trigger input buffer with controllable pull-up						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VCC = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VCC = 3.3 V
Hystersis	VTH	0.5	1.2		V	VCC = 3.3 V
Input High Leakage	ILIH			+10	µA	VIN = 3.3 V
Input Low Leakage	ILIL			-10	µA	VIN = 0 V
IN_{tsp5} – 5V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VCC = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VCC = 3.3 V
Hystersis	VTH	0.5	1.2		V	VCC = 3.3 V
Input High Leakage	ILIH			+10	µA	VIN = 3.3 V
Input Low Leakage	ILIL			-10	µA	VIN = 0 V
IN_{tdp5} – 5V TTL-level input pin with internal pull-down resistor						
Input Low Voltage	VIL			0.8	V	

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PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	μA	VIN = 3.3V
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
O8 – Output pin with 8mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
Output High Voltage	VOH	2.4			V	IOH = -8 mA
OD8 – Open-drain output pin with 8mA sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
O12 – Output pin with 12mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
OD12 – Open-drain output pin with 12mA sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
O24 – Output pin with 24mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
Output High Voltage	VOH	2.4			V	IOH = -24 mA
OD24 – Open-drain output pin with 24mA sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
O48 – Output pin with 48mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 48 mA
Output High Voltage	VOH	2.4			V	IOH = -48 mA
OD48 – Open-drain output pin with 48mA sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 48 mA
I/O_{V3} – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® PECI						
Input Low Voltage	V_{IL}	0.275*V_{tt}		0.5*V_{tt}	V	
Input High Voltage	V_{IH}	0.55*V_{tt}		0.725*V_{tt}	V	
Output Low Voltage	V_{OL}			0.25*V_{tt}	V	
Output High Voltage	V_{OH}	0.75*V_{tt}			V	
Hysterisis	V_{Hys}	0.1*V_{tt}			V	
O12cu – Output pin 12mA source-sink capability with controllable pull-up						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
OD12cu – Open-drain 12mA sink capability output pin with controllable pull-up						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA

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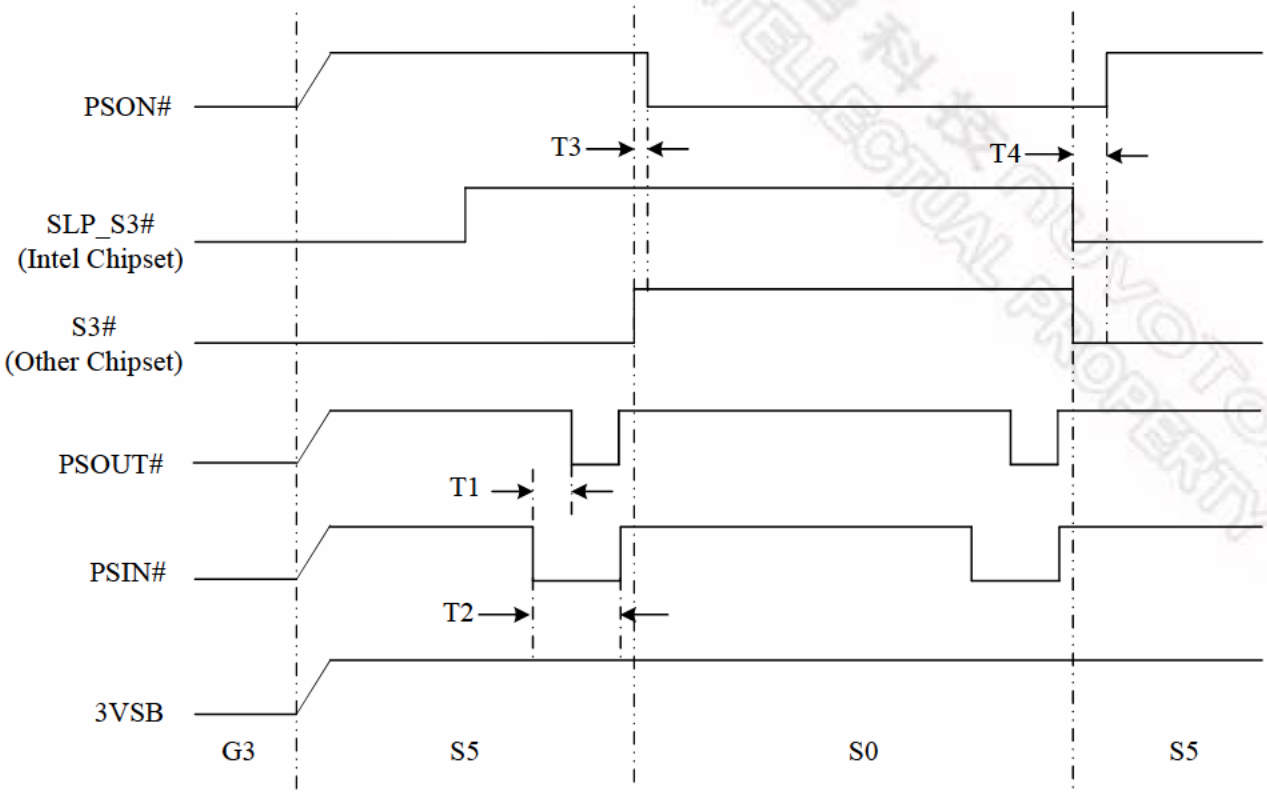
25. AC CHARACTERISTICS

25.1 Power On / Off Timing



	T1	T2	T3	T4
IDEAL TIMING	64ms	Over 64ms at least	< 10ns	32ms

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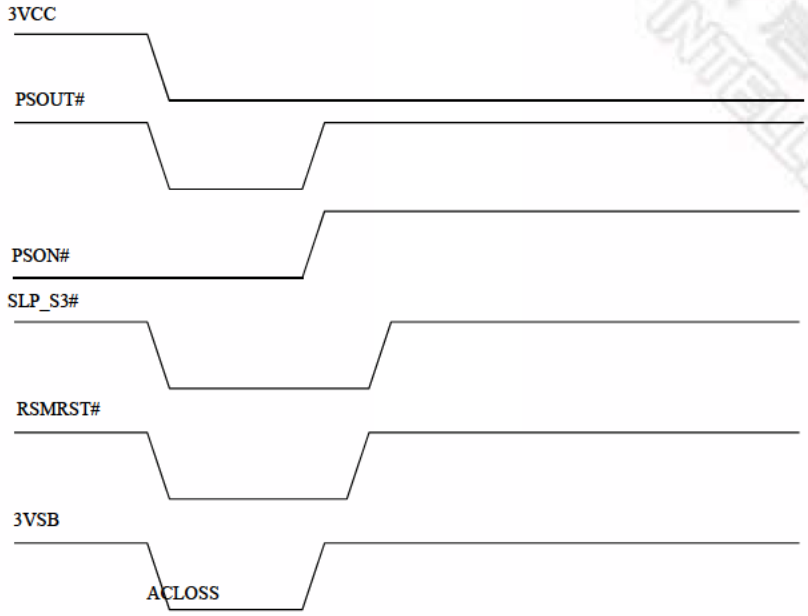
25.2 AC Power Failure Resume Timing

(1) Logical Device A, CR [E4h] bits [6:5] =00 means "OFF" state

("OFF" means the system is always turned off after the AC power loss recovered.)



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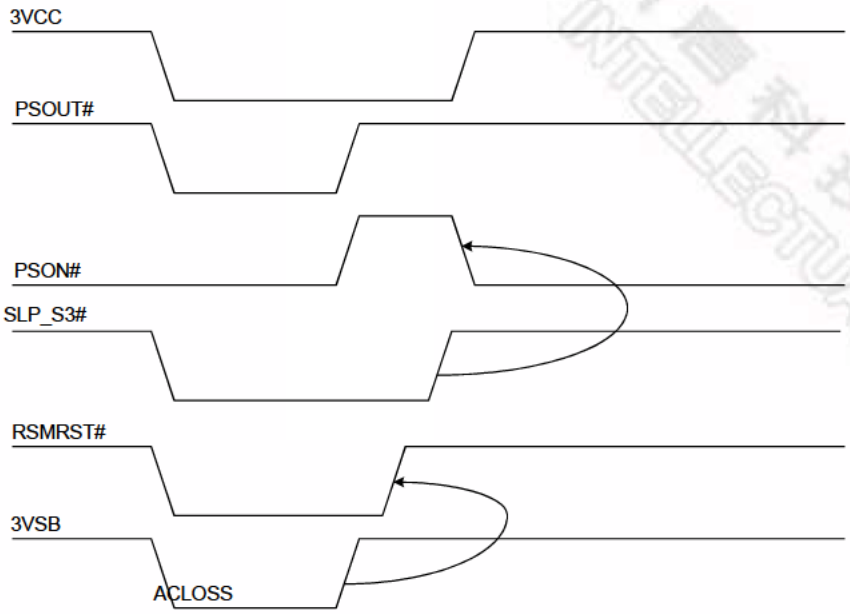
(2) Logical Device A, CR [E4h] bits [6:5]=01 means “ON” state.
(“ON” means the system is always turned on after AC power loss recovered.)



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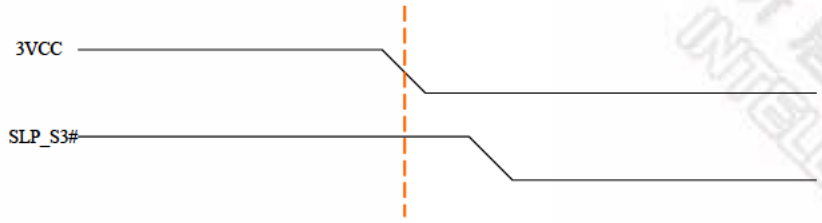
**** What's the definition of former state at AC power failure?**

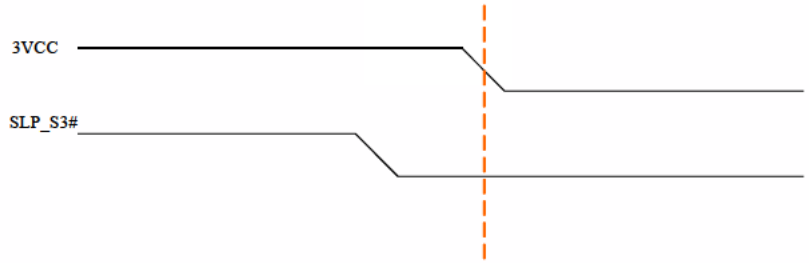
1) The previous state is "ON"

VCC falls to 2.6V and SLP_S3# keeps at VIH 2.0V



2) The previous state is "OFF"

VCC fall to 2.6V and SLP_S3# keeps at VIL 0.8V



To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT6102D / NCT6106D adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state for the system to be "On" or "Off". According to this setting, the system chooses the state after the AC power recovery.

Please refer to the descriptions of bit 6~5 of CR E4h and bit 4 of CR E6h in Logical Device A.

CR E4h

BIT	READ/WRITE	DESCRIPTION
6~5	R / W	Power-loss control bits => (VBAT) 0 0: System always turns off when it returns from power-loss state. 0 1: System always turns on when it returns from power-loss state. 1 0: System turns off / on when it returns from power-loss state depending on the state before the power loss. 1 1: User defines the resuming state before power loss.(refer to Logic Device A, CRE6[4])

CR E6h

BIT	READ/WRITE	DESCRIPTION
4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF

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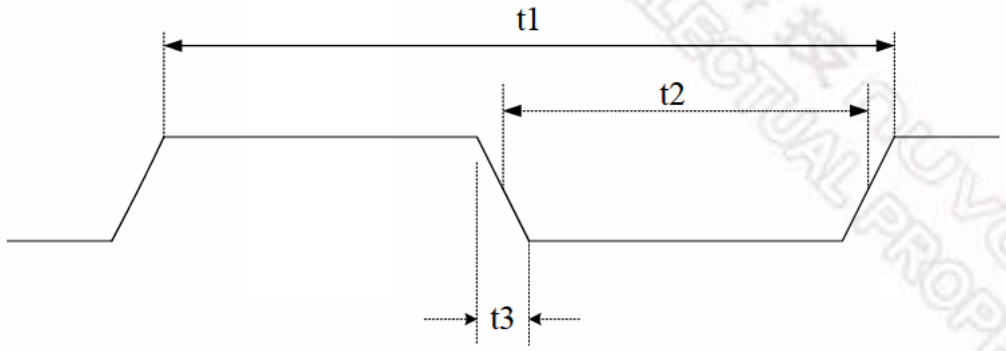
25.3 Clock Input Timing

PARAMETER	48MHZ / 24MHZ		UNIT
	MIN	MAX	
Cycle to cycle jitter		300/500	ps
Duty cycle	45	55	%



PARAMETER	DESCRIPTION	48MHZ / 24MHZ			UNIT
		MIN	TYP	MAX	
t1	Clock cycle time		20.8 / 41.7		ns
t2	Clock high time/low time	9 / 19	10 / 21		ns
t3	Clock rising time/falling time (0.4V~2.4V)			3	ns

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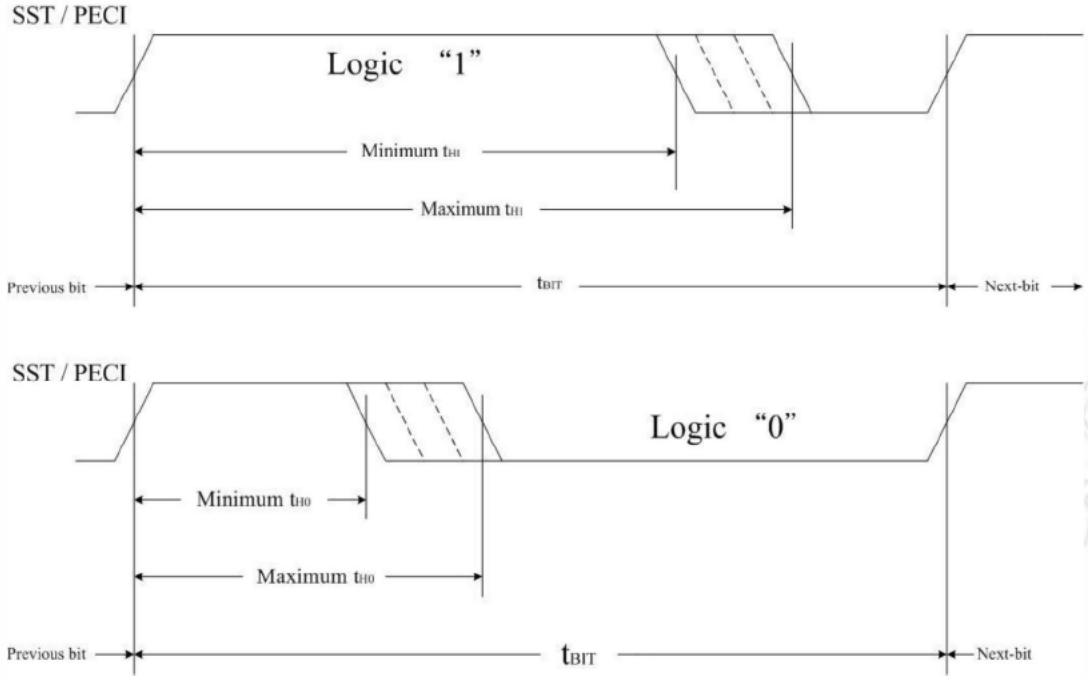
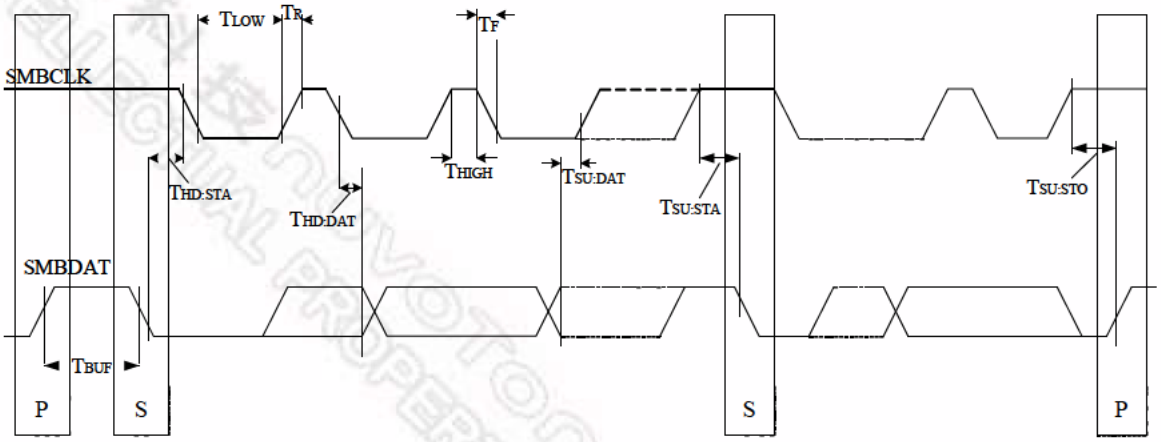
25.4 PECI Timing



SYMBOL		MIN	TYP	MAX	UNITS
t_{BIT}	Client	0.495		500	μs
	Originator	0.495		250	
t_{H1}		0.6	3/4	0.8	× t_{BIT}
t_{H0}		0.2	1/4	0.4	× t_{BIT}

25.5 SMBus Timing



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25.6 Floppy Disk Drive Timing

FDC: Data rate = 1MB, 500KB, 300KB, 250KB/sec.

PARAMETER	SYM.	MIN.	TYP. (NOTE 1)	MAX.	UNIT
DIR# setup time to STEP#	TDST	1.0/1.6 /2.0/4.0			µS
DIR# hold time from STEP#	TSTD	24/40 /48/96			µS
STEP# pulse width	TSTP	6.8/11.5 /13.8/27. 8	7/11.7 /14/28	7.2/11.9 /14.2/28. 2	µS
STEP# cycle width	TSC	NOTE 2	NOTE 2	NOTE 2	mS
INDEX# pulse width	TIDX	125/250 /417/500			nS
RDATA# pulse width	TRD	40			nS
WD# pulse width	TWD	100/185 /225/475	125/210 /250/500	150/235 /275/525	nS

Notes:

1. Typical values for T = 25°C and normal supply voltage.
2. Programmable from 0.5 mS through 32 mS as described in step rate table. (Please refer to the description of the SPECIFY command set.)

Step Rate Table

DATA RATE / SRT	1MB/S	500KB/S	300KB/S	250KB/S
0	8	16	26.7	32
1	7.5	15	25	30
…	…	…	…	…
E	1.0	2	3.33	4
F	0.5	1	1.67	2

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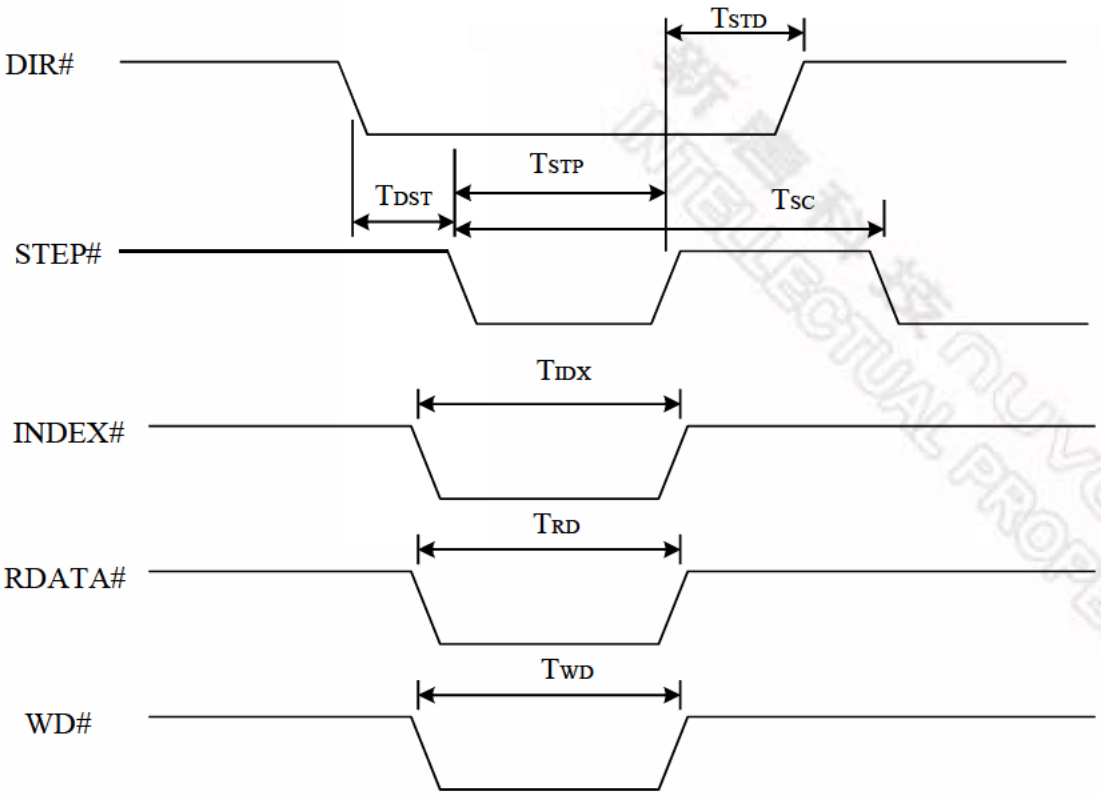
Floppy Disk Driving Timing



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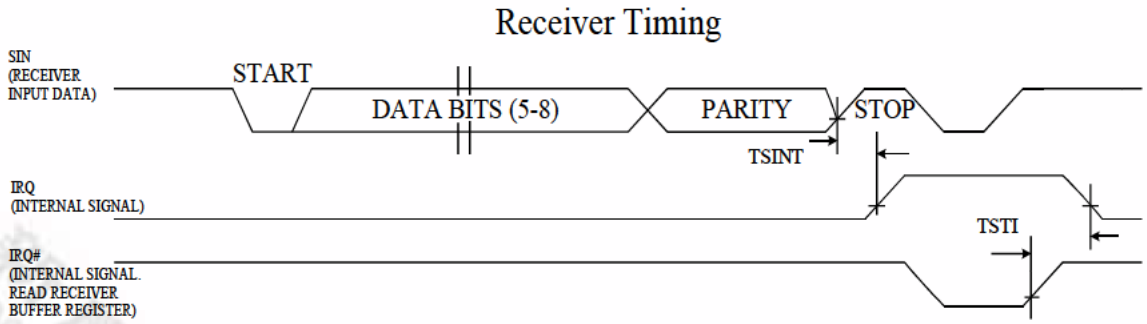
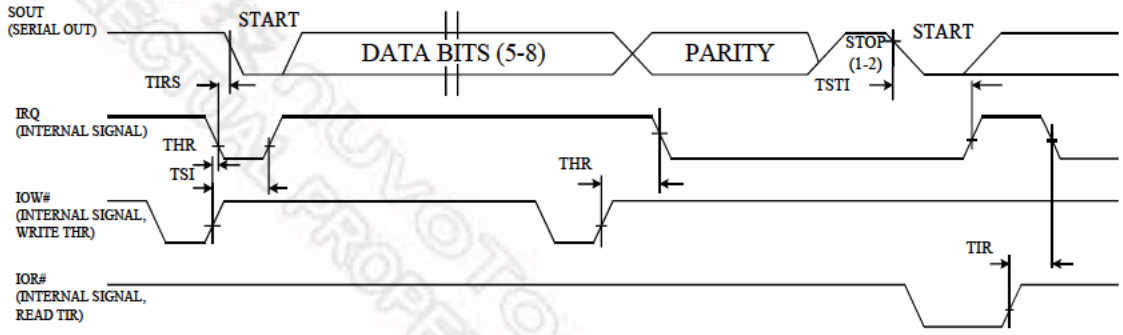
25.7 UART/Parallel Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	TRINT		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR			175	nS
Delay from Initial $\overline{IOW}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			8/16	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	TIR		8	250	nS
Delay from $\overline{IOR}$ to Output	TMWO		6	200	nS
Set Interrupt Delay from Modem Input	TSIM		18	250	nS
Reset Interrupt Delay from $\overline{IOR}$	TRIM		9	250	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

UART Receiver Timing



UART Transmitter Timing



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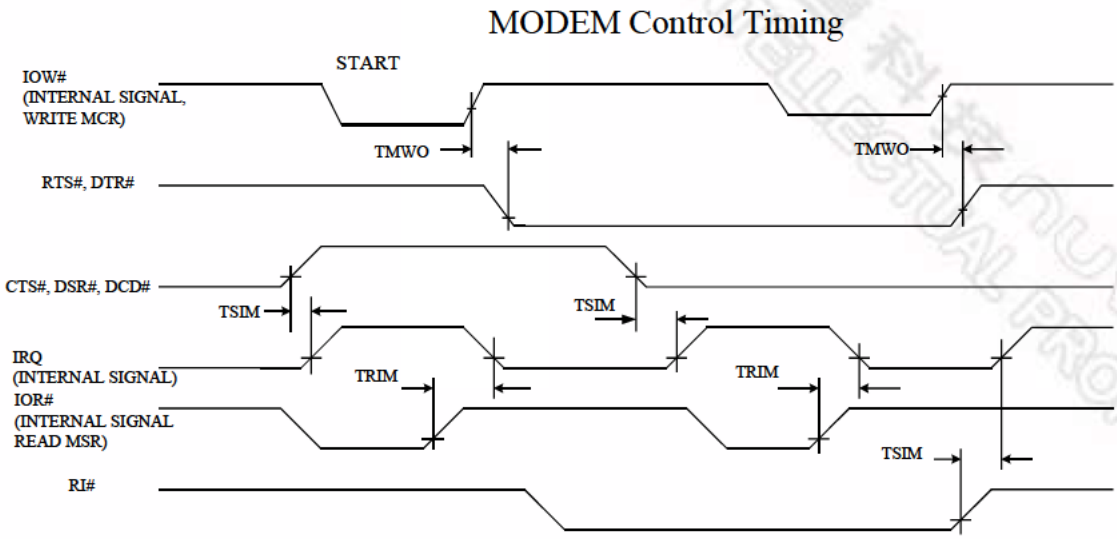
25.8 Modem Control Timing

Modem Control Timing



25.9 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS

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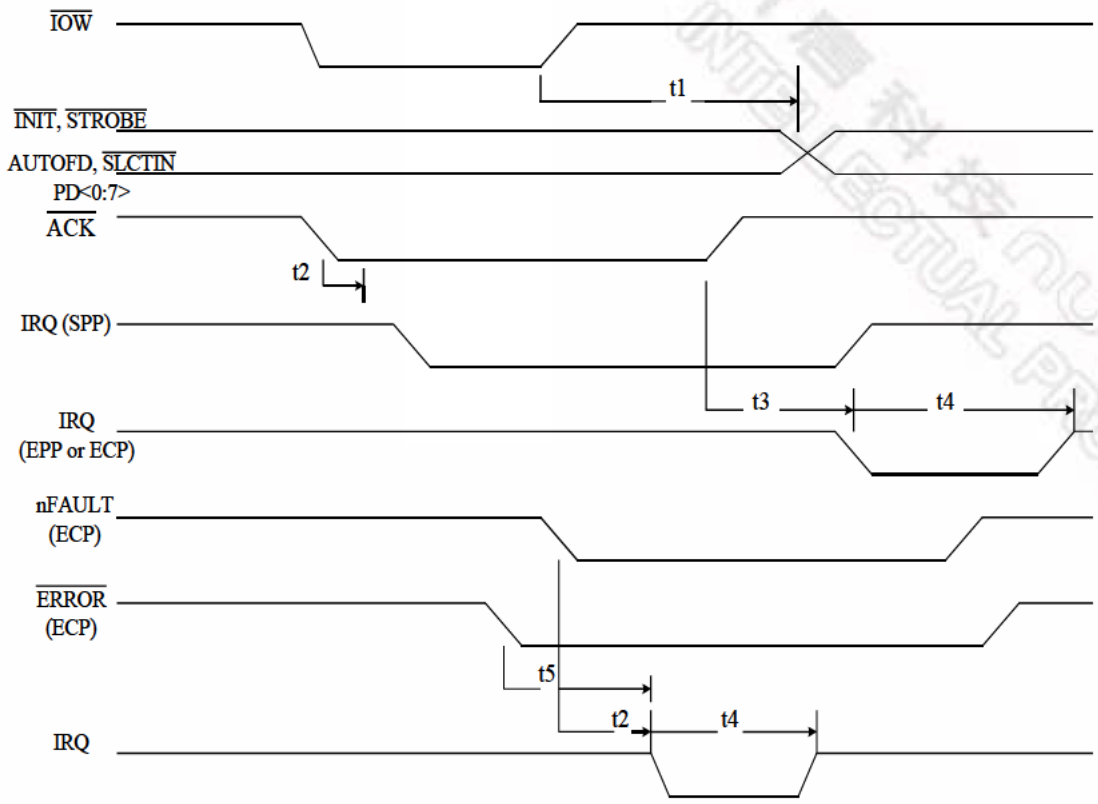
25.9.1 Parallel Port Timing

Parallel Port Timing



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25.9.2 EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS
PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOR}}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{\text{IOR}}$ Deasserted	t2	0		nS
$\overline{\text{IOR}}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{\text{IOR}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t4	40		
$\overline{\text{IOR}}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{\text{IOR}}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	µS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{\text{WRITE}}$ Deasserted to $\overline{\text{IOR}}$ Asserted	t13	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{IOR}}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS

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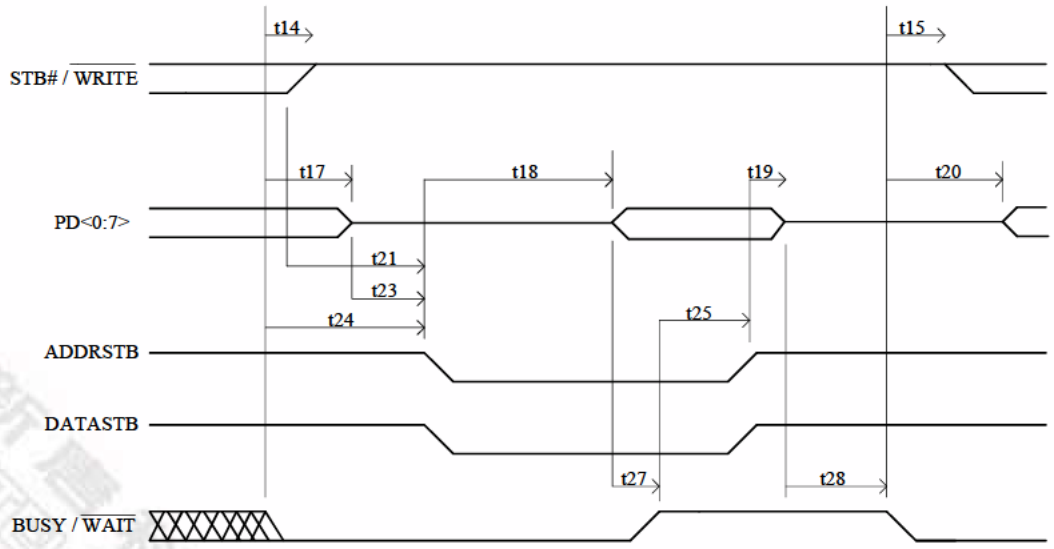
PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS

25.9.3 EPP Data or Address Read Cycle (EPP Version 1.9)

EPP Data or Address Read Cycle (EPP Version 1.9)



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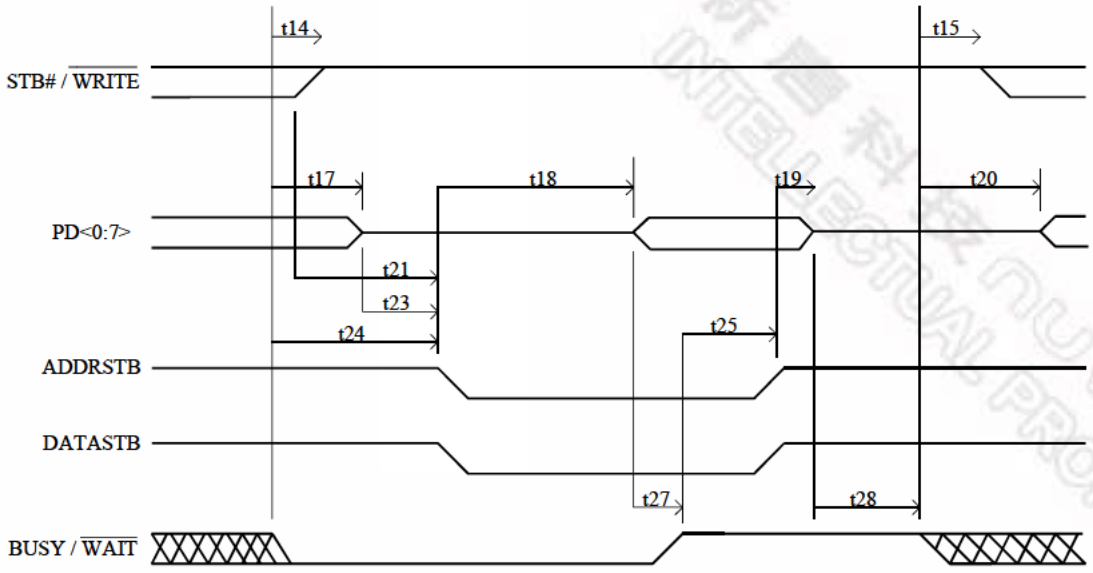
25.9.4 EPP Data or Address Read Cycle (EPP Version 1.7)

EPP Data or Address Read Cycle (EPP Version 1.7)



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25.9.5 EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	µS
Time out	t20	10	12	µS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOW}}$ Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
$\overline{\text{IOW}}$ Deasserted to Ax Invalid	t3	10		nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t5	10		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted	t7	0	24	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{IOW}}$ Asserted to PD Valid	t13	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{IOW}}$ to Command Asserted	t16	5	35	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	µS
Time out	t20	10	12	µS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{WRITE}}$ Deasserted and PD invalid	t22	0		nS
$\overline{\text{WRITE}}$ to Command Asserted	t16	5	35	nS

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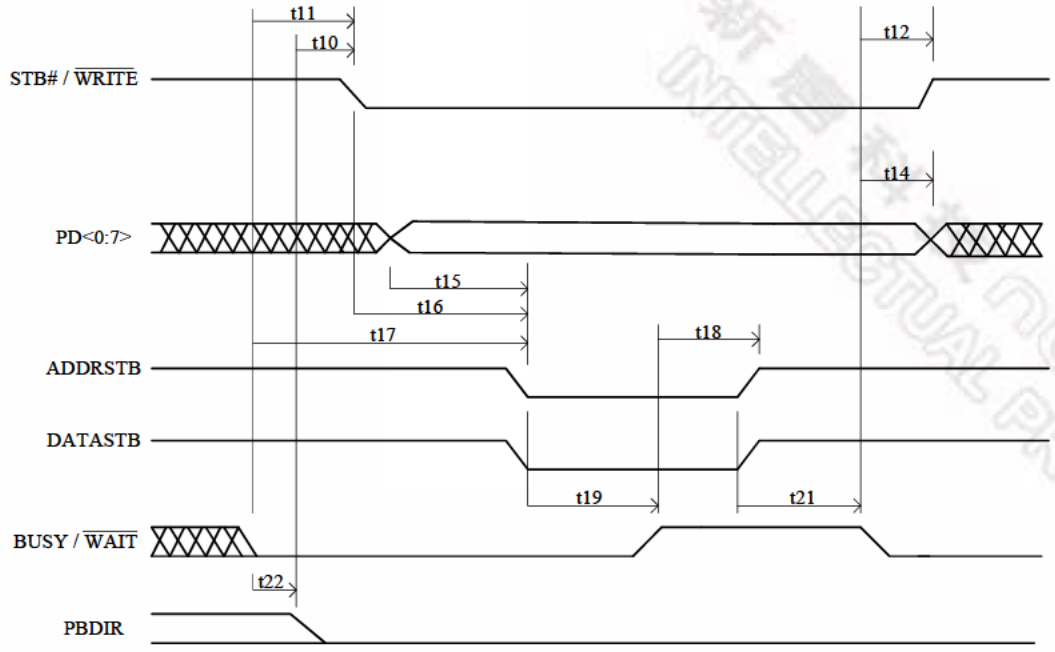
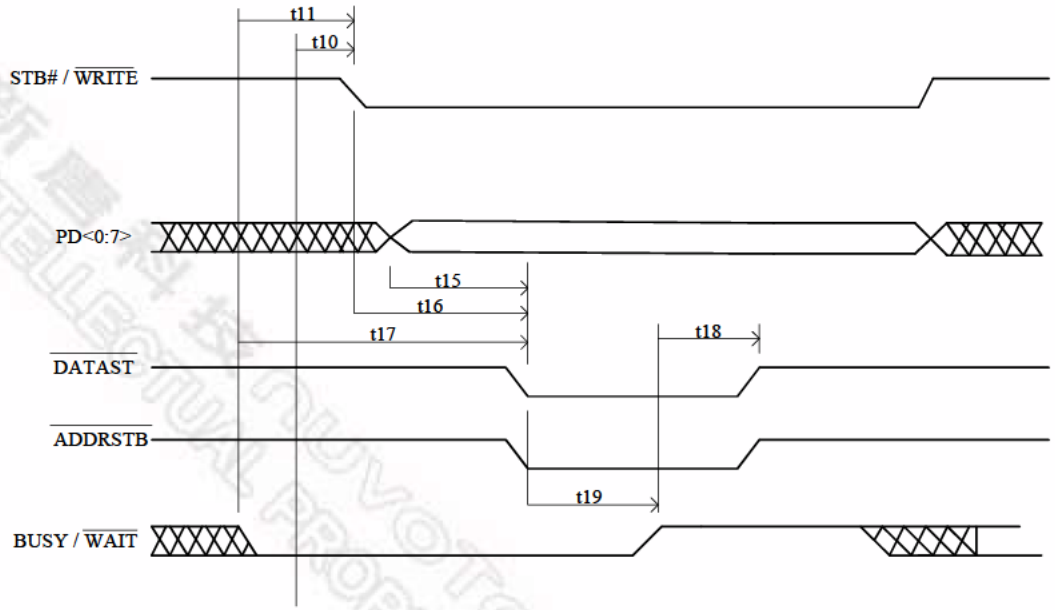
25.9.6 EPP Data or Address Write Cycle (EPP Version 1.9)

EPP Data or Address Write Cycle (EPP Version 1.9)



25.9.7 EPP Data or Address Write Cycle (EPP Version 1.7)

EPP Data or Address Write Cycle (EPP Version 1.7)



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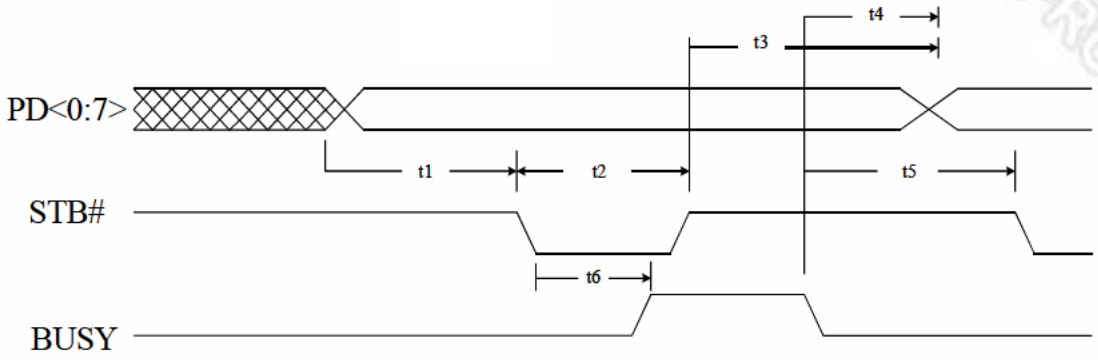
25.9.8 Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

25.9.9 Parallel FIFO Timing

Parallel FIFO Timing



25.9.10ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

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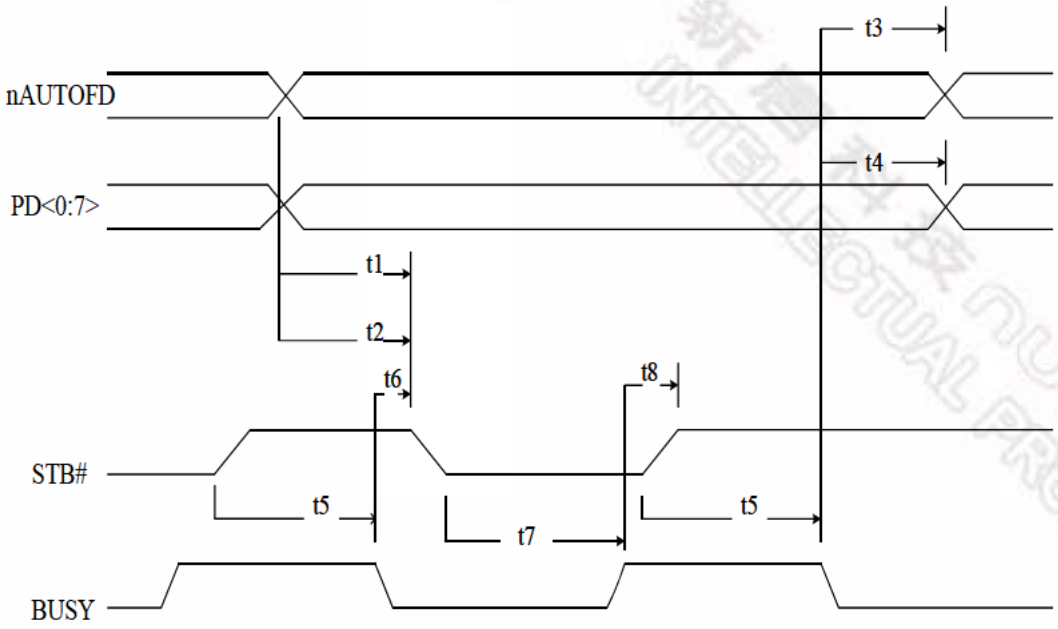
25.9.11ECP Parallel Port Forward Timing

ECP Parallel Port Forward Timing



25.9.12ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

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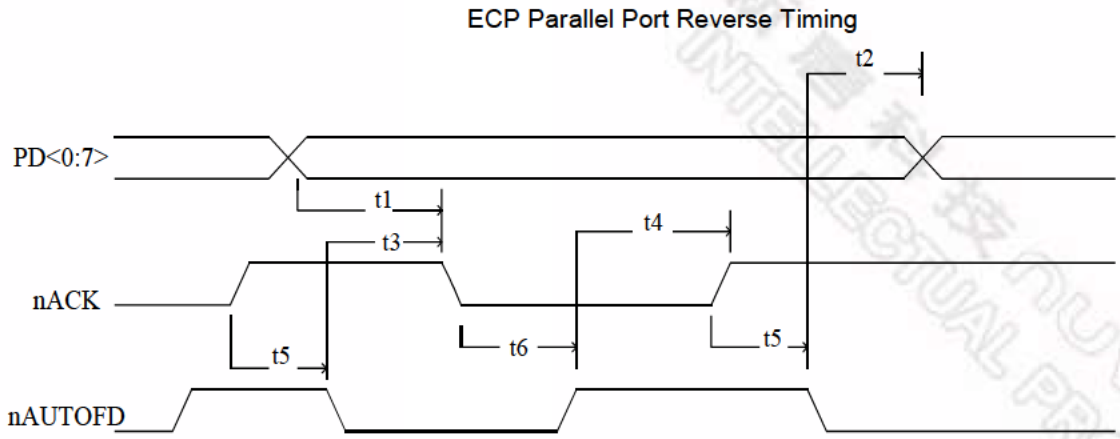
25.9.13ECP Parallel Port Reverse Timing



25.9.14KBC Timing Parameters

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	µS
T13	K/B Clock Period	20		µS
T14	K/B Clock Pulse Width	10		µS
T15	Data Valid Before Clock Falling (RECEIVE)	4		µS
T16	K/B ACK After Finish Receiving	20		µS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		µS

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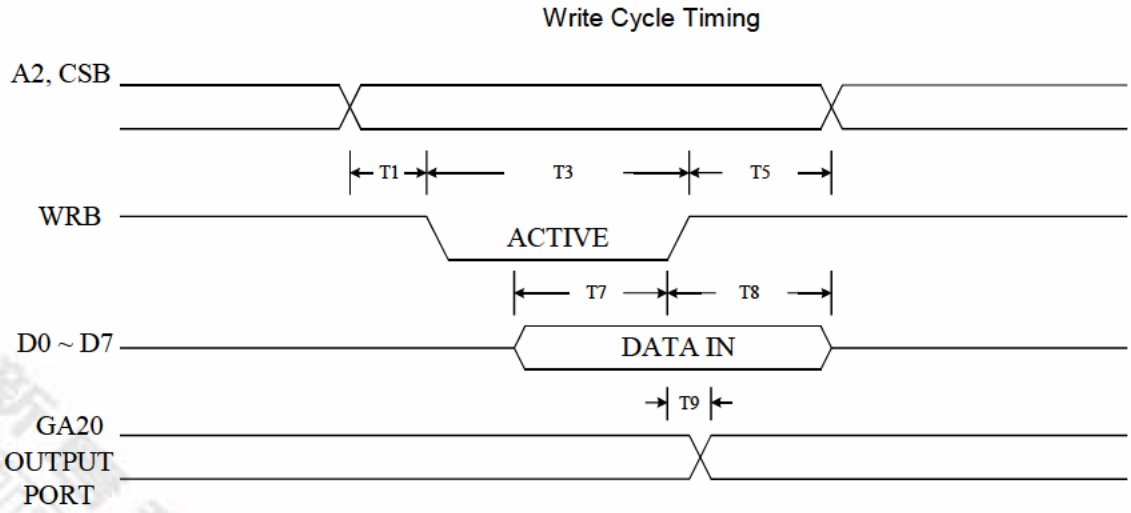
NO.	DESCRIPTION	MIN.	MAX.	UNIT
T21	Input Clock Period (6–16 Mhz)	63	167	nS
T22	Duration of CLK inactive	30	50	µS
T23	Duration of CLK active	30	50	µS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	µS
T25	Time of inhibit mode	100	300	µS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	µS
T27	Duration of CLK inactive	30	50	µS
T28	Duration of CLK active	30	50	µS
T29	Time from DATA transition to falling edge of CLK	5	25	µS

25.9.15Writing Cycle Timing



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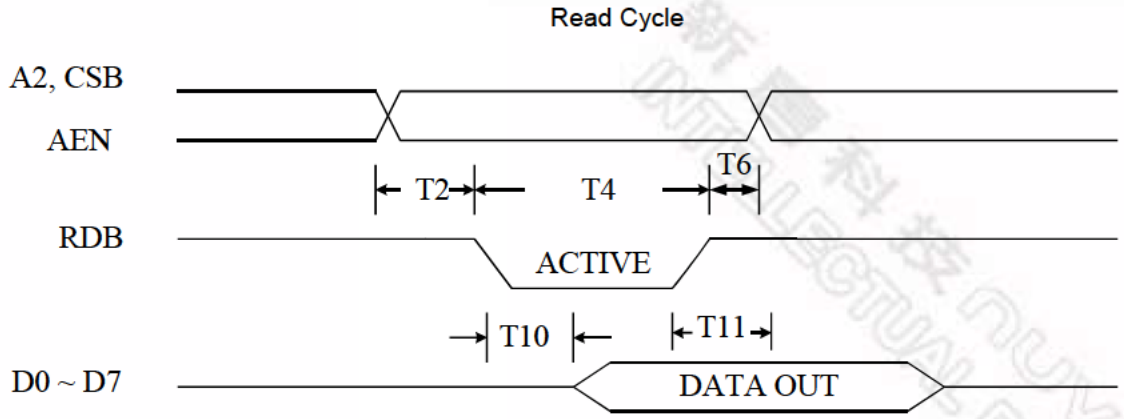
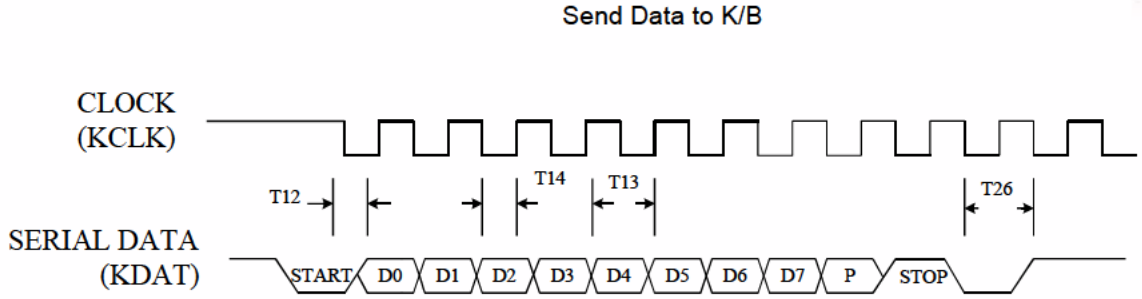
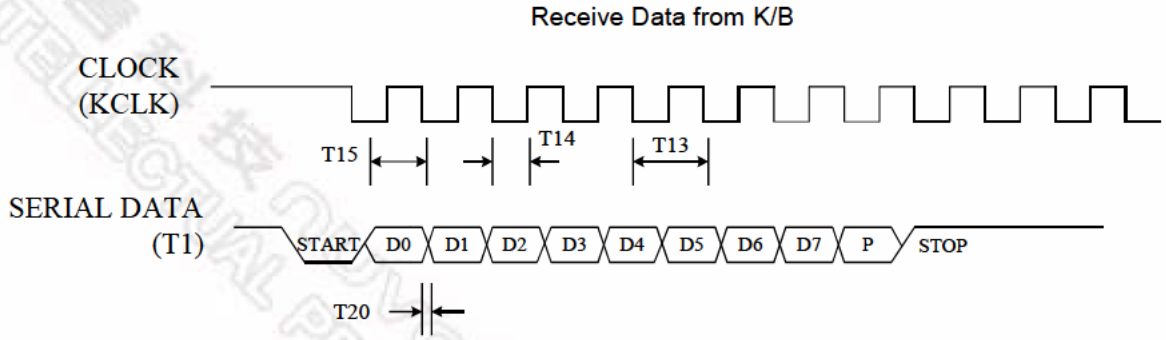
25.9.16 Read Cycle Timing



25.9.17 Send Data to K/B



25.9.18 Receive Data from K/B



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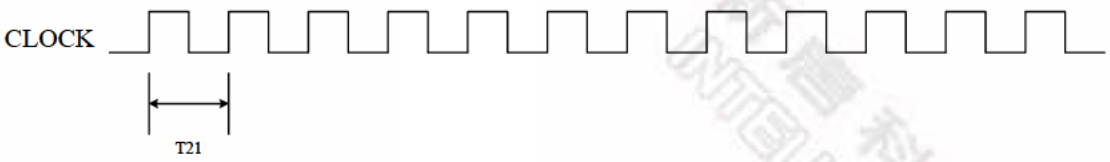
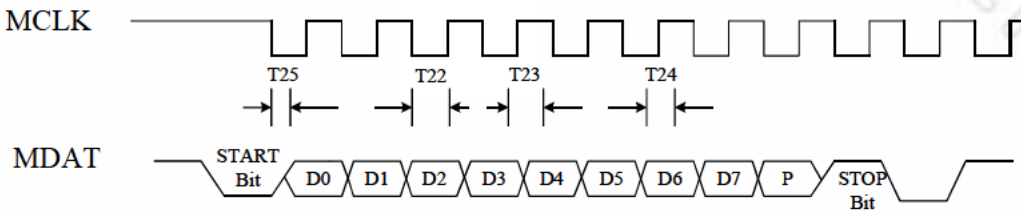
25.9.19 Input Clock

Input Clock



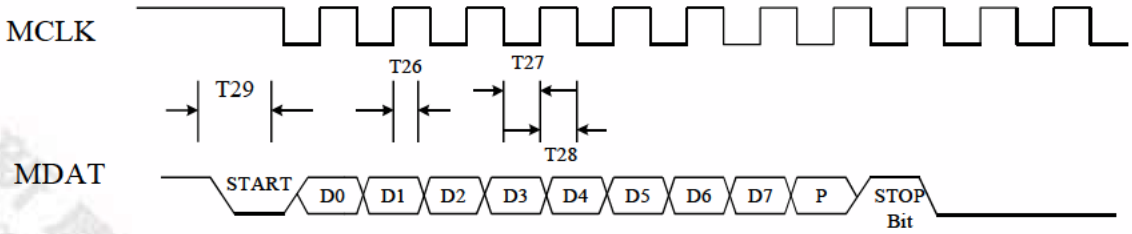
25.9.20 Send Data to Mouse

Send Data to Mouse



25.9.21 Receive Data from Mouse

Receive Data from Mouse



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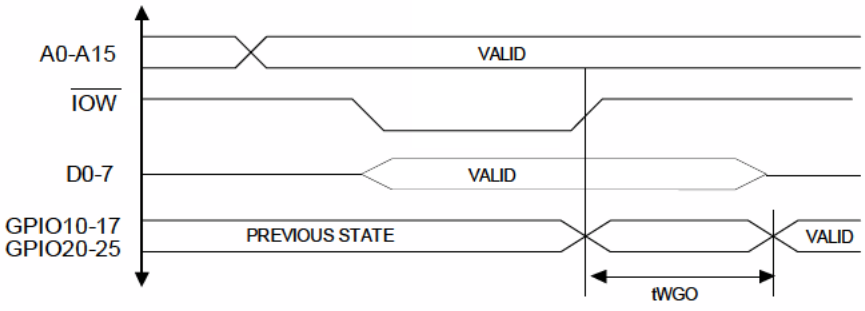
25.10 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300(Note 1)	ns
t_{SWP}	SWITCH pulse width	16		msec

Note: Refer to Microprocessor Interface Timing for Read Timing.

25.10.1 GPIO Write Timing

GPIO Write Timing diagram



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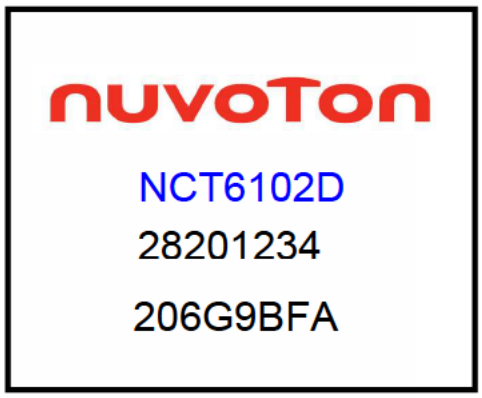
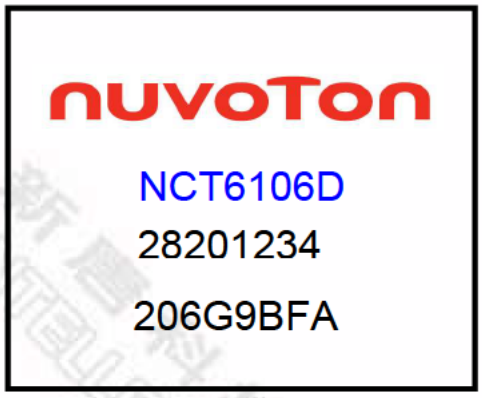
26. TOP MARKING SPECIFICATIONS



1st line: Nuvoton logo
2nd line: part number NCT6102D
3rd line: wafer production series lot number 28201234
4th line: tracking code 206G9BFA
206: packages made in 2012, week 06
G: assembly house ID; G means GR, A means ASE, etc
9: code version; 9 means code 009
B: IC revision; A means version A; B means version B, and C means version C
FA: Nuvoton internal use



1st line: Nuvoton logo
2nd line: part number NCT6106D
3rd line: wafer production series lot number 28201234
4th line: tracking code 206G9BFA
206: packages made in 2012, week 06
G: assembly house ID; G means GR, A means ASE, etc
9: code version; 9 means code 009
B: IC revision; A means version A; B means version B, and C means version C
FA: Nuvoton internal use

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27. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
NCT6102D	128Pin LQFP (Green package)	-40℃~+85℃
NCT6106D	128Pin LQFP (Green package)	-40℃~+85℃

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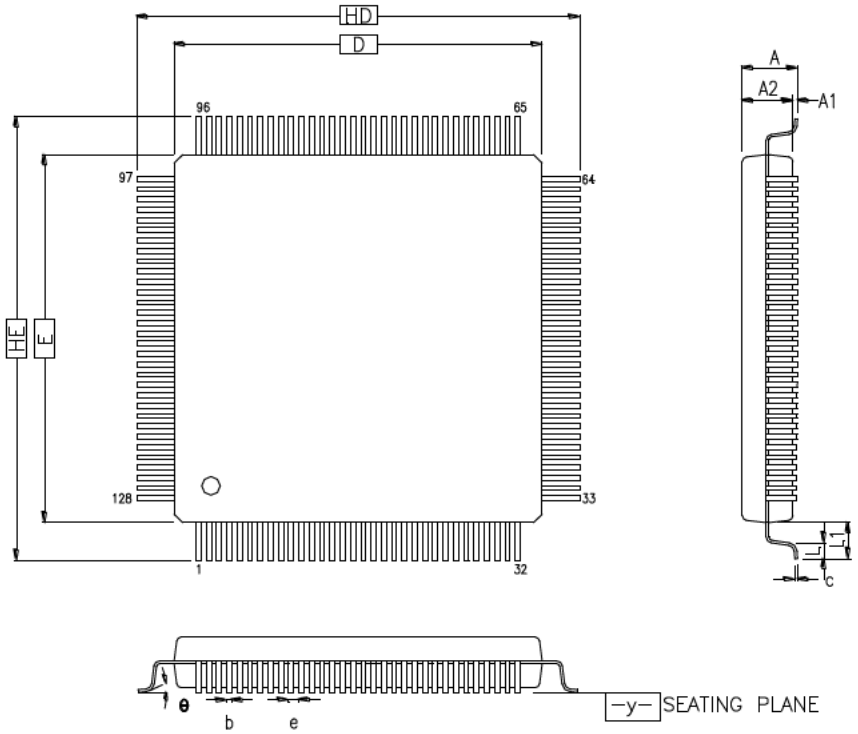
28. PACKAGE SPECIFICATION



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

128-pin LQFP (14x14x1.4mm)

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29. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.1	08/03/2010	N.A.	Draft datasheet
0.5	06/27/2011	N.A.	Preliminary datasheet
0.6	09/29/2011	N.A.	Move PCHVSB from pin #78 to pin #69
1.0	01/11/2012	N.A.	Add part number NCT6102D Update GPIO7 description

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