

FDMS001N025DSD

PowerTrench® Power Clip

25 V Asymmetric Dual N-Channel MOSFET

General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET (Q2) have been designed to provide optimal power efficiency.

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 3.25 m Ω at V_{GS} = 10 V, I_D = 19 A
- Max $r_{DS(on)}$ = 4 m Ω at V_{GS} = 4.5 V, I_D = 17 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 0.92 m Ω at V_{GS} = 10 V, I_D = 38 A
- Max $r_{DS(on)}$ = 1.20 m Ω at V_{GS} = 4.5 V, I_D = 34 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

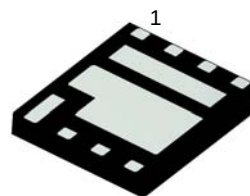
Applications

- Computing
- Communications
- General Purpose Point of Load

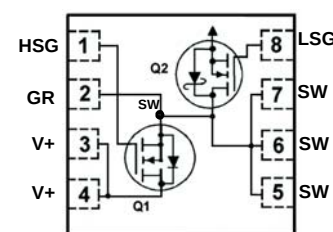
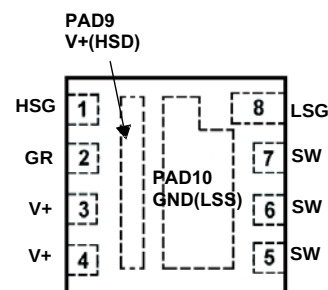


ON Semiconductor®

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PQFN8
POWER CLIP
CASE 483AR



PIN ASSIGNMENT

Pin	Name	Description
1	HSG	High Side Gate
2	GR	Gate Return
3,4,9	V+(HSD)	High Side Drain
5,6,7	SW	Switching Node, Low Side Drain
8	LSG	Low Side Gate
10	GND(LSS)	Low Side Source

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

Table 1. MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	25 (Note 1)	25	V
V_{GS}	Gate to Source Voltage	+16/-12V	+16/-12V	V
I_D	Drain Current –Continuous $T_C = 25^\circ\text{C}$ (Note 2)	69	165	A
	–Continuous $T_C = 100^\circ\text{C}$ (Note 2)	43	104	
	–Continuous $T_A = 25^\circ\text{C}$	19 (Note 7a)	38 (Note 7b)	
	–Pulsed $T_A = 25^\circ\text{C}$ (Note 3)	381	1240	
E_{AS}	Single Pulse Avalanche Energy (Note 4)	121	337	mJ
P_D	Power Dissipation for Single Operation $T_C = 25^\circ\text{C}$	26	42	W
	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	2.1 (Note 7a)	2.3 (Note 7b)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The continuous V_{DS} rating is 25 V; However, a pulse of 30 V peak voltage for no longer than 100 ns duration at 600 KHz frequency can be applied.
2. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.
3. Pulsed I_D please refer to Figure 11 and Figure 24 SOA graphs for more details.
4. Q1: E_{AS} of 121 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3\text{ mH}$, $I_{AS} = 9\text{ A}$, $V_{DD} = 25\text{ V}$. 100% tested at $L = 0.1\text{ mH}$, $I_{AS} = 29\text{ A}$.
Q2: E_{AS} of 337 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3\text{ mH}$, $I_{AS} = 15\text{ A}$, $V_{DD} = 25\text{ V}$. 100% tested at $L = 0.1\text{ mH}$, $I_{AS} = 48\text{ A}$.

Table 2. THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.9	3.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60 (Note 7a)	55 (Note 7b)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130 (Note 7c)	120 (Note 7d)	

Table 3. ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	Q1 Q2	25 25			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, referenced to 25°C $I_D = 10\text{ mA}$, referenced to 25°C	Q1 Q2		15 28		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$ $V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$	Q1 Q2			1 500	μA μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = +16\text{ V}/-12\text{ V}$, $V_{DS} = 0\text{ V}$ $V_{GS} = +16\text{ V}/-12\text{ V}$, $V_{DS} = 0\text{ V}$	Q1 Q2			± 100 ± 100	nA nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 320\text{ }\mu\text{A}$ $V_{GS} = V_{DS}$, $I_D = 1\text{ mA}$	Q1 Q2	0.8 1.0	1.3 1.5	2.5 3.0	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 1\text{ mA}$, referenced to 25°C $I_D = 10\text{ mA}$, referenced to 25°C	Q1 Q2		–4 –3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 19\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 17\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 19\text{ A}$, $T_J = 125^\circ\text{C}$	Q1		2.5 3.0 3.5	3.25 4.0 5.0	m Ω
		$V_{GS} = 10\text{ V}$, $I_D = 38\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 34\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 38\text{ A}$, $T_J = 125^\circ\text{C}$	Q2		0.70 0.92 0.96	0.92 1.20 1.38	

FDMS001N025DSD

Table 3. ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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ON CHARACTERISTICS

g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 19\text{ A}$	Q1		98		S
		$V_{DS} = 5\text{ V}, I_D = 38\text{ A}$	Q2		262		

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	Q1: $V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ Q2: $V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1		1370		pF
			Q2		5105		
C_{oss}	Output Capacitance		Q1		625		pF
			Q2		1810		
C_{rss}	Reverse Transfer Capacitance		Q1		44		pF
			Q2		173		
R_g	Gate Resistance		Q1	0.1	0.4	1.2	Ω
			Q2	0.1	0.3	1.0	

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	Q1: V _{DD} = 13 V, I _D = 19 A, R _{GEN} = 6 Ω Q2: V _{DD} = 13 V, I _D = 38 A, R _{GEN} = 6 Ω		Q1 Q2		8 15	16 26	ns
t _r	Rise Time			Q1 Q2		2 5	10 10	ns
t _{d(off)}	Turn-Off Delay Time			Q1 Q2		22 39	34 62	ns
t _f	Fall Time			Q1 Q2		2 4	10 10	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to 10 V	Q1 V _{DD} = 13 V, I _D = 19 A Q2 V _{DD} = 13 V, I _D = 38 A	Q1 Q2		21 75	30 104	nC
Q _g	Total Gate Charge	V _{GS} = 0 V to 4.5 V		Q1 Q2		9.7 35	14 49	nC
Q _{gs}	Gate to Source Gate Charge			Q1 Q2		2.9 12		nC
Q _{gd}	Gate to Drain “Miller” Charge			Q1 Q2		2.0 7.9		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 19\text{ A}$ (Note 6) $V_{GS} = 0\text{ V}, I_S = 38\text{ A}$ (Note 6)	Q1		0.8	1.2	V
			Q2		0.8	1.2	
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$ (Note 2)	Q1			69	A
			Q2			125	
$I_{S,pulse}$	Diode pulse current	$T_C = 25^\circ\text{C}$ (Note 3)	Q1			381	A
			Q2			1240	
t_{rr}	Reverse Recovery Time	Q1 $I_F = 19\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ Q2 $I_F = 38\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	Q1		27	44	ns
			Q2		39	62	
Q_{rr}	Reverse Recovery Charge		Q1		12	21	nC
			Q2		55	87	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

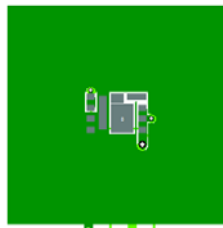
5. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.

6. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

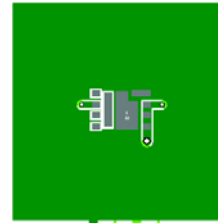
PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS001N025DSD	FDMS001N025DSD	Power Clip 56	13"	12 mm	3000 units

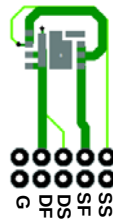
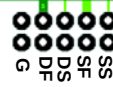
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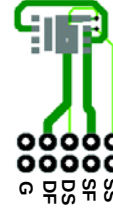
(Note 7a)



(Note 7b)



(Note 7c)



(Note 7d)

7. a) 60°C/W when mounted on a 1 in² pad of 2 oz copper
- b) 55°C/W when mounted on a 1 in² pad of 2 oz copper
- c) 130°C/W when mounted on a minimum pad of 2 oz copper
- d) 120°C/W when mounted on a minimum pad of 2 oz copper

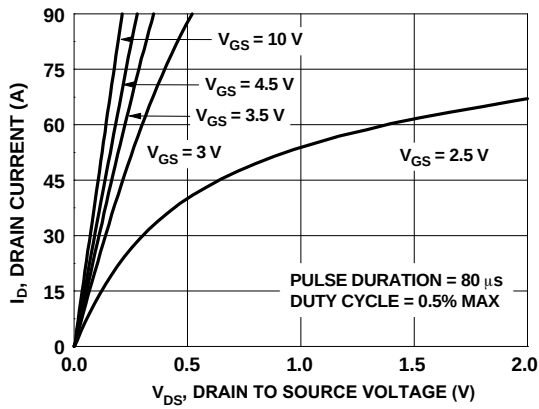
TYPICAL CHARACTERISTICS (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

Figure 1. On Region Characteristics

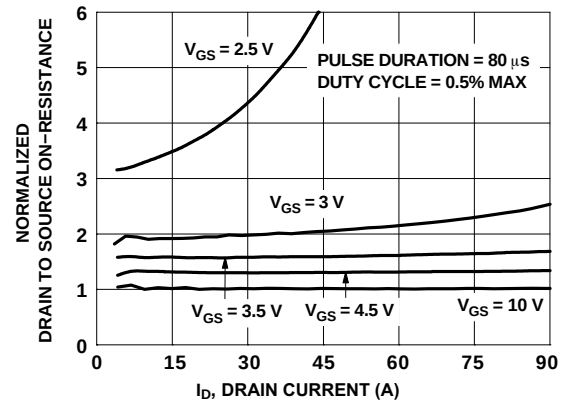


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

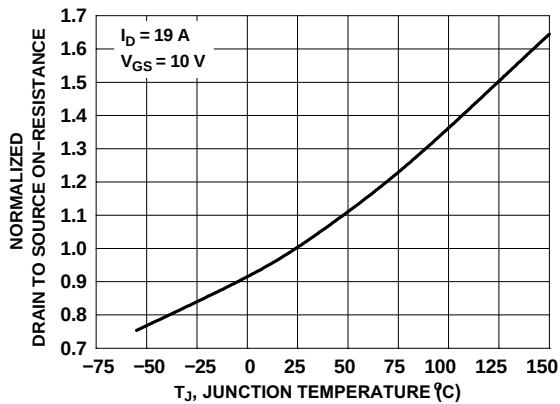


Figure 3. Normalized On Resistance vs. Junction Temperature

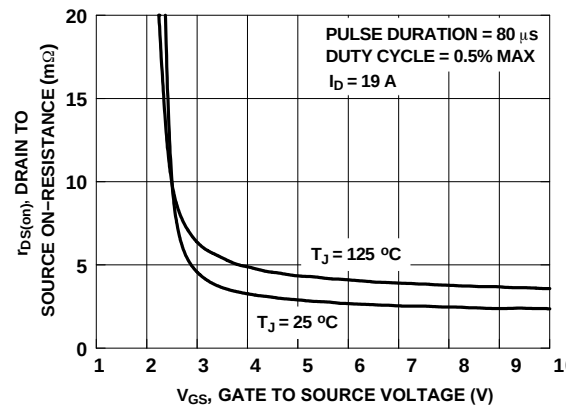


Figure 4. On-Resistance vs. Gate to Source Voltage

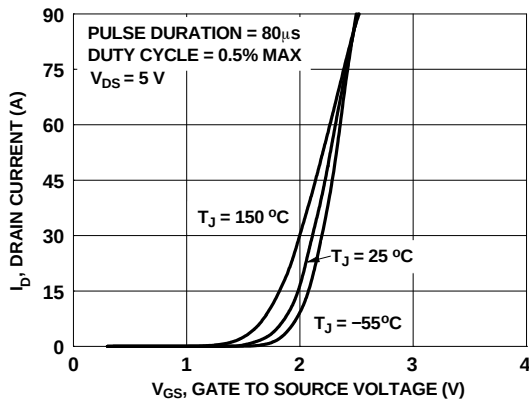


Figure 5. Transfer Characteristics

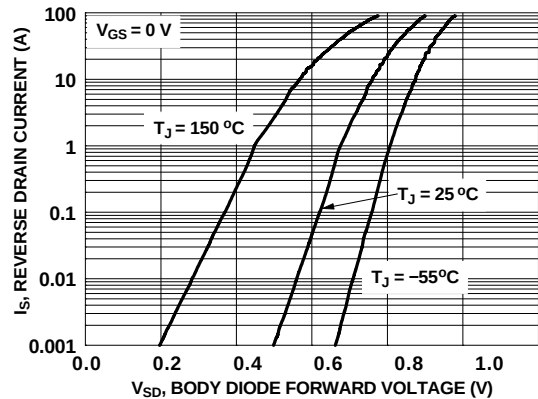


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

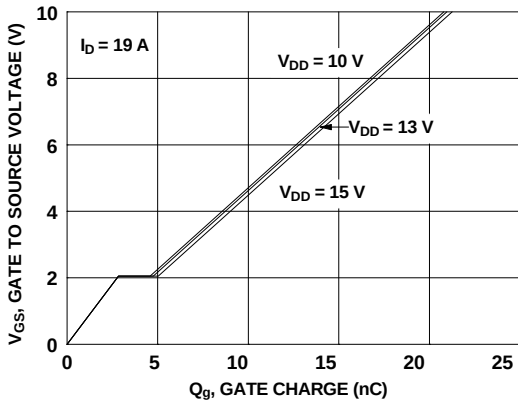


Figure 7. Gate Charge Characteristics

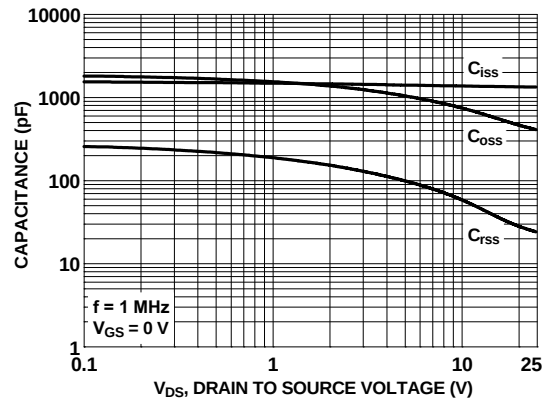


Figure 8. Capacitance vs. Drain to Source Voltage

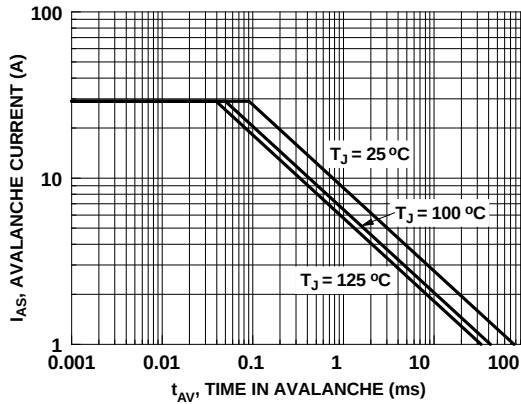


Figure 9. Unclamped Inductive Switching Capability

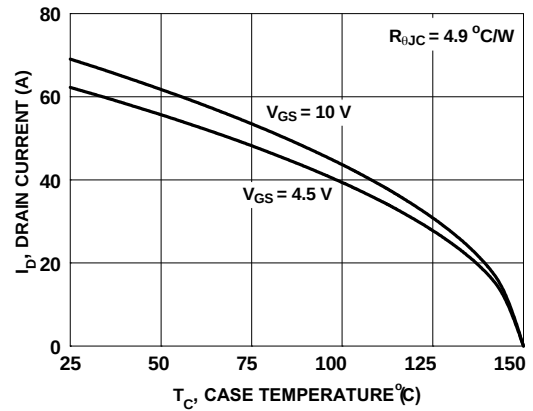


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

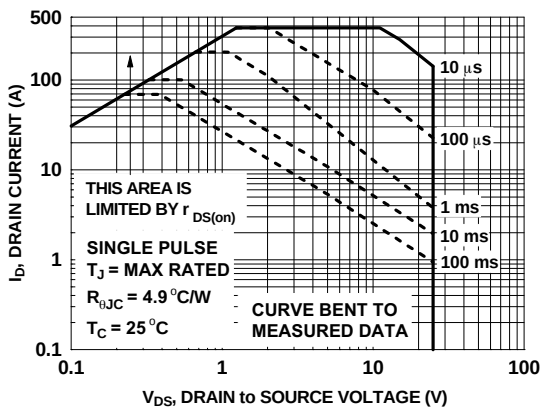


Figure 11. Forward Bias Safe Operating Area

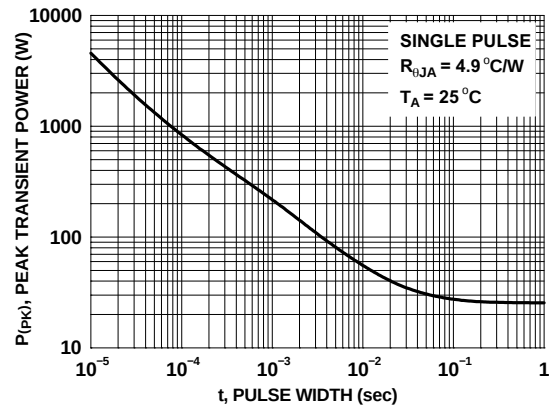


Figure 12. Single Pulse Maximum Power Dissipation

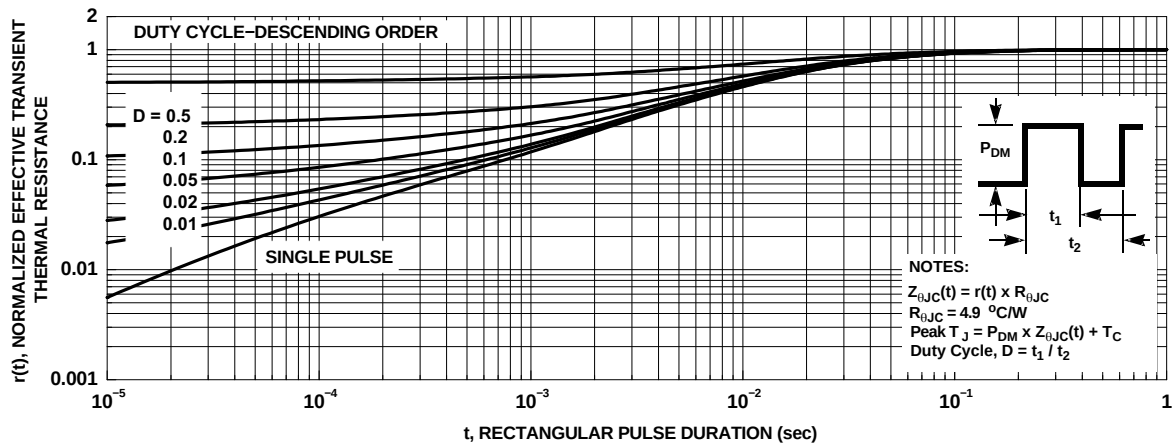
TYPICAL CHARACTERISTICS (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

Figure 13. Junction-to-Case Transient Thermal Response Curve

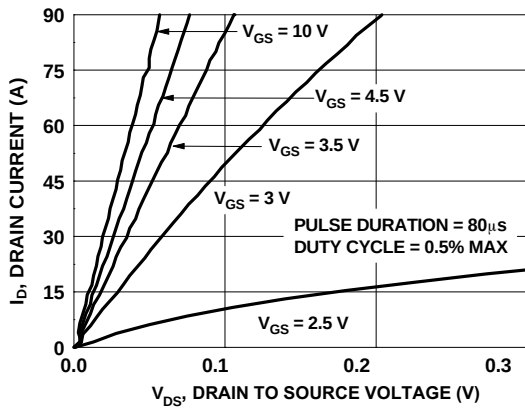
TYPICAL CHARACTERISTICS (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

Figure 14. On Region Characteristics

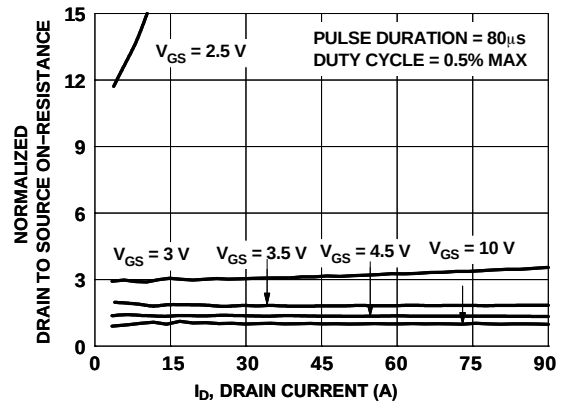


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

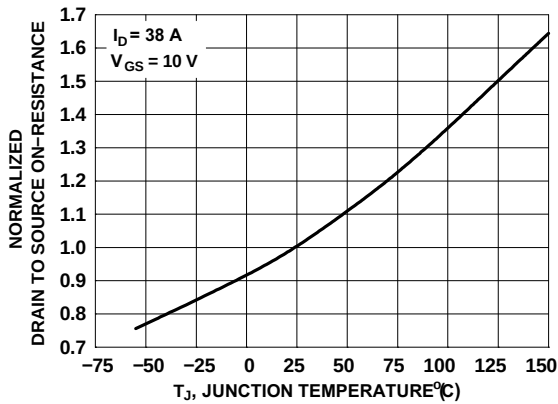


Figure 16. Normalized On Resistance vs. Junction Temperature

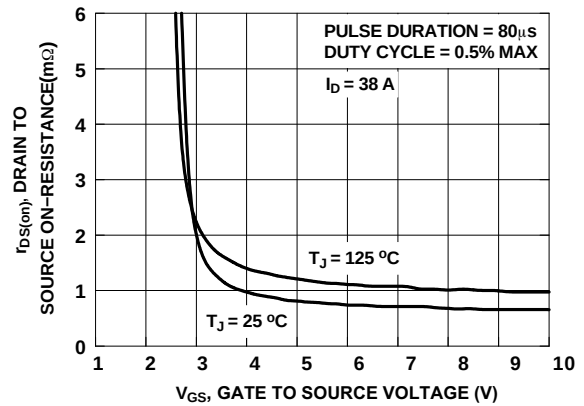


Figure 17. On-Resistance vs. Gate to Source Voltage

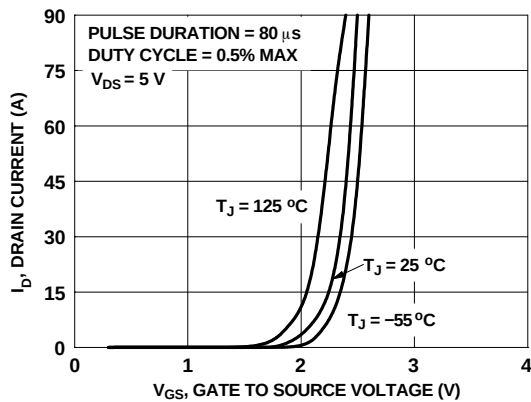


Figure 18. Transfer Characteristics

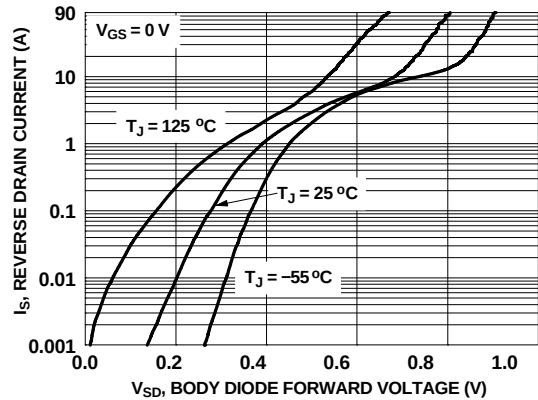


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

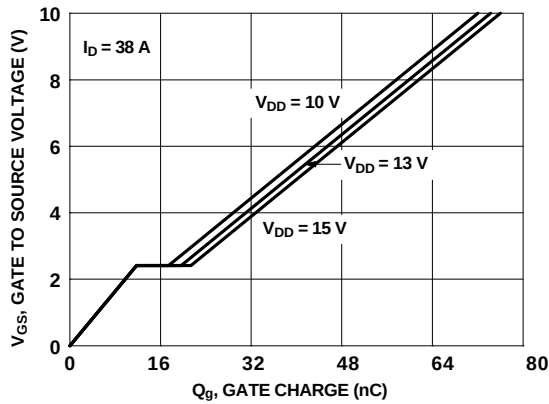


Figure 20. Gate Charge Characteristics

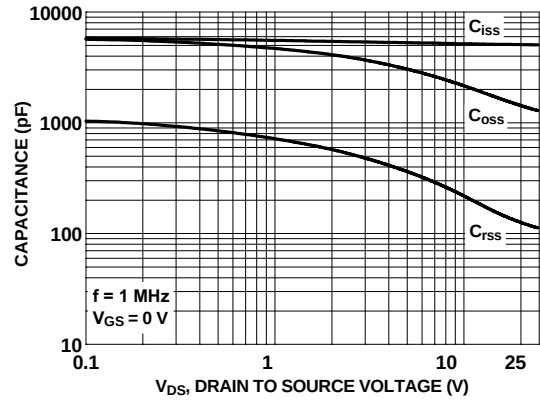


Figure 21. Capacitance vs. Drain to Source Voltage

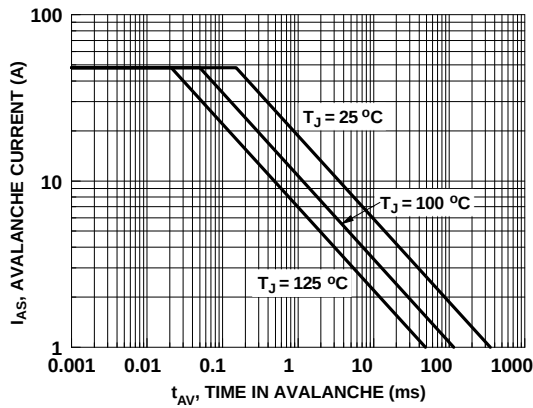


Figure 22. Unclamped Inductive Switching Capability

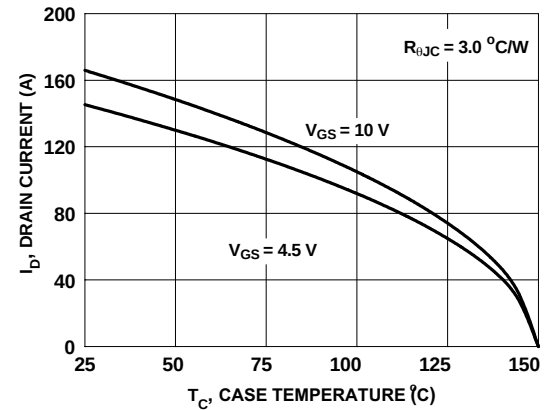


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

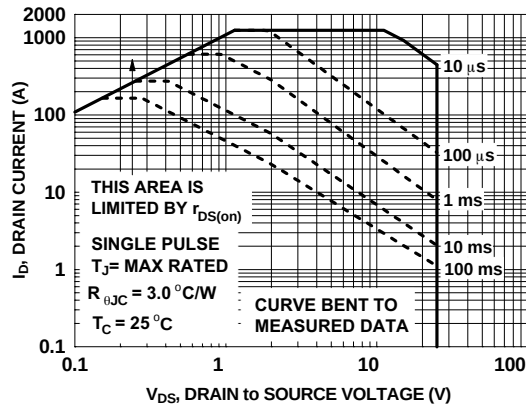


Figure 24. Forward Bias Safe Operating Area

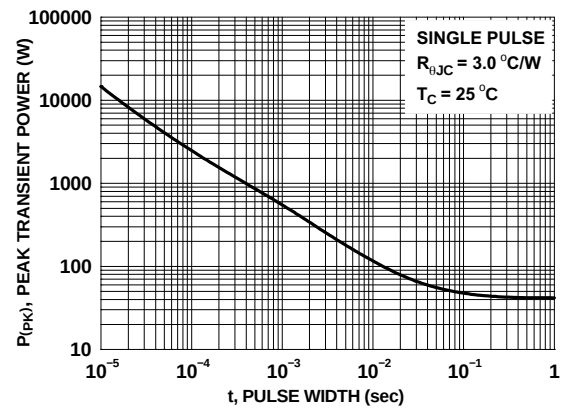


Figure 25. Single Pulse Maximum Power Dissipation

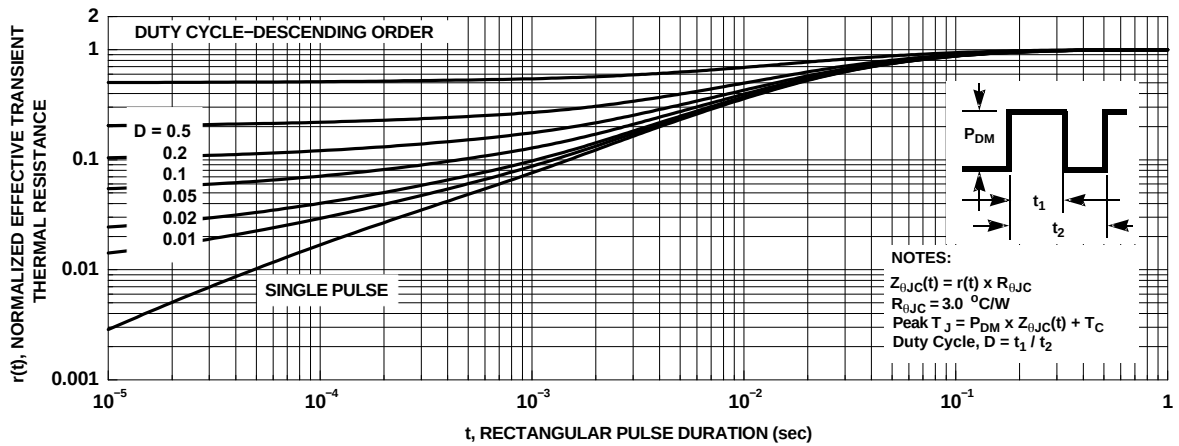
TYPICAL CHARACTERISTICS (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

Figure 26. Junction-to-Case Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (continued)

ON Semiconductor's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS001N025DSD.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

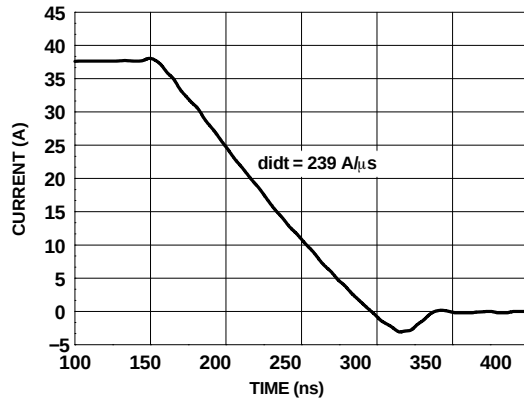


Figure 27. FDMS001N025DSD SyncFET Body Diode Reverse Recovery Characteristic

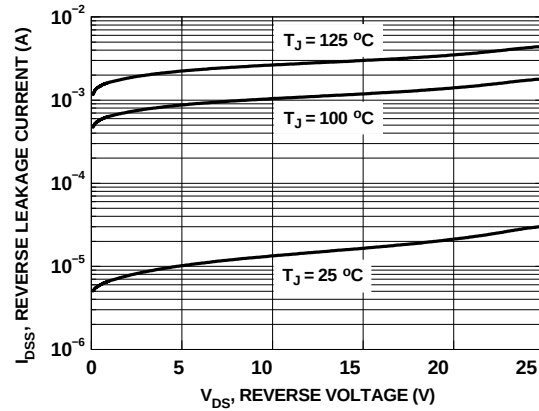
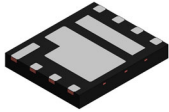


Figure 28. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage

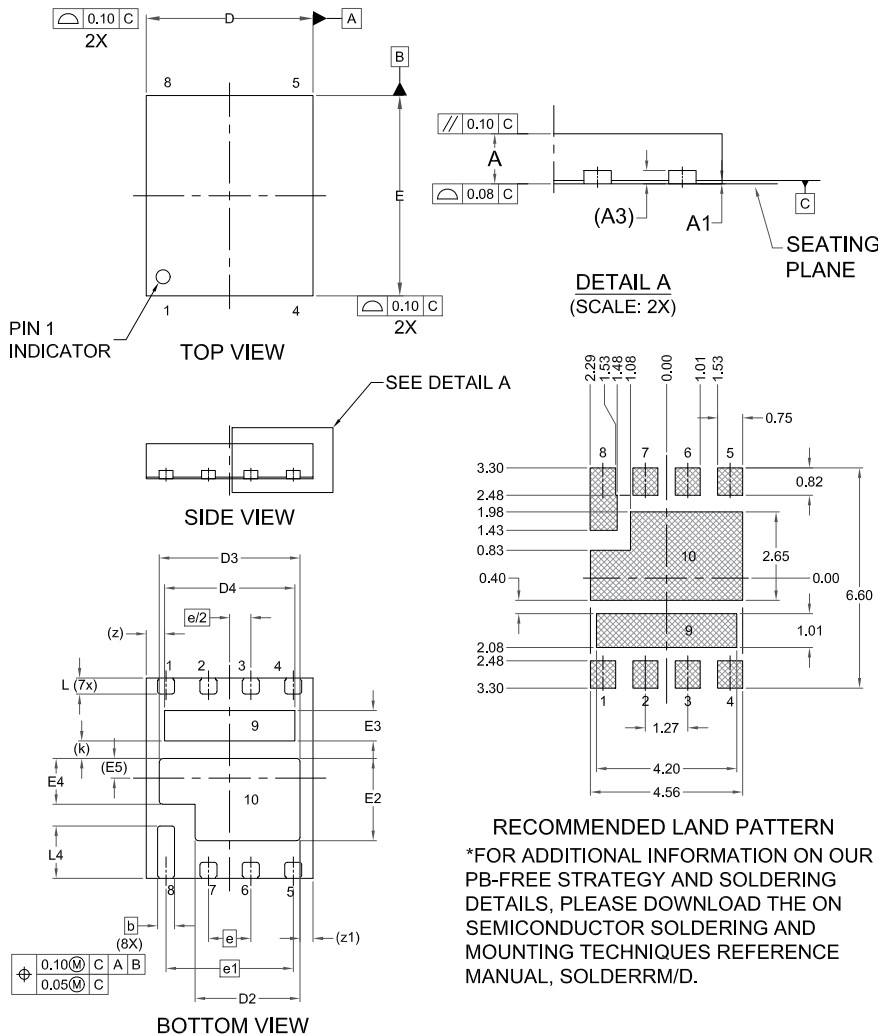


PQFN8 5.00x6.00x0.75, 1.27P
CASE 483AR
ISSUE D

DATE 06 NOV 2023

NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.51 BSC		
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
D3	4.12	4.22	4.32
D4	3.80	3.90	4.00
E	5.90	6.00	6.10
E2	2.36	2.46	2.56
E3	0.81	0.91	1.01
E4	1.27	1.37	1.47
E5	0.59 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
k	0.52 REF		
L	0.38	0.48	0.58
L4	1.47	1.57	1.67
z	0.55 REF		
z1	0.39 REF		

RECOMMENDED LAND PATTERN
*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING
DETAILS, PLEASE DOWNLOAD THE ON
SEMICONDUCTOR SOLDERING AND
MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D.

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DESCRIPTION:	PQFN8 5.00x6.00x0.75, 1.27P	PAGE 1 OF 1

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