AzureWave Technologies, Inc.

AW-XM369

IEEE 802.11 2X2 WiFi 6 SU and MU-MIMO DBC Wireless LAN + Bluetooth 5.3 Combo LGA Module

Datasheet

Rev. B

DF

For Standard

Features

WLAN

- Support 2x2 802.11 a/b/g/n/ac/ax
- Dual bands: 2.4 GHz and 5 GHz
- Support 20/40/80 MHz channel Bandwidths.
- 5GHz PHY data rates up to 1.2 Gbps
- 2.4 GHz PHY data rates up to 458 Mbps
- Uplink and downlink OFDMA and MU-MIMO
- Instantaneous 0-DFS

Bluetooth

- Bluetooth 5.3
- Bluetooth class 2
- Bluetooth class 1
- PCM interface for voice applications
- 2Mbit/s LE
- Long range
- LTE/MWS coexistence
- 2 x wide band speech (WBS) calls
- Security: AES

WLAN Dual-Radios

- Dual, independent direct-conversion WLAN radios (with dual-MACs and dual-Basebands) supports true, simultaneous WLAN network operation at 2 different frequency bands,

Revision History

Document NO: R2-2369-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2020/01/21	DCN022547	● Draft version	Renton Tao	N.C Chen
B	2021/06/21	DCN024414	● Modify datasheet form	Roger Liu	N.C Chen
			●		
			●		
			●		

AzureWave Technologies, Inc.

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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the IEEE 802.11a/b/g/n/ac/ax Concurrent Dual WiFi(CDW) and BT, combo module – **AW-XM369.** With High Efficiency Wireless(HEW) and backward compatible with 802.11ac technologies integrated into a module, AW-XM369 provides the best and most convenient SMT process. The module is targeted to mobile devices including, Navigation , Infotainment , Telematics , Remote diagnostics, Hands-free audio, User interface mirroring which need convenient SMT process, low power consumption.

By using AW-XM369, the customers can easily integrate the Wi-Fi, BT, by a combo module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11a/b/g/n/ac/ax standard, the AW-XM369 uses **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-XM369.

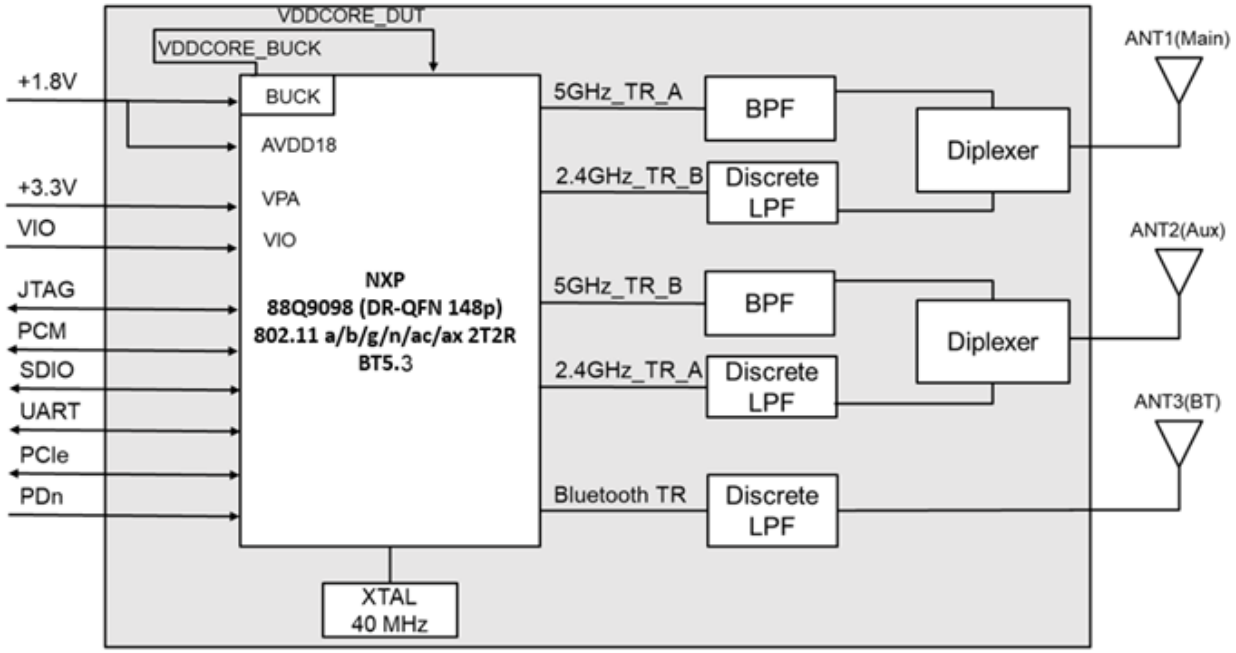
The AW-XM369 supports standard interface **PCIe or SDIO for WLAN** interface connection and High-Speed **UART for BT** interface connection. AW-XM369 provide a flexible design for easy integration into demanding automotive applications..

Scenario	2.4GHz Band			5GHz Band		
	Mode	Technology	BW	Mode	Technology	BW
1	2x2	802.11n	40MHz	2x2	802.11ax	80MHz
2	2x2	802.11n	40MHz	1x1 1Rx	802.11ax Zero Wait DFS	80MHz 80MHz
3	2x2	802.11ax	40MHz	2x2	802.11ac	40MHz

Concurrent 2.4GHz and 5GHz modes supported table

1.2 Block Diagram

A simplified block diagram of the AW-XM369 module is depicted in the figure below.



AW-XM369 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 2X2 WiFi 6 MIMO Wireless LAN + Bluetooth 5.3 Combo LGA Module
Major Chipset	NXP 88Q9098 (DR-QFN 148pin)
Host Interface	WiFi + BT ● PCIe2.0 + UART ● SDIO3.0 + UART (For Host configuration interface, please refer to section 2.3)
Dimension	20 mm X 18 mm x 2.8 mm(Max) (Tolerance remarked in mechanical drawing)
Form factor	LGA module, 98 pins
Antenna	2T2R for WiFi, standalone antenna for BT ANT1(Main)：WiFi_A → TX/RX ANT2(Aux)：WiFi_B→ TX/RX ANT3(BT): BT
Weight	0.0019kg

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax 2T2R
WLAN VID/PID	
WLAN SVID/SPID	TBD
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM, 256QAM, 1024QAM, OFDMA
Number of Channels	2.4GHz: ■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11 ■ China, Australia, Most European Countries - 1 ~ 13 ■ Japan, 1 ~ 13

<table>
<tr><td></td><td>5GHz:
■ USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165
■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140
■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165</td></tr>
<tr><td>Output Power
(RF specifications are at 25℃)</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps) @EVM<35%</td><td>16</td><td>18</td><td>20</td><td>dBm</td></tr>
<tr><td>11g (54Mbps) @EVM≦-27 dB</td><td>15.5</td><td>17</td><td>18.5</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-28 dB</td><td>14.5</td><td>16</td><td>17.5</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-28 dB</td><td>14.5</td><td>16</td><td>17.5</td><td>dBm</td></tr>
<tr><td>11ax (HE20 MCS11) @EVM≦-35 dB</td><td>12.5</td><td>14</td><td>15.5</td><td>dBm</td></tr>
<tr><td>11ax (HE40 MCS11) @EVM≦-35 dB</td><td>12.5</td><td>14</td><td>15.5</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps) @EVM≦-27 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-28 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-28 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8) @EVM≦-31 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
<tr><td>11ac(VHT40 MCS9) @EVM≦-32 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
<tr><td>11ac(VHT80 MCS9) @EVM≦-32 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11) @EVM≦-35 dB</td><td>10</td><td>12</td><td>14</td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11) @EVM≦-35 dB</td><td>10</td><td>12</td><td>14</td><td>dBm</td></tr>
<tr><td>11ax(HE80 MCS11) @EVM≦-35 dB</td><td>10</td><td>12</td><td>14</td><td>dBm</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>Receiver Sensitivity (RF specifications are at 25℃)</td><td>
2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps)</td><td>-</td><td>-88</td><td>-85</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>-</td><td>-75</td><td>-72</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-72</td><td>-69</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-70</td><td>-66</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11)</td><td>-</td><td>-62</td><td>-58</td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11)</td><td>-</td><td>-59</td><td>-53</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps)</td><td>-</td><td>-72</td><td>-68</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-70</td><td>-66</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-68</td><td>-64</td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8)</td><td>-</td><td>-65</td><td>-61</td><td>dBm</td></tr>
<tr><td>11ac(VHT40 MCS9)</td><td>-</td><td>-62</td><td>-58</td><td>dBm</td></tr>
<tr><td>11ac(VHT80 MCS9)</td><td>-</td><td>-59</td><td>-55</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11)</td><td>-</td><td>-60</td><td>-56</td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11)</td><td>-</td><td>-57</td><td>-53</td><td>dBm</td></tr>
<tr><td>11ax(HE80 MCS11)</td><td>-</td><td>-55</td><td>-51</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Data Rate</td><td>■ 802.11b: 1, 2, 5.5, 11Mbps
■ 802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
■ 802.11n: up to 150Mbps-single
■ 802.11n: up to 300Mbps-2x2 MIMO
■ 802.11ac:up to 192.6Mbps (20MHz channel)
■ 802.11ac:up to 400Mbps (40MHz channel)
■ 802.11ac:up to 866.7Mbps (80MHz channel)
■ 802.11ax:2.4GHz up to 458Mbps, 5GHz up to 1.2Gbps</td></tr>
<tr><td>Security</td><td>WiFi: WPA/WPA2/WPA3</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

Features	Description
Bluetooth Standard	Bluetooth 5.3
Bluetooth VID/PID	N/A
Frequency Rage	2402MHz~2483MHz
Modulation	Header GFSK Payload 2M: π/4-DQPSK

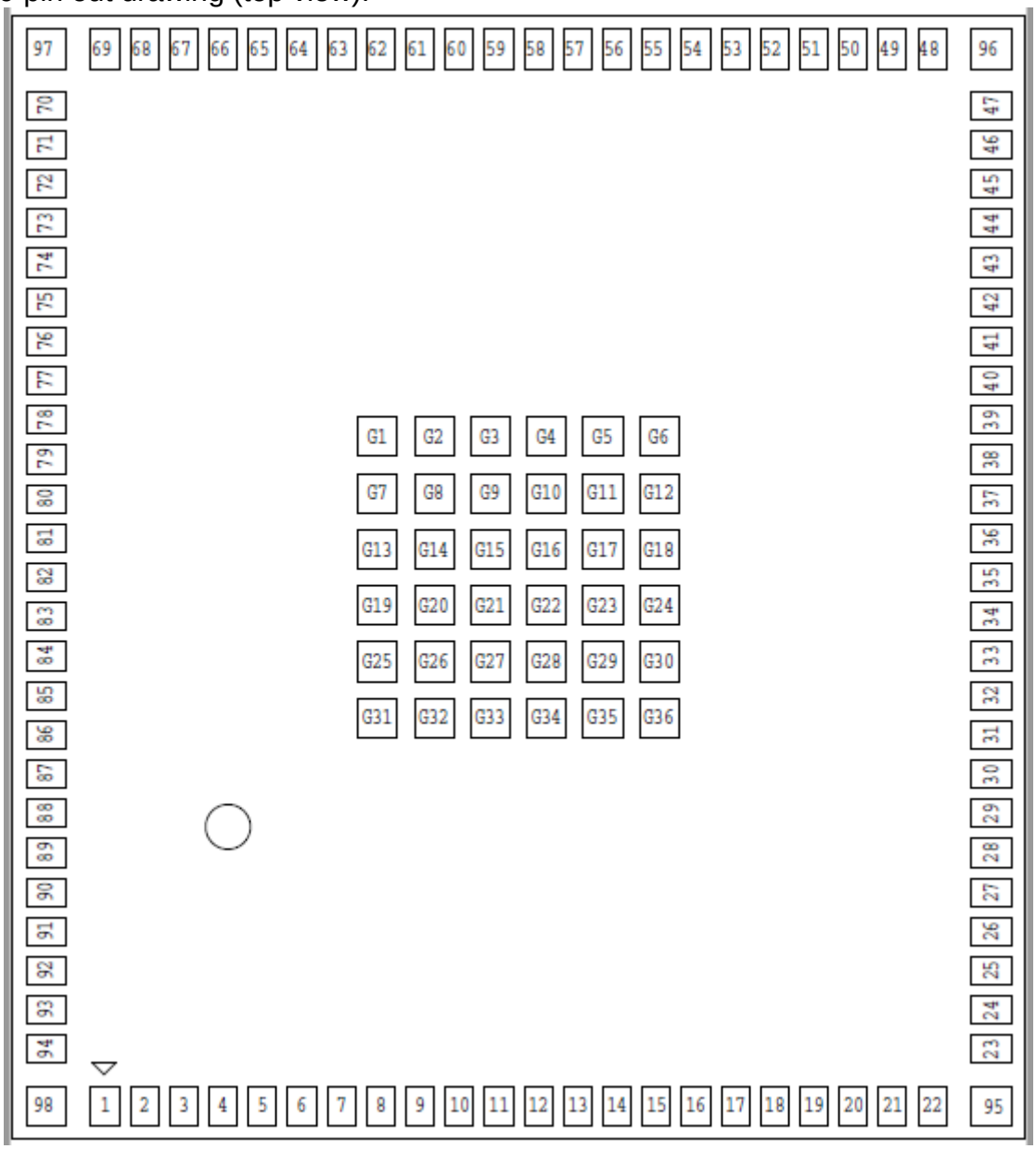
	Payload 3M: 8DPSK				
Output Power		Min	Typ	Max	Unit
	BDR	0	2	4	dBm
	EDR	0	2	4	dBm
	Low Energy (1MHz)	0	2	4	dBm
	Low Energy (2MHz)	0	2	4	dBm
Receiver Sensitivity		Min	Typ	Max	Unit
	BDR	-	-90	-87	dBm
	EDR	-	-87	-84	dBm
	Low Energy (1MHz)	-	-86	-83	dBm
	Low Energy (2MHz)	-	-85	-82	dBm

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V+-5%
Operating Temperature	-40 ℃~ 85℃
Operating Humidity	less than 85% R.H.
Storage Temperature	-40 ℃~ 125℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	+-2kV
Changed Device Model	+-500V

2.1 Pin Map

AW-XM369 pin out drawing (top view).



2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	PCM_OUT	PCM_OUT, GPIO Mode : GPIO[5].	VDDIO	I/O
2	PCM_CLK	PCM_CLK, GPIO Mode : GPIO[6].	VDDIO	I/O
3	GPIO[1]	GPIO Mode : GPIO[1].	VDDIO	I/O
4	GND	Ground	---	---
5	PCIE_RCLK_P	PCI Express Differential Clock Input—Positive	1V8	I
6	PCIE_RCLK_N	PCI Express Differential Clock Input—Negative	1V8	I
7	GND	Ground	---	---
8	PCIE_TX_P	PCI Express Transmit Data—Positive	1V8	O
9	PCIE_TX_N	PCI Express Transmit Data—Negative	1V8	O
10	GND	Ground	---	---
11	PCIE_RX_N	PCI Express Receive Data—Negative	1V8	I
12	PCIE_RX_P	PCI Express Receive Data—Positive	1V8	I
13	GND	Ground	---	---
14	DNC	DNC	---	---
15	DNC	DNC	---	---
16	GND	Ground	---	---
17	SD_DAT[3]	SDIO Data line Bit[3]	VIO_SD	I/O
18	SD_DAT[2]	SDIO Data line Bit[2]	VIO_SD	I/O
19	SD_DAT[1]	SDIO Data line Bit[1]	VIO_SD	I/O
20	SD_DAT[0]	SDIO Data line Bit[0]	VIO_SD	I/O
21	SD_CMD	SDIO Command/response (input/output)	VIO_SD	I/O
22	SD_CLK	SDIO Clock input	VIO_SD	I
23	VIO_SD	1.8V/3.3V Digital I/O SDIO Power Supply	1.8 or 3.3V	I
24	GND	Ground	---	---
25	PCIE_PERSTn	PCIe host indication to reset the device (active low)	VIO	I
26	PCIE_CLKREQn	PCIe clock request (active low)	VIO	I/O
27	PCIE_WAKEn	PCIe wake signal (active low)	VIO	I/O
28	PCIE_DISABLEn	PCIe DISABLEn(active low)	VIO	I
29	GND	Ground	---	---
30	UART_RTSn	UART Mode: UART_RTSn (active low)	VDDIO	O
31	UART_CTSn	UART Mode: UART_CTSn (active low)	VDDIO	I
32	UART_RX	UART SIN pin	VDDIO	I
33	UART_TX	UART SOUT.pin	VDDIO	O
34	GPIO[12]	GPIO Mode : GPIO[12].	VDDIO	I/O
35	GPIO[13]	GPIO Mode : GPIO[13].	VDDIO	I/O
36	JTAG_TDO	JTAG_TDO/GPIO[31]	VDDIO	I/O
37	JTAG_TMS	JTAG_TMS/GPIO[29]	VDDIO	I/O
38	JTAG_TDI	JTAG_TDI/GPIO[30]	VDDIO	I/O
39	JTAG_TCK	JTAG_TCK/GPIO[28]	VDDIO	I/O
40	NC	NC	---	floating

41	NC	NC	---	floating
42	NC	NC	---	floating
43	NC	NC	---	floating
44	NC	NC	---	floating
45	NC	NC	---	floating
46	NC	NC	---	floating
47	NC	NC	---	floating
48	ANT3	RF I/O pad for BT	---	I/O
49	GND	Ground	---	---
50	GND	Ground	---	---
51	GND	Ground	---	---
52	ANT2	RF I/O pad for WLAN ANT 2	---	I/O
53	GND	Ground	---	---
54	GND	Ground	---	---
55	GND	Ground	---	---
56	GND	Ground	---	---
57	GND	Ground	---	---
58	GND	Ground	---	---
59	GND	Ground	---	---
60	GND	Ground	---	---
61	GND	Ground	---	---
62	GND	Ground	---	---
63	GND	Ground	---	---
64	GND	Ground	---	---
65	GND	Ground	---	---
66	GND	Ground	---	---
67	GND	Ground	---	---
68	GND	Ground	---	---
69	ANT1	RF I/O pad for WLAN ANT 1	---	I/O
70	3V3	3.3V DC power supply	3.3V	I
71	3V3	3.3V DC power supply	3.3V	I
72	GND	Ground	---	---
73	CON[0]	Firmware Boot Options. See below table*	VIO	I
74	CON[1]	Firmware Boot Options. See below table*	VIO	I
75	CON[2]	Firmware Boot Options. See below table*	VIO	I
76	NC	NC	---	floating
77	NC	NC	---	floating
78	NC	NC	---	floating
79	NC	NC	---	floating
80	NC	NC	---	floating
81	GPIO[18]	GPIO Mode : GPIO[18].	VDDIO	I/O
82	GPIO[19]	GPIO Mode : GPIO[19].	VDDIO	I/O
83	GND	Ground	---	---
84	PDn	Full Power-down input pin (active low)	3V3	I

		0 = full power-down mode 1 = normal mode		
85	GPIO[0]	GPIO Mode : GPIO[0].	VDDIO	I/O
86	GPIO[14]*	CON[4]* / GPIO[14]	VDDIO	I/O
87	GPIO[15]	GPIO Mode : GPIO[15].	VDDIO	I/O
88	GPIO[16]	GPIO Mode : GPIO[16].	VDDIO	I/O
89	PCM_SYNC	PCM_SYNC, GPIO Mode : GPIO[7].	VDDIO	I/O
90	VIO	Digital I/O power supply	1.8 or 3.3V	I
91	GND	Ground	---	---
92	1V8	1.8V DC power supply	1.8V	I
93	1V8	1.8V DC power supply	1.8V	I
94	PCM_DIN	PCM_DIN, GPIO Mode : GPIO[4].	VDDIO	I/O
95	GND	Ground	---	---
96	GND	Ground	---	---
97	GND	Ground	---	---
98	GND	Ground	---	---
G1~36	GND	Ground	---	---

*Due to CON[4] strap function, need to pull down with 51k resistor external

2.3 Host Configuration Interface Table

*Firmware Boot options

Strap Value	WLAN	Bluetooth/LE
000	SDIO	UART
011	PCIe	UART

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3V3	DC supply for the 3.3V input	-	3.3	3.63	V
1V8	DC supply for the 1.8V input		1.8	2.16	
VIO	I/O power supply	-	3.3	3.63	V
		-	1.8	1.98	
VIO_SD	SDIO power supply	-	3.3	3.63	V
		-	1.8	1.98	

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3.3V	DC supply for the 3.3V input	3.14	3.3	3.46	V
1V8	DC supply for the 1.8V input	1.71	1.8	1.89	V
VIO	1.8V/3.3V digital I/O power supply	3.14	3.3	3.46	V
		1.71	1.8	1.89	
VIO_SD	1.8V/3.3V SDIO power supply	3.14	3.3	3.46	V
		1.71	1.8	1.89	

3.3 Digital IO Pin DC Characteristics

3.3.1 1.8V Operation (VIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output high voltage	VIO-0.4	-	-	
V_{OL}	Output low voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.2 3.3V Operation (VIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output High Voltage	VIO-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.3 1.8V Operation (VIO_SD)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO_SD	-	VIO_SD+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO_SD	
V_{OH}	Output High Voltage	VIO_SD-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.4 3.3V Operation (VIO_SD)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO_SD	-	VIO_SD+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3* VIO_SD	
V_{OH}	Output High Voltage	VIO_SD-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.4 Host Interface

3.4.1 SDIO Interface

The AW-XM369 supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-XM369 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the frvice through the use of BARs and a DMA engine.

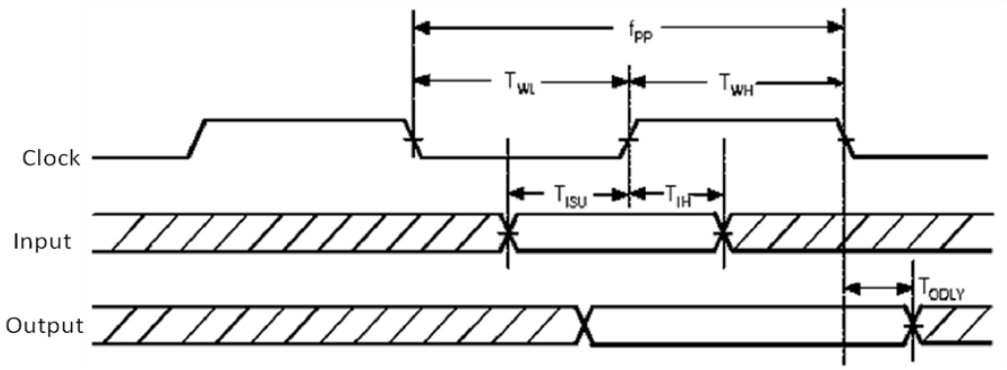
- Support SDIO 3.0 Standard.
- On-chip memory used for CIS.
- Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- Special interrupt register for information exchange.
- Allows card to interrupt host.

SDIO Interface Signals

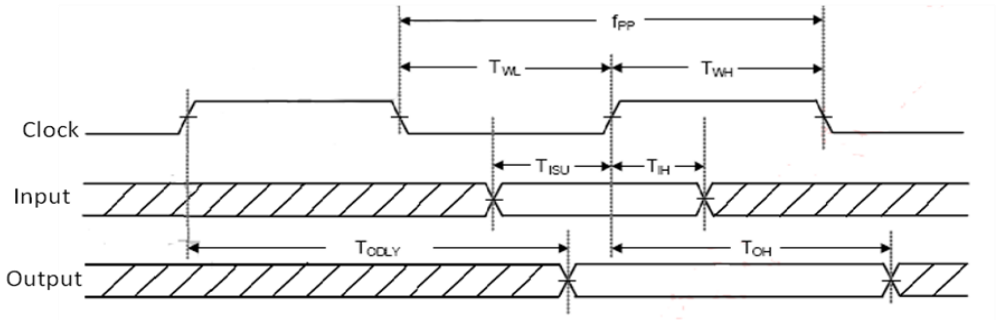
AW-XM369 SDIO Pin Name	Type	Description
SDIO_DATA_CLK	I	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
SDIO_DATA_CMD	I/O	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
SDIO_DATA_3	I/O	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
SDIO_DATA_2	I/O	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
SDIO_DATA_1	I/O	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
SDIO_DATA_0	I/O	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line

3.4.2 SDIO Protocol Timing

3.4.2.1 Default Speed, High-Speed Modes (3.3V)



SDIO protocol timing Diagram - Default mode. (3.3V)

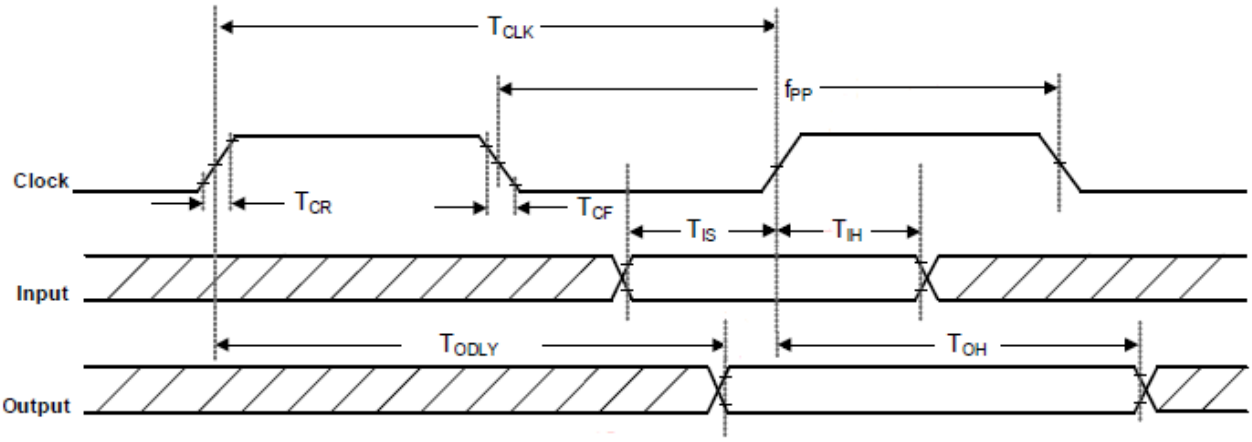


SDIO protocol timing Diagram - High Speed mode. (3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
fpp	CLK Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WH}	CLK High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{WL}	CLK Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time	Normal	--	--	14	ns
	CL ≦ 40pF (1 card)	High Speed	--	--	14	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

SDIO Timing Data – Default Speed / High-Speed modes. (3.3V)

3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)



SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes (up to 100 MHz)(1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR12/25/50	25	-	100	MHz
T_{CLK}	Clock Time	SDR12/25/50	10	-	40	ns
T_{IS}	Input Setup Time	SDR12/25/50	3	-	-	ns
T_{IH}	Input Hold Time	SDR12/25/50	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR ,TCF <2ns(max) at 100MHz CCARD =10pF	SDR12/25/50	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output Delay Time CL ≦ 30pF	SDR12/25/50	-	-	7.5	ns
T_{OH}	Output Hold Time CL =15pF	SDR12/25/50	1.5	-	-	ns

SDIO Timing Data - SDR12/25/50 modes. (1.8V)

3.4.2.3 SDR104 Mode (208MHz) (1.8V)

SDIO Protocol Timing Diagram –SDR104 Mode (208MHz)

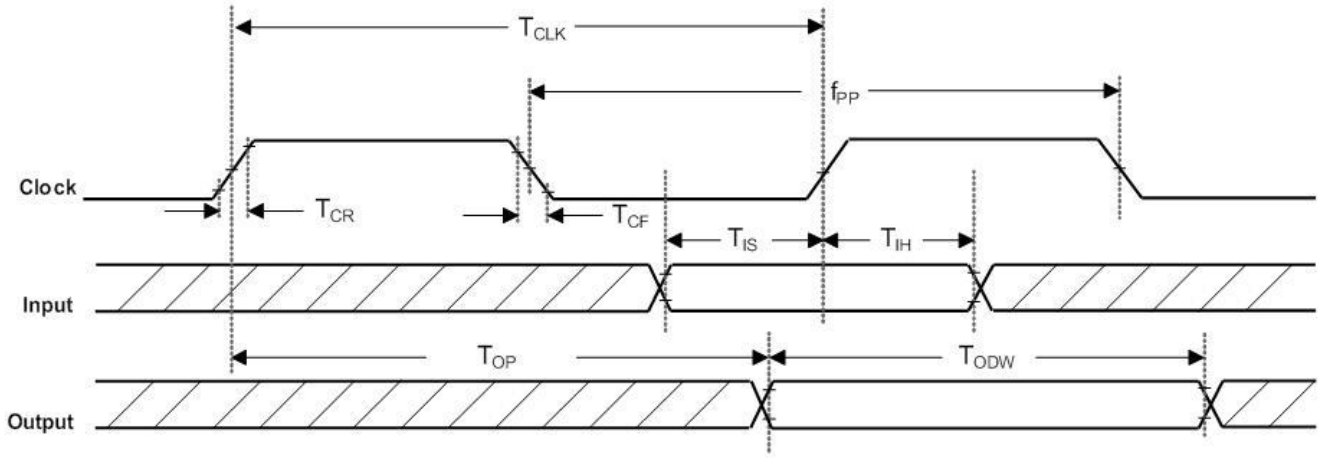
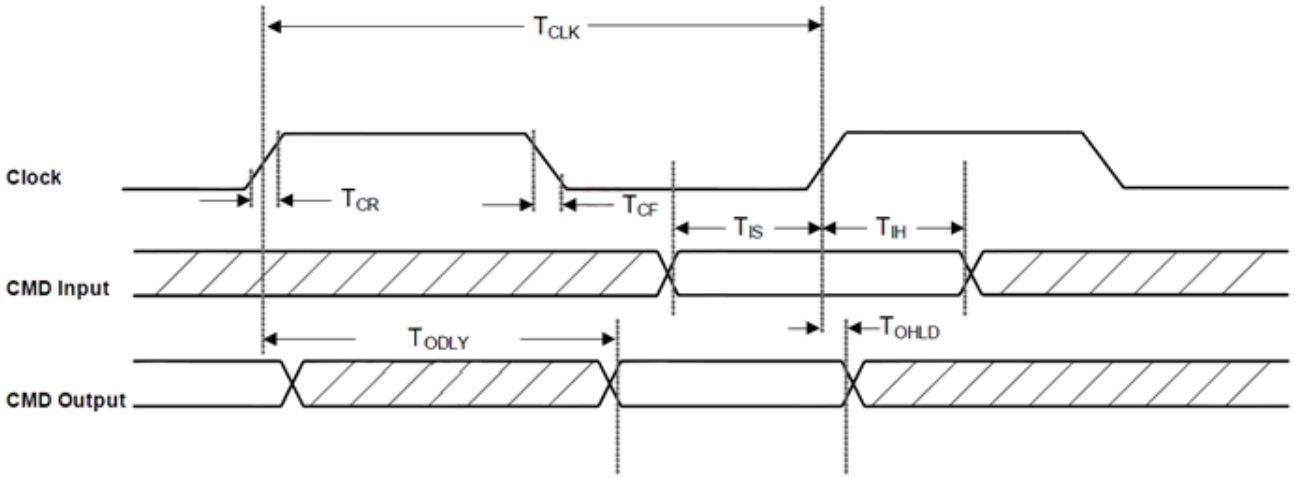


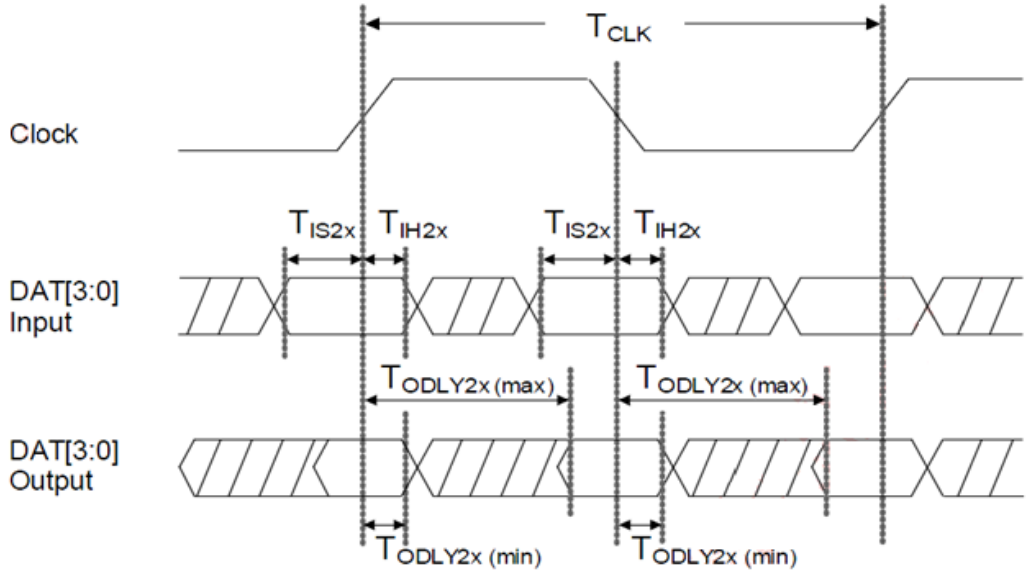
Table shows SDIO Timing Data—SDR104 Mode (208MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{pp}	CLK Frequency	SDR104	0	-	208	MHz
T_{CLK}	Clock Time	SDR104	4.8	-	-	ns
T_{IS}	Input Setup Time	SDR104	1.4	-	-	ns
T_{IH}	Input Hold Time	SDR104	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time T_{CR} ,T_{CF} <0.96ns(max) at 208MHz C_{CARD}=10pF	SDR104	-	-	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	-	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	-	-	ns

3.4.2.4 DDR50 Mode (50MHz) (1.8V)



SDIO CMD Timing Diagram - DDR50 Mode (50 MHz)



SDIO DAT[3:0] Timing Diagram - DDR50 Mode[1] (50 MHz)

[1] In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock						
T_{CLK}	Clock time	DDR50	20	-	-	ns
T_{CR}, T_{CF}	Rise time, fall time	DDR50	-	-	0.2*T_{CLK}	Ns
Clock Duty		DDR50	45	-	55	%
CMD Input						
T_{IS}	Input setup time	DDR50	6	-	-	ns
T_{IH}	Input hold time	DDR50	0.8	-	-	ns
CMD Output						
T_{ODLY}	Output delay time during data transfer mode	DDR50	-	-	13.7	ns
T_{OHLD}	Output hold time	DDR50	1.5	-	-	ns
DAT [3:0] Input						
T_{IS2X}	Input setup time	DDR50	3	-	-	ns
T_{IH2X}	Input hold time	DDR50	0.8	-	-	ns
DAT [3:0] Output						
$T_{ODLY2X(max)}$	Output delay time during data transfer mode	DDR50	-	-	7	ns
$T_{ODLY2X(min)}$	Output hold time	DDR50	1.5	-	-	ns

SDIO Timing Data - DDR50 Mode (50MHz)

3.4.3 PCI Express Interface

3.4.3.1 Differential Tx Output Electricals

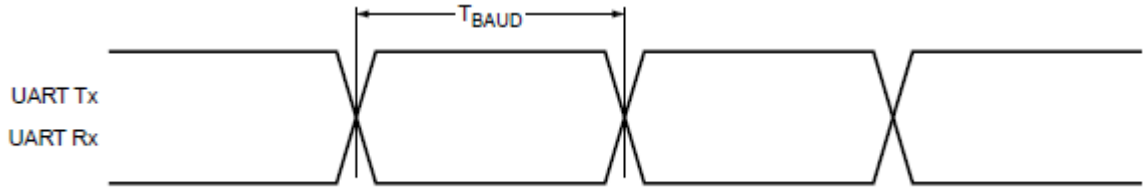
Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval Each UI is 400 ps ±300 PPM. UI does not account for SSC dictated variations.	399.98	400	400.12	ps
V_{Tx_DIFFpp}	Differential peak-to-peak output voltage $V_{Tx\_DIFFpp} = 2*\|V_{TX-D+} - V_{TX-D-}\|$	0.800	--	1.2	V
$V_{Tx\_DE\_RATIO}$	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	db
T_{Rx_EYE}	Minimum Tx eye width	0.75	--	--	UI
$T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$	Maximum time between jitter median and maximum deviation from median	--	--	0.125	UI
T_{Tx_RISE}, T_{Tx_FALL}	D+/D- Tx output rise/fall time	0.125	--	--	UI
$V_{Tx\_CM\_DC\_ACTIVE\_IDLE\_DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0-	-	100	mV
$V_{Tx\_CM\_DC\_LINE\_DELTA}$	Absolute delta of DC common mode voltage between D+ and D-	0-	-	25	mV
$V_{Tx\_IDLE\_DIFFp}$	Electrical idle differential peak output voltage	0	--	20	mV
$V_{Tx\_RCV\_DETECT}$	Voltage change allowed during receiver detection	--	--	600	mV
$V_{Tx\_DC\_CM}$	Tx DC common mode voltage	--	--	3.6	V
I_{Tx_SHORT}	Tx short circuit current limit	--	--	90	mA
$T_{Tx\_IDLE\_MIN}$	Minimum time spent in electrical idle	50	--	--	UI
$T_{Tx\_IDLE\_SET\_TO\_IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	--	--	20	UI
$T_{Tx\_IDLE\_TO\_DIFF\_DATA}$	Maximum time to transition to valid Tx specifications after leaving an electrical idle condition	--	--	20	UI
RL_{Tx_DIFF}	Differential return loss	10	--	--	dB
RL_{Tx_CM}	Common mode return loss	6	--	--	dB
C_{Tx}	AC coupling capacitor	75	--	200	nF
$T_{Crosstalk}$	Crosstalk random timeout	0	--	1	ms

3.4.3.2 Differential Rx Iutput Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations.	399.98	400	400.12	ps
V_{Rx_DIFFpp}	Differential peak-to-peak voltage $V_{Rx\_DIFFpp} = 2*\|V_{RX-D+} - V_{RX-D-}\|$	0.175	--	1.2	V
T_{Rx_EYE}	Minimum receiver eye width	0.4	--	--	UI
$T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$	Maximum time between jitter median and maximum deviation from median	--	--	0.3	UI
$V_{Rx\_CM\_ACp}$	AC peak common mode input voltage	--	--	150	mV
RL_{Rx_DIFF}	Differential return loss	10	--	--	dB
RL_{Rx_CM}	Common mode return loss	6	--	--	dB
$Z_{Rx\_DIFF\_DC}$	DC differential input impedance	80	100	120	Ω
Z_{Rx_DC}	DC input impedance	40	50	60	Ω
$Z_{Rx\_HIGH\_IMP\_DC\_POS}$	Powered down DC input impedance positive	50	--	--	k
$Z_{Rx\_HIGH\_IMP\_DC\_NEG}$	Powered down DC input impedance negative	1	--	--	kΩ
$V_{Rx\_IDLE\_DET\_DIFFpp}$	Electrical idle detect threshold	65	--	175	mV
$T_{Rx\_IDLE\_DET\_DIFF\_ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	--	--	10	ms
L_{Rx_SKEW}	Total skew	---	-2	0	ns

3.4.5.High-Speed UART Interface

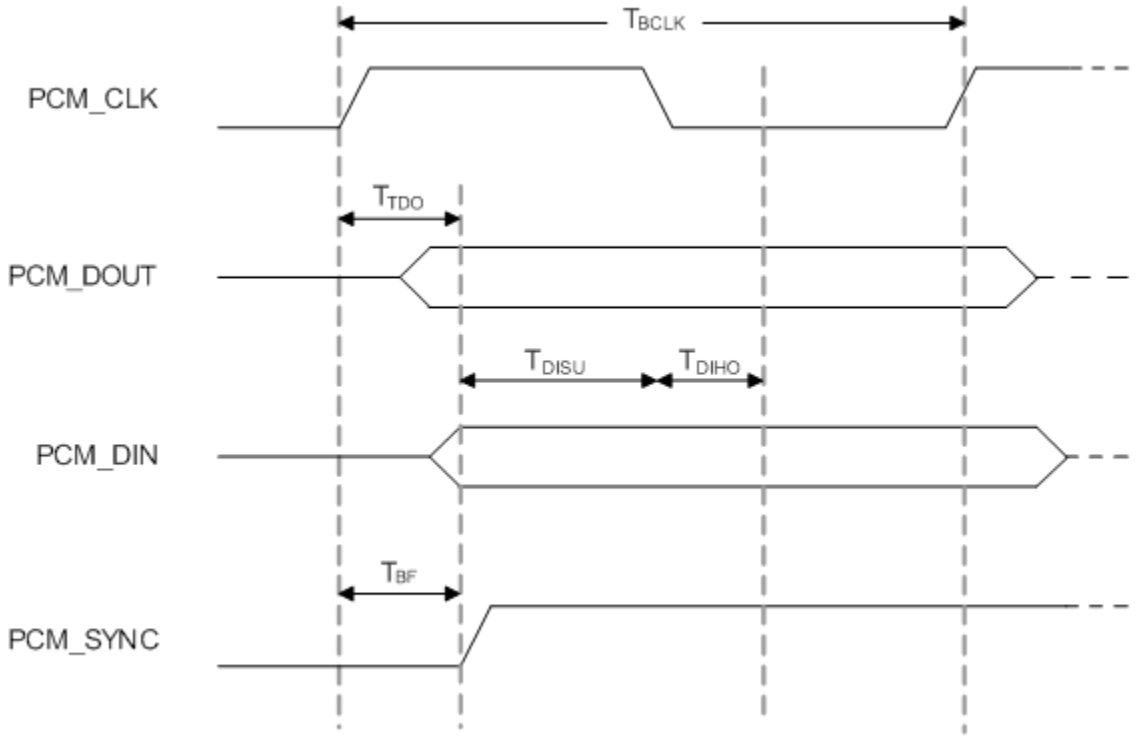
The AW-XM369 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.



Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	26MHz input clock	250	-	-	ns

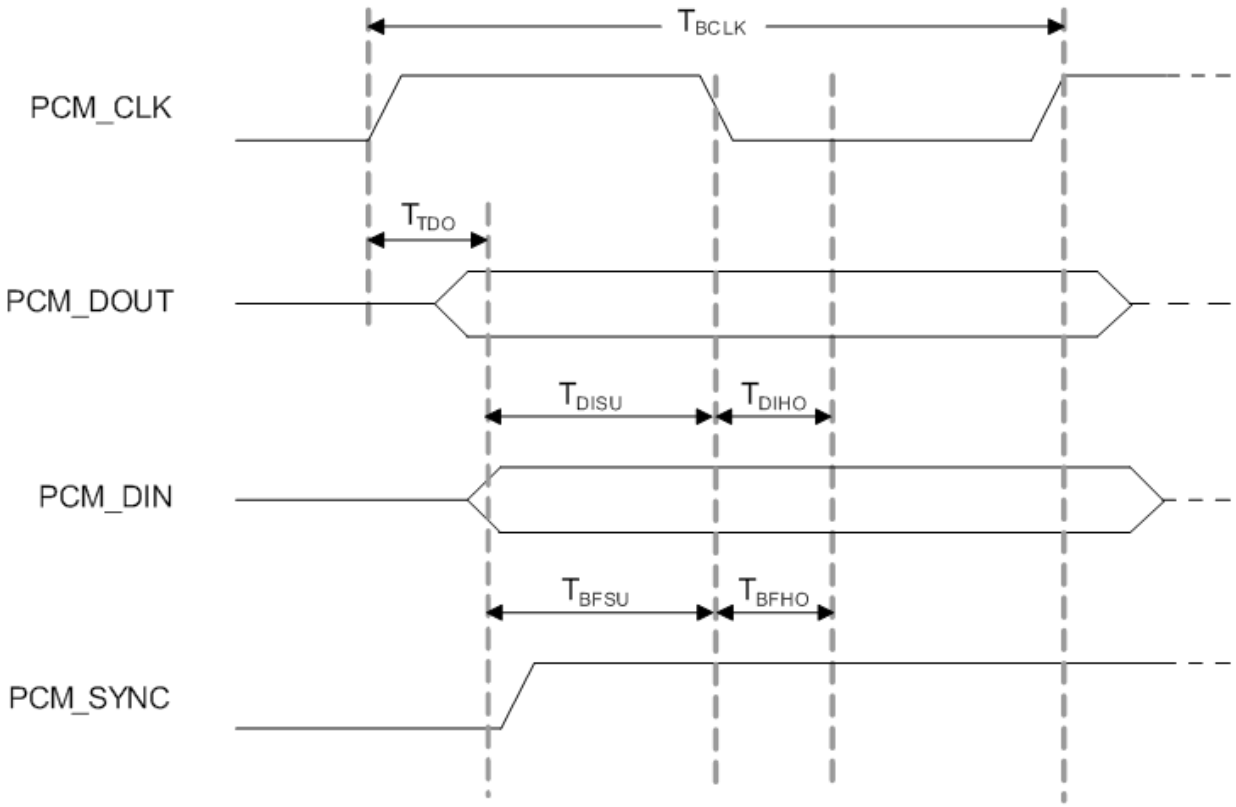
3.4.6 PCM Interface

3.4.6.1 PCM Timing Specification – Master Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

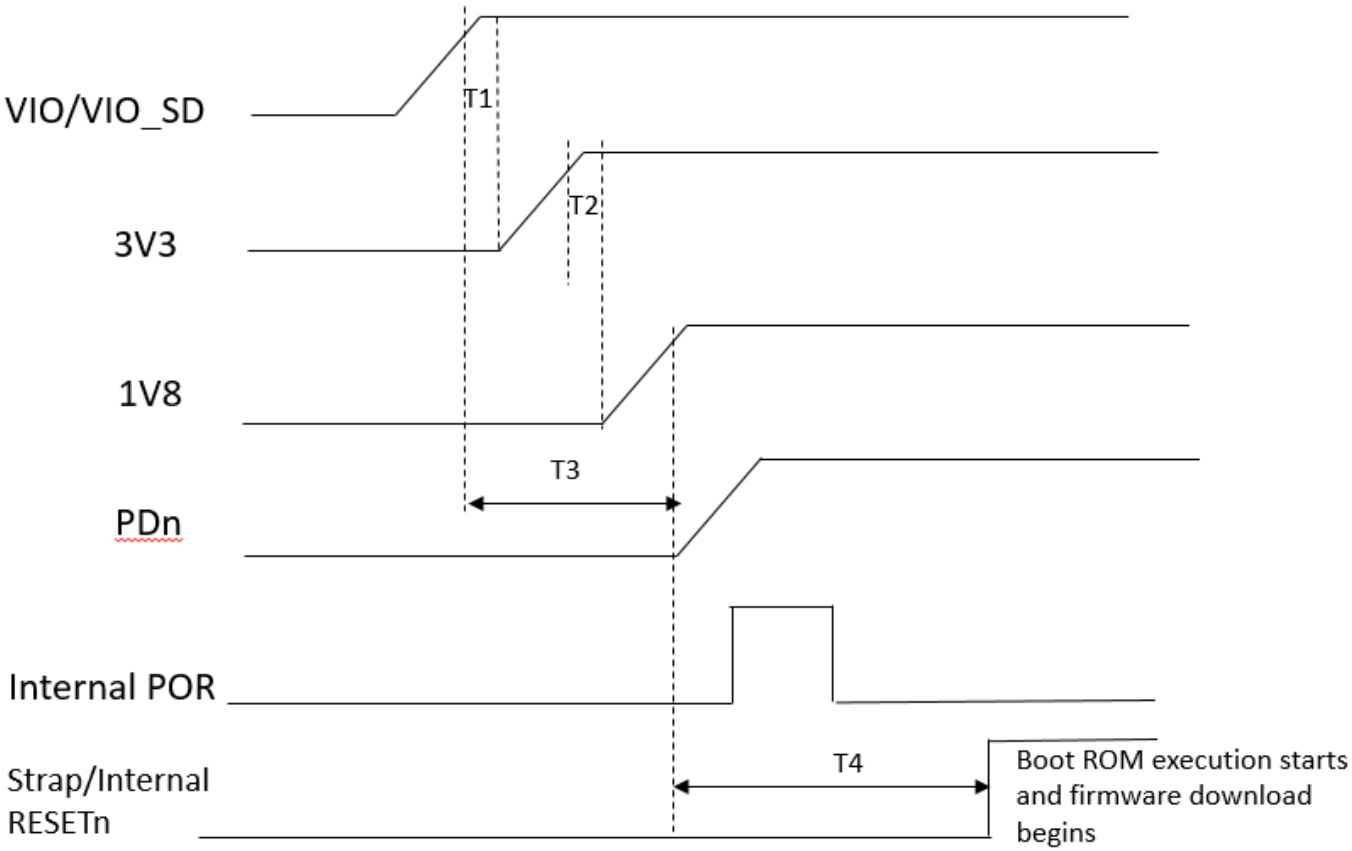
3.4.6.2 PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}			10		--	ns

3.5 Timing Sequence

AW-XM369 power up timing sequence.



Symbol	Description	Min	Typ	Max	Units
T1	Delay from VIO/VIO_SD high (at least 90%) to start of VPA ramp-up	0	--	--	ms
T2	Delay from 3.3 high (at least 90%) to start of AVDD18 ramp-up	0	100	--	ms
T3	Delay from VIO/VIO_SD high (at least 90%) to start of PDn ramp-up	0	--	--	ms
T4	Delay from 18 high (90%) to start of Boot ROM	--	10	--	ms

3.6 Power Consumption*

3.6.1 WLAN

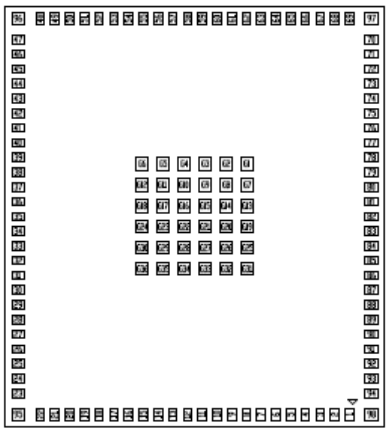
TBD

3.6.2 Bluetooth

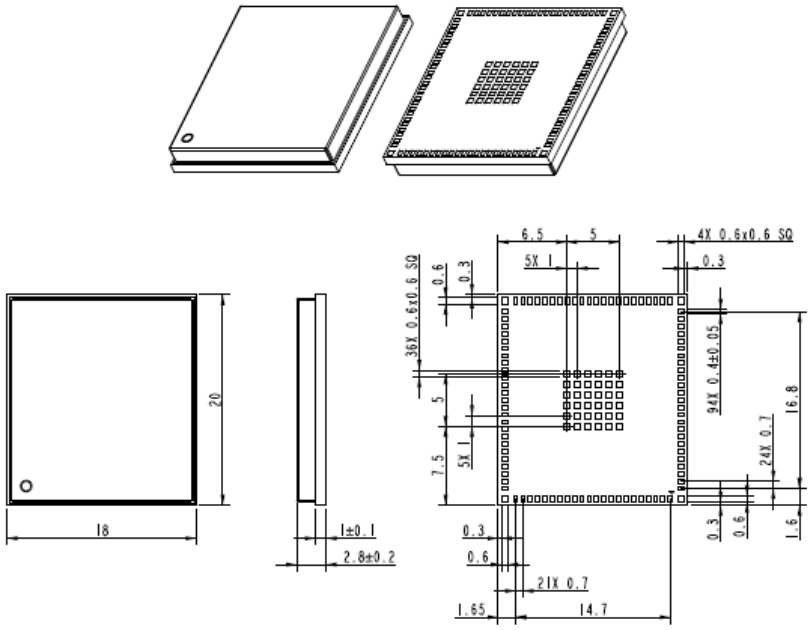
TBD

4. Mechanical Information

4.1 Mechanical Drawing



PIN DEFINED (BOTTOM VIEW)

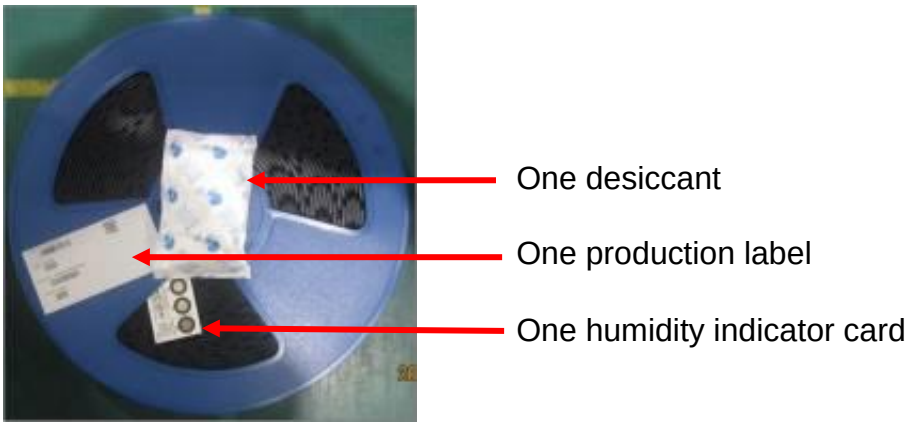


TOLERANCES UNLESS OTHERWISE SPECIFIED:±0.1mm

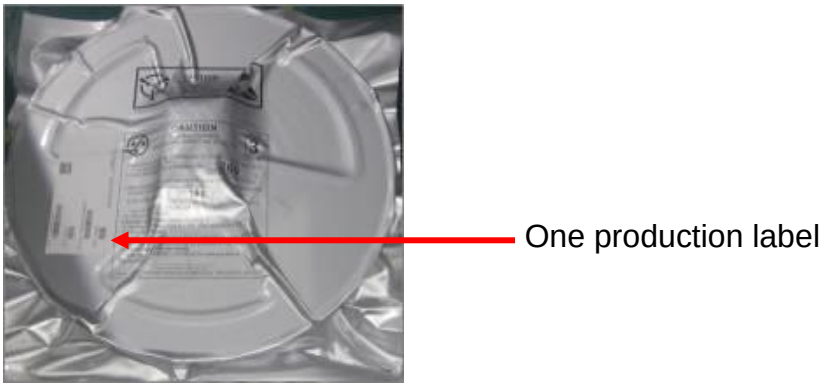
5. Packing Information

1. One reel can pack 650pcs

2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel



3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag



4. A bag is put into the anti-static pink bubble wrap

5. A bubble wrap is put into the inner box and then one label is pasted on the inner box

6. **4 inner boxes** could be put into one carton

7. Sealing the carton by AzureWave tape

8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton

Example of carton label	AzureWave Technologies Inc. AzureWave P/N Customer: 由業務提供 Customer P/N: 由業務提供 Customer PO: 由業務提供 Description: AW-XXXXXX QTY: 1200 pcs C/N N.W. G.W. RoHS COMPLIANT
Example of box label	

Example of production label	
Example of balance label