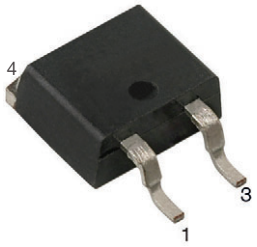
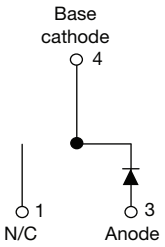
650 V Gen 3 Power SiC Merged PIN Schottky Diode, 8 A



D²PAK 2L (TO-263AB 2L)



LINKS TO ADDITIONAL RESOURCES

3D Models

Application Notes

PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	8 A
V_R	650 V
V_F at I_F at 25 °C, typ.	1.3 V
T_J max.	175 °C
I_R at V_R at 175 °C	1.9 µA
Q_C (V_R = 400 V)	22 nC
Package	D²PAK 2L (TO-263AB 2L)
Circuit configuration	Single

FEATURES

- Majority carrier diode using Schottky technology on SiC wide band gap material
- Improved V_F and efficiency by thin wafer technology
- Positive V_F temperature coefficient for easy paralleling
- Virtually no recovery tail and no switching losses
- Temperature invariant switching behavior
- Minimum creepage and clearance distances are 5.2 mm and 5.4 mm respectively
- Molding Compound Comparative Tracking Index: CTI ≥ 600, provides excellent electrical insulation at relevant working voltages
- 175 °C maximum operating junction temperature
- Meets MSL level 1, per J-STD-020, LF maximum peak of 245 °C
- MPS structure for high ruggedness to forward current surge events
- Meets JESD 201 class 1A whisker test
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

HALOGEN FREE

DESCRIPTION / APPLICATIONS

Wide band gap SiC based 650 V Schottky diode, designed for high performance and ruggedness.

Optimum choice for high speed hard switching and efficient operation over a wide temperature range, it is also recommended for all applications suffering from Silicon ultrafast recovery behavior.

Typical applications include AC/DC PFC and DC/DC ultra high frequency output rectification in FBPS and LLC converters.

MECHANICAL DATA

Case: D²PAK 2L (TO-263AB 2L)
Molding compound meets UL 94 V-0 flammability rating
Base P/N-M3 - halogen-free, RoHS-compliant
Terminals: matte tin plated leads, solderable per J-STD-002 and JESD 22-B102

MAXIMUM RATINGS (T_A = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage	V_{RRM}		650	V
Continuous forward current	I_F (1)	T_C = 142 °C (DC)	8	A
	I_F (2)	T_C = 149 °C (DC)		
DC blocking voltage	V_{DC}		650	V
Repetitive peak forward current	I_{FRM}	T_C = 25 °C, f = 50 Hz, square wave, DC = 25 %	35	A
Non-repetitive peak forward surge current	I_{FSM}	T_C = 25 °C, t_p = 10 ms, half sine wave	54	
		T_C = 110 °C, t_p = 10 ms, half sine wave	52	
Power dissipation	P_{tot} (1)	T_C = 25 °C	58	W
		T_C = 110 °C	25	
	P_{tot} (2)	T_C = 25 °C	75	W
		T_C = 110 °C	32	
I^2t value	$\int i^2 dt$	T_C = 25 °C	13.5	A^2s
		T_C = 110 °C	12.5	
Operating junction and storage temperatures	T_J (2), T_{Stg}		-55 to +175	°C

Notes

(1) Based on maximum R_{th}

(2) Based on typical R_{th}

(3) The heat generated must be less than the thermal conductivity from junction-to-ambient: $dP_D/dT_J < 1/R_{\theta JA}$

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ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Forward voltage	V_F	I_F = 8 A	-	1.3	1.5	V
		I_F = 8 A, T_J = 150 °C	-	1.5	1.8	
		I_F = 8 A, T_J = 175 °C	-	1.58	-	
Reverse leakage current	I_R	V_R = V_R rated	-	0.25	45	µA
		V_R = V_R rated, T_J = 150 °C	-	1.1	100	
		V_R = V_R rated, T_J = 175 °C	-	1.9	-	
Total capacitance	C	V_R = 1 V, f = 1 MHz	-	340	-	pF
		V_R = 400 V, f = 1 MHz	-	34	-	
Total capacitive charge	Q_C	V_R = 400 V, f = 1 MHz	-	22	-	nC

THERMAL - MECHANICAL SPECIFICATIONS (T_A = 25 °C unless otherwise specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Thermal resistance, junction to case	R_{thJC}		-	2.0	2.6	°C/W
Marking device			3C08ET07S			

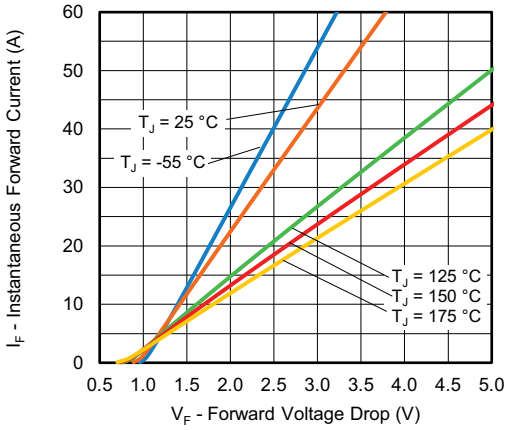


Fig. 1 - Typical Forward Voltage Drop Characteristics

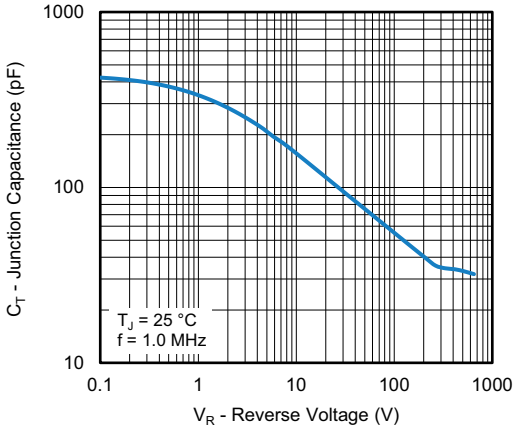


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

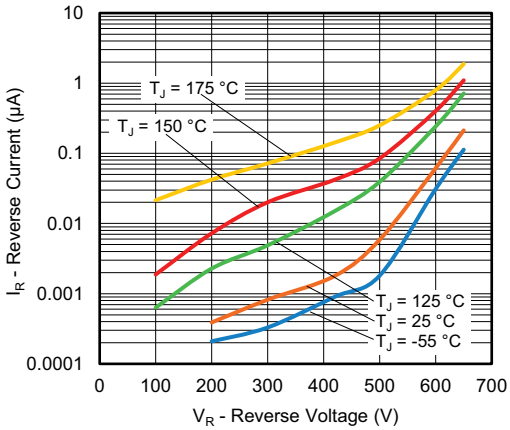


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

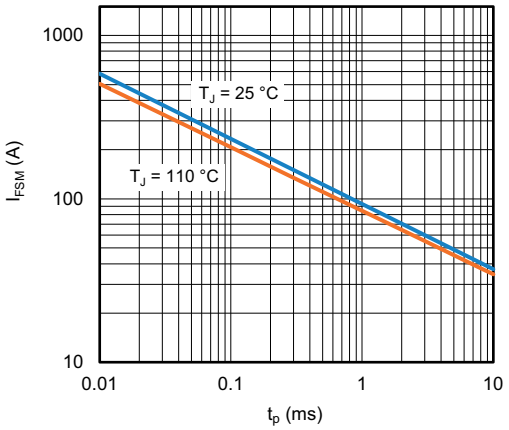


Fig. 4 - Non-Repetitive Peak Forward Surge Current vs. Pulse Duration (Square Wave)

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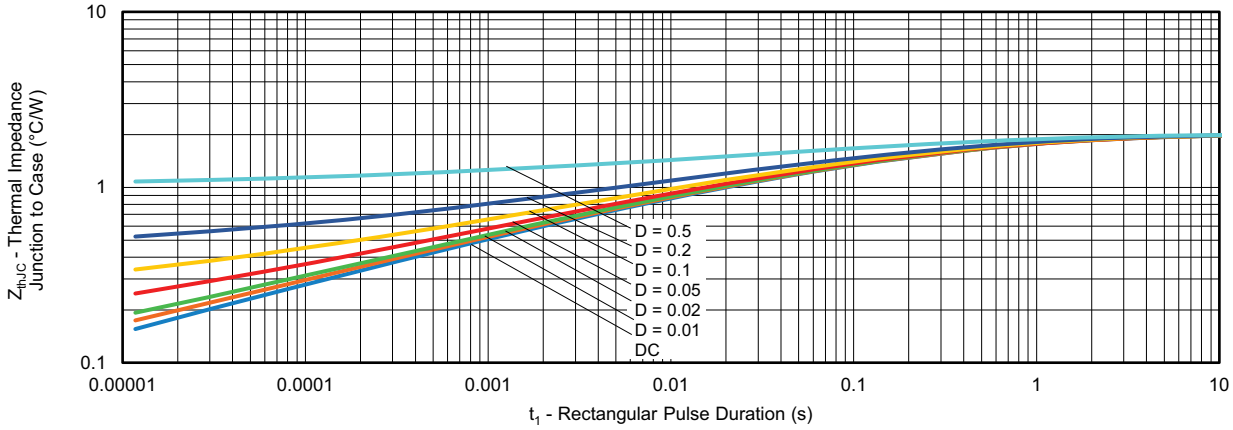


Fig. 5 - Typical Thermal Impedance Z_{thJC} Characteristics

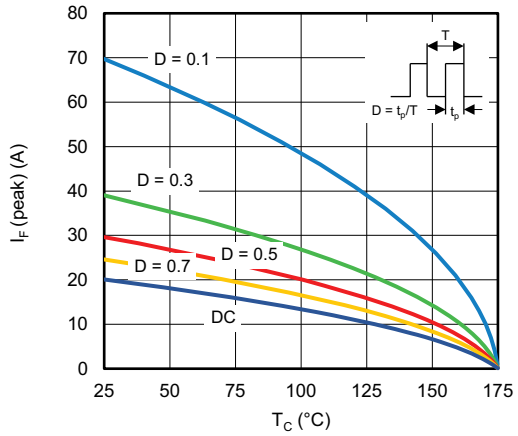


Fig. 6 - Peak Forward Current vs. Maximum Allowable Case Temperature

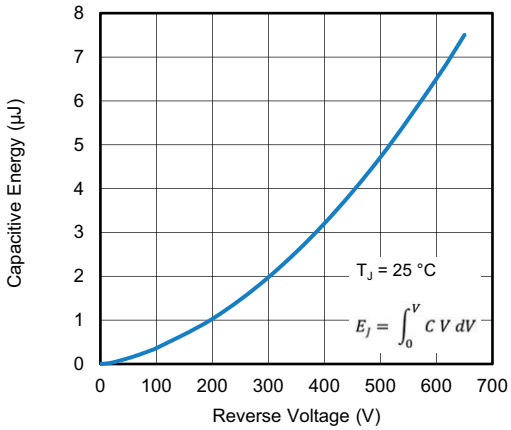


Fig. 8 - Typical Capacitive Energy vs. Reverse Voltage

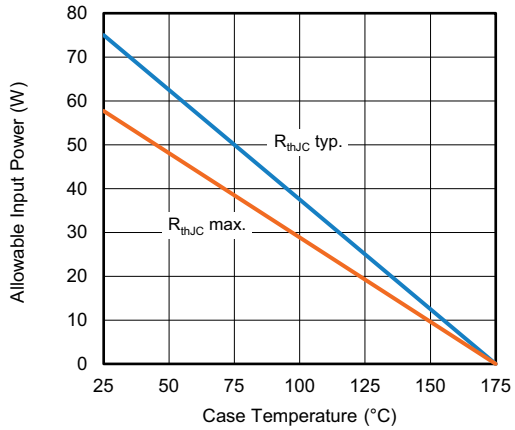


Fig. 7 - Forward Power Loss Characteristics

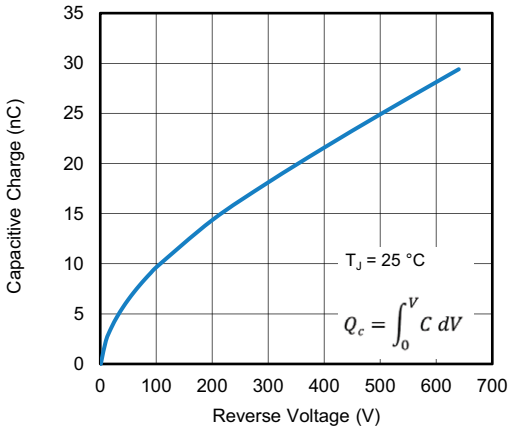


Fig. 9 - Typical Capacitive Charge vs. Reverse Voltage

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ORDERING INFORMATION TABLE

Device code

VS-	3C	08	E	T	07	S	2	L	-M3
1	2	3	4	5	6	7	8	9	10

1 - Vishay Semiconductors product
2 - 3C = SiC diode, generation 3
3 - Current rating (08 = 8 A)
4 - E = single diode
5 - T = D^2PAK package
6 - Voltage rating: (07 = 650 V)
7 - S = surface mountable
8 - 2 = true 2 pin D^2PAK
9 - L = tape and reel (left oriented)
10 - Environmental digit:
-M3 = halogen-free, RoHS-compliant, and termination lead (Pb)-free

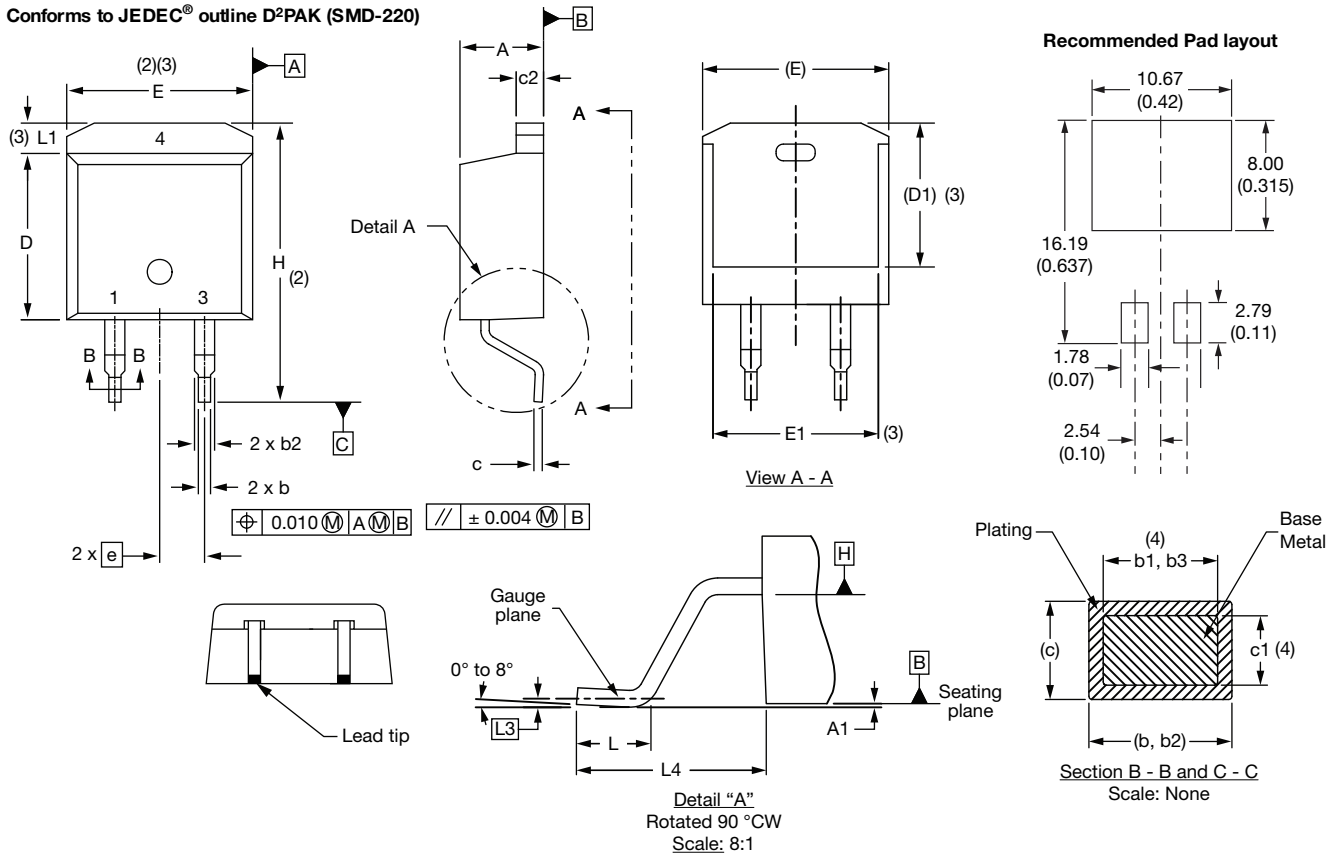
ORDERING INFORMATION		
PREFERRED P/N	**BASE QUANTITY**	**PACKAGING DESCRIPTION**
VS-3C08ET07S2L-M3	800 per reel	13" diameter reel

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?96683
Part marking information	www.vishay.com/doc?96693
Packaging information	www.vishay.com/doc?95032

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D^2PAK 2L (TO-263AB 2L)

DIMENSIONS in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	0.160	0.190	
A1	0.00	0.254	0.000	0.010	
b	0.51	0.99	0.020	0.039	
b1	0.51	0.89	0.020	0.035	4
b2	1.14	1.78	0.045	0.070	
b3	1.14	1.73	0.045	0.068	4
c	0.38	0.74	0.015	0.029	
c1	0.38	0.58	0.015	0.023	4
c2	1.14	1.65	0.045	0.065	
D	8.51	9.65	0.335	0.380	2

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
D1	6.86	8.00	0.270	0.315	3
E	9.65	10.67	0.380	0.420	2, 3
E1	7.90	8.80	0.311	0.346	3
e	2.54 BSC		0.100 BSC		
H	14.61	15.88	0.575	0.625	
L	1.78	2.79	0.070	0.110	
L1	-	1.65	-	0.066	3
L3	0.25 BSC		0.010 BSC		
L4	4.78	5.28	0.188	0.208	

Notes

(1) Dimensioning and tolerancing per ASME Y14.5 M-1994

(2) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body

(3) Thermal pad contour optional within dimension E, L1, D1 and E1

(4) Dimension b1 and c1 apply to base metal only

(5) Datum A and B to be determined at datum plane H

(6) Controlling dimension: inch

(7) Outline conforms to JEDEC® outline TO-263AB

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