

# 16-Mbit (1M Words × 16-Bit) Static RAM with Error-Correcting Code (ECC)

## Features

- AEC-Q100 qualified
- Ultra-low standby power
  - Typical standby current: 5.5  $\mu$ A
  - Maximum standby current: 75  $\mu$ A
- High speed: 45 ns / 55 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Temperature Ranges:
  - Automotive-A: -40 °C to +85 °C
  - Automotive-E: -40 °C to +125 °C
- Operating voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

## Functional Description

CY62167G is high-performance CMOS low-power (MoBL) SRAM devices with embedded ECC. This device is offered in dual chip-enable.

Devices with dual chip-enable are accessed by asserting both chip-enable inputs –  $\overline{CE}_1$  as LOW and  $\overline{CE}_2$  as HIGH.

Data writes are performed by asserting the Write Enable input ( $\overline{WE}$ ) LOW, and providing the data and address on device data ( $I/O_0$  through  $I/O_{15}$ ) and address ( $A_0$  through  $A_{19}$ ) pins respectively. The Byte High/Low Enable ( $\overline{BHE}$ ,  $\overline{BLE}$ ) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified.  $\overline{BHE}$  controls  $I/O_8$  through  $I/O_{15}$ ;  $\overline{BLE}$  controls  $I/O_0$  through  $I/O_7$ .

Data reads are performed by asserting the Output Enable ( $\overline{OE}$ ) input and providing the required address on the address lines. Read data is accessible on I/O lines ( $I/O_0$  through  $I/O_{15}$ ). Byte accesses can be performed by asserting the required byte enable signal ( $\overline{BHE}$ ,  $\overline{BLE}$ ) to read either the upper byte or the lower byte of data from the specified address location.

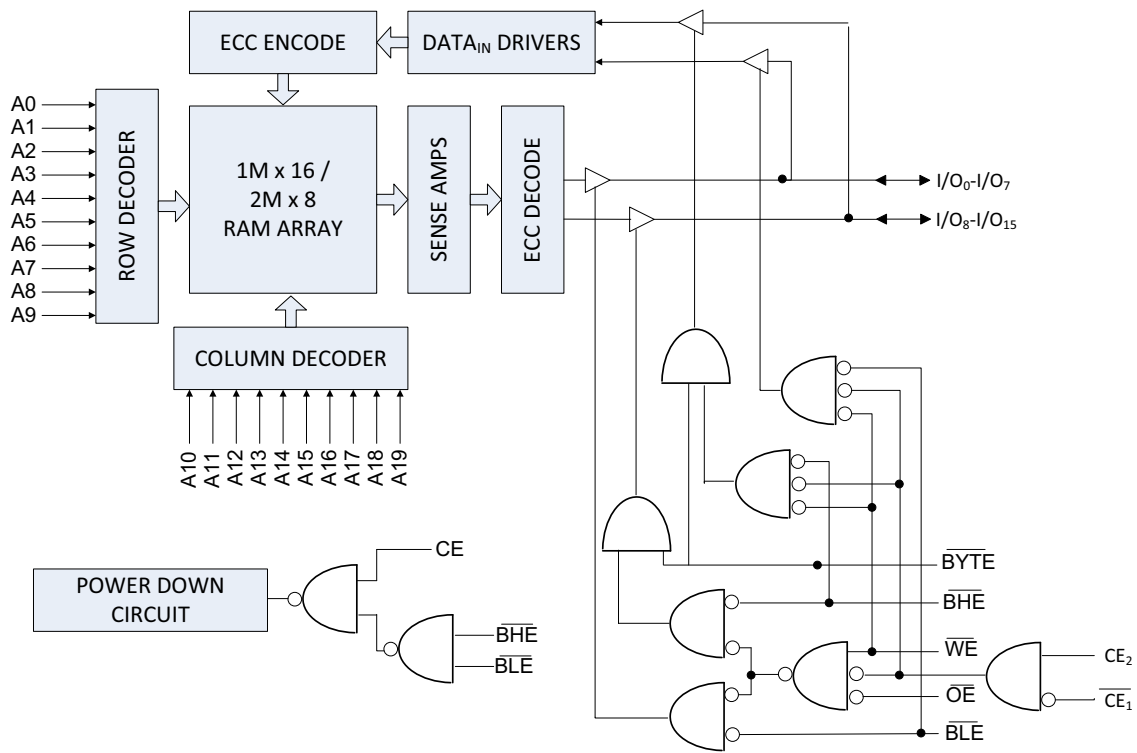
All I/Os ( $I/O_0$  through  $I/O_{15}$ ) are placed in a HI-Z state when the device is deselected ( $\overline{CE}_1$  HIGH /  $\overline{CE}_2$  LOW for dual chip-enable device), or control signals are de-asserted ( $\overline{OE}$ ,  $\overline{BLE}$ , and  $\overline{BHE}$ ).

These devices also have a unique “Byte Power down” feature where if both the Byte Enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) are disabled, the devices seamlessly switches to standby mode irrespective of the state of the chip enable(s), thereby saving power.

The CY62167G device is available in a Pb-free 48-ball VFBGA and 48-pin TSOP I packages. The device in the 48-pin TSOP I package can also be configured to function as a 2M words × 8 bit device. The logic block diagram is on page 2. Refer to [Pin Configurations on page 4](#) and the associated footnotes for details.

### Note

1. This device does not support automatic write-back on error detection.

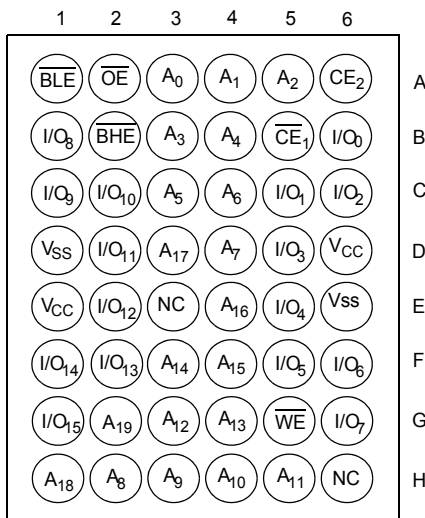
**Logic Block Diagram – CY62167G**


## Contents

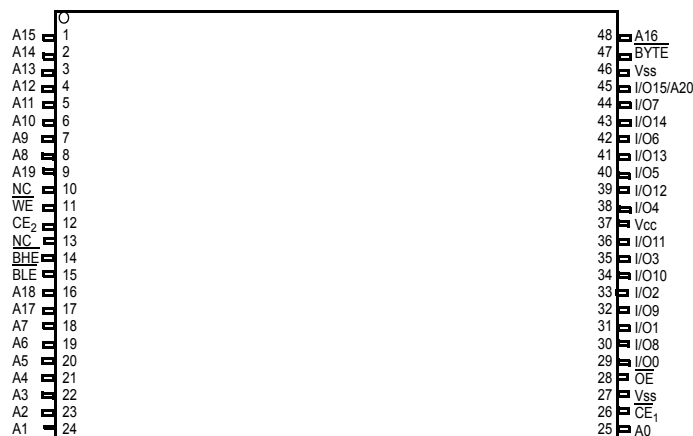
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## Pin Configurations

**Figure 1. 48-ball VFBGA pinout <sup>[2]</sup>**  
**CY62167G**



**Figure 2. 48-pin TSOP I pinout (Dual Chip Enable without ERR) – CY62167G <sup>[2, 3]</sup>**



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)	Speed (ns)	Power Dissipation			
				Operating I <sub>CC</sub> , (mA), f = f <sub>max</sub>		Standby, I <sub>SB2</sub> (μA)	
				Typ <sup>[4]</sup>	Max	Typ <sup>[4]</sup>	Max
CY62167G30	Automotive-E	2.2 V–3.6 V	55	29.0	40.0	5.5	75.0
	Automotive-A		45	29.0	36.0	5.5	16.0

### Notes

- NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
- The BYTE pin in the 48-pin TSOP I package must be tied to V<sub>CC</sub> to use the device as a 1M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2M × 8 SRAM by tying the BYTE signal to V<sub>SS</sub>. In the 2M × 8 configuration, pin 45 is A20, while BHE, BLE and I/O<sub>8</sub> to I/O<sub>14</sub> pins are not used.
- Indicates the value for the center of Distribution at 3.0 V, 25 °C and not 100% tested.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to + 150 °C

Ambient temperature  
with power applied ..... -55 °C to + 125 °C

Supply voltage  
to ground potential <sup>[5]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

DC voltage applied to outputs  
in HI-Z state <sup>[5]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

DC input voltage <sup>[5]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >140 mA

## Operating Range

Grade	Ambient Temperature	V <sub>CC</sub>
Automotive-E	-40 °C to +125 °C	2.2 V to 3.6 V
Automotive-A	-40 °C to +85 °C	

## DC Electrical Characteristics

Over the Operating Range

Parameter	Description		Test Conditions	55 ns (Automotive-E)			45 ns (Automotive-A)			Unit		
				Min	Typ <sup>[6]</sup>	Max	Min	Typ <sup>[6]</sup>	Max			
V <sub>OH</sub>	Output HIGH voltage	2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	2.0	—	—	2.0	—	—	V		
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA	2.4	—	—	2.4	—	—			
V <sub>OL</sub>	Output LOW voltage	2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA	—	—	0.4	—	—	0.4	V		
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA	—	—	0.4	—	—	0.4			
V <sub>IH</sub>	Input HIGH voltage <sup>[5]</sup>	2.2 V to 2.7 V	—	1.8	—	V <sub>CC</sub> + 0.3	1.8	—	V <sub>CC</sub> + 0.3	V		
		2.7 V to 3.6 V	—	2.0	—	V <sub>CC</sub> + 0.3	2.0	—	V <sub>CC</sub> + 0.3			
V <sub>IL</sub>	Input LOW voltage <sup>[5]</sup>	2.2 V to 2.7 V	—	-0.3	—	0.6	-0.3	—	0.6	V		
		2.7 V to 3.6 V	—	-0.3	—	0.8	-0.3	—	0.8			
I <sub>IX</sub>	Input leakage current		GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-4.0	—	+4.0	-1.0	—	+1.0	μA		
I <sub>OZ</sub>	Output leakage current		GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled	-4.0	—	+4.0	-1.0	—	+1.0	μA		
I <sub>CC</sub>	V <sub>CC</sub> operating supply current		V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, CMOS levels	f = f <sub>MAX</sub>		—	29.0	40.0	—	29.0	36.0	mA
				f = 1 MHz		—	7.0	18.0	—	7.0	9.0	mA
I <sub>SB1</sub> <sup>[7]</sup>	Automatic power down current – CMOS inputs; V <sub>CC</sub> = 2.2 to 3.6 V		$\overline{CE_1} \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≤ 0.2 V, f = f <sub>max</sub> (address and data only), f = 0 (OE, and WE), V <sub>CC</sub> = V <sub>CC(max)</sub>	—	5.5	75.0	—	5.5	16.0	μA		
I <sub>SB2</sub> <sup>[7]</sup>	Automatic power down current – CMOS inputs; V <sub>CC</sub> = 2.2 to 3.6 V		$\overline{CE_1} \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0, V <sub>CC</sub> = V <sub>CC(max)</sub>	—	5.5	75.0	—	5.5	16.0	μA		

### Notes

5. V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.

6. Indicates the value for the center of Distribution at 3.0 V, 25 °C and not 100% tested.

7. Chip enables (CE<sub>1</sub> and CE<sub>2</sub>) and BHE, BLE and BYTE must be tied to CMOS levels to meet the I<sub>SB1</sub> / I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

## Capacitance

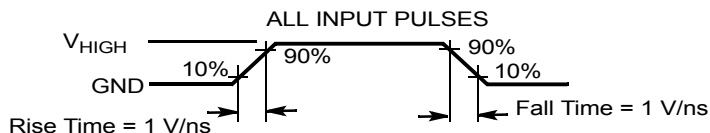
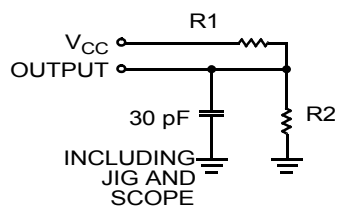
Parameter <sup>[8]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(\text{typ})}$	10	pF
$C_{OUT}$	Output capacitance		10	pF

## Thermal Resistance

Parameter <sup>[8]</sup>	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board	31.50	57.99	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		15.75	13.42	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameters	3.0 V	Unit
R1	317	$\Omega$
R2	351	$\Omega$
$V_{HIGH}$	3.0	V

### Note

8. Tested initially and after any design or process changes that may affect these parameters.

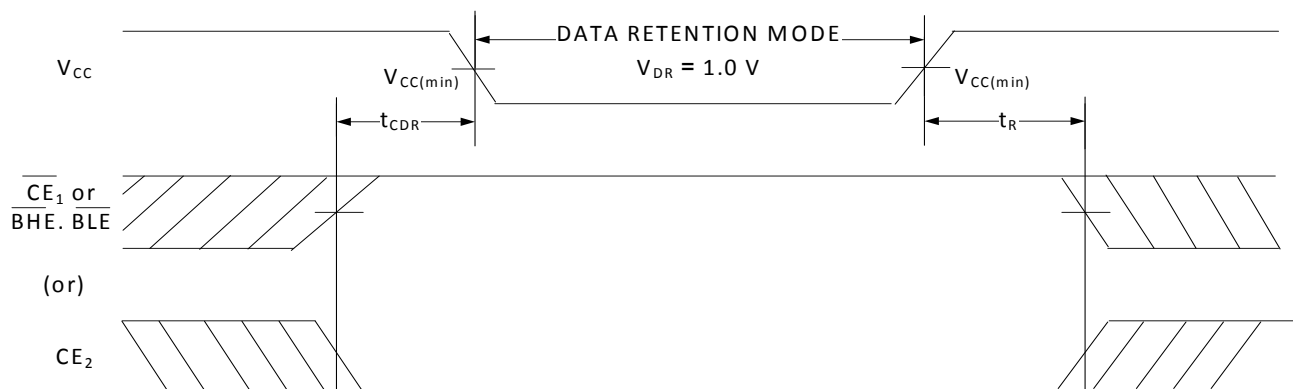
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	55 ns (Automotive-E)			45 ns (Automotive-A)			Unit
			Min	Typ <sup>[9]</sup>	Max	Min	Typ <sup>[9]</sup>	Max	
$V_{DR}$	$V_{CC}$ for data retention		1	–	–	1	–	–	V
$I_{CCDR}^{[10]}$	Data-retention current	$2.2\text{ V} < V_{CC} \leq 3.6\text{ V}$ $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	5.5	75.0	–	5.5	16.0	$\mu\text{A}$
$t_{CDR}^{[11]}$	Chip deselect to data-retention time		0	–	–	0	–	–	–
$t_R^{[12]}$	Operation-recovery time		55	–	–	45	–	–	ns

## Data Retention Waveform

Figure 4. Data-Retention Waveform <sup>[13]</sup>



### Notes

9. Indicates the value for the center of distribution at 3.0 V, 25°C and not 100% tested.
10. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) and BYTE must be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .
13.  $\overline{BHE}.\overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Parameter <sup>[14]</sup>	Description	55 ns (Automotive-E)		45 ns (Automotive-A)		Unit
		Min	Max	Min	Max	
Read Cycle						
t <sub>RC</sub>	Read cycle time	55	–	45	–	ns
t <sub>AA</sub>	Address to data valid	–	55	–	45	ns
t <sub>OHA</sub>	Data hold from address change	10	–	10	–	ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to data valid / $\overline{CE}$ LOW	–	55	–	45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid / $\overline{OE}$ LOW	–	25	–	22	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[15]</sup>	5	–	5	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[15, 16]</sup>	–	20	–	18	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low Z <sup>[15]</sup>	10	–	10	–	ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to High Z <sup>[15, 16]</sup>	–	20	–	18	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to power-up	0	–	0	–	ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to power-down	–	55	–	45	ns
t <sub>DBE</sub>	BLE / BHE LOW to data valid	–	55	–	45	ns
t <sub>LZBE</sub>	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z <sup>[15]</sup>	5	–	5	–	ns
t <sub>HZBE</sub>	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High Z <sup>[15, 16]</sup>	–	20	–	18	ns
Write Cycle <sup>[17]</sup>						
t <sub>WC</sub>	Write cycle time	55	–	45	–	ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to write end	40	–	35	–	ns
t <sub>AW</sub>	Address setup to write end	40	–	35	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	40	–	35	–	ns
t <sub>BW</sub>	BLE / BHE LOW to write end	40	–	35	–	ns
t <sub>SD</sub>	Data setup to write end	25	–	25	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	0	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[15, 16]</sup>	–	20	–	18	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[15]</sup>	10	–	10	–	ns

### Notes

14. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3$  V) and  $V_{CC}/2$  (for  $V_{CC} < 3$  V), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3$  V) and 0 to  $V_{CC}$  (for  $V_{CC} < 3$  V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.

15. At any temperature and voltage condition,  $t_{HZOE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.

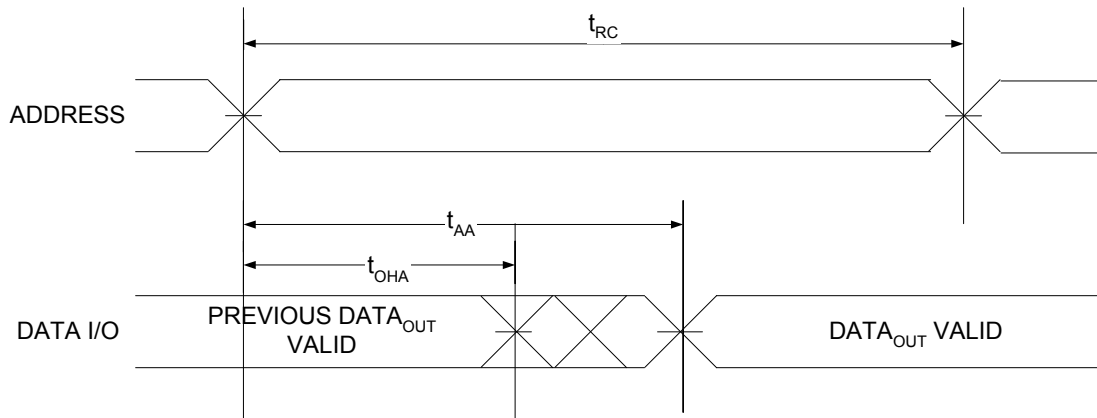
16.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.

17. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write. Any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

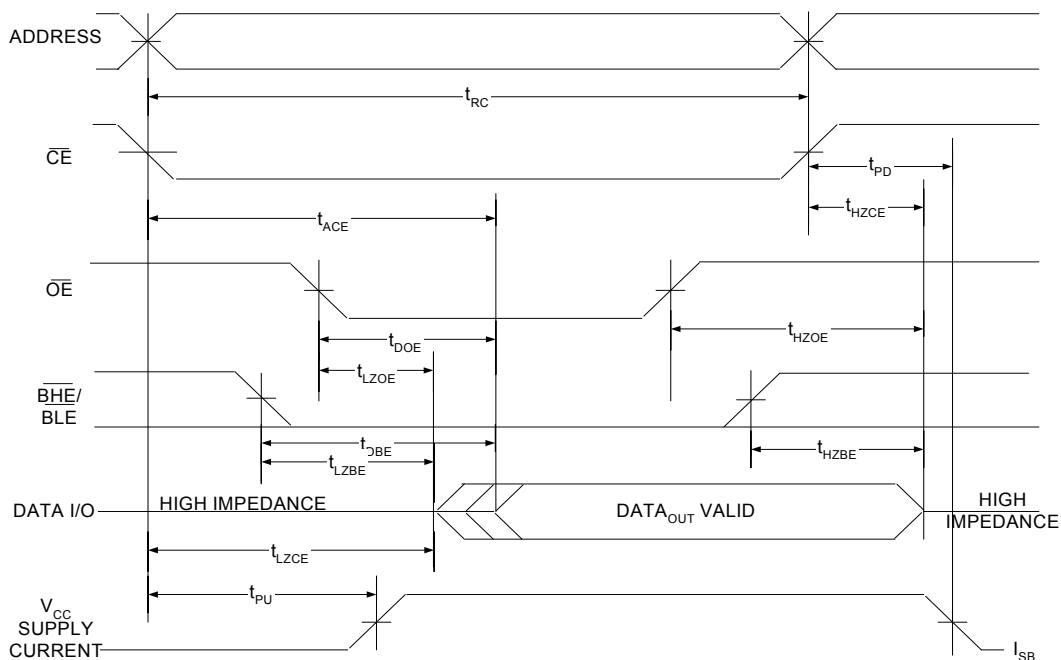


## Switching Waveforms

**Figure 5. Read Cycle No. 1 of CY62167G (Address Transition Controlled)** [18, 19]



**Figure 6. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)** [19, 20, 21]



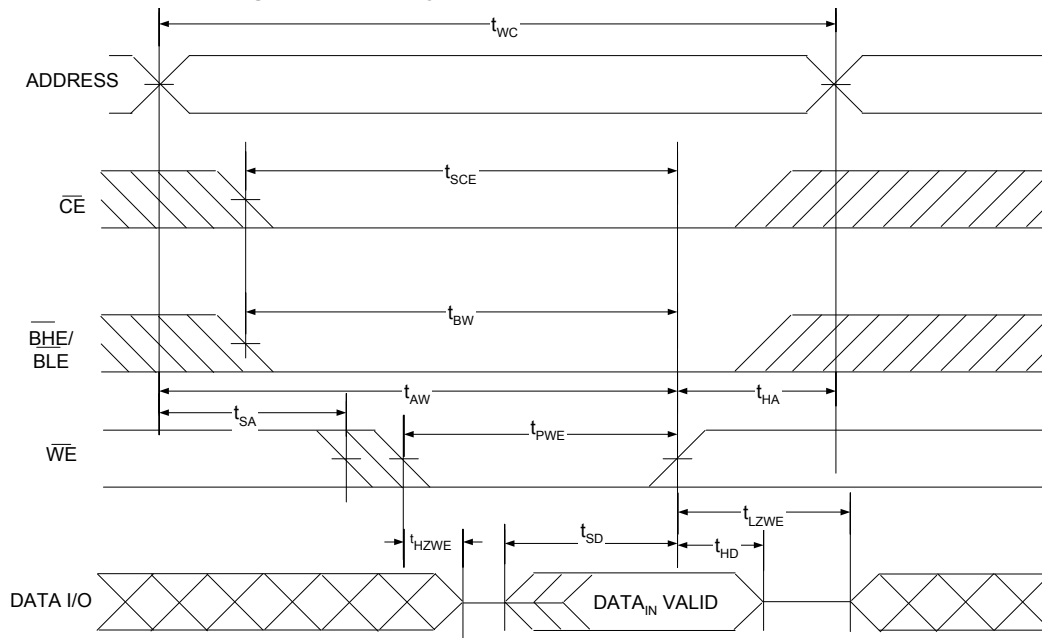
### Notes

18. The device is continuously selected.  $\overline{\text{OE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ .

19.  $\overline{\text{WE}}$  is HIGH for read cycle.

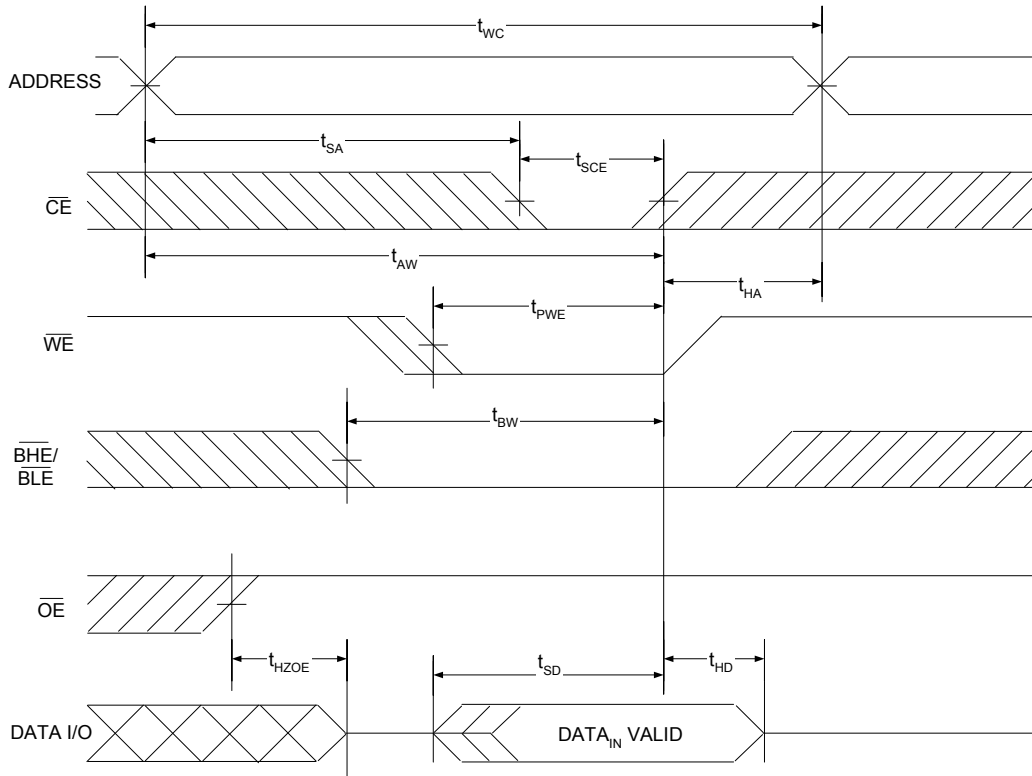
20. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.

21. Address valid prior to or coincident with  $\overline{\text{CE}}$  LOW transition.

**Switching Waveforms (continued)**
**Figure 7. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled) [22, 23, 24]**

**Notes**

22. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
23. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
24. Data I/O is in HI-Z state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .

**Switching Waveforms** (continued)

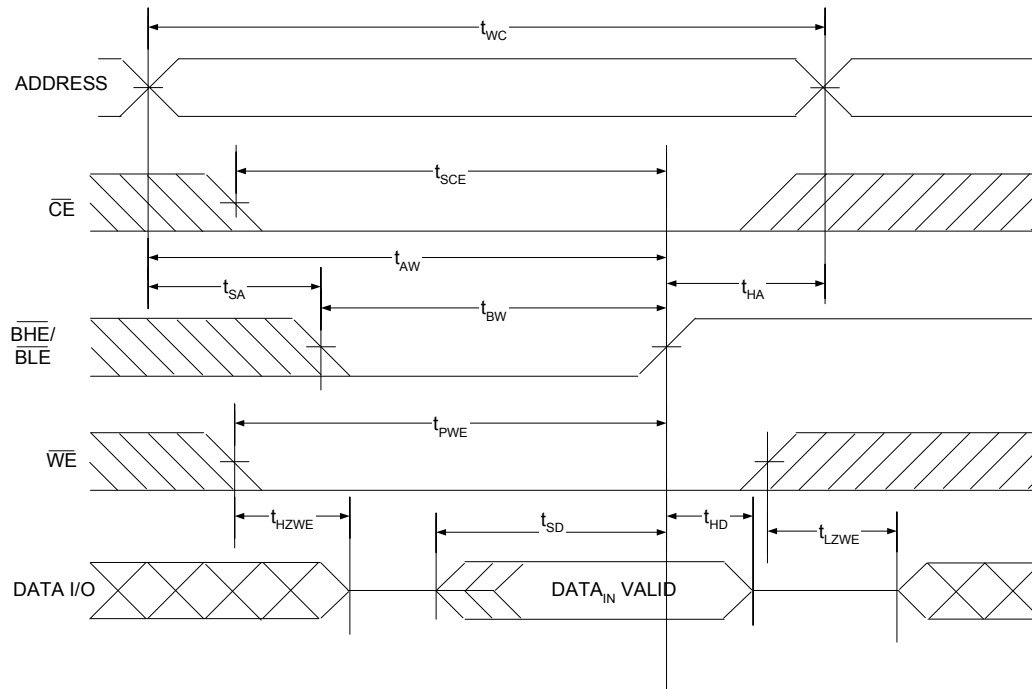
**Figure 8. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** [25, 26, 27]

**Notes**

25. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.

26. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

27. Data I/O is in high impedance state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .

**Switching Waveforms** (continued)

**Figure 9. Write Cycle No. 3 ( $\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [28, 29, 30]**

**Notes**

28. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
29. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}}_1 = V_{IL}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{IL}$ , and  $\text{CE}_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
30. Data I/O is in high impedance state if  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{OE}} = V_{IH}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

**Truth Table – CY62167G**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X <sup>[31]</sup>	X	X	X	X	HI-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X <sup>[31]</sup>	L	X	X	X	X	HI-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X <sup>[31]</sup>	X <sup>[31]</sup>	X	X	H	H	HI-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); HI-Z ( $I/O_8$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	HI-Z ( $I/O_0$ – $I/O_7$ ); Data Out ( $I/O_8$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	H	X	X	HI-Z	Output disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); HI-Z ( $I/O_8$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	HI-Z ( $I/O_0$ – $I/O_7$ ); Data In ( $I/O_8$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )

**Note**

31. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.



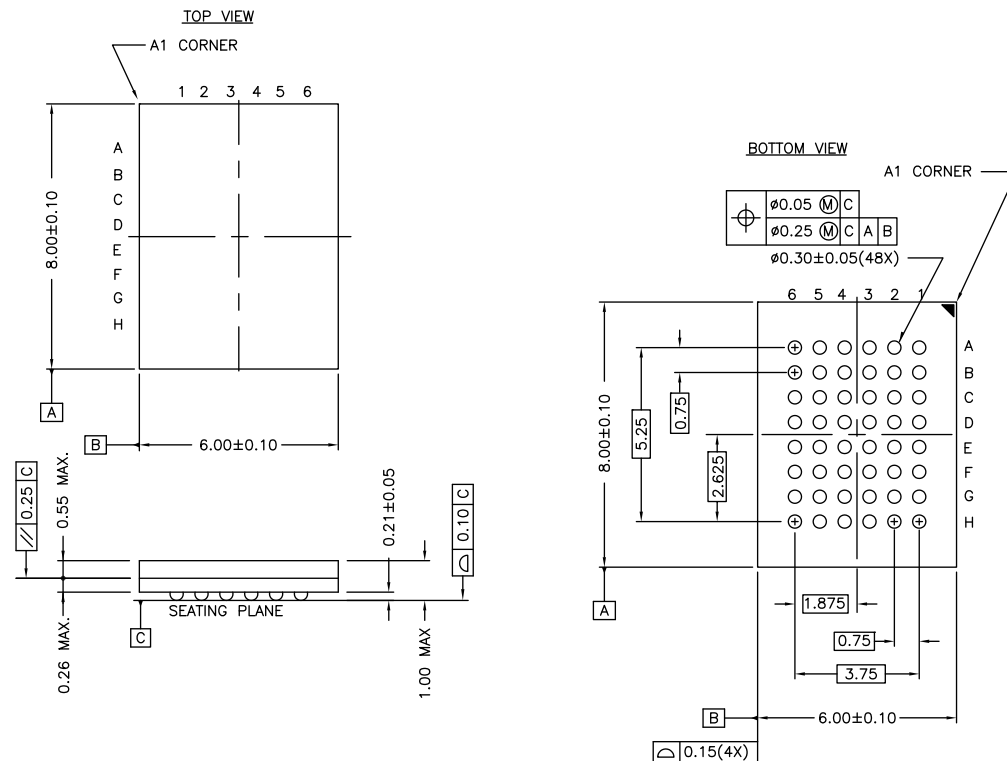
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62167G30-55BVXE	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	Automotive-E
	CY62167G30-55BVXET			
	CY62167G30-55ZXE	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Package Code: Z48A	
	CY62167G30-55ZXET			
45	CY62167G30-45ZXA	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Package Code: Z48A	Automotive-A
	CY62167G30-45ZXAT			
	CY62167G30-45BVXA	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	
	CY62167G30-45BVXAT			

The diagram shows a 10-character part number structure: **CY 621 6 7 G XX - XX XX X X**. Each character or group of characters is connected by a line to its corresponding description:

- CY**: Company ID: CY = Cypress
- 621**: Family Code: 621 = MoBL SRAM family
- 6**: Density: 6 = 16-Mbit
- 7**: Bus Width: 7 = × 16
- G**: Process Technology: G = 65 nm
- XX**: Voltage Range: 30 = 3 V typ
- : Separator
- XX**: Speed Grade: XX = 45 or 55  
45 = 45 ns; 55 = 55 ns
- XX**: Package Type: XX = BV or Z  
BV = 48-ball VFBGA; Z = 48-pin TSOP I
- X**: Pb-free
- X**: Temperature Range: X = E or A  
E = Automotive-E; A = Automotive-A
- X**: X = blank or T  
blank = Bulk; T = Tape and Reel

## Package Diagram

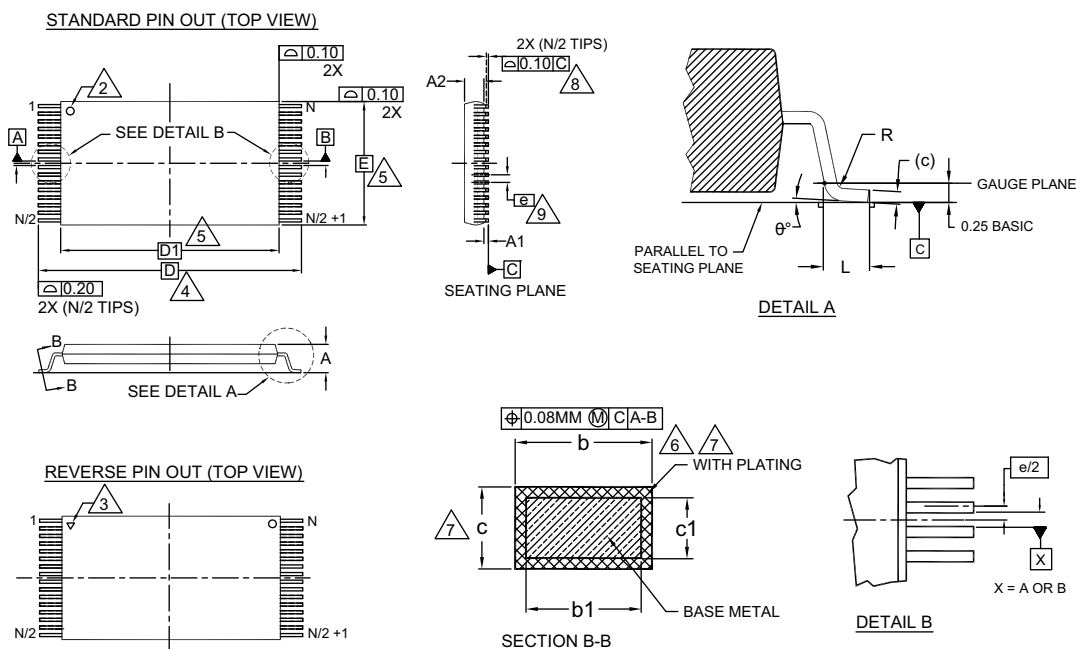
**Figure 10. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150**



NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 \*H

**Package Diagram (continued)**
**Figure 11. 48-pin TSOP I (18.4 × 12 × 1.2 mm) Package Outline, 51-85183**


SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

**NOTES:**

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN); INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE  $-C-$ . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 \*F



## Acronyms

Acronym	Description
BHE	byte high enable
BLE	byte low enable
CE	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
SRAM	static random access memory
VFBGA	very fine-pitch ball grid array
WE	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
μA	microamperes
μs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

## Document History Page

Document Title: CY62167G Automotive, 16-Mbit (1M Words × 16-Bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-84902				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*C	5083752	NILE	01/13/2016	Changed status from Preliminary to Final.
*D	5130998	NILE	02/12/2016	Updated <a href="#">Logic Block Diagram – CY62167G</a> . Updated <a href="#">Pin Configurations</a> : Added Note 3 and referred the same note in <a href="#">Figure 2</a> . Updated <a href="#">DC Electrical Characteristics</a> : Updated Note 7. Updated <a href="#">Data Retention Characteristics</a> : Updated Note 10.
*E	5555173	VINI	01/18/2017	Updated <a href="#">Features</a> : Added “AEC-Q100 qualified”. Updated <a href="#">Maximum Ratings</a> : Updated Note 5 (Replaced “2 ns” with “20 ns”). Updated <a href="#">DC Electrical Characteristics</a> : Replaced “55 ns (Automotive-E)” with “45 ns (Automotive-A)” in column heading. Replaced “55 ns (Automotive-A)” with “55 ns (Automotive-E)” in column heading. Changed minimum value of $V_{OH}$ parameter from 2.2 V to 2.4 V corresponding to Operating Range “2.7 V to 3.6 V”. Changed minimum value of $V_{IH}$ parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”. Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagram</a> : spec 51-85183 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*F	5725191	NILE	05/03/2017	Updated <a href="#">DC Electrical Characteristics</a> : Fixed typo in values of $I_{IX}$ and $I_{OZ}$ parameters (both “Min” and “Max” columns). Fixed typo in values of $I_{SB1}$ and $I_{SB2}$ parameters (only “Max” column). Updated <a href="#">Data Retention Characteristics</a> : Fixed typo in values of $I_{CCDR}$ parameter (only “Max” column). Updated to new template.

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