# FDA802AB



life.augmented

## Data brief

# 2x150 W/1x300 W class D digital input automotive power amplifier with diagnostics features and low voltage



# LQFP64 10x10x1.4 mm (exposed pad up)

Product status link			
FDA802AB			
Product summary			
Order code	Package	Packing	
FDA802AB- VYY	LQFP64 (exp. pad	Tray	
FDA802AB- VYT	up)	Tape and reel	

### **Features**

- AEC-Q100 qualified
- Integrated 110 dB D/A conversion
- I<sup>2</sup>S and TDM digital input (3.3/1.8 V)
- Input sampling frequency: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Full I<sup>2</sup>C bus driving (3.3/1.8 V) with 8 different I<sup>2</sup>C bus addresses
- EMI control for FM/AM compatibility
- EMI compliance evaluated following normative CISPR25 (class V)
- Low radiation function (LRF)
- Very low quiescent current
- Output low-pass filter included in the feedback allowing outstanding audio performances
- Wide operating supply range: target 5.5 V-50 V
- Supply voltage monitoring on I<sup>2</sup>C
- MOSFET power outputs allowing high output power capability under step-up voltage:
  - 2x120 W /4 Ω at 35 V, 1 kHz THD = 1% (2x150 W /4 Ω at 35 V, 1 kHz THD = 10%)
  - 2x140 W /8 Ω at 50 V, 1 kHz THD = 1% (2x180 W /8 Ω at 50 V, 1 kHz THD = 10%)
    2x270 W /8 Ω at 50 V max output power
- Operation under standard car battery with high output power:
  - 2x22 W /4 Ω at 14 V, 1 kHz THD = 1%
  - (2x28 W /4 Ω at 14 V, 1 kHz THD = 10%) - 2x37 W /2 Ω at 14 V, 1 kHz THD = 1%
  - (2x46 W /2 Ω at 14 V, 1 kHz THD = 10%)
- Possibility to drive 2 Ω loads:
  - up to 18 V in normal mode
  - up to 35 V in parallel mode
  - Independent channel operation
- I<sup>2</sup>C bus diagnostics:
  - Short to  $V_{CC}$ /GND diagnostic (including soft shorts up to 1 k $\Omega$ )
  - DC load diagnostic
  - AC load diagnostic (working both with internally generated and externally generated tone)
- Digital impedance-meter (DIM)
- Integrated fault protection
- Input and output offset detector
- Clipping detector

lectronics sales office

- Legacy mode ('no I<sup>2</sup>C' mode)
- Short circuit and ESD integrated protections

Package: LQFP64 exposed pad up

#### **Description**

The FDA802AB is a dual bridge class D amplifier, designed in the most advanced BCD technology specially intended for car radio applications.

The FDA802AB integrates a high performance D/A converter together with powerful MOSFET outputs in class D, to get an outstanding efficiency compared with the standard class AB.

The integrated D/A converter allows to reach outstanding performances (115 dB S/N ratio with 110 dB of dynamic range).

Thanks to the high-voltage MOSFET output stages it can operate both under standard car battery (6 -18 V) and under boosted power supply (up to 50 V) to reach the highest possible power with integrated solution.

The feedback loop includes the output L-C low-pass filter, allowing superior frequency response linearity and lower distortion independently from the inductor and capacitor quality.

FDA802AB is fully configurable through I<sup>2</sup>C bus interface and integrates a complete diagnostics array specially intended for automotive applications.

Thanks to the solutions implemented to solve the EMI problems, the device is intended to be used in the standard single DIN car-radio box together with the tuner.

Moreover FDA802AB is able to work with power supply as low as 5.5 V, thus supporting the most recent low voltage ('start-stop') car-makers specification.

# 1 Block and pins description diagrams

#### 1.1 Block diagram



## 1.2 Pins description

57

Figure 2. Pins connection diagram



#### Table 1. Pins list description

N#	Pin	Function
1	FB1+	Channel 1, half bridge plus, feedback
2	OUT1+	Channel 1, half bridge plus, output
3	OUT1+	Channel 1, half bridge plus, output
4	VCC1+	Channel 1, half bridge plus, boosted power supply
5	VCC1-	Channel 1, half bridge minus, boosted power supply
6	OUT1-	Channel 1, half bridge minus, output
7	OUT1-	Channel 1, half bridge minus, output
8	FB1-	Channel 1, half bridge minus, feedback
9	GND1-	Channel 1, half bridge minus, power ground
10-13	N.C.	Not connected
14	Vbat	Main battery voltage (14 V)
15	Vbat	Main battery voltage (14 V)
16-17	N.C.	Not connected
18	Enable4	Chip enable 4
19	N.C.	Not connected
20	Enable3	Chip enable 3

21   Enable2   Chip enable 2     22   Enable1   Chip enable 1     23   DCSVR   Negative analog supply V(SVR)-0.9 V (internally generated)     24   D1V8SVR   Positive digital supply V(SVR)+0.9 V (internally generated)     26   Dgnd   Digital supply   Digital supply     26   Dgnd   Digital ground     27   CPump1   Charge pump output voltage     28   VddCP   Charge pump output voltage     29   CPump2   Charge pump pin 2     30-34   N.C.   Not connected     35   Vbat   Main battery voltage (14 V)     36-39   N.C.   Not connected     40   GND2-   Channel 2, half bridge minus, power ground     41   FB2-   Channel 2, half bridge minus, output     43   OUT2-   Channel 2, half bridge plus, boosted power supply     44   VCC2+   Channel 2, half bridge plus, boosted power supply     45   VCC2+   Channel 2, half bridge plus, boosted power supply     46   OUT2+   Channel 2, half bridge plus, boosted power supply     47   OUT2+   Channel 2, half bridge plus, output <th>N#</th> <th>Pin</th> <th>Function</th>	N#	Pin	Function
23DGSVRNegative analog supply V(SVR)-0.9 V (internally generated)24D1V8SVRPositive digital supply V(SVR)+0.9 V (internally generated)25DVddDigital supply26DgndDigital ground27CPump1Charge pump output voltage29CPump2Charge pump output voltage30.34N.C.Not connected35VbatMain battery voltage (14 V)36-39N.C.Not connected40GND2-Channel 2, half bridge minus, power ground41FB2-Channel 2, half bridge minus, output43OUT2-Channel 2, half bridge minus, output44VCC2-Channel 2, half bridge minus, output45VCC2+Channel 2, half bridge minus, output46OUT2-Channel 2, half bridge plus, boosted power supply45VCC2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, output49TABDevice slug connection50GND2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2C-DataI <sup>2</sup> C clock53I2C-DataI <sup>2</sup> C flock54I2Sdata2I <sup>2</sup> S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I <sup>2</sup> S/TDM data 2 (data input, NOT used in TDM mode)56I2ScWI <sup>2</sup> S/TDM data 2 (data input, NOT used in TDM mode)58Agnd <td>21</td> <td>Enable2</td> <td>Chip enable 2</td>	21	Enable2	Chip enable 2
24D1V8SVRPositive digital supply V(SVR)+0.9 V (internally generated)25DVddDigital supply26DgndDigital ground27CPump1Charge pump pin128VddCPCharge pump output voltage29CPump2Charge pump pin 230-34N.C.Not connected35VbatMain battery voltage (14 V)36-39N.C.Not connected40GND2-Channel 2, half bridge minus, power ground41FB2-Channel 2, half bridge minus, feedback42OUT2-Channel 2, half bridge minus, output43OUT2-Channel 2, half bridge minus, output44VCC2-Channel 2, half bridge plus, boosted power supply45VCC2+Channel 2, half bridge plus, boosted power supply46OUT2+Channel 2, half bridge plus, output47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, output49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CCkiI²C cok53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdat1I²S/TDM wis (frame sync Input)56I2ScikI2S/TDM wis (frame sync Input)58AgndAnalog ground59AVddAnalog supply <td>22</td> <td>Enable1</td> <td>Chip enable 1</td>	22	Enable1	Chip enable 1
25DVddDigital supply26DgndDigital ground27CPump1Charge pump pin128VddCPCharge pump output voltage29CPump2Charge pump pin 230-34N.C.Not connected35VbatMain battery voltage (14 V)36-39N.C.Not connected40GND2-Channel 2, half bridge minus, power ground41FB2-Channel 2, half bridge minus, feedback42OUT2-Channel 2, half bridge minus, output43OUT2-Channel 2, half bridge pinus, output44VCC2-Channel 2, half bridge pinus, output45VCC2+Channel 2, half bridge pinus, output46OUT2+Channel 2, half bridge pinus, output47OUT2+Channel 2, half bridge pinus, output48FB2+Channel 2, half bridge pinus, output49TABDevice slug connection50GND2+Channel 2, half bridge pinus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C clock54I2Sdata2I²S/TDM data 1(data input)56I2SclkI2S/TDM vs (frame sync Input)58AgndAnalog ground59AVddAnalog ground	23	DGSVR	Negative analog supply V(SVR)-0.9 V (internally generated)
26DgridDigital ground27CPump1Charge pump pin128VddCPCharge pump output voltage29CPump2Charge pump pin 230-34N.C.Not connected35VbatMain battery voltage (14 V)36-39N.C.Not connected40GND2-Channel 2, half bridge minus, power ground41FB2-Channel 2, half bridge minus, feedback42OUT2-Channel 2, half bridge minus, output43OUT2-Channel 2, half bridge minus, output44VCC2-Channel 2, half bridge plus, output45VCC2+Channel 2, half bridge plus, output46OUT2+Channel 2, half bridge plus, output47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, output49TABDevice sig connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1(data input)56I2SWsI²S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	24	D1V8SVR	Positive digital supply V(SVR)+0.9 V (internally generated)
27CPump1Charge pump pin128VddCPCharge pump output voltage29CPump2Charge pump pin 230-34N.C.Not connected35VbatMain battery voltage (14 V)36-39N.C.Not connected40GND2-Channel 2, half bridge minus, power ground41FB2-Channel 2, half bridge minus, feedback42OUT2-Channel 2, half bridge minus, output43OUT2-Channel 2, half bridge minus, output44VCC2-Channel 2, half bridge minus, output45VCC2+Channel 2, half bridge plus, boosted power supply46OUT2+Channel 2, half bridge plus, output47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, output49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CCIKI²C clock53I2C-DataI²C clock54I2Sdata1I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1(data input)56I2SolkI2S/TDM look57I2SwsI²S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	25	DVdd	Digital supply
28VddCPCharge pump output voltage29CPump2Charge pump pin 230-34N.C.Not connected35VbatMain battery voltage (14 V)36-39N.C.Not connected40GND2-Channel 2, half bridge minus, power ground41FB2-Channel 2, half bridge minus, feedback42OUT2-Channel 2, half bridge minus, output43OUT2-Channel 2, half bridge minus, output44VCC2-Channel 2, half bridge minus, boosted power supply45VCC2+Channel 2, half bridge plus, boosted power supply46OUT2+Channel 2, half bridge plus, output47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, output49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DlagClip detector / diagnostic pin (output, open drain)52I2CCIkI <sup>2</sup> C clock53I2C-DataI <sup>2</sup> C data input54I2Sdata2I <sup>3</sup> S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I <sup>3</sup> S/TDM data 1(data input)56I2SvikI2S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog ground	26	Dgnd	Digital ground
29CPump2Charge pump pin 230-34N.C.Not connected35VbatMain battery voltage (14 V)36-39N.C.Not connected40GND2-Channel 2, half bridge minus, power ground41FB2-Channel 2, half bridge minus, feedback42OUT2-Channel 2, half bridge minus, output43OUT2-Channel 2, half bridge minus, output44VCC2-Channel 2, half bridge minus, output45VCC2+Channel 2, half bridge plus, boosted power supply46OUT2+Channel 2, half bridge plus, output47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, output49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C clock54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1(data input)56I2SclkI2S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog ground	27	CPump1	Charge pump pin1
30-34N.C.Not connected35VbatMain battery voltage (14 V)36-39N.C.Not connected40GND2-Channel 2, half bridge minus, power ground41FB2-Channel 2, half bridge minus, output43OUT2-Channel 2, half bridge minus, output44VCC2-Channel 2, half bridge minus, output45VCC2+Channel 2, half bridge minus, output46OUT2+Channel 2, half bridge plus, boosted power supply46OUT2+Channel 2, half bridge plus, boosted power supply47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, output49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM dock57I2SwsI²S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	28	VddCP	Charge pump output voltage
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36-39N.C.Not connected40GND2-Channel 2, half bridge minus, power ground41FB2-Channel 2, half bridge minus, feedback42OUT2-Channel 2, half bridge minus, output43OUT2-Channel 2, half bridge minus, output44VCC2-Channel 2, half bridge minus, boosted power supply45VCC2+Channel 2, half bridge plus, boosted power supply46OUT2+Channel 2, half bridge plus, output47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, output49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI <sup>2</sup> C clock53I2C-DataI <sup>2</sup> C data input54I2Sdata2I <sup>2</sup> S/TDM data 2 (data input, NOT used in TDM mode)55I2SclkI2S/TDM lock57I2SwsI <sup>2</sup> S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	30-34	N.C.	Not connected
40GND2-Channel 2, half bridge minus, power ground41FB2-Channel 2, half bridge minus, feedback42OUT2-Channel 2, half bridge minus, output43OUT2-Channel 2, half bridge minus, output44VCC2-Channel 2, half bridge minus, boosted power supply45VCC2+Channel 2, half bridge plus, boosted power supply46OUT2+Channel 2, half bridge plus, boosted power supply47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, output49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C tock54I2Sdata1I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	35	Vbat	Main battery voltage (14 V)
41FB2-Channel 2, half bridge minus, feedback42OUT2-Channel 2, half bridge minus, output43OUT2-Channel 2, half bridge minus, output44VCC2-Channel 2, half bridge minus, boosted power supply45VCC2+Channel 2, half bridge plus, boosted power supply46OUT2+Channel 2, half bridge plus, output47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, edeback49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1(data input)56I2SclkI2S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	36-39	N.C.	Not connected
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43OUT2-Channel 2, half bridge minus, output44VCC2-Channel 2, half bridge minus, boosted power supply45VCC2+Channel 2, half bridge plus, boosted power supply46OUT2+Channel 2, half bridge plus, output47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, feedback49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdat1I²S/TDM data 1(data input)56I2SclkI2S/TDM lock57I2SwsI²S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	41	FB2-	Channel 2, half bridge minus, feedback
44VCC2-Channel 2, half bridge minus, boosted power supply45VCC2+Channel 2, half bridge plus, boosted power supply46OUT2+Channel 2, half bridge plus, output47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, feedback49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI <sup>2</sup> C clock53I2C-DataI <sup>2</sup> C data input54I2Sdata2I <sup>2</sup> S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I <sup>2</sup> S/TDM data 1(data input)56I2SclkI2S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	42	OUT2-	Channel 2, half bridge minus, output
45VCC2+Channel 2, half bridge plus, boosted power supply46OUT2+Channel 2, half bridge plus, output47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, feedback49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1(data input)56I2SclkI2S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	43	OUT2-	Channel 2, half bridge minus, output
46OUT2+Channel 2, half bridge plus, output47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, feedback49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1(data input)56I2SclkI2S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	44	VCC2-	Channel 2, half bridge minus, boosted power supply
47OUT2+Channel 2, half bridge plus, output48FB2+Channel 2, half bridge plus, feedback49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1(data input)56I2SclkI2S/TDM clock57I2SwsI²S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	45	VCC2+	Channel 2, half bridge plus, boosted power supply
48FB2+Channel 2, half bridge plus, feedback49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1(data input)56I2SclkI2S/TDM clock57I2SwsI²S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	46	OUT2+	Channel 2, half bridge plus, output
49TABDevice slug connection50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1(data input)56I2SclkI2S/TDM clock57I2SwsI²S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	47	OUT2+	Channel 2, half bridge plus, output
50GND2+Channel 2, half bridge plus, power ground51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1 (data input)56I2SclkI2S/TDM clock57I2SwsI²S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	48	FB2+	Channel 2, half bridge plus, feedback
51CD/DiagClip detector / diagnostic pin (output, open drain)52I2CClkI²C clock53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1(data input)56I2SclkI2S/TDM clock57I2SwsI²S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	49	TAB	Device slug connection
52I2CClkI²C clock53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1 (data input)56I2SclkI2S/TDM clock57I2SwsI²S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	50	GND2+	Channel 2, half bridge plus, power ground
53I2C-DataI²C data input54I2Sdata2I²S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I²S/TDM data 1 (data input)56I2SclkI2S/TDM clock57I2SwsI²S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	51	CD/Diag	Clip detector / diagnostic pin (output, open drain)
54I2Sdata2I2S/TDM data 2 (data input, NOT used in TDM mode)55I2Sdata1I2S/TDM data 1(data input)56I2SclkI2S/TDM clock57I2SwsI2S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	52	I2CClk	I <sup>2</sup> C clock
55I2Sdata1I2S/TDM data 1(data input)56I2SclkI2S/TDM clock57I2SwsI2S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	53	I2C-Data	I <sup>2</sup> C data input
55I2Sdata1I2S/TDM data 1(data input)56I2SclkI2S/TDM clock57I2SwsI2S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	54	I2Sdata2	I <sup>2</sup> S/TDM data 2 (data input, NOT used in TDM mode)
57I2SwsI2S/TDM ws (frame sync Input)58AgndAnalog ground59AVddAnalog supply	55	I2Sdata1	
58 Agnd Analog ground   59 AVdd Analog supply	56	I2Sclk	I2S/TDM clock
59 AVdd Analog supply	57	I2Sws	I <sup>2</sup> S/TDM ws (frame sync Input)
	58	Agnd	Analog ground
60 AGSVR Negative analog supply V(SVR)-2.5 V (internally generated)	59	-	Analog supply
	60	AGSVR	Negative analog supply V(SVR)-2.5 V (internally generated)
61 A5VSVR Positive analog supply V(SVR)+2.5 V (internally generated)	61	A5VSVR	Positive analog supply V(SVR)+2.5 V (internally generated)
62 SVR Supply voltage ripple rejection capacitor	62	SVR	Supply voltage ripple rejection capacitor
63 HWMute Hardware mute pin	63	HWMute	Hardware mute pin
64 GND1+ Channel 1, half bridge plus, power ground	64	GND1+	Channel 1, half bridge plus, power ground

# 2 Application diagram



## **3** General introduction

FDA802AB is a fully digital single chip class D amplifier with high immunity to the demodulation filter effects. The high integration level and the on-board signal processing allow excellent audio performance to be achieved. Thanks to the digital input and to the feedback strategy in the power stage (that makes the amplifier immune from

the output filter components non-linearity), the number and size of the external components are minimized. A number of features is included to reduce EMI and the fully digital approach provides a very high immunity to GSM/RF interferences.

FDA802AB includes: digital I<sup>2</sup>C and I<sup>2</sup>S interfaces, internal 24 bits DAC conversion, digital signal processing for interpolation and noise shaping, innovative self-diagnostic functions and automatic detection of wrong load connections or variation of the load, internal PLL for a clock generation.

#### **Package information** 4

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

#### LQFP64 (10x10x1.4 mm exp. pad up) package information 4.1



Figure 4. LQFP64 (10x10x1.4 mm exp. pad up) package outline

- STAND OFF

ŧθ

STAND OFF +

Symbol		Dimension in mm		
Symbol	Min.	Тур.	Max.	
θ	0°	3.5°	6°	
Θ1	0°	9°	12°	
Θ2	11°	12°	13°	
θ3	11°	12°	13°	
А	-	-	1.49	
A1	-0.04	-	0.04	
A2	1.35	1.4	1.45	
b	-	-	0.27	
b1	0.17	0.20	0.23	
С	0.09	-	0.20	
c1	0.09	0.127	0.16	
D		12.00 BSC		
D1 <sup>(1)(2)</sup>		10.00 BSC		
D2		See VARIATIONS		
D3	See VARIATIONS			
е		0.50 BSC		
E	12.00 BSC			
E1 <sup>(1)(2)</sup>	10.00 BSC			
E2	See VARIATIONS			
E3	See VARIATIONS			
L	0.45	0.6	0.75	
L1	1.00 REF			
N	-	64	_	
R1	0.08	-	-	
R2	0.08	-	0.20	
S	0.20	-	_	
	Tolerance of f	orm and position		
aaa	-	0.20	-	
bbb	-	0.20	_	
CCC	-	0.08	_	
ddd	-	0.08	_	
	VAR	IATIONS		
		5.0x6.0 (T1-T3) <sup>(3)</sup>		
D2	-	-	6.61	
E2	_		6.61	
D3	4.8		-	
E3	4.8			

#### Table 2. LQFP64 (10x10x1.4 mm exp. pad up) package mechanical data

1. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusion is "0.25 mm" per side.

2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.



3. Number, dimension and position of groves shown in Figure 5 are for reference only.

Figure 5. Exposed-pad groove's shapes



# **Revision history**

#### Table 3. Document revision history

Date	Version	Changes
28-Sep-2022	1	Initial release.



## Contents

1	Block and pins description diagrams				
	1.1	Block diagram	3		
	1.2	Pins description	4		
2	Appli	cation diagram	6		
3	Gene	ral introduction	7		
4	Packa	age information	8		
	4.1	[Package name] package information	8		
Revi	sion h	iistory1	1		

# List of tables

Table 1.	Pins list description
Table 2.	LQFP64 (10x10x1.4 mm exp. pad up) package mechanical data 9
Table 3.	Document revision history

# List of figures

Figure 1.	Block diagram	3
Figure 2.	Pins connection diagram	4
Figure 3.	Application diagram.	6
Figure 4.	LQFP64 (10x10x1.4 mm exp. pad up) package outline	8
Figure 5.	Exposed-pad groove's shapes 1	0

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