To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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DATA SHEET

RENESAS

MOS FIELD EFFECT TRANSISTOR

2SK2341

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2341 is N-channel Power MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
  $R_{DS(on)}$ = 0.26 Ω MAX. (V_{GS} = 10 V, I_D = 6.0 A)
- Low C_{iss} C_{iss} = 1090 pF TYP.
- High Avalanche Capability Ratings

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DSS}	250	V
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DC)}$	±11	A
Drain Current (pulse)	$I_{D(pulse)}$*	±44	A
Total Power Dissipation (T_C = 25 °C)	P_{T1}	35	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	2.0	W
Storage Temperature	T_{stg}	–55 to +150	°C
Channel Temperature	T_{ch}	150	°C
Single Avalanche Current	I_{AS}**	11	A
Single Avalanche Energy	E_{AS}**	320	mJ

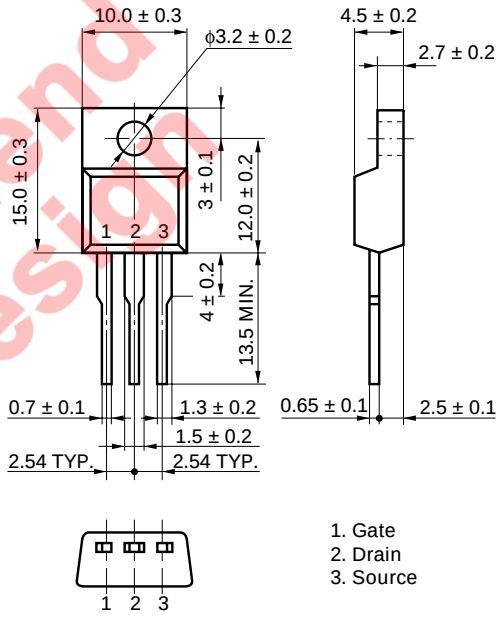
*PW ≤ 10 μs, Duty Cycle ≤ 1 %

**Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

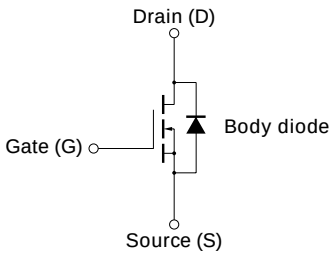
PACKAGE DIMENSIONS

(in millimeters)



1. Gate
2. Drain
3. Source

MP-45F(SIOLATED TO-220)



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(O.D. No. TC–8070)
Date Published January 1995 P
Printed in Japan

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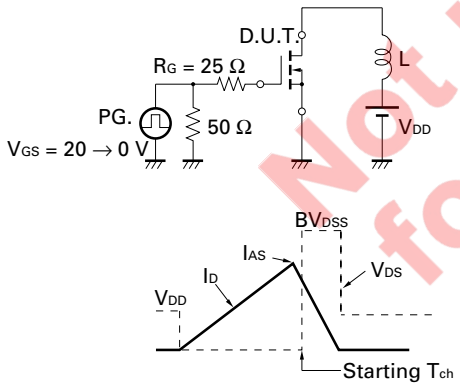
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ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

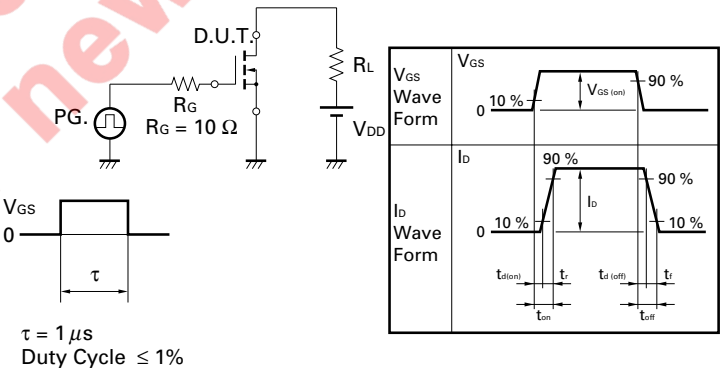
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.21	0.26	Ω	V_{GS} = 10 V, I_D = 6 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.0		4.0	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	3.0			S	V_{DS} = 10 V, I_D = 6 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 250V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		1090		pF	V_{DS} = 10 V
Output Capacitance	C_{oss}		420		pF	V_{GS} = 0
Reverse Transfer Capacitance	C_{rss}		80		pF	f = 1 MHz
Turn-On Delay Time	$t_{d(on)}$		20		ns	V_{GS} = 10 V
Rise Time	t_r		20		ns	V_{DD} = 150 V
Turn-Off Delay Time	$t_{d(off)}$		50		ns	I_D = 6 A, R_G = 10 Ω
Fall Time	t_f		15		ns	R_L = 25 Ω
Total Gate Charge	Q_G		33		nC	V_{GS} = 10 V
Gate to Source Charge	Q_{GS}		6.0		nC	I_D = 11 A
Gate to Drain Charge	Q_{GD}		13		nC	V_{DD} = 200 V
Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	I_F = 11 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		220		ns	1_F = 11 A
Reverse Recovery Charge	Q_{rr}		1.0		μC	di/dt = 50 A/μs

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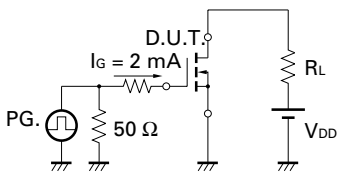
Test Circuit 1 : Avalanche Capability



Test Circuit 2 : Switching Time



Test Circuit 3 : Gate Charge

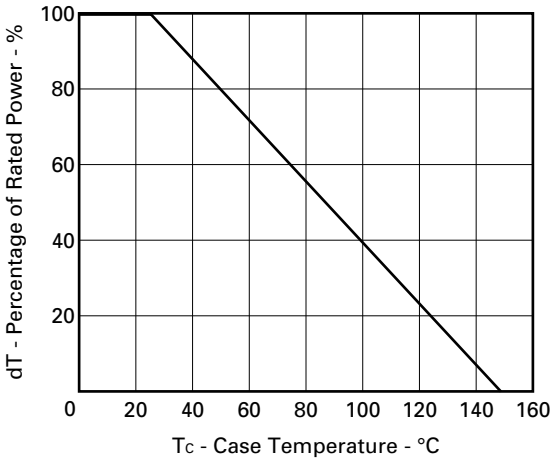


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

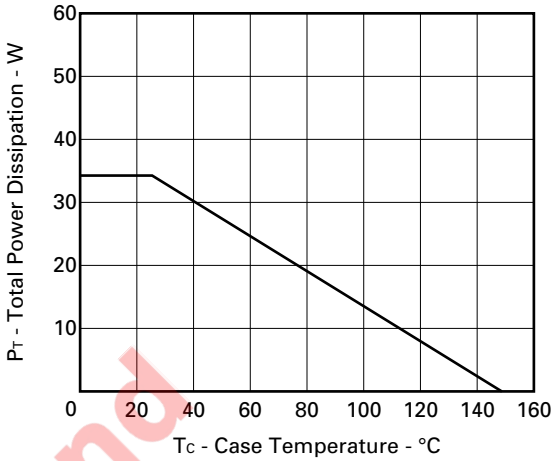
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TYPICAL CHARACTERISTICS (T_A = 25 °C)

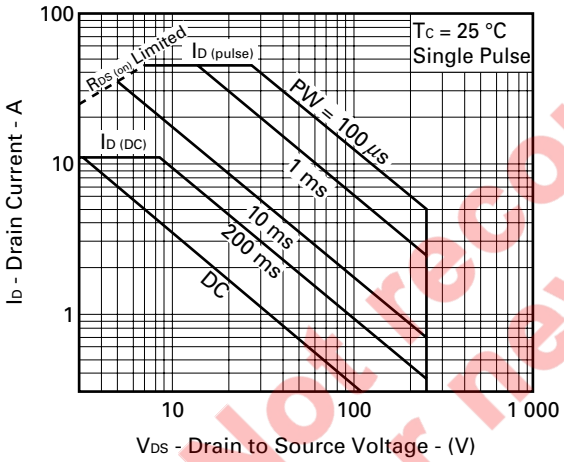
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



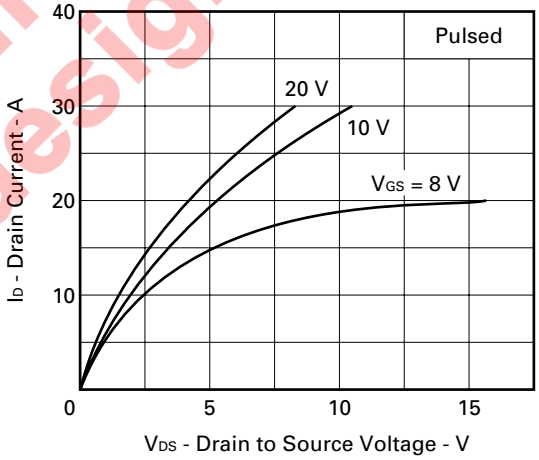
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



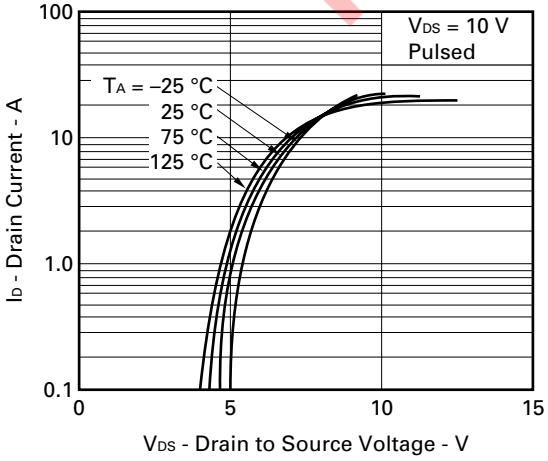
FORWARD BIAS SAFE OPRATING AREA



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



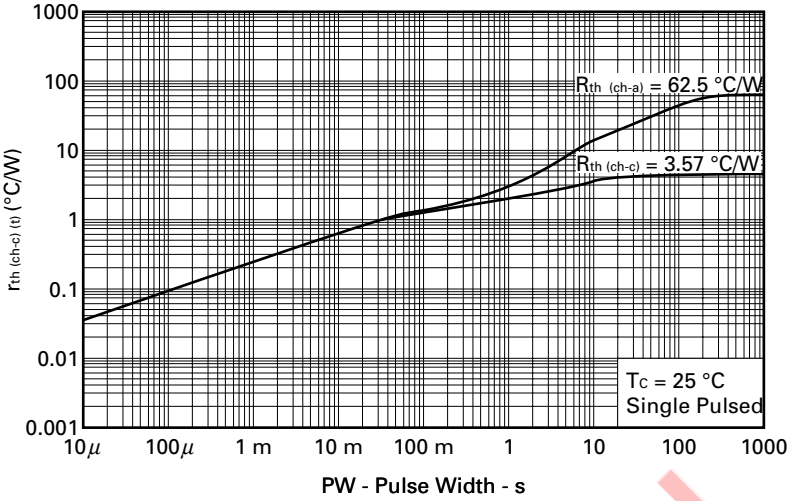
TRANSFER CHARACTERISTICS



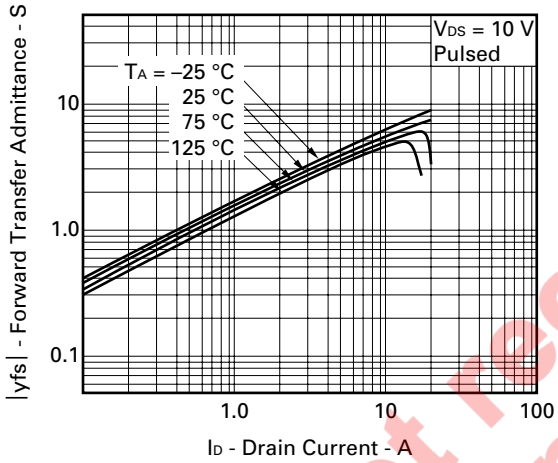
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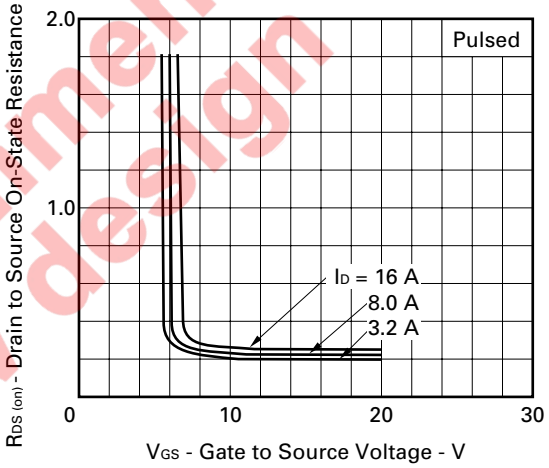
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



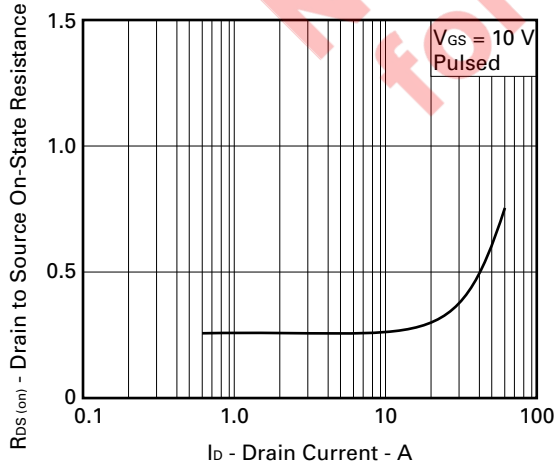
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



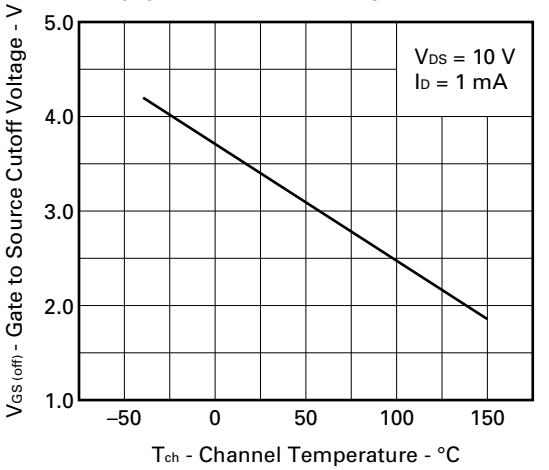
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



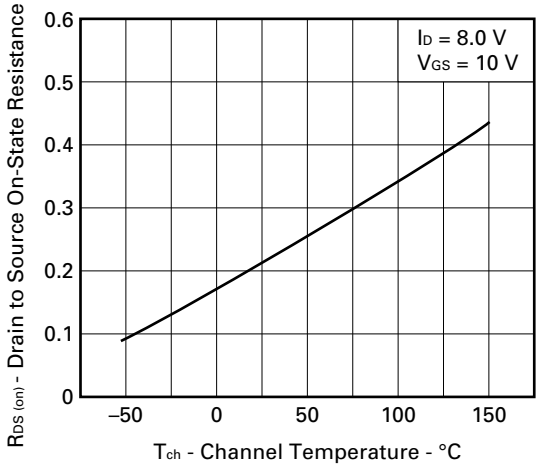
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



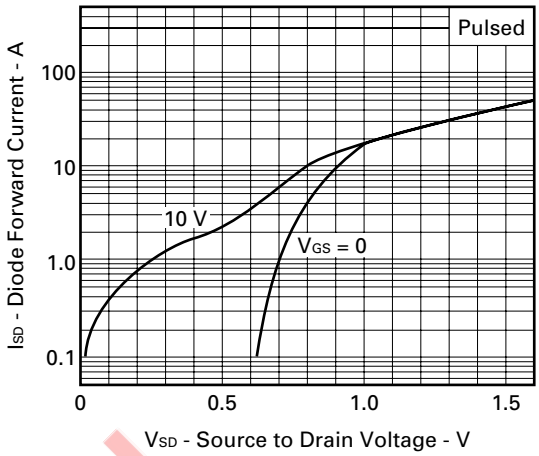
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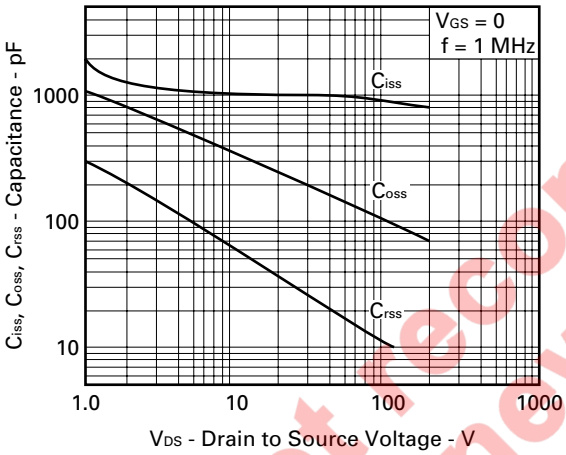
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



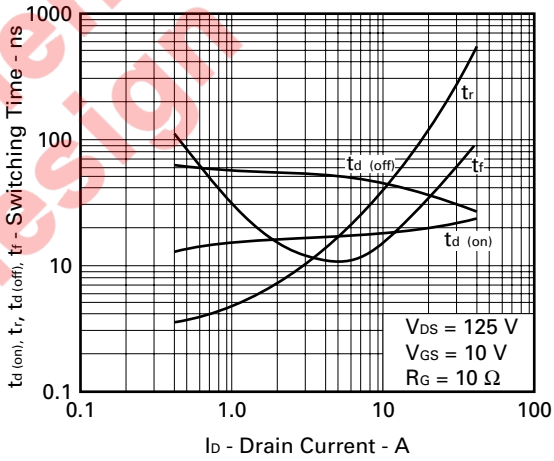
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

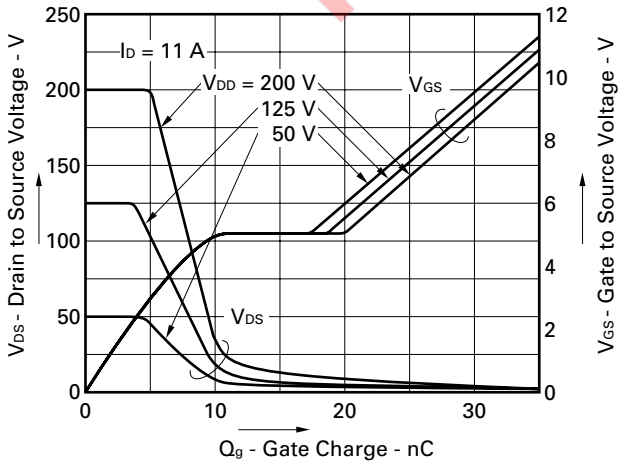


SWITCHING CHARACTERISTICS

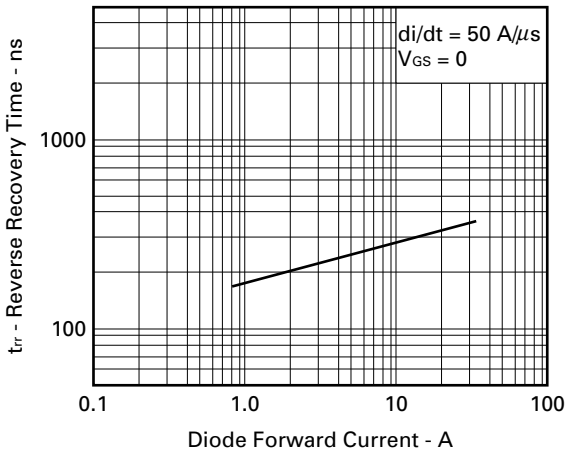


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DYNAMIC INPUT/OUTPUT CHARACTERISTICS

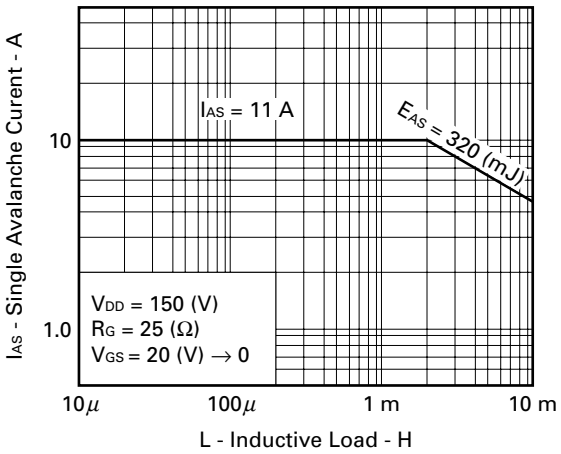


REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT

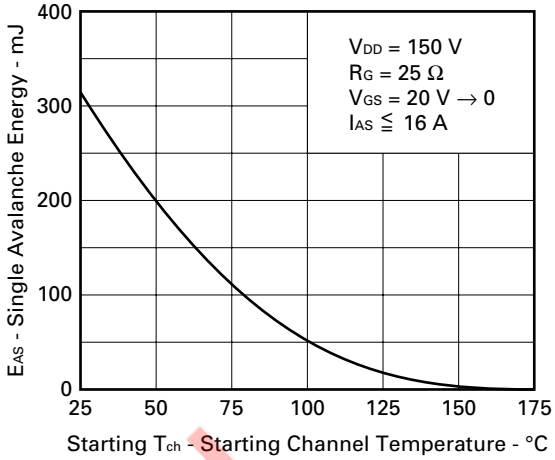


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SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE



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REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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