System Basis Chip

TLE9266-2QX

System Basis Chip

Body System IC with Integrated Voltage Regulators, Power Management Functions, HS-CAN and LIN Transceiver.
Featuring Multiple High-Side and Low-Side Switches including Wake Inputs.

Data Sheet

Rev. 1.1, 2014-02-01

Automotive Power

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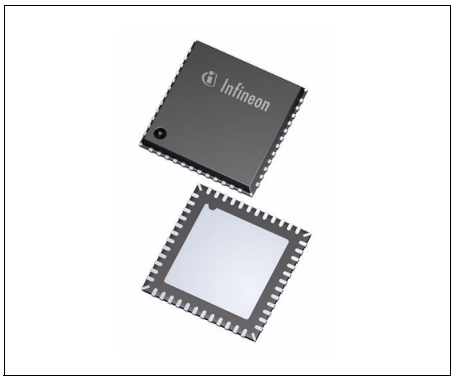
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1 Overview



PG-VQFN-48-31

Features

- Very low quiescent current consumption in Stop- and Sleep Mode
- Periodic cyclic sense in Normal-, Stop- and Sleep Mode
- Periodic cyclic wake in Normal- and Stop Mode
- Low-Drop Voltage Regulator 5V, 250mA
- Low-Drop Voltage Regulator 5V, 100mA, robust against short to VS
- High-Speed CAN Transceiver ISO11898-2/5
- LIN Transceiver LIN 2.2, J2602-2
- Two Low-Side Outputs for Relay Drive with active zener clamping
- Two High-Side Output 2Ω typ., Four High-Side Outputs 7Ω typ., e.g. for LED lighting, cyclic sensing, etc.
- Four independent PWM generators and two On/Off Timers
- Three universal High-Voltage Wake Inputs for voltage level monitoring with cyclic sense functionality
- Alternate High-Voltage Measurement Function, e.g. for battery voltage sensing
- One universal Low-Voltage Wake Input for voltage level monitoring with cyclic sense functionality
- SYNC input for external cyclic sense control via microcontroller
- Reset Output and Fail Output
- Over temperature and short circuit protection feature
- Wide input voltage and temperature range
- Green Product (RoHS compliant) & AEC Qualified

Description

The TLE9266-2QX is a monolithic integrated circuit in an exposed pad VQFN-48 (7mm x 7mm) power package. The device is designed for various CAN-LIN automotive body applications as a main supply for the microcontroller and as an interface for a CAN and LIN bus network

To support these applications, the System Basis Chip (SBC) provides the main functions, such as a 5V low-dropout voltage regulator (LDO) for microcontroller supply, a 5V low-dropout voltage regulator with short circuit protection against supply voltage VS for e.g. sensor supply, HS-CAN transceiver and LIN transceiver for data transmission, Low- and High-Side switches providing protective functions, and a 16-bit Serial Peripheral Interface (SPI) to control and monitor the device. Also implemented are a Window Watchdog circuit with a reset feature, a Fail Output and an under voltage reset feature.

The device offers low-power modes in order to support applications that are permanently connected to the battery. A wake up from the low-power mode is possible via a message on the buses, via the bi-level sensitive monitoring/wake-up inputs as well as via cyclic wake. The device is designed to withstand the severe conditions of automotive applications.

Type	Package	Marking
TLE9266-2QX	PG-VQFN-48-31	TLE9266-2QX

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2 Block Diagram

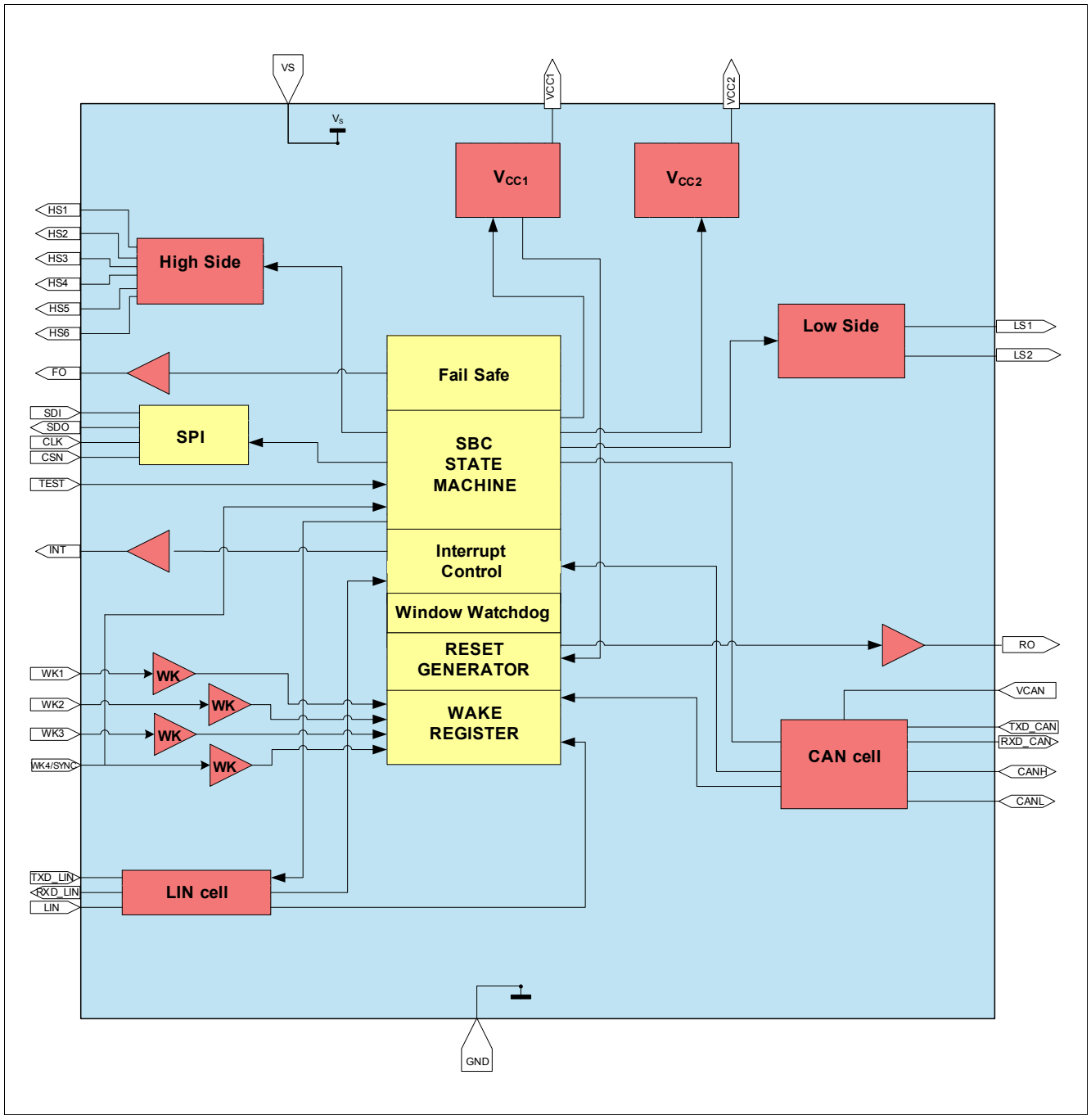


Figure 1 Block Diagram

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3 Pin Configuration

3.1 Pin Assignment

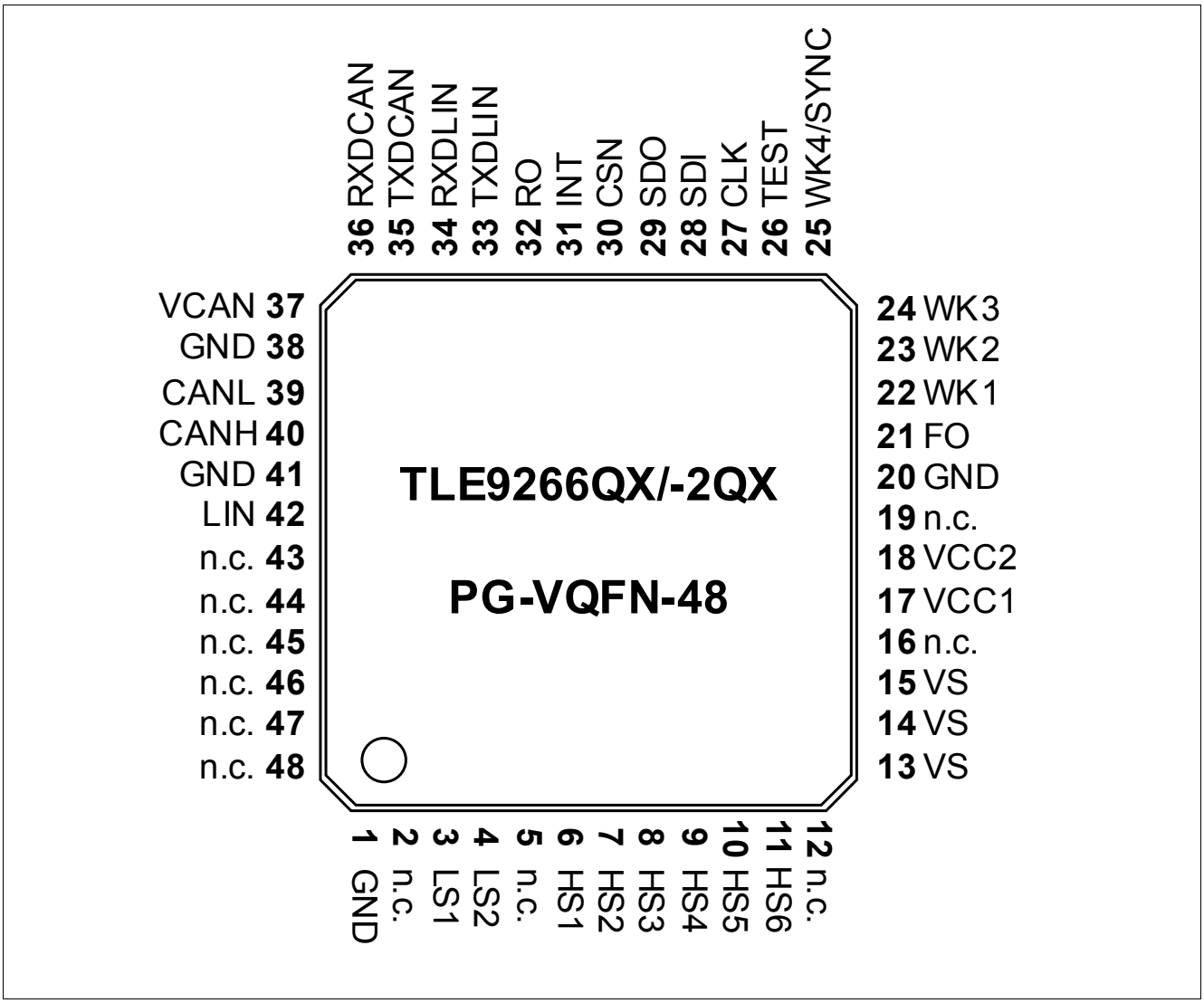


Figure 2 TLE9266 Pin Configuration

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3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**Ground;**
2	n.c.	**not connected;**
3	LS1	**Low-Side Output 1;**
4	LS2	**Low-Side Output 2;**
5	n.c.	**not connected;**
6	HS1	**High-Side Output 1;** typ. 2Ω
7	HS2	**High-Side Output 2;** typ. 2Ω.
8	HS3	**High-Side Output 3;** typ. 7Ω
9	HS4	**High-Side Output 4;** typ. 7Ω
10	HS5	**High-Side Output 5;** typ. 7Ω
11	HS6	**High-Side Output 6;** typ. 7Ω
12	n.c	**not connected;**
13	VS	**Supply Voltage;** Connected to Battery Voltage with Reverse protection Diode and Filter against EMC
14	VS	**Supply Voltage;** Connected to Battery Voltage with Reverse protection Diode and Filter against EMC
15	VS	**Supply Voltage;** Connected to Battery Voltage with Reverse protection Diode and Filter against EMC
16	n.c.	**not connected;**
17	VCC1	**Voltage Regulator Output 1;**
18	VCC2	**Voltage Regulator Output 2;**
19	n.c.	**not connected**
20	GND	**GND;**
21	FO	**Fail Output;**
22	WK1	**Wake Input 1;**
23	WK2	**Wake Input 2;**
24	WK3	**Wake Input 3;**
25	WK4/SYNC	**Wake Input 4 (Low-Voltage) / Synchronization Input for cyclic sense / cyclic wake;**
26	TEST	**TEST Pin;**
27	CLK	**SPI Clock Input;**
28	SDI	**SPI Data Input;** into SBC (=MOSI)
29	SDO	**SPI Data Output;** out of SBC (=MISO)
30	CSN	**SPI Chip Select Not Input;**
31	INT	**Interrupt Output;**
32	RO	**Reset Output;**
33	TXDLIN	**Transmit LIN;**
34	RXDLIN	**Receive LIN;**
35	TXDCAN	**Transmit CAN;**

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Pin	Symbol	Function
36	RXDCAN	**Receive CAN;**
37	VCAN	**Supply Input;** for internal HS-CAN cell
38	GND	**GND;**
39	CANL	**CAN Low Bus Pin;**
40	CANH	**CAN High Bus Pin;**
41	GND	**Ground;**
42	LIN	**LIN Bus;** Bus line for the LIN interface, according to ISO. 9141 and LIN specification 2.2 as well as SAE J2602-2.
43	n.c.	**not connected;**
44	n.c.	**not connected;**
45	n.c.	**not connected;**
46	n.c.	**not connected;**
47	n.c.	**not connected;**
48	n.c.	**not connected;**
Cooling Tab	GND	**Cooling Tab - Exposed Die Pad**; For cooling purposes only, do not use as an electrical ground.[1)]

1) The exposed die pad at the bottom of the package allows better power dissipation of heat from the SBC via the PCB. The exposed die pad is not connected to any active part of the IC an can be left floating or it can be connected to GND (recommended) for the best EMC performance.

Note: All VS Pins must be connected on the PCB;
all GND pins as well as the Cooling Tap must be also connected on the PCB

3.3 Hints for Unused Pins

It must be ensured that the correct configurations are also selected via SPI, e.g. when connecting WKx to GND, then the respective WK pin must be disabled as wake source and the correct pull-up/-down configuration must be selected:

- WK1/2/3/4: connect to GND and configure correctly
- LS1/2: leave open
- HSx: leave open
- RO / FO: leave open
- INT: leave open
- VCAN: Connect to VCC1
- CANH/CANL: leave open
- LIN: leave open
- TEST: leave open for normal operation. Connect to VCC1 to enter SBC Development Mode

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3.4 Hints for Alternate Pin Functions

In case of alternate pin functions, it must be ensured that the correct configurations are also selected via SPI, in case it is not done automatically. Please consult the respective chapter. In addition, following topics shall be considered:

- WK4 / SYNC pin: The pin can be either used as a low-voltage wake pin or as a control pin for cyclic sense / cyclic wake, The respective function can be selected via the SPI bit **WK4_SYNC**. See also **Chapter 12.2.1**.
- WK1..2: The pins can be either used as HV wake / voltage monitoring inputs or for a voltage measurement function. The respective function can be selected via the SPI bit **WK_MEAS**. In the later case, the WK1..2 pins shall not be used / assigned for any wake detection nor cyclic sense functionality because any level changes at the pins will be ignored. See also **Chapter 12.2.2**.

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4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply Voltage	$V_{s,\,max}$	-0.3	–	28	V	–	P_4.1.1
Supply Voltage	$V_{s,\,max}$	-0.3	–	40	V	Load Dump, max. 400 ms	P_4.1.2
Voltage Regulator 1 Output	$V_{CC1,\,max}$	-0.3	–	5.5	V	–	P_4.1.3
Voltage Regulator 2 Output	$V_{CC2,\,max}$	-0.3	–	V_S + 0.3	V	–	P_4.1.4
Wake Inputs 1...3	$V_{WK,\,max}$	-0.3	–	40	V	–	P_4.1.5
High-Side 1...6	$V_{HS,\,max}$	-0.3	–	V_S + 0.3	V	–	P_4.1.6
Low-Side 1...2, FO	$V_{LS,\,max}$	-0.3	–	40	V	DC value only	P_4.1.7
LIN, CANH, CANL	$V_{BUS,\,max}$	-27	–	40	V	–	P_4.1.8
Logic Input / Output Voltage, TEST Pin, WK4/SYNC	$V_{IO,\,max}$	-0.3	–	V_{CC1} + 0.3	V	–	P_4.1.9
VCAN Input Voltage	$V_{VCAN,\,max}$	-0.3	–	5.5	V	–	P_4.1.10
Currents							
Wake Inputs 1..2	$I_{WK1,2,\,max}$	-500		500	µA	2)	P_4.1.11
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.12
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.13
ESD Susceptibility							
ESD Resistivity all pins	V_{ESD}	-2	–	2	kV	HBM[3)]	P_4.1.14
ESD Resistivity CANH, CANL, LIN vs. GND	V_{ESD}	-8	–	8	kV	HBM[4)3)]	P_4.1.15
ESD Resistivity vs. GND	V_{ESD}	-500	–	500	V	CDM[5)]	P_4.1.18
ESD Resistivity Pin 1, 12,13,24,25,36,37,48 (corner pins) vs. GND	$V_{ESD1,12,13,24,25,36,37,48}$	-750	–	750	V	CDM[5)]	P_4.1.19

1) Not subject to production test, specified by design.

2) Applies only if WK1 and WK2 are configured as alternative HV-measurement function

3) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001 (1.5kΩ, 100pF)

4) ESD “GUN” Resistivity 6KV information according to IEC61000-4-2 “gun test” (330Ω, 150pF) is shown in Application Information in **Chapter 17.2**

5) ESD susceptibility, Charged Device Model “CDM” according to EIA/JESD22-C101 or ESDA STM5.3.1,

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Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage	$V_{S,func}$	V_{POR}	–	28	V	1) V_{POR} see section **Chapter 15.10**	P_4.2.1
LIN Supply Voltage	$V_{S,LIN}$	6	–	18	V	2)	P_4.2.2
CAN Supply Voltage	V_{CAN}	4.75	–	5.25	V	–	P_4.2.3
SPI frequency	f_{SPI}	–	–	4	MHz	see **Chapter 16.7** for $f_{SPI,max}$	P_4.2.4
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.5

1) Including Power-on Reset, Over- and Under voltage Protection

2) Parameter Specification according to LIN 2.2 standard

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Device behavior outside of specified functional range:

- 28V < $V_{S,func}$ < 40V: Device will still be functional including the state machine; the specified electrical characteristics might not be ensured anymore. The regulators VCC1/2 are working properly; however, a thermal shutdown might occur due to high power dissipation.
  HSx switches might be turned OFF depending on VS_OV configurations.;
  The absolute maximum ratings are not violated, however the device operation at high junction temperatures for long periods might reduce the operating life time;
- 18V < $V_{S,LIN}$ <28V: The LIN transceiver is still functional. However, the communication might fail due to out-of-spec operation;
- V_{CAN} < 4.75V: The undervoltage bit **VCAN_UV** will be set in the SPI register **BUS_CTRL** and the transmitter will be disabled as long as the UV condition is present;
- 5.25V < V_{CAN} < 5.50V: CAN transceiver still functional. However, the communication might fail due to out-of-spec operation;
- 5.5V < V_S < 28V: Parameter specification applies;
- $V_{POR,f}$ < V_S < 5.5V: Device will be still be functional; the specified electrical characteristics might not be ensured anymore. The LIN transmitter will be disabled if V,UVD,f is reached; HSx switches might be turned OFF depending on VS_UV configurations. The voltage regulators will enter the low-drop operation mode.
  A VCC1_UV reset could be triggered depending on the Vrtx settings

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4.3 Thermal Resistance

Table 3 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	6	–	K/W	Exposed Pad	P_4.3.1
Junction to Ambient	R_{thJA}	–	33	–	K/W	2)	P_4.3.2

1) Not subject to production test, specified by design.

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board for 1.5W. Board: 76.2x114.3x1.5mm³ with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm2 cooling area on the bottom layer (70µm).

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4.4 Current Consumption

Table 4 Current Consumption[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SBC Normal Mode							
Normal Mode current consumption	I_{Normal}	–	3.5	6	mA	VCC2 ON (no load); CAN, LIN, HSx, LSx = OFF	P_4.4.1
SBC Stop Mode							
Stop Mode current Consumption	$I_{Stop,25}$	–	40	53	µA	VCC2, HSx = OFF; CAN, LIN, WKx not wake capable.	P_4.4.2
Stop Mode current Consumption	$I_{Stop,85}$	–	50	70	µA	T_j = 85°C[2)]; VCC2, HSx = OFF; CAN, LIN, WKx not wake capable.	P_4.4.3
SBC Sleep Mode							
Sleep Mode current consumption	$I_{Sleep,25}$	–	14	22	µA	VCC2, HSx = OFF; CAN, LIN, WKx not wake capable	P_4.4.7
Sleep Mode current consumption	$I_{Sleep,85}$	–	25	35	µA	T_j = 85°C[2)]; VCC2, HSx = OFF; CAN, LIN, WKx not wake capable	P_4.4.8
Feature Incremental Current Consumption							
Current consumption for CAN module, recessive state	$I_{CAN,rec}$	–	3	5.5	mA	SBC Normal Mode; CAN Normal Mode; VCC2 connected to VCAN; VTXDCAN = VCC1; no RL on CAN	P_4.4.18
Current consumption for CAN module, dominant state	$I_{CAN,dom}$	–	5	6.5	mA	[2)]SBC Normal Mode; CAN Normal Mode; VCC2 connected to VCAN; VTXDCAN = GND; no RL on CAN	P_4.4.19
Current consumption for CAN module, Receive Only Mode	$I_{CAN,RcvOnly}$	–	1.35	1.50	mA	[2)]SBC Stop Mode; CAN Receive Only Mode; VCC2 connected to VCAN; VTXDCAN = VCC1; no RL on CAN	P_4.4.20
Current consumption for LIN module, recessive state	$I_{LIN,rec}$	–	0.5	1.5	mA	SBC Normal Mode; LIN Normal Mode; VTXDLIN = VCC1; no RL on LIN	P_4.4.22

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Table 4 Current Consumption[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current consumption for LIN module, dominant state	$I_{LIN,dom}$	–	1.2	2.0	mA	[2)]SBC Normal Mode; LIN Normal Mode; VTXDLIN = GND; no RL on LIN	P_4.4.23
Current consumption for LIN module, Receive Only Mode	$I_{LIN,RcvOnly}$	–	0.5	1.1	mA	[2)]SBC Stop Mode; LIN Receive Only Mode; VTXDLIN = VCC1; no RL on LIN	P_4.4.24
Current consumption for WK1..3 wake capability	$I_{Wake,WKx,25}$	–	5	7.5	µA	[3)] SBC Sleep Mode; WK1..3 wake capable; LIN,CAN = OFF	P_4.4.15
Current consumption for LIN wake capability	$I_{Wake,LIN,25}$	–	3	4	µA	SBC Sleep Mode; LIN wake capable; WK1..3, CAN = OFF	P_4.4.16
Current consumption for CAN wake capability	$I_{Wake,CAN,25}$	–	5	6	µA	[2)]SBC Sleep Mode; CAN wake capable; WK1..3, LIN = OFF	P_4.4.17
Current consumption for VCC2 in SBC Stop Mode	$I_{Stop,VCC2,25}$	–	20	26	µA	SBC Stop Mode; VCC2 = ON (no load); LIN, CAN, WK1..3 = OFF	P_4.4.28
Current consumption for VCC2 in SBC Stop Mode	$I_{Stop,VCC2,85}$	–	22	28	µA	[2)]SBC Stop Mode; T_j= 85°C; VCC2 = ON (no load); LIN, CAN, WK1..3 = OFF	P_4.4.29
Current consumption for cyclic sense function	$I_{Stop,C25}$	–	20	26	µA	[4)]SBC Stop Mode;	P_4.4.32

1) The current consumption values are specified with T_j = 25°C, V_S = 13.5V, no load on VCC1 and TEST = 0V (unless otherwise specified). Current consumption adders of features in SBC Stop Mode also apply for SBC Sleep Mode (unless otherwise specified).

2) Specified by design; not subject to production test.

3) No pull-up or pull-down configuration selected. The current consumption in SBC Stop Mode cannot be reduced by disabling the WK1..3 as wake sources because the current is needed for the voltage level monitoring.

4) HS2 used for cyclic sense, Timer 2, 20ms period, 0.1ms on-time, no load on HS2.
In general the current consumption adder for cyclic sense in SBC Stop Mode can be calculated with below equation:
$I_{Stop,CS}$ = 18µA + (700µA *t_{ON}/T_{Per})

Note: To achieve the target low-quiescent current consumption the user must make sure to set the pull-up or pull-down current sources for the WKx pins accordingly or to disable them.

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5 System Features

This chapter describes the system features and behavior of the TLE9266-2QX:

- State machine
- SBC mode control
- State of supply and peripherals
- System functions such as cyclic sense, cyclic wake or PWM control of HS
- Supervision and diagnosis functions

The System Basis Chip is controlled via a 16-bit SPI interface. A detailed description can be found in **Chapter 16**.The configuration as well as the diagnosis is handled via the SPI. The SPI mapping of the TLE9266-2QX is compatible to other devices of the TLE92xx family.

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5.1 Block Description State Machine

The different SBC Modes are selected via SPI by setting the respective SBC **MODE** bits in the register **M_S_CTRL**. The SBC **MODE** bits are cleared when going through SBC Restart Mode and thus always show the current SBC mode.

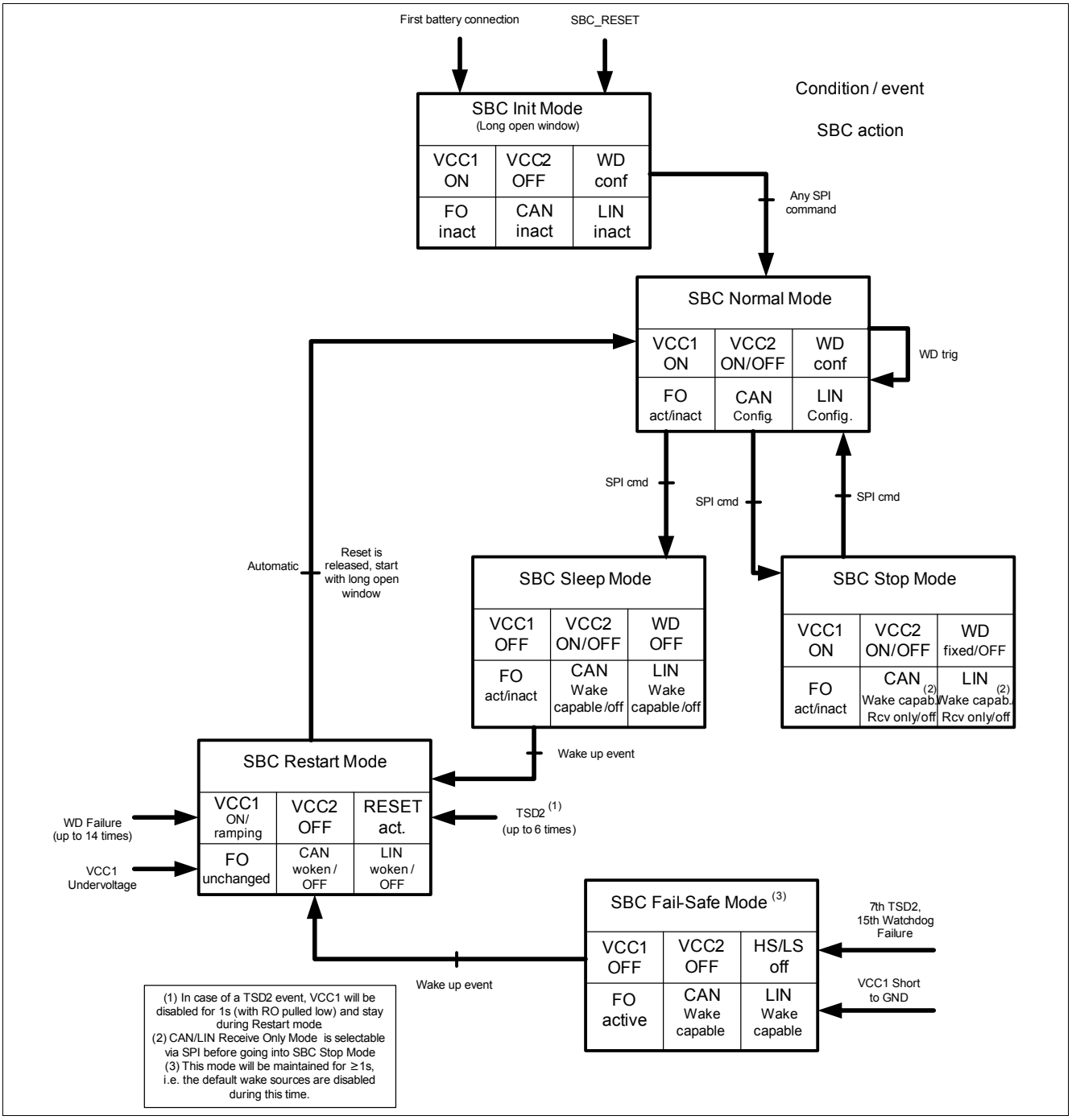


Figure 3 State Diagram showing the SBC Operating Modes

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5.1.1 SBC Init Mode

The SBC starts up in SBC Init Mode after crossing the $V_{POR,r}$ threshold and the window watchdog will start with a long open window. The SBC waits for the microcontroller to finish its startup and initialization sequence. From this transition mode, the SBC can be switched via SPI command to the main operating mode - SBC Normal Mode. Any SPI command will bring the SBC to SBC Normal Mode.

Wake-up events are ignored during SBC Init Mode and will therefore be lost.

*Note: For a safe start-up, it is recommended to send first a SPI command that triggers the watchdog and sets the watchdog configuration. The watchdog triggering is achieved by writing to the watchdog register **WD_CTRL**. After powering up, the watchdog must be triggered within the long-open window t_{LW} to avoid a watchdog failure reset.*

*Note: In case of slow supply voltage ramps at power up the SPI flags **VCC1_UV** and **FAILURE** will not be updated and FO will not be triggered as long as VCC1 is below the $V_{RT1,r}$ threshold. However, the RO pin will be pulled LOW and will stay LOW for at least t_{RD1}. The SBC Fail-Safe Mode will be entered if the VCC1 output voltage has not crossed the $V_{CC1,SC}$ after the filter time $t_{VCC1,SC}$.*

5.1.2 SBC Normal Mode

The SBC Normal Mode is the standard operating mode for the SBC. All configurations have to be done in SBC Normal Mode before entering a low-power mode. A wake-up event on CAN, LIN and WKx will create an interrupt on pin INT - however, no change of SBC mode will occur. The configuration options are listed below:

- VCC1 is active
- VCC2 can be switched on or off (default = OFF)
- CAN is configurable (OFF, wake capable, Receive Only, ON)
- LIN is configurable (OFF, wake capable, Receive Only, ON)
- Outputs can be switched on or off (default = OFF)
- Wake pins show the input level
- Cyclic sense and cyclic wake can be selected

5.1.3 SBC Stop Mode

The SBC Stop Mode is the first level technique to reduce the overall current consumption. In this mode, VCC1 is still active and supplying the microcontroller, which can enter a power down mode. The VCC2 supply as well as the HSx outputs can be configured to stay enabled. The settings have to be done before entering SBC Stop Mode. A wake-up event on CAN, LIN and WKx will create an interrupt on pin INT - however, no change of SBC mode will occur. The configuration options are listed below:

- VCC1 is ON
- VCC2 can be ON or OFF
- CAN can be selected for ‘Receive Only Mode’ and to be wake capable (interrupt) or OFF
- LIN can be selected for ‘Receive Only Mode’ and to be wake capable (interrupt) or OFF
- WK pins show the input level and can be selected to be wake capable (interrupt)
- HS1...6 can be switched on or can be controlled by PWM
- LS driver are OFF
- Cyclic sense can be done with HS1...6 and Timer 1 or Timer 2;
- Cyclic wake is selectable in SBC Stop Mode with Timer 1 or Timer 2;
- Watchdog can be disabled via SPI or is automatically disabled if IVCC1< I_{WD_OFF} (see **Chapter 15.2.3**)

*Note: If switches are enabled during sleep mode, e.g. HSx on with or without PWM, then the SBC current consumption will increase (**Chapter 4.4**).*

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Note: It is not possible to switch directly from SBC Stop Mode to SBC Sleep Mode. Doing so will also set the ***SPI_FAIL*** flag and will bring the SBC into SBC Restart Mode.

5.1.4 SBC Sleep Mode

The SBC Sleep Mode is the second level technique to reduce the current overall consumption to a minimum needed to react on wake-up events or for the SBC to perform autonomous actions (e.g. cyclic sense). In this mode, VCC1 is OFF and not supplying the microcontroller anymore.The VCC2 supply as well as the HSx outputs can be configured to stay enabled. The settings have to be done before entering SBC Sleep Mode. A wake-up event on CAN, LIN or WKx will bring the device via SBC Restart Mode into SBC Normal Mode again and signal the wake source. The configuration options are listed below:

- VCC1 is OFF
- VCC2 can be switched on or OFF
- CAN can be selected to be wake capable or OFF
- LIN can be selected to be wake capable or OFF
- WK pins can be selected to be wake capable
- HS1...6 can be switched on or can be controlled by PWM
- LS drivers are OFF
- Cyclic sense can be done with HS1...6 and Timer 1 and Timer 2
- The watchdog is OFF

It is not possible to switch off all wake sources in SBC Sleep Mode. Doing so will set the **SPI_FAIL** flag and will bring the SBC into SBC Restart Mode.

All settings must be done before entering SBC Sleep Mode.

Note: If switches are enabled during sleep mode, e.g. HSx ON with or without PWM, then the SBC current consumption will increase

5.1.5 SBC Restart Mode

There are multiple reasons to enter the SBC Restart Mode. The purpose of the SBC Restart Mode is to reset the microcontroller:

- in case of under voltage on VCC1 in SBC Normal and in SBC Stop Mode,
- due to incorrect watchdog triggering (for the first 14 times, then SBC Fail-Safe Mode is entered),
- due to an overall thermal shutdown (TSD2) event (the first 6 times within one minute - see also **Chapter 15.9**). SBC Restart Mode will be maintained for 1s in this case to avoid thermal toggling,
- In case of a wake-up event from SBC Sleep Mode, this transition is used to ramp up VCC1 after wake in a defined way.

From SBC Restart Mode, the SBC goes automatically to SBC Normal Mode, i.e the mode is left automatically by the SBC without any microcontroller influence. The SBC **MODE** bits are cleared. The Reset Output (RO) is pulled LOW when entering Restart Mode and is released at the transition to Normal Mode after the reset delay time (t_{RD1}). The watchdog timer will start with a long open window starting from the moment of the rising edge of RO. However, the watchdog period setting in the register **WD_CTRL** remains unchanged.

Leaving the SBC Restart Mode will not result in changing / deactivating the Fail output.

The configuration options are listed below:

- VCC1 is ON or ramping up,
- VCC2 will be disabled if it was activated before,
- CAN and LIN transceivers are “woken” in case of a wake-up event in SBC Sleep Mode or SBC Fail-Safe Mode, wake capable when they were ON or in “Receive Only” before Restart Mode, or OFF if they were OFF before the SBC Restart Mode (See also Chapter **Chapter 10** and **Chapter 11** and register **BUS_CTRL**),
- The HS1...6 will be disabled if they were activated before,
- LS switches are switched off automatically,

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- RO is pulled LOW during SBC Restart Mode
- The SPI communication is ignored by the SBC, i.e. it is not interpreted,

Table 5 Reasons for Restart - State of SPI Status bits after return to Normal Mode

SBC Mode	Event	DEV_STAT	TSD2	WD_FAIL	VCC1_UV	VCC1_SC
Normal	Watchdog Failure	01	xxx	0001...1110	x	0
Normal	TSD2	01	001...110	xxxx	x	0
Normal	VCC1 under voltage reset	01	xxx	xxxx	1	0
Stop Mode	Watchdog Failure	01	xxx	0001...1110	x	0
Stop Mode	TSD2	01	001...110	xxxx	x	0
Stop Mode	VCC1 under voltage reset	01	xxx	xxxx	1	0
Sleep Mode	Wake-up event	10	xxx	xxxx	x	0
Fail-Safe	Wake-up event	01	see “Reasons for Fail-Safe, **Table 6**”			

*Note: In case of a TSD2 event, VCC1 is switched off and the device remains in SBC Restart Mode for 1s to allow cooling down of the chip. Afterwards the reset is released and SBC Normal Mode is entered. The **TSD2** counter will be increased if the TSD event occurred within one minute. In case of a WD failure event, the SBC Restart Mode is also entered and the **WD_FAIL** counter is increased up to 14x.*

5.1.6 SBC Fail-Safe Mode

The Fail-Safe Mode is automatically reached after 7 times over temperature (TSD2) within 1 minute, after 15 watchdog fails, or if VCC1 is shorted to GND. In this case, the default wake sources (see register **WK_CTRL_1** and **BUS_CTRL**) are activated, the wake-up events are cleared in the register **WK_STAT**, and all output drivers and both voltage regulator are switched off. This mode will be maintained for at least 1s to avoid any fast toggling behavior. All wake sources will be disabled during this time. Leaving the SBC Fail-Safe Mode will not result in deactivation of the Fail Output pin. The following functions are influenced during Fail-Safe Mode:

- FO is activated
- VCC1 is OFF
- VCC2 is OFF
- CAN is wake capable
- LIN is wake capable
- HS1...6 are OFF
- LS driver are OFF
- WK1...3 pins are wake capable, WK4 is disabled
- Cyclic sense and cyclic wake is disabled, static sense is active with default filter time

Table 6 Reasons for Fail-Safe - State of SPI Status bits after return to Normal Mode

SBC Mode	Event	DEV_STAT	TSD2	WD_FAIL	VCC1_UV	VCC1_SC
Normal	15 x watchdog failure	01	xxx	1111	x	0
Normal	7 x TSD2	01	111	xxxx	x	0
Normal	VCC1 short to GND	01	xxx	xxxx	1	1
Stop Mode	15 x watchdog failure	01	xxx	1111	x	0
Stop Mode	7 x TSD2	01	111	xxxx	x	0
Stop Mode	VCC1 short to GND	01	xxx	xxxx	1	1

Note: After 7 TSD2 within 1 min. the SBC goes to SBC Fail-Safe Mode. The time is counted starting from the first TSD2 event. If the minute passed and less than 7 TSD2 events occurred, then the first event is discarded

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and the minute is considered to be counted from the second event and so on. A wake-up event will lead via SBC Restart Mode to SBC Normal Mode. The TSD2 register will show "7" to signal that Fail-Safe was reached due to 7 TSD2 events. The TSD2 register can then be cleared by SPI, i.e. it is not cleared automatically. With the next TSD2 event the device will go to Restart Mode, and show TSD2 = "1" regardless if the TSD2 register was cleared before the event. The counter will start new.

Note: After 15 watchdog failures the SBC goes to SBC Fail-Safe Mode. A wake-up event will lead via SBC Restart Mode to SBC Normal Mode. The WD_FAIL register will show "15" to signal that SBC Fail-Safe Mode was reached due to 15x watchdog failure. The WD_FAIL register is cleared by a correct Watchdog Trigger or can be cleared by SPI. With the next watchdog failure the device will go to SBC Restart Mode, and show WD_FAIL = "1" regardless if the WD_FAIL register was cleared before the event. The counter will start new.

5.1.7 SBC Development Mode

The SBC Development Mode is used during development phase of the module, especially for software development. The mode is reached by setting the TEST pin to HIGH. In this mode, the watchdog does not need to be triggered. No reset is triggered because of watchdog failure, SBC Fail-Safe Mode is not reached after 15 watchdog fails.

If the TEST pin is set from HIGH to LOW during operation, then the watchdog starts with a long open window.

Independent from the SBC Development Mode, there is the possibility by testing the FO output, i.e. if setting the FO pin to LOW will create the intended behavior within the system. The FO output can be enabled by the microcontroller by setting the **FO_ON** SPI bit.

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5.2 Cyclic Sense and Cyclic Wake Feature

Both features are intended to reduce the quiescent current of the device and application.
In the cyclic sense configuration, one or more high-side drivers are switched on periodically (controlled by a timer) and supplies an external circuitry e.g. switches and/or resistor array, which is connected to one or more wake inputs (see **Figure 4**). Any edge change of the WKx input signal causes a wake. The behavior of the WK4 pin is the same as the WK1..3 pins even though it is a 5V-pin only. Depending on the SBC mode, either the INT is pulled LOW (SBC Normal Mode and SBC Stop Mode) or the SBC is enabling the VCC1 (after SBC Sleep Mode).

Cyclic Wake means that a timer is enabled as an internal wake source (in SBC Normal and SBC Stop Mode) and causes periodic interrupt at the timer overflow.

Two timers are integrated and can be used for cyclic sense and/or cyclic wake. The timers can be mapped to the dedicated HS outputs by SPI (via **HS_CTRL1**...3). Both timers have the same configuration options but can be configured independently.

In addition, cyclic sense can also be controlled via the SYNC pin. In this case the WK4/SYNC pin needs to be configured by setting the bit **WK4_SYNC** (default = ‘0’). See also **Chapter 12** for more information regarding the cyclic sense configuration of SYNC and the WKx pins.

5.2.1 Timer 1

The Timer 1 is typically used to wake-up the microcontroller periodically or to do cyclic sense on the wake inputs with assigned HS switches (= cyclic sense).

Following periods and on-times can be selected via the register **TIMER1_CTRL**:

- Period: 10ms / 20ms / 50ms / 100ms / 200ms / 1s / 2s / controllable via SYNC
- On-time: 0.1ms / 0.3ms / 1.0ms / 10ms / 20ms / controllable via SYNC / OFF at HIGH or LOW

5.2.2 Timer 2

The Timer 2 is identical to Timer 1 but can be operated completely independently, e.g. Timer1 is used for cyclic sense and Timer2 is used for cyclic wake.

Following periods and on-times can be selected via the register **TIMER2_CTRL**:

- Period: 10ms / 20ms / 50ms / 100ms / 200ms / 1s / 2s / controllable via SYNC
- On-time: 0.1ms / 0.3ms / 1.0ms / 10ms / 20ms / controllable via SYNC / OFF at HIGH or LOW

5.2.3 Cyclic Sense

The principle of the cyclic sense function is shown in **Figure 4** in a simplified block diagram. As mentioned, the SYNC pin can also be used to control the cyclic sense function.

The first sample of the WK input value (HIGH or LOW) is taken as the reference for the next cycle.
A wake from SBC Sleep Mode or an Interrupt in SBC Stop- or Normal Mode via WK pin can therefore only happen with the second cycle (on-time) and onwards.

During Cyclic Sense, **WK_LVL_STAT** is updated and only with the samples voltage levels of the WKx pins in SBC Normal and SBC Stop Mode.

If SYNC is selected to control the cyclic sense or cyclic wake timing, then the WK4/SYNC pin is automatically configured with a pull down (**WK4_PUPD** = ‘01’) but register values will be kept. When SYNC is selected to stop the on-time, then the default filter time (see **WK_FLT_CTRL**) is selected.

Note: When SYNC is selected in cyclic sense for either starting the period or the end of the on-time it is recommended to also select SYNC for the other parameter, i.e. ending the on-time or starting the period.

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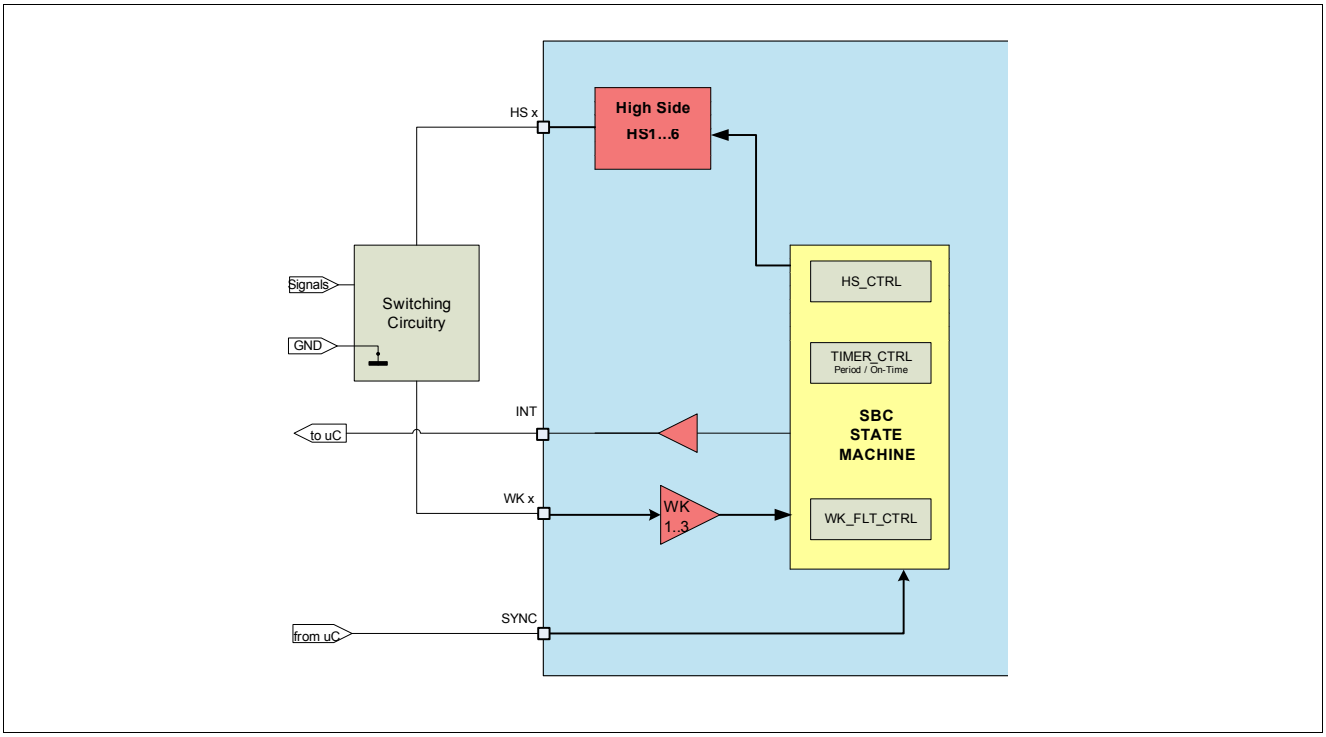


Figure 4 Cyclic Sense Working Principle including SYNC Control

5.2.3.1 Configuration and Start of Cyclic Sense

The correct sequence to configure the cyclic sense is shown in **Figure 5**. The settings “OFF / LOW” and “OFF / HIGH” define the voltage level of the respective HS driver before the start of the cyclic sense. The intention of this selection is to avoid an unintentional wake due to a voltage level change at the start of the cyclic sense.

Cyclic sense (=TimerX) will start as soon as the respective on-time has been selected independently from the assignment of the HS and filter configuration. The selection of Config C/D (see **Chapter 12.2.1**) must therefore be done before starting the timer. The correct configuration sequence is as follows:

- Mapping of a Timer or SYNC input to the respective HSx outputs
- Configuring the respective filter timing, i.e. assigning the respective WK pin for cyclic sense
- Configuring the timer period and on-time

Note: It is not possible to select SYNC (ON, OFF or both) for cyclic sense / cyclic wake when WK4 is enabled. In this case the timer is not started and the SPI_FAIL bit is set. So first the pin must be configured to SYNC via the bit WK4_SYNC before starting cyclic wake / cyclic sense.

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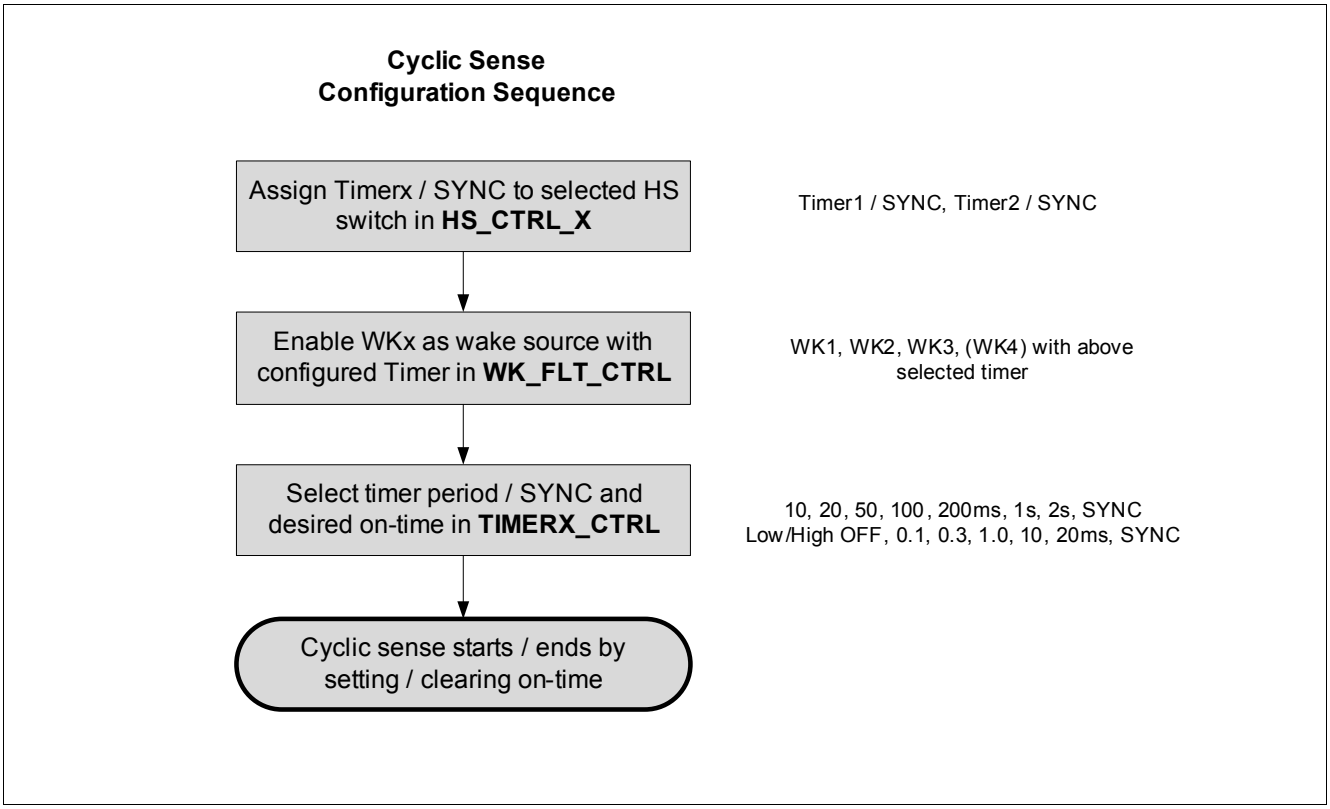


Figure 5 Cyclic Sense: Configuration and Sequence

The first WK input value (HIGH or LOW) is taken as the reference for the next cycle. A wake from SBC Sleep Mode or an Interrupt in SBC Stop- or Normal Mode via WK pin can therefore only happen with the second cycle (on-time). A wake-up event due to cyclic sense in SBC mode will set the bit WK1_WU, WK2_WU, WK3_WU or WK4_WU.

To ensure that no change of the WK input level was missed during the settle time of the first cyclic sense cycle the level can be checked at the WKx bit. The functionality of the sampling and the different scenarios is depicted in **Figure 6** to **Figure 8**. A edge change on a WK pin is only sensed and signalled after the filter time of the respective on-time.

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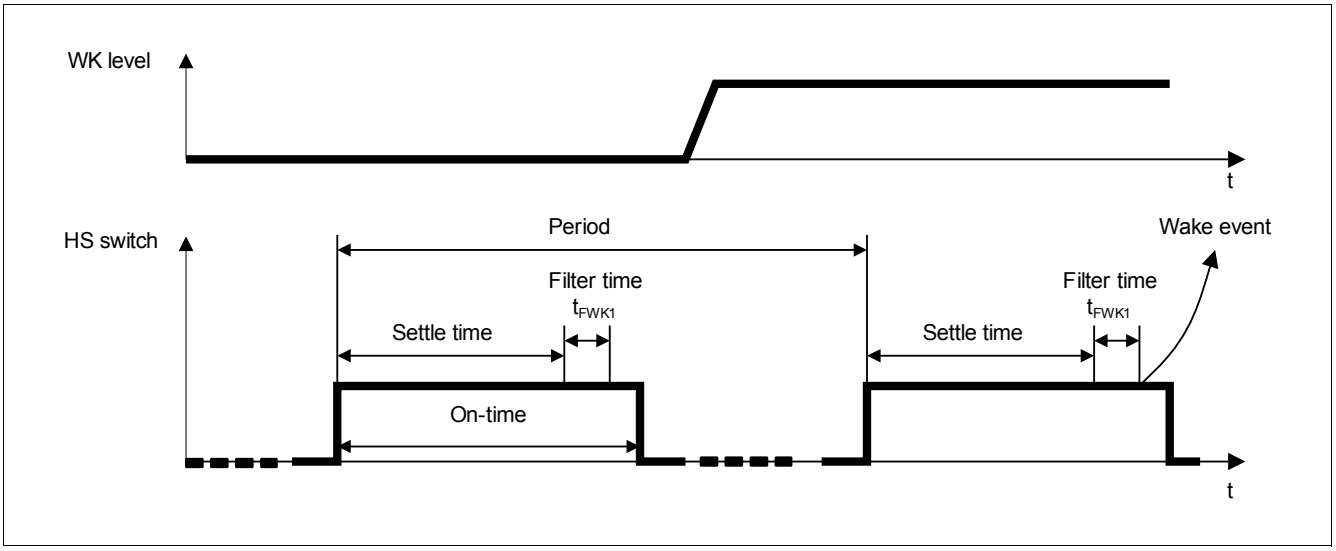


Figure 6 Wake Input Timing

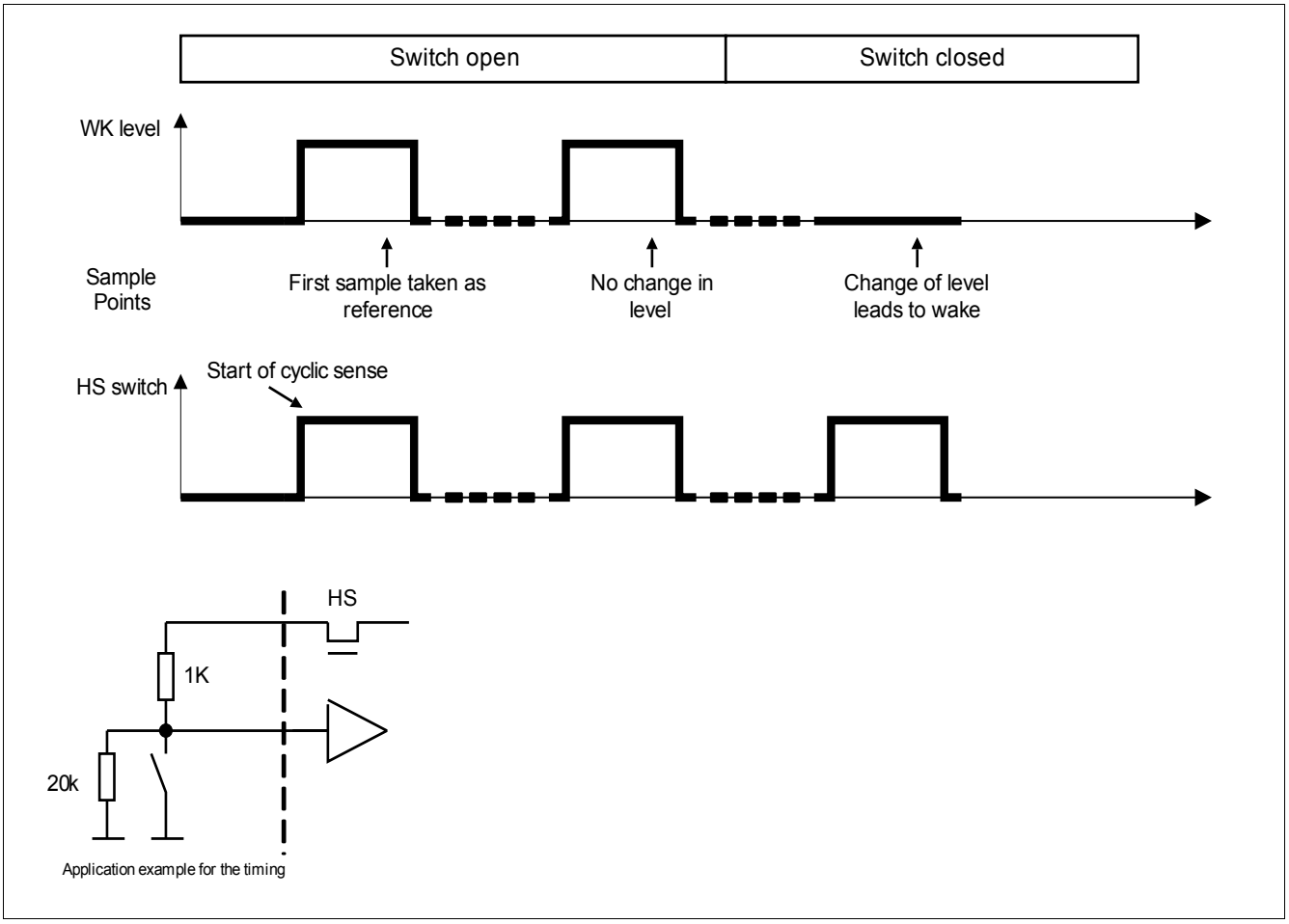


Figure 7 Start of Cyclic Sense, HS “OFF” before Cycle Sense Start

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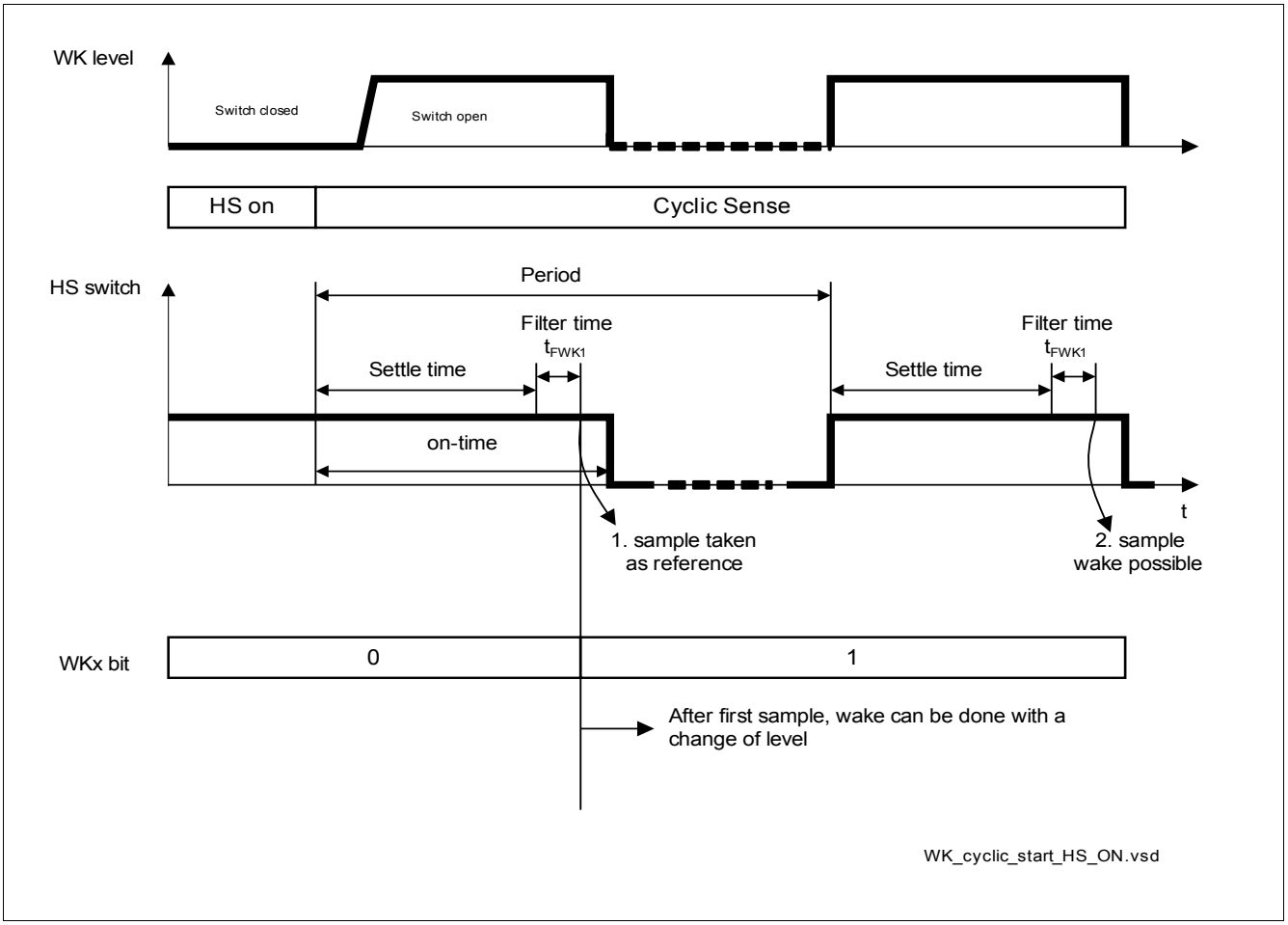


Figure 8 Start of Cyclic Sense, HS 'ON' before Cycle Sense Start

5.2.3.2 Cyclic Sense in Low-Power Mode

If cyclic sense is intended for SBC Stop or SBC Sleep Mode mode, it is necessary to activate the cyclic sense in SBC Normal Mode before going to the low-power mode. A wake-up event due to cyclic sense will set the bit WK1_WU, WK2_WU, WK3_WU or WK4_WU. In SBC Stop Mode the wake-up event will trigger an interrupt, in SBC Sleep Mode the wake-up event will send the device via SBC Restart Mode to SBC Normal Mode. Before returning to SBC Sleep Mode, the wake status register **WK_STAT** needs to be cleared. Trying to go to SBC Sleep Mode with uncleared wake flags, such as WKx_WU the SBC will directly wake-up from SBC Sleep Mode by going via SBC Restart Mode to SBC Normal Mode, a reset is issued. The WKx_WU bit is seen as source for the wake. This is implemented in order not to loose an wake-up event during the transition.

Note: Cyclic sense remains active even if the respective HS switch is disabled due to a failure. Therefore, it is recommended not to enter SBC Sleep Mode with only cyclic sense activated as awake source.

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5.2.4 Cyclic Wake

For the cyclic wake feature one or both timers are configured as internal wake-up source and will periodically trigger an interrupt in SBC Normal and SBC Stop Mode.

The correct sequence to configure the cyclic wake is shown in **Figure 9**. The sequence is as follows:

- Enable Timer1 and/or Timer2 as a wake-up source in the register **WK_CTRL_1**.
- Configure the respective period of Timer1 and/or Timer2

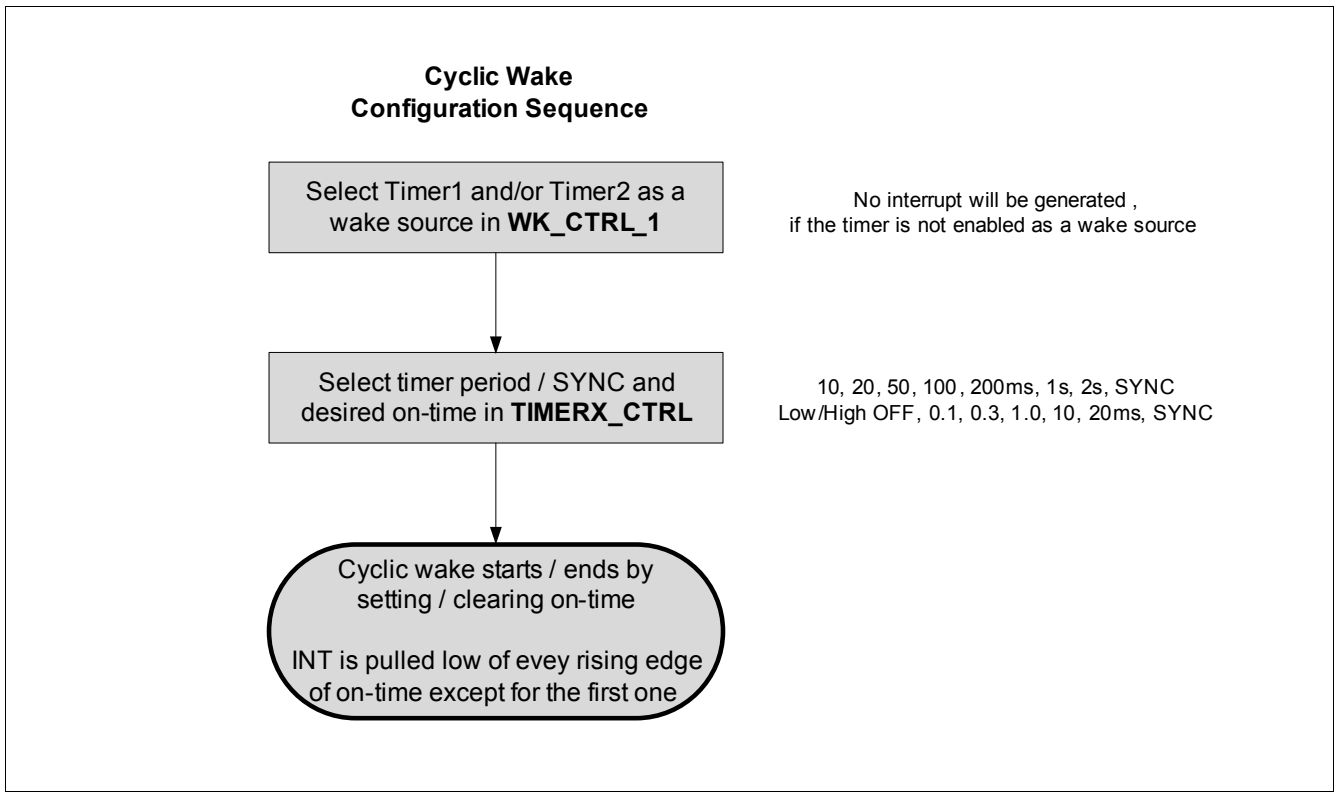


Figure 9 Cyclic Wake: Configuration and Sequence

As in cyclic sense, the cyclic wake function will start as soon as the on-time is configured. An interrupt is generated for every start of the on-time except for the very first time when the timer is started.

Note: The Timer on-time has no function during cyclic wake operation except for starting the cyclic wake function.

Note: It is not possible to select SYNC (ON, OFF or both) for cyclic sense / cyclic wake when WK4 is enabled. In this case the timer is not started and the SPI_FAIL bit is set. So first the pin must be configured to SYNC via the bit WK4_SYNC before starting cyclic wake / cyclic sense.

5.3 Supervision Features

The device offers various supervision features to support functional safety requirements. Please see **Chapter 15** for more information.

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6 Voltage Regulator 1

6.1 Block Description

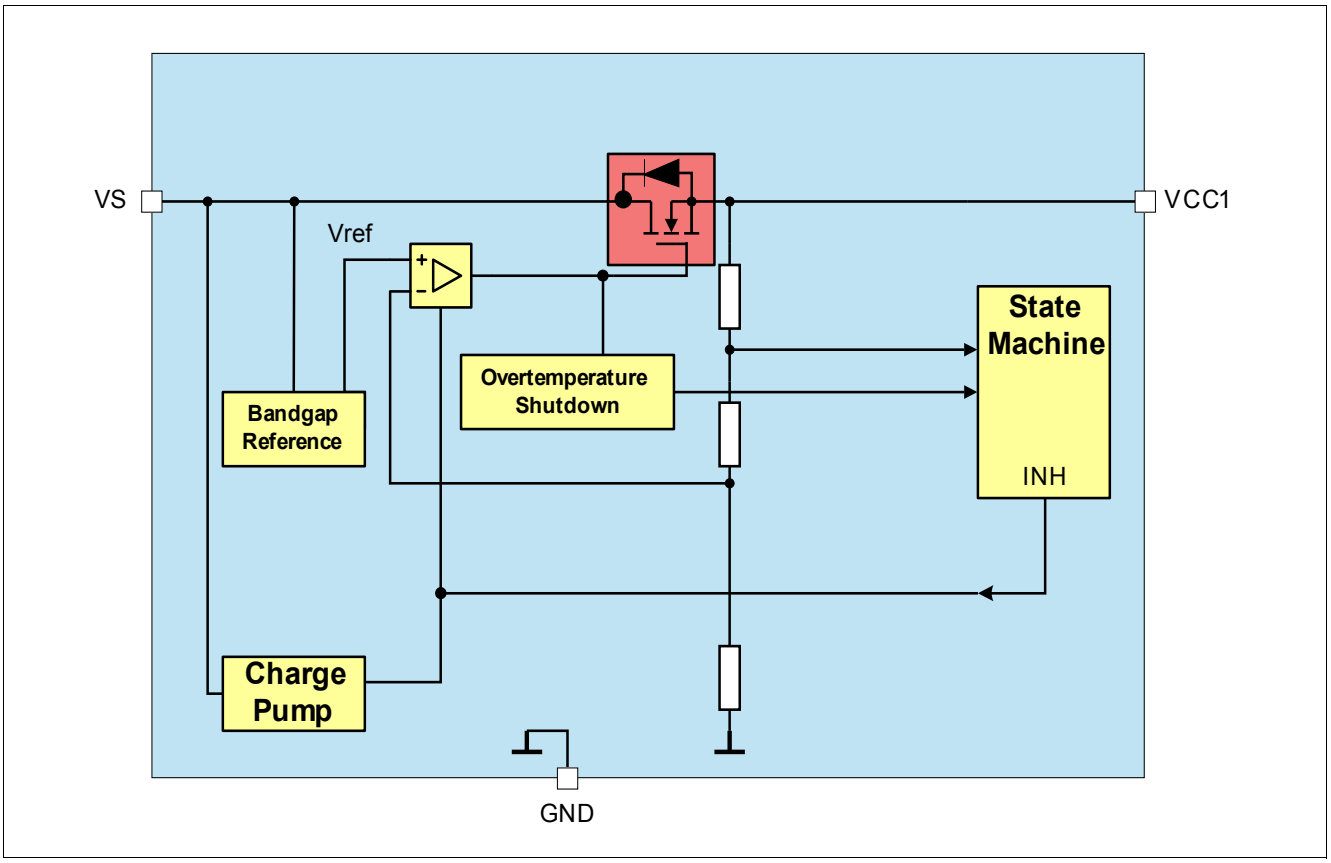


Figure 10 Module Block Diagram

Functional Features

- 5 V low-drop voltage regulator
- Under voltage monitoring with adjustable reset level, VCC1 failure and VCC1 short circuit detection ($V_{RT1/2/3/4}$, $V_{CC1,fail}$, $V_{CC1,SC}$). Please refer to **Chapter 15.6** and **Chapter 15.7** for more information.
- Short circuit detection and switch off with under voltage fail threshold, device enters SBC Fail-Safe Mode
- ≥ 470nF ceramic capacitor at voltage output for stability, with ESR < 3Ω @ f = 10kHz, to achieve the voltage regulator control loop stability based on the safe phase margin (bode diagram).
- Output current capability up to $I_{VCC1,lim}$.

6.2 Functional Description

The Voltage Regulator 1 (=VCC1) is “ON” in SBC Normal Mode and is disabled in SBC Sleep Mode. To reduce the current consumption of the SBC (see **Chapter 4.4**), the VCC1 output voltage is supplied by a low-power regulator (see also P_6.3.18) in SBC Stop Mode with a reduced voltage output accuracy ($V_{CC1,out4}$). The output current of VCC1 is limited at $I_{VCC1,lim}$.

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6.3 Electrical Characteristics

Table 7 Electrical Characteristics

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage including line and Load regulation	$V_{CC1,out1}$	4.9	5.0	5.1	V	1mA < I_{VCC1} < 150mA; SBC Normal Mode	P_6.3.1
Output Voltage including line and Load regulation	$V_{CC1,out2}$	4.85	5.0	5.15	V	150mA < I_{VCC1} < 250mA; SBC Normal Mode	P_6.3.2
Output Voltage including line and Load regulation	$V_{CC1,out4}$	4.8	5.0	5.2	V	0mA < I_{VCC1} < 15mA; SBC Stop Mode	P_6.3.4
Output Drop	$V_{CC1,d1}$	–	–	400	mV	I_{VCC1} = 50mA V_S =5V	P_6.3.5
Output Drop	$V_{CC1,d2}$	–	–	500	mV	I_{VCC1} = 150mA V_S =5V	P_6.3.6
Output Drop	$V_{CC1,d3}$	–	–	500	mV	1) IVCC1 = 100mA VS =4.5V	P_6.3.7
Output Drop	$V_{CC1,d4}$	–	–	600	mV	1) IVCC1 = 150mA VS =4.5V	P_6.3.8
Active Peak Threshold VCC1	$I_{Peak_Vcc1,r}$	7.0	9.7	15.0	mA	1)I_{VCC1} rising	P_6.3.18
Over Current Limitation	$I_{VCC1,lim}$	250	–	1100	mA	current flowing out of pin, VCC1 = 0V	P_6.3.9

1) Specified by design; not subject to production test.

*Note: Please see **Chapter 15.7** for the power-up blanking time and short circuit protection.*

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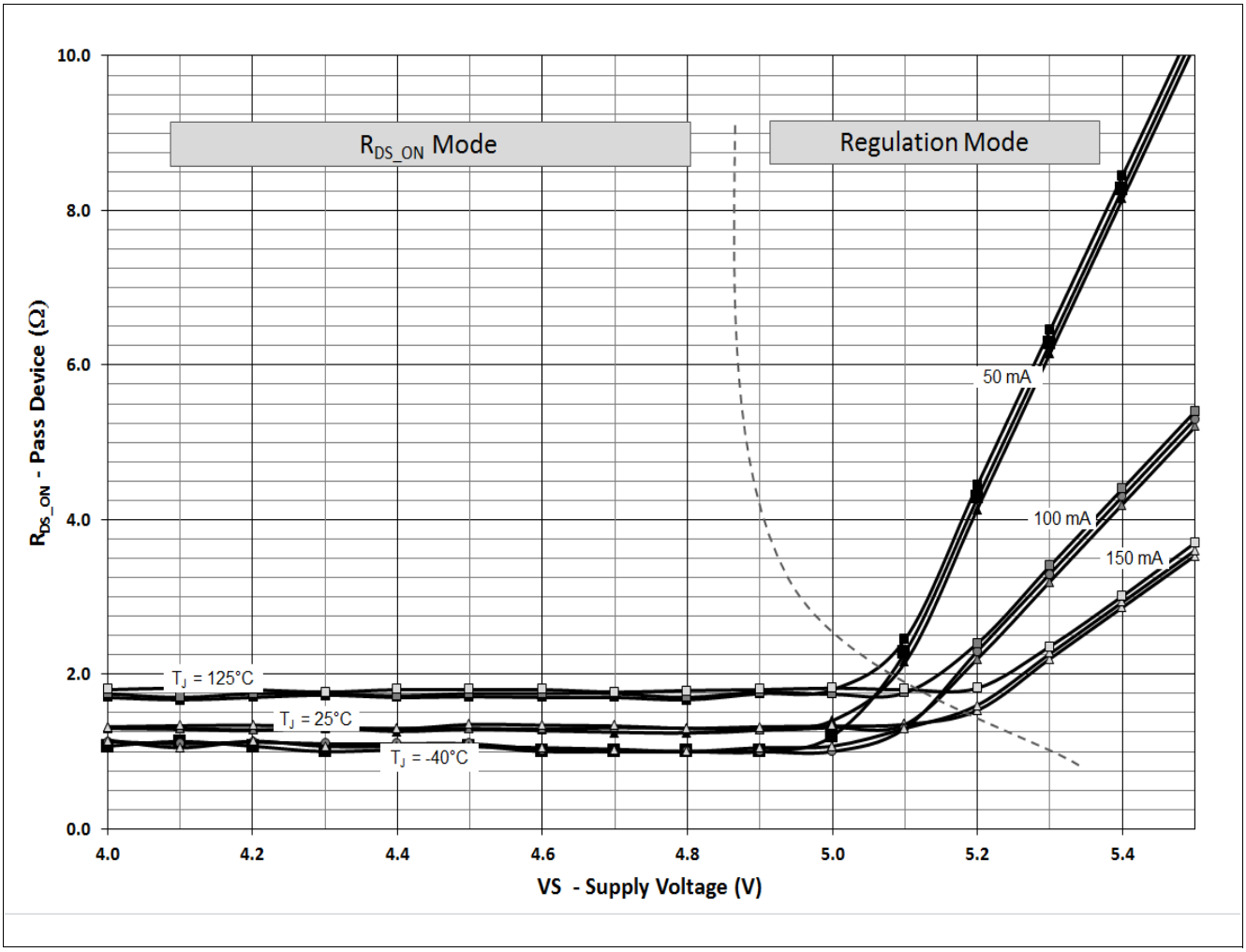


Figure 11 VCC1 Pass Device On-Resistance during Low-Drop Operation

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7 Voltage Regulator 2

7.1 Block Description

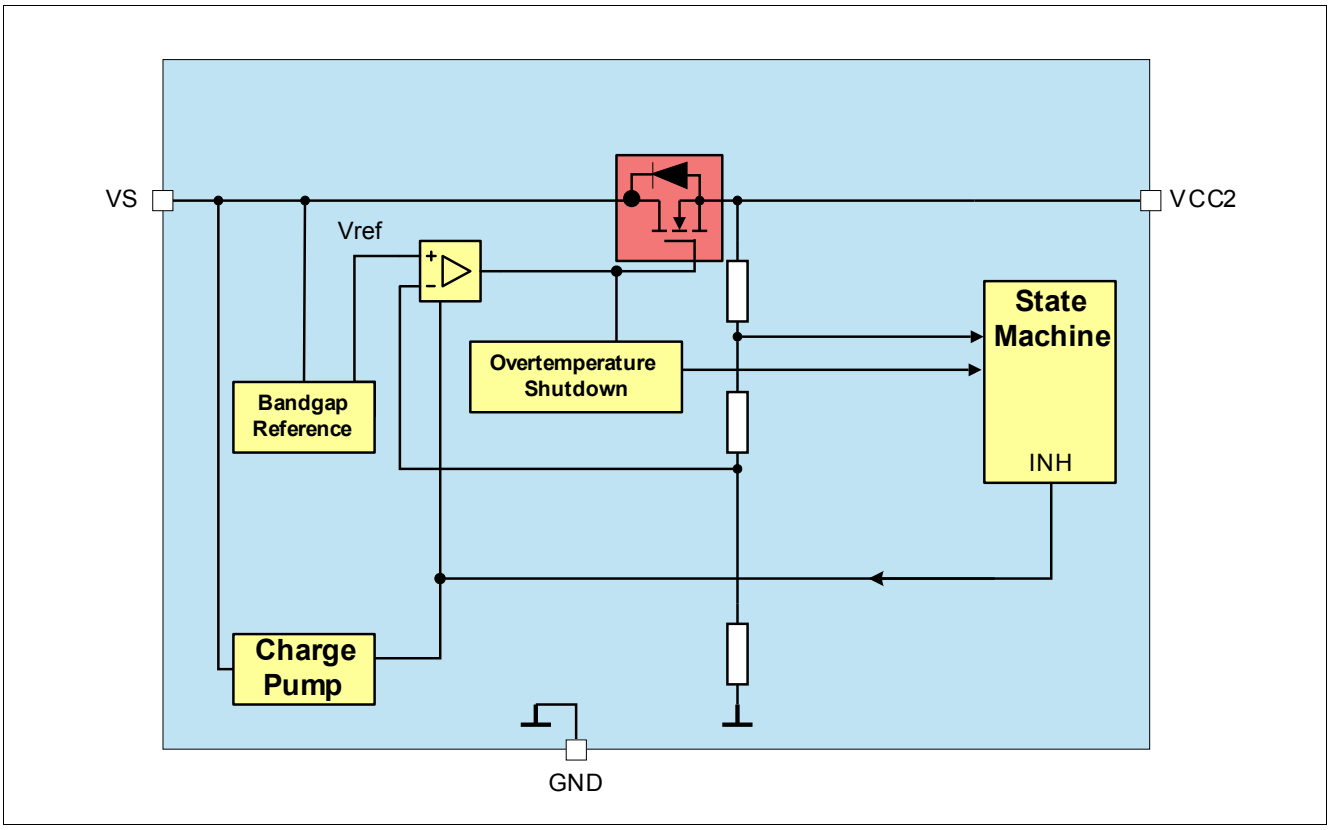


Figure 12 Module Block Diagram

Functional Features

- 5 V low-drop voltage regulator
- Under voltage monitoring with VCC2 failure and VCC2 short circuit detection ($V_{CC2,fail}$, $V_{CC2,SC}$). Please refer to **Chapter 15.8** for more information
- VCC2 Switch off after entering SBC Restart Mode. Switch-off is latched, LDO must be enabled via SPI after shutdown.
- Over temperature Protection
- Short-circuit robustness against supply voltage VS
- ≥ 470 nF ceramic capacitor at output voltage for stability, with ESR < 3Ω @ f = 10kHz, to achieve the voltage regulator control loop stability based on the safe phase margin (bode diagram).
- Output current capability up to $I_{VCC2,lim}$.

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7.2 Functional Description

In SBC Normal Mode VCC2 can be switched on or off via SPI.

In SBC Stop- or Sleep Mode, the VCC2 has to be switched on or off before entering the respective SBC mode.

To reduce the current consumption of the SBC in SBC Stop- and Sleep Mode (see **Chapter 4.4**), the current consumption of the VCC2 regulator is also reduced with a reduced voltage output accuracy ($V_{CC2,out2}$). The output current of VCC1 is limited at $I_{VCC2,lim.}$

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7.3 Electrical Characteristics

Table 8 Electrical Characteristics

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage including line and Load regulation	$V_{CC2,out1}$	4.85	5.0	5.15	V	1mA < I_{VCC2} < 100mA; SBC Normal Mode	P_7.3.1
Output Voltage including line and Load regulation	$V_{CC2,out2}$	4.8	5.0	5.2	V	0mA < I_{VCC2} < 15mA; SBC Stop and Sleep	P_7.3.2
Output Drop	$V_{CC2,d2}$	–	–	500	mV	I_{VCC2} = 100mA; V_S = 5V	P_7.3.3
Over Current limitation	$I_{VCC2,Lim}$	100	–	500	mA	current flowing out of pin, VCC2 = 0V	P_7.3.4

*Note: Please see **Chapter 15.8** for power-up blanking time and short circuit protection.*

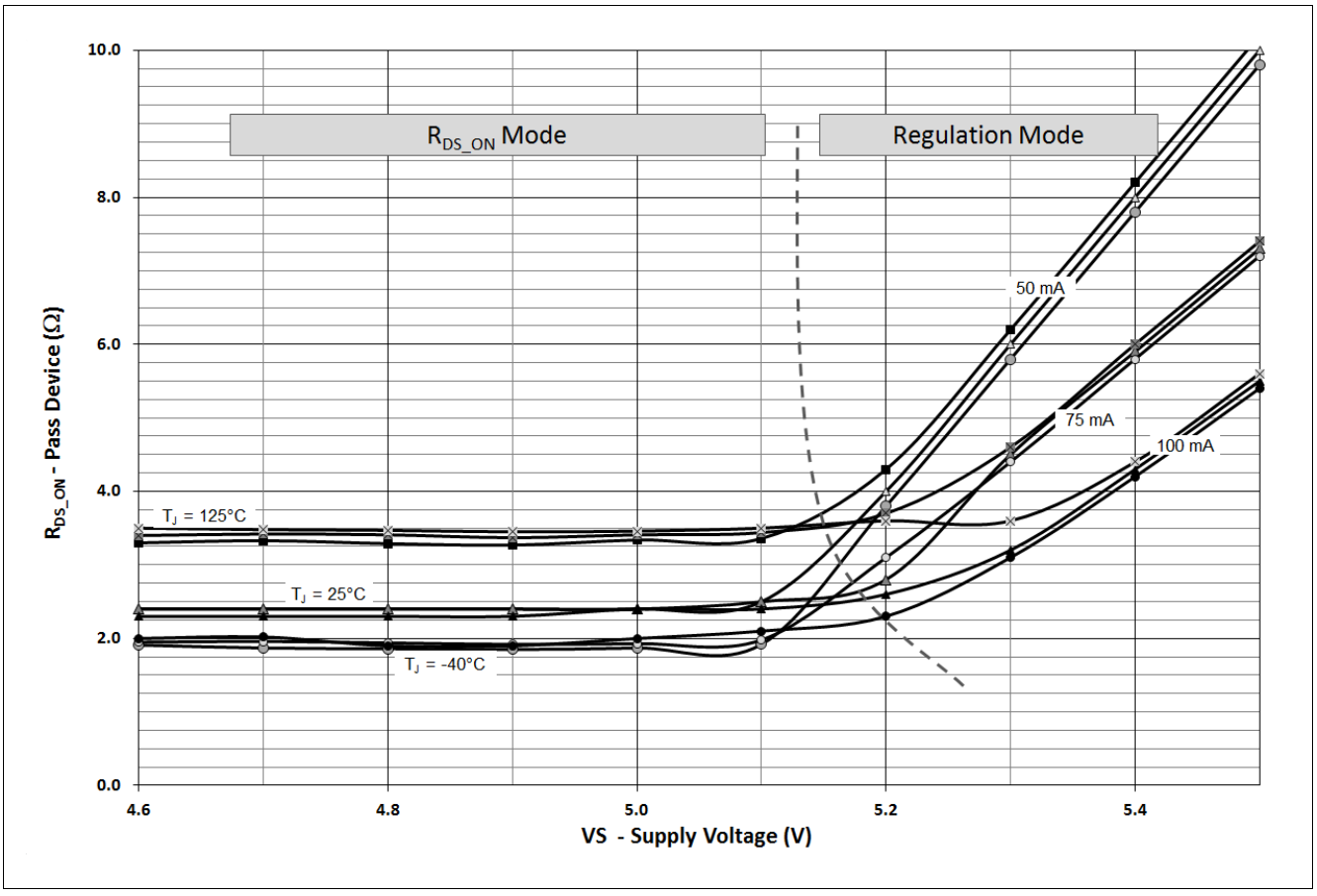


Figure 13 VCC2 Pass Device On-Resistance during Low-Drop Operation

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8 High-Side Switch

8.1 Block Description

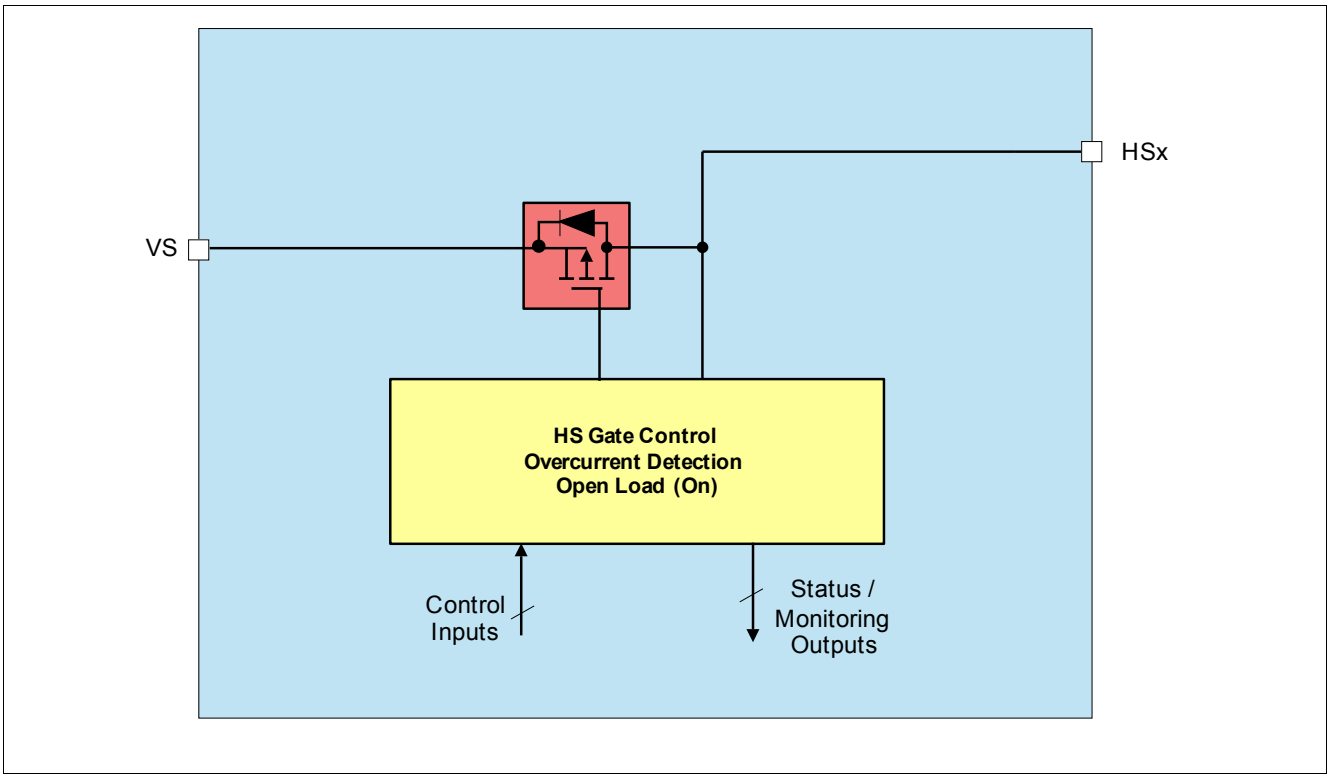


Figure 14 High-Side Module Block Diagram

Functional Features

- Over-voltage and under-voltage switch off - configurable via SPI
- Over-current detection and switch off
- Open-load detection in ON-state
- PWM capability with internal timer configurable via SPI
- Supports cyclic sense features - see **Chapter 5.2.3**
- Switch recovery after removal of OV or UV condition configurable via SPI
- HS1...2 have a typical Ron of 2Ω and HS3...6 have a typical Ron of 7Ω
- The over-current and open-load detection of HS1...2 can be configured via SPI depending on the external load

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8.2 Functional Description

The high-side switches can be used for control of LEDs, as supply of the wake inputs and for other loads. The high-side outputs can be controlled either directly via SPI by (**HS_CTRL1**, **HS_CTRL2**, **HS_CTRL3**) or by the integrated PWM timers.

HS1 and HS2 feature two different open load and over current detection thresholds. This allows to adapt the system to different loads. The selection between the two configurations can be done via the SPI bits **HS1_SEL** and **HS2_SEL** in the register **HS_CTRL1**. The higher thresholds are activated by configuring the respective switch with the low on-resistance $R_{ON,HS11}$and vice versa.

The high-side drivers can be kept ON also in SBC Stop- and SBC Sleep Mode and also during a long open window, i.e. no successful watchdog trigger is required to turn on the drivers (as compared to the low-side switches).

The configuration of the high-side drivers (permanent ON, PWM, cyclic sense, etc.) must be done in SBC Normal Mode. When entering SBC Restart Mode the HSx outputs are disabled.

8.2.1 Over- and Under Voltage Switch-Off

All HS drivers in on-state are switched off in case of over voltage on VS ($V_{OVD,r}$). If the voltage drops below the over voltage threshold the HS drivers are activated again. The feature can be disabled by setting the SPI bit **HS_OV _SD_EN**.

The HS drivers are switched off in case of under voltage on VS ($V_{UVD,f}$). If the voltage rises above the under voltage threshold the HS drivers are activated again. The feature can be disabled by setting the SPI bit **HS_UV _SD_EN**.

So after release of under voltage or over voltage condition the HS switch goes back to programmed state in which it was configured via SPI. This behavior is only valid if the bit **HS_OV_UV _REC** is set to ‘1’. Otherwise the switches will stay OFF (Configuration registers HS_CTRLx will be cleared).

The over voltage and under voltage is signaled in the bits **VS_OV** and **VS_UV**, no other error bits are set.

8.2.2 Over-Current Detection and Switch-Off

If the load current exceeds the short circuit shutdown current for a time longer then the short circuit shutdown filter time the output is switched off.

The over current condition and the switch off is signaled with the respective HSx_OC_OT bit in the register **HS_OC_OT_STAT**. The HSx configuration is then reset to 000 by the SBC. To activate the high-side switch again the HSx configuration has to be set to ON (001) or be programmed to a timer function. It is recommended to CLEAR the over-current bit before activation the high-side switch, as the bits are not cleared automatically by the SBC.

8.2.3 Open-Load Detection

Open load detection on the high-side outputs is done during on-state of the output. If the current in the activated output falls below then open-load detection current, the open load is detected and signaled via the respective bit HS1_OL, HS2_OL, HS3_OL, HS4_OL, HS5_OL, HS6_OL in the register **HS_OL_STAT**. The high-hide output stays activated. If the open load condition disappears the Open Load bit in the SPI can be cleared. The bits are not cleared automatically by the SBC.

8.2.4 HSx Operation in Different SBC Modes

- In SBC Normal Mode the output stage is fully functional. Protection functions as over current detection and open load detection are available.
- Using the HSx outputs for the cyclic sense feature during SBC Stop- and SBC Sleep Mode the open-load detection functionality is disabled for power consumption reasons. Short circuit shut down as well as over

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voltage and under voltage shutdown is available. The device is not woken because of short circuit shutdown of a HS output[1]. Only the respective HS will be disabled.
- the HSx output can also be enabled for SBC Stop- and SBC Sleep Mode as well as controlled by the PWMx generator. The HSx outputs must be configured in SBC Normal Mode before entering a low-power mode.
- The HSx outputs are switched off during SBC Restart- or SBC Fail-Safe Mode. They can be enabled via SPI if the failure condition is removed.

8.2.5 PWM and Timer Function

Four 8-bit PWM generators are dedicated to generate a PWM signal on the HS outputs, e.g. for brightness adjustment or compensation of supply voltage fluctuation. The PWM generators are mapped to the dedicated HS outputs, and the duty cycle can be independently configured with a 8-bit resolution via SPI (**PWM1_CTRL**... **PWM4_CTRL**). Two different frequencies (150Hz, 300Hz) can be selected independently for every PWM generator in the register **PWM_FREQ_CTRL**.

In addition, the HSx outputs can also be used for cyclic sensing via a the timer or SYNC control (see **Chapter 5.2**) and the timers can be used for the cyclic wake function. Below assignment is possible:

HS1... HS6:
- Timer 1
- Timer 2
- PWM 1
- PWM 2
- PWM 3
- PWM 4

Note: The min. on-time during PWM is limited by the actual Ton and Toff time of the respective HS switch, e.g. the PWM setting '0000 0001' could not be realized.
In addition, the minimum PWM setting for reliable detection of over-current and open-load measurement is 5 digits for a period of 300Hz and 3 digits for a period of 150Hz.

1) A shutdown of an HSx output for the above described reasons could lead to an unintended wake-up. This must be checked in the respective status register if it was the case.

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8.3 Electrical Characteristics

Table 9 Target Specifications

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output HS1, HS2							
Static Drain-Source ON Resistance HS1...2	$R_{ON,HS11}$	–	2	–	Ω	1)Ids=60mA, T_j < 25°C, SPI Setting	P_8.3.1
Static Drain-Source ON Resistance HS1...2	$R_{ON,HS12}$	–	4.2	5.0	Ω	1)Ids=60mA, T_j < 150°C,	P_8.3.2
Output Slew Rate (rising)	$SR_{raise,HS1}$	0.6	–	2.8	V/µs	2)20 to 80% V_S= 6 to 18V R_L=220Ω	P_8.3.3
Output Slew Rate (falling)	$SR_{fall,HS1}$	-2.8	–	-0.6	V/µs	2)80 to 20% V_S= 6 to18V R_L=220Ω	P_8.3.4
Switch-On time HS1...2	$t_{ON,HS1}$	3	–	70	µs	CSN = HIGH to 0.8*V_S; R_L=220Ω V_S= 6 to 18V	P_8.3.5
Switch-Off time HS1...2	$t_{OFF,HS1}$	3	–	70	µs	CSN = HIGH to 0.2*V_S; R_L=220Ω V_S= 6 to 18V	P_8.3.6
Short Circuit Shutdown Current 1	$I_{SD1,HS1}$	150	215	330	mA	SPI Setting V_S= 6 to 28V	P_8.3.7
Short Circuit Shutdown Current 2	$I_{SD2,HS1}$	260	375	490	mA	SPI Setting V_S= 6 to 28V	P_8.3.8
Short Circuit Shutdown Filter Time	$t_{SD,HS1}$	–	64	–	µs	3) 4)	P_8.3.9
Open Load Detection Current 1	$I_{OL1,HS1}$	0.4	–	4	mA	SPI Setting V_S= 6 to 28V	P_8.3.10
Open Load Detection Current 2	$I_{OL2,HS1}$	6	–	13.5	mA	SPI Setting V_S= 6 to 28V	P_8.3.11
Open Load Detection Filter Time	$t_{OL,HS1}$	–	64	–	µs	3) 4)	P_8.3.12

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Table 9 Target Specifications (cont'd)

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output HS3, HS4, HS5, HS6							
Static Drain-Source ON Resistance HS3...6	$R_{ON,H21}$	–	7	–	Ω	Ids=60mA, T_j < 25°C	P_8.3.13
Static Drain-Source ON Resistance HS3...6	$R_{ON,HS22}$	–	11.5	16	Ω	Ids=60mA, T_j < 150°C	P_8.3.14
Output Slew Rate (rising)	$SR_{raise,HS2}$	0.6	–	2.8	V/µs	2)20 to 80% V_S = 6 to 18V R_L=220Ω	P_8.3.15
Output Slew Rate (falling)	$SR_{fall,HS2}$	-2.8	–	-0.6	V/µs	2)80 to 20% V_S= 6 to 18V R_L=220Ω	P_8.3.16
Switch-On time HS3...6	$t_{ON,HS2}$	3	–	70	µs	CSN = HIGH to 0.8*V_S; R_L=220Ω V_S= 6 to 18V	P_8.3.17
Switch-Off time HS3...6	$t_{OFF,HS2}$	3	–	70	µs	CSN = HIGH to 0.2*V_S; R_L=220Ω V_S= 6 to 18V	P_8.3.18
Short Circuit Shutdown Current	$I_{SD1,HS2}$	150	215	330	mA	V_S= 6 to 20V V_S= 6 to 28V	P_8.3.19
Short Circuit Shutdown Filter Time	$t_{SD,HS2}$	–	64	–	µs	3) 4)	P_8.3.20
Open Load Detection Current	$I_{OL,HS2}$	0.4	–	4	mA	V_S= 6 to 28V	P_8.3.21
Open Load Detection Filter Time	$t_{OL,HS2}$	–	64	–	µs	3) 4)	P_8.3.22

1) In case the low over current and open load threshold is selected (HSx_SEL = 0) for the respective HS1 or HS2 output, then the Static Drain-Source ON Resistance values of P_8.3.13/14 apply for this configuration.

2) Not subject to production test, specified by design.

3) Not subject to production test, tolerance defined by internal oscillator tolerance.

4) The minimum PWM setting for reliable detection of over-current and open-load measurement is 5digits for a period of 300Hz and 3 digits for a period of 150Hz

Note: The slew rate values might be determined by the external components if the component values are large.

Note: There is a timing offset of max. 20µs (typ.) to control the high-side switches due to internal signal transmission. This offset is already included in the specified turn-on and -off times.

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9 Low-Side Switch

9.1 Block Description

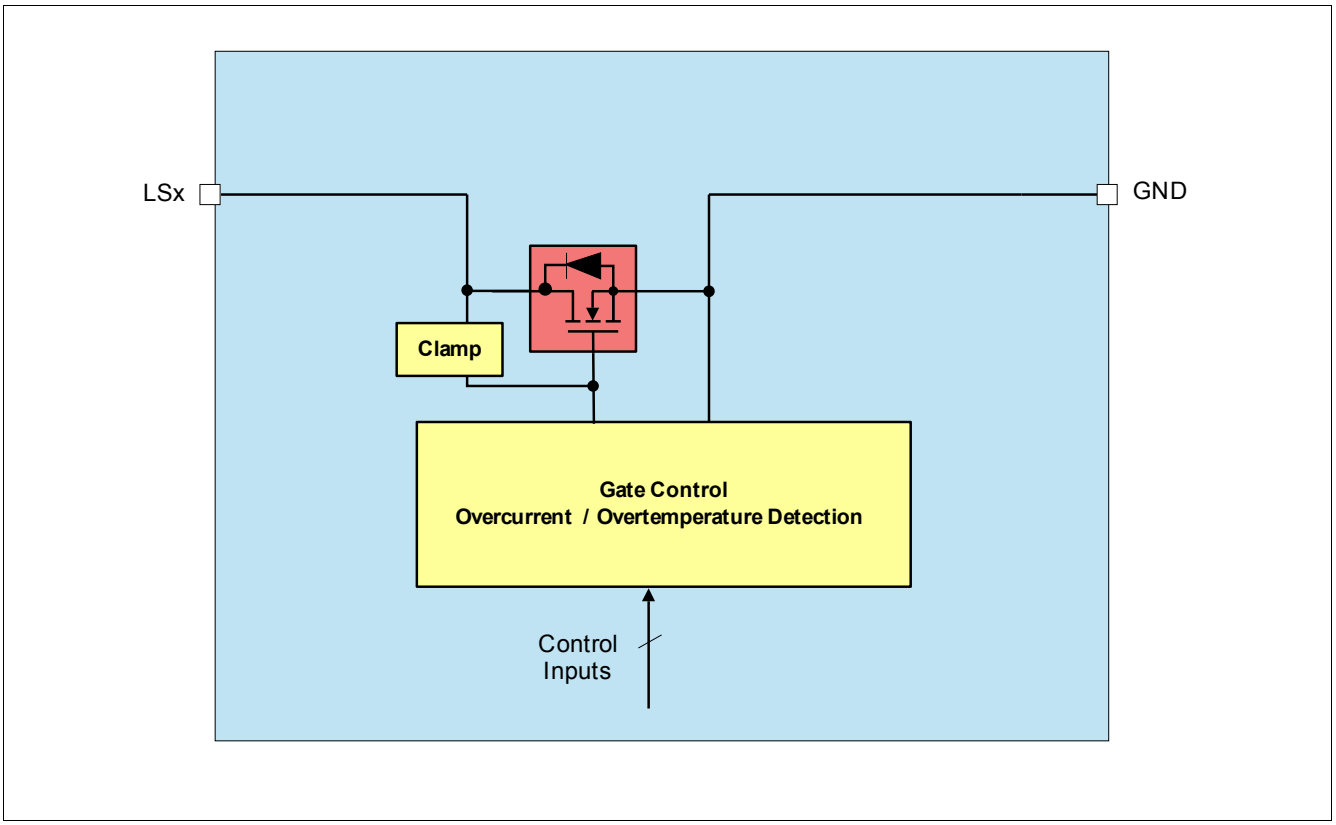


Figure 15 Module Block Diagram

Functional Features

- Multi purpose low-side switch
- Intended mainly for relay driver
- Integrated clamping for inductive loads
- Over-current shutdown, signaled via SPI
- Switch-on via SPI
- Switch recovery after removal of OV or UV condition - configurable via SPI
- Over- and Under Voltage shutdown -configurable via SPI

9.2 Functional Description

The general purpose low-side switches are mainly intended for on-board relay control, e.g. for power window control. The outputs feature an active output zener clamping for demagnetization of the relay coil.

The low-side drivers can only be active during SBC Normal Mode and will automatically be switched off when going to SBC Sleep- or SBC Stop Mode or due to failures (TSD1, WD fail or VCC1_UV). The LSx outputs will not be turned on automatically when going back to SBC Normal Mode.
Diagnosis registers will be kept until they are actively cleared by the microcontroller. For safety reasons, the below described protection functions are implemented.

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Note: The drivers cannot be turned on in a long open Watchdog Window, i.e. they can only be turned on after a first successful watchdog trigger or in SBC Software Development Mode.

9.2.1 Over- and Under Voltage Detection and Switch-Off

The LSx drivers and the respective loads can be protected against supply over voltage ($V_{OVD,r}$) and supply under voltage ($V_{UVD,f}$) conditions. The over voltage shutdown feature can be disabled by setting the bit **LS_OV _SD_EN**. The under voltage shutdown feature can be disabled respectively by setting the bit **LS_UV _SD_EN**.

Depending of the bit **LS_OV_UV _REC** the LSx outputs stay disabled (**LS_OV_UV _REC** = 0, i.e. the configuration register **LS_CTRL** will be cleared)) or are enabled again after crossing the respective VS threshold again.

Over voltage and under voltage conditions are signaled and latched in the SPI Status bits **VS_OV** and **VS_UV**. No other error bits are set.

9.2.2 Over-Current Detection and Switch-Off

If the load current exceeds the short circuit shutdown current for a time longer then the short-circuit shutdown filter time t_{ocf} the respective LSx output is switched off.

The over-current condition and switch off is signaled with the respective bit in the registers **LS_CTRL LS_normal** and **LS_OC_OT_STAT**. It is recommended to CLEAR the over current bit before re-activation of the low-side switch, as the bits are not cleared automatically by the SBC.

9.2.3 Inverted Low-Side Logic Option

A derivative of the device offers a different behavior of the low-side switches and the Fail Output pin. In case the motor (e.g. for window lift, seat, sun roof, etc.) in the application is not controlled by a double relay but rather by a H-bridge, then the function of the LSx outputs is to block the inputs of the H-bridge (i.e. the low-side switches) and to avoid any unintended movement of the motor.

The Fail Output is now logically connected to the LSx outputs as shown in **Figure 16**. This means that the low-side switches now follow the Fail Output pin, which inverses their behavior. The default SPI setting of LSx (**LS_CTRL**) after POR or Soft Restart is also changed. **Table 10** shows the default behavior of the low-side switches if they are not modified via SPI and if there is no LS overcurrent or overtemperature event.

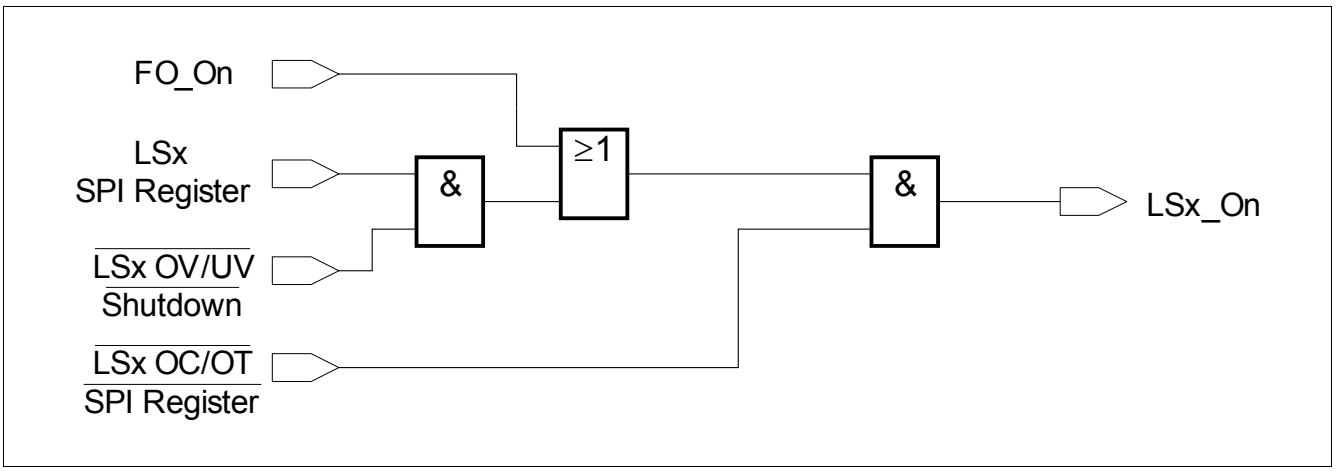


Figure 16 Low-side Switch Behavior depending on SPI Settings and FO Status

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Table 10 Default Setting of LSx for Inverted Low-side Logic Option, FO = OFF

SBC Mode, FO = OFF	LSx
SBC Init Mode	ON
SBC Normal Mode	ON
SBC Stop Mode	OFF
SBC Sleep Mode	OFF
SBC Restart Mode	OFF
SBC Fail-Safe Mode	ON

Note: The low-side switches are disabled in SBC Stop and SBC Sleep mode for current consumption savings as well as in case of over current or over temperature conditions.

In case of OC/OT, the LSx outputs are also disabled for self protection reasons. In order to enable the outputs again, the failure condition must be removed and the OC/OT must be cleared.
The LSx outputs are still controllable via SPI and can be disabled to allow the motor control. Both, LSx and FO are enabled automatically or stay enabled in case of (see also **Table 11**):

- Watchdog trigger failure,
- VCC1 UV condition,
- TSD2 event,
- SPI Stuck at LOW or HIGH

Table 11 LSx Setting for Inverted Low-side Logic Option after a failure condition (FO = ON)

SBC Mode, FO = ON	LSx
SBC Normal Mode	ON
SBC Stop Mode	ON
SBC Sleep Mode	ON
SBC Restart Mode	ON
SBC Fail-Safe Mode	ON

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9.3 Electrical Characteristics

Table 12 Electrical Characteristics Low-Side Switch

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
LS1, LS2							
Static Drain - Source ON Resistance	$R_{ON,LS}$	–	6.5	8	Ω	V_S > 5.5 V, Ids=100mA, T_j = 150°C	P_9.3.1
Static Drain - Source ON Resistance	$R_{ON,LS}$	–	4		Ω	T_j = 25°C	P_9.3.2
Switch-On time	$t_{ON,LS}$	5	25	100	µs	CSN=HIGH to 0.2*V_S R_L = 220Ω; V_S = 6 to 20V	P_9.3.3
Switch-Off time	$t_{OFF,LS}$	5	25	100	µs	CSN=HIGH to 0.8*V_S; R_L = 220Ω; V_S = 6V to 20V	P_9.3.4
Zener Clamp Voltage	V_{AZ}	40	50	60	V	Ids=100mA	P_9.3.5
Clamping Energy (repetitive)	$E_{Clamp,rep}$	2.5	–	–	mJ	1)1.000.000 cycles	P_9.3.6
Clamping Energy (single), cold	$E_{Clamp,single,c}$	10	–	–	mJ	1)1 cycle, T_{start} = 25°C	P_9.3.7
Clamping Energy (single), hot	$E_{Clamp,single,c}$	7	–	–	mJ	1)1 cycle, T_{start} = 85°C	P_9.3.8
Over Current Shut Down Threshold							
Over current threshold	I_{octh}	250		500	mA	–	P_9.3.9
Over current filter time	t_{ocf}	–	64	–	µs	2)	P_9.3.10

1) Not subject to production test, specified by design.

2) Not subject to production test; tolerance defined by internal oscillator tolerance.

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10 High-Speed CAN Transceiver

10.1 Block Description

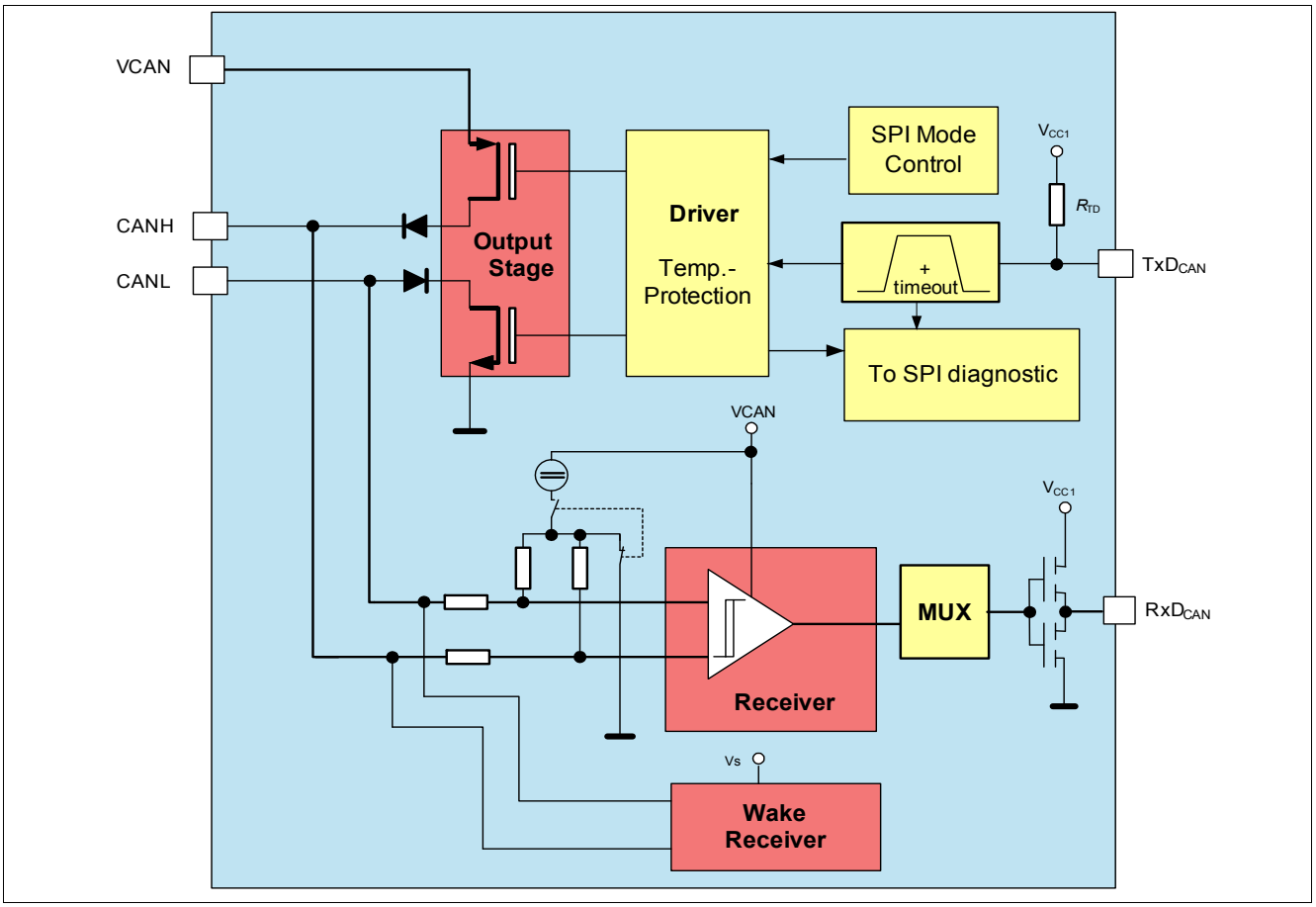


Figure 17 Functional Block Diagram

10.2 High-Speed CAN Functional Description

The Controller Area Network (CAN) transceiver part of the SBC provides high-speed (HS) differential mode data transmission (up to 1 Mbaud) and reception in automotive and industrial applications. It works as an interface between the CAN protocol controller and the physical bus lines compatible to ISO 11898-2 and 11898-5 as well as SAE J2284.

The CAN transceiver offers low-power modes to reduce current consumption. This supports networks with partially powered down nodes. To support software diagnostic functions, a CAN Receive-only Mode is implemented.

It is designed to provide excellent passive behavior when the transceiver is switched off (mixed networks, clamp15/30 applications).

A wake-up from the CAN Wake capable Mode is possible via a message on the bus. Thus, the microcontroller can be powered down or idled and will be woken up by the CAN bus activities.

The CAN transceiver is designed to withstand the severe conditions of automotive applications and to support 12 V applications.

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10.2.1 CAN OFF Mode

The CAN OFF Mode is the default mode after power-up of the SBC. It is available in all SBC modes and is intended to completely stop CAN activities or when CAN communication is not needed. The CANH/L bus interface acts as a high impedance input with a very small leakage current. In CAN OFF Mode, a wake-up event on the bus will be ignored.

10.2.2 CAN Normal Mode

The CAN Transceiver is enabled via SPI in SBC Normal Mode. CAN Normal Mode is designed for normal data transmission/reception within the HS CAN network. The mode is available in SBC Normal Mode. The bus biasing is set to 0.5x VCAN.

Transmission

The signal from the microcontroller is applied to the TXDCAN input of the SBC. The bus driver switches the CANH/L output stages to transfer this input signal to the CAN bus lines.

Enabling sequence

The CAN transceiver requires an enabling time $t_{CAN,EN}$ before a message can be sent on the bus. This means that the TXDCAN signal can only be pulled LOW after the enabling time. If this is not ensured, then the TXDCAN needs to be set back to HIGH (=recessive) until the enabling time is completed. Only the next dominant bit will be transmitted on the bus. **Figure 18** shows different scenarios and explanations for CAN enabling.

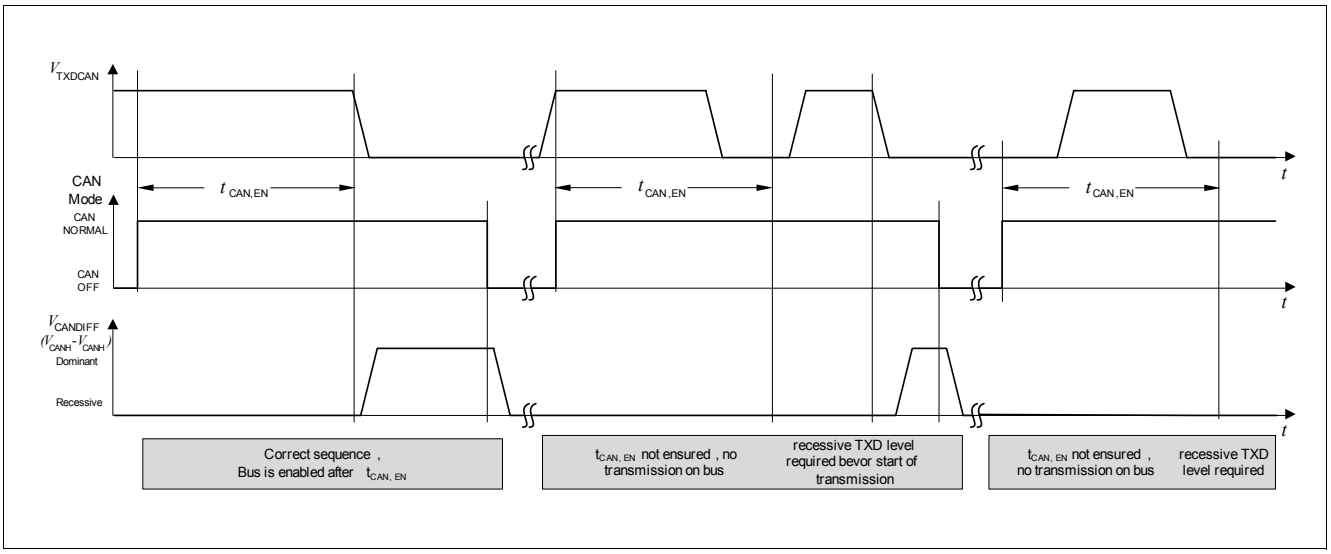


Figure 18 CAN Transceiver Enabling Sequence

Reduced Electromagnetic Emission

To reduce electromagnetic emissions (EME), the bus driver controls CANH/L slopes symmetrically.

Reception

Analog CAN bus signals are converted into digital signals at RXD via the differential input receiver.

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10.2.3 CAN Receive Only Mode

In CAN Receive Only Mode (RXD only), the driver stage is de-activated but reception is still operational. This mode is accessible by an SPI command in Normal Mode and in Stop Mode. The bus biasing is set to VCAN/2.

Note: The transceiver is still properly working in Receive Only mode even if VCAN is not available because of an independent receiver supply.

10.2.4 CAN Wake Capable Mode

This mode can be used in SBC Stop-, Sleep-, Restart- and SBC Normal Mode by programming via SPI and it is used to monitor bus activities. It is automatically accessed in SBC Fail-Safe Mode. A wake-up signal on the bus results in a change of behavior of the SBC, as described in **Table 13**. As a signalization to the microcontroller, the RXD_CAN pin is set LOW and will stay LOW until the CAN transceiver is changed to any other mode or until the SBC mode is changed to SBC Sleep-, Stop- or Fail-Safe Mode (automatic rearming - see also below). After a wake-up event, the transceiver can be switched via SPI to CAN Normal Mode for communication. Both bus pins CANH/L are connected to GND via the input resistors.

A wake-up pattern is signaled on the bus by two consecutive dominant bus levels for at least t_{Wake1} (filtering time $t > t_{Wake1}$). However the time between two consecutive dominant pulses must be less than t_{Wake2}.

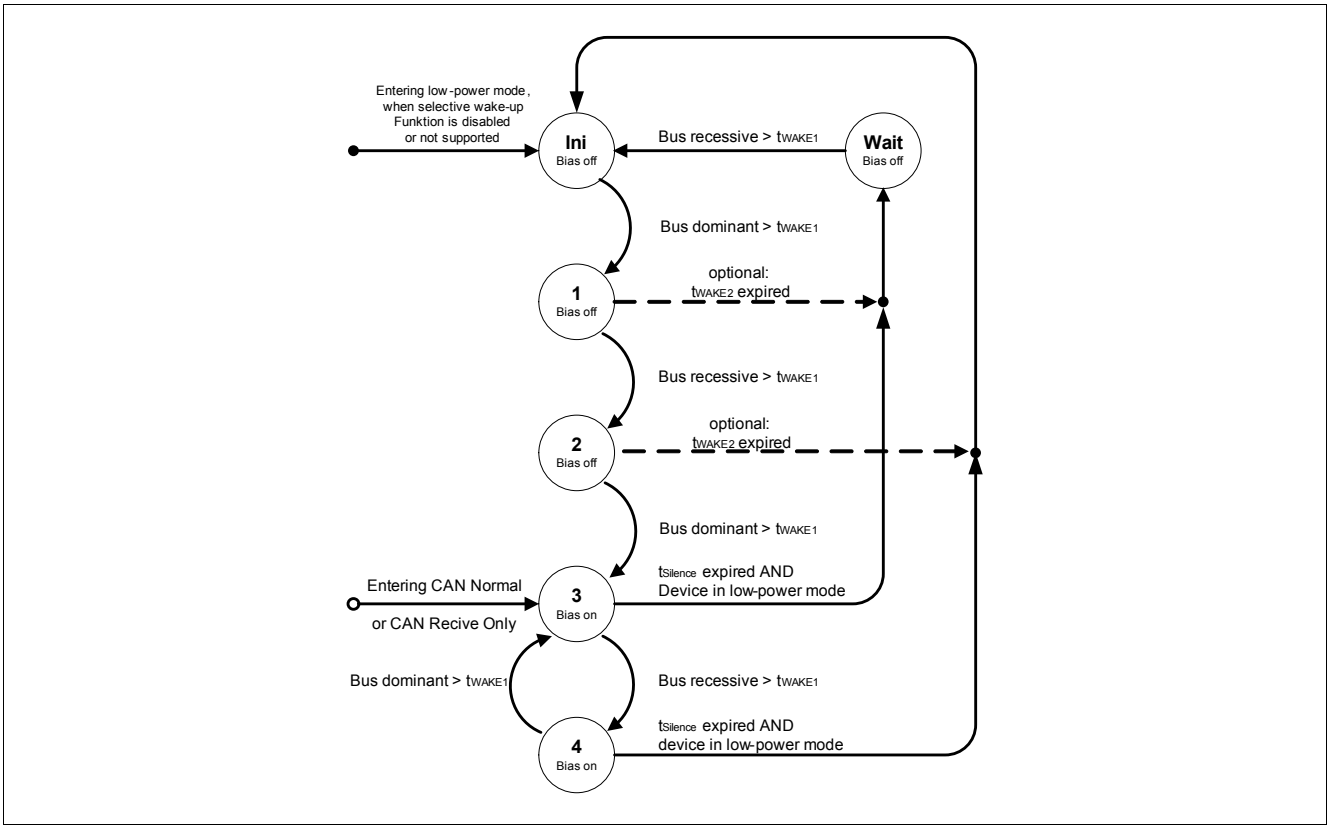


Figure 19 WUP detection following the definition in ISO 11898-5

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Rearming the Transceiver for Wake Capability

After a BUS wake-up event, the transceiver is woken. However, the **CAN** transceiver mode bits will still show wake capable (=‘01’) so that the RXD signal will be pulled LOW. There are two possibilities how the CAN transceiver’s wake capable mode is enabled again after a wake-up event:

- The CAN transceiver mode must be toggled, i.e. switched from Wake Capable mode to CAN Normal Mode, CAN Receive Only Mode or CAN OFF, before switching to CAN Wake Capable Mode again.
- Rearming is done automatically when the SBC is changed to SBC Stop-, SBC Sleep-, or SBC Fail-Safe Mode to ensure wake-up capability.

Wake-Up in SBC Stop- and SBC Normal Mode

In SBC Stop Mode, if a wake-up is detected, it is signaled by the INT output and in the **WK_STAT** SPI register. It is also signaled by RXDCAN put to LOW. The same applies for the SBC Normal Mode. The microcontroller should set the device from SBC Stop Mode to SBC Normal Mode, there is no automatic transition to Normal Mode.

For functional safety reasons, the watchdog will be automatically enabled in SBC Stop Mode after a Bus wake-up event in case it was disabled before (only if **WD_EN_ WK_BUS** = 1).

Wake-Up in SBC Sleep Mode

Wake-up is possible via a CAN message (filtering time $t > t_{WK,bus}$). The wake-up automatically transfers the SBC into the SBC Restart Mode and from there to Normal Mode the corresponding RxD pins in set to LOW. The microcontroller is able to detect the LOW signal on RxD and to read the wake source out of the **WK_STAT** register via SPI. No Interrupt is generated when coming out of Sleep Mode. The microcontroller can now for example switch the CAN transceiver into CAN Normal Mode via SPI to start communication.

Table 13 Action due to CAN Bus Wake Up

SBC Mode	SBC Mode after Wake	VCC1	INT	RXD
Normal Mode	Normal Mode	ON	LOW	LOW
Stop Mode	Stop Mode	ON	LOW	LOW
Sleep Mode	Restart Mode	Ramping Up	HIGH	LOW
Restart Mode	Restart Mode	ON	HIGH	LOW
Fail-Safe Mode	Restart Mode	Ramping up	HIGH	LOW

10.2.5 TXD Time-out Feature

If the TXD signal is dominant for a time $t > t_{TXD_CAN_TO}$, the TXD time-out function deactivates the transmission of the signal at the bus. This is implemented to prevent the bus from being blocked permanently due to an error. The CAN transceiver is switched to Receive Only Mode. The failure is stored in the SPI flag **CAN_FAIL**.

The CAN transmitter stage is activated again after the dominant time-out condition is removed. The level on the TXD pin must be recessive for at least one clock cycle ($1/f_{CLKSBC}$) to consider the dominant time-out condition is removed. Once this condition is fulfilled, the CAN transceiver requires an enabling time $t_{CAN,EN}$ before a dominant bit can be sent on the bus again (see also **Figure 18**).

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10.2.6 Bus Dominant Clamping

If the HS CAN bus signal is dominant for a time $t > t_{BUS_CAN_TO}$, a bus dominant clamping is detected and the SPI bit **CAN_FAIL** is set.

10.2.7 VCAN Under Voltage

The voltage at the CAN supply pin is monitored in CAN Normal Mode. In case of VCAN under voltage a signalization via SPI bit **VCAN_UV** is triggered and the TLE9266-2QX disables the transmitter stage. If the power supply reaches a higher level than the under voltage detection threshold (VCAN > **VCAN_UV**), then the transmitter is enabled again. Once this condition is fulfilled, the CAN transceiver requires an enabling time $t_{CAN,EN}$ before a dominant bit can be sent on the bus again (see also **Figure 18**). A transceiver mode change will only occur if the power supply V_S drops below the power on reset level.

VCAN_UV comparator is enabled in SBC Normal Mode if CAN_1 = ‘1’.

Note: In order to enable the sending on the CAN bus again after a VCAN under voltage event TXD needs to be HIGH (=send recessive bit) first before sending a dominant bit.

*Note: Please see also **BUS_STAT** for an application hint on the **VCAN_UV** behavior during CAN Receive Only Mode.*

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10.3 Electrical Characteristics

Table 14 Electrical Characteristics

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
CAN Supply Voltage							
CAN Supply under voltage detection threshold	$V_{CAN_UV,f}$	4.5	–	4.75	V	CAN Normal Mode; VCAN falling;	P_10.3.1
CAN Bus Receiver							
Differential Receiver Threshold Voltage, recessive to dominant edge	V_{diff,rd_N}	–	0.80	0.90	V	V_{diff} = V_{CANH} - V_{CANL} ; -12V ≤ V_{CM}(CAN) ≤ +12 V; CAN Normal Mode	P_10.3.2
Differential Receiver Threshold Voltage, dominant to recessive edge	V_{diff,dr_N}	0.50	0.60	–	V	V_{diff} = V_{CANH} - V_{CANL}; -12V ≤ V_{CM}(CAN) ≤ +12 V; CAN Normal Mode	P_10.3.3
Common Mode Range	CMR	-12	–	12	V	–	P_10.3.4
CANH, CANL Input Resistance	R_{in}	20	40	50	kΩ	CAN Normal / Wake capable Mode; Recessive state	P_10.3.6
Differential Input Resistance	R_{diff}	40	80	100	kΩ	CAN Normal / Wake capable Mode; Recessive state	P_10.3.7
Input Resistance Deviation between CANH and CANL	ΔR_i	-3	–	3	%	[3)]Recessive state	P_10.3.38
Input Capacitance CANH, CANL versus GND	C_{in}	–	20	40	pF	[3)]VTXD = 5V	P_10.3.39
Differential Input Capacitance	C_{diff}	–	10	20	pF	[3)]VTXD = 5V	P_10.3.40
Wake-up Receiver Threshold Voltage, recessive to dominant edge	$V_{diff,\ rd_W}$	–	0.8	1.15	V	-12V ≤ V_{CM}(CAN) ≤ +12 V; CAN Wake Capable Mode	P_10.3.8
Wake-up Receiver Threshold Voltage, dominant to recessive edge	$V_{diff,\ dr_W}$	0.4	0.7	–	V	-12V ≤ V_{CM}(CAN) ≤ +12 V; CAN Wake Capable Mode	P_10.3.9

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Table 14 Electrical Characteristics (cont'd)

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
CAN Bus Transmitter							
CANH/CANL Recessive Output Voltage	$V_{CANL/H}$	2.0	–	3.0	V	CAN Normal Mode; VTXD = V_{cc1}; no load	P_10.3.11
CANH/CANL Recessive Output Voltage (CAN Wake Capable Mode)	V_{CANL/H_LP}	-0.1	–	0.1	V	CAN Wake Capable Mode; V_{TXD} = V_{cc1}; no load	P_10.3.43
CANH, CANL Recessive Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$ (CAN Normal Mode)	$V_{diff_r_N}$	-500	–	50	mV	CAN Normal Mode V_{TXD} = V_{cc1}; no load	P_10.3.12
CANH, CANL Recessive Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$ (CAN Wake Capable Mode)	$V_{diff_r_W}$	-500	–	50	mV	CAN Wake Capable Mode; V_{TXD} = V_{CC1}; no load	P_10.3.41
CANL Dominant Output Voltage	V_{CANL}	0.5	–	2.25	V	CAN Normal Mode; V_{TXD} = 0 V; V_{CAN} = 5 V; 50Ω ≤ R_L ≤ 65Ω	P_10.3.13
CANH Dominant Output Voltage	V_{CANH}	2.75	–	4.5	V	CAN Normal Mode; V_{TXD} = 0 V; V_{CAN} = 5 V; 50Ω ≤ R_L ≤ 65Ω	P_10.3.14
CANH, CANL Dominant Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff_d_N}$	1.5	–	3.0	V	CAN Normal Mode; V_{TXD} = 0 V; V_{CAN} = 5 V; 50Ω ≤ R_L ≤ 65Ω	P_10.3.16
Driver Symmetry $V_{SYM} = V_{CANH} + V_{CANL}$	V_{SYM}	4.5	–	5.5	V	[1)]CAN Normal Mode; V_{TXD} = 0 V / 5 V; V_{CAN} = 5 V; C_{SPLIT} = 4.7nF; 50Ω ≤ R_L ≤ 60Ω	P_10.3.42
CANH Short Circuit Current	I_{CANHsc}	-100	-80	-50	mA	CAN Normal Mode; $V_{CANHshort}$ = 0 V	P_10.3.17

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Table 14 Electrical Characteristics (cont'd)

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
CANL Short Circuit Current	I_{CANLsc}	50	80	100	mA	CAN Normal Mode $V_{CANLshort}$ = 18 V	P_10.3.18
Leakage Current (unpowered device)	$I_{CANH,lk}$ $I_{CANL,lk}$	–	5	7.5	µA	V_S=V_{CAN} =0V; 0V < $V_{CANH,L}$ ≤ 5V; 2)Rtest = 0 / 47 kΩ	P_10.3.19
Receiver Output RXD							
HIGH level Output Voltage	$V_{RXD,H}$	0.8 × V_{CC1}	–	–	V	CAN Normal Mode $I_{RXD(CAN)}$ = -2 mA;	P_10.3.20
LOW Level Output Voltage	$V_{RXD,L}$	–	–	0.2 × V_{CC1}	V	CAN Normal Mode $I_{RXD(CAN)}$ = 2 mA;	P_10.3.21
Transmission Input TXD							
HIGH Level Input Voltage Threshold	$V_{TXD,H}$	–	–	0.7 × V_{CC1}	V	CAN Normal Mode recessive state	P_10.3.22
LOW Level Input Voltage Threshold	$V_{TXD,L}$	0.3 × V_{CC1}	–	–	V	CAN Normal Mode dominant state	P_10.3.23
TXD Input Hysteresis	$V_{TXD,hys}$	–	0.12 × V_{CC1}	–	mV	3)	P_10.3.24
TXD Pull-up Resistance	R_{TXD}	20	40	80	kΩ	–	P_10.3.25
CAN Transceiver Enabling Time	$t_{CAN,EN}$	–	10	–	µs	5) CSN = HIGH to first valid transmitted TXD dominant	P_10.3.37
Dynamic CAN-Transceiver Characteristics							
Min. Dominant Time for Bus Wake-up	t_{Wake1}	0.5	3	5	µs	-12V ≤ V_{CM}(CAN) ≤ +12 V; CAN Wake capable Mode	P_10.3.26
Wake-up Time-out, Recessive Bus	t_{Wake2}	0.5	–	10	ms	5)CAN Wake capable Mode	P_10.3.36
WUP Wake-up reaction time	t_{WU_WUP}	–	–	100	µs	3)4)5) Wake-up reaction time after a valid WUP on CAN bus;	P_10.3.44

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Table 14 Electrical Characteristics (cont'd)

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Propagation Delay TXD-to-RXD LOW (recessive to dominant)	$t_{d(L),TR}$	–	150	255	ns	1)CAN Normal Mode CL = 100 pF; RL = 60 Ω; VCAN = 5 V; C_{RXD} = 15 pF	P_10.3.27
Propagation Delay TXD-to-RXD HIGH (dominant to recessive)	$t_{d(H),TR}$	–	150	255	ns	1)CAN Normal Mode CL = 100 pF; RL = 60 Ω; VCAN = 5 V; C_{RXD} = 15 pF	P_10.3.28
Propagation Delay TXD LOW to bus dominant	$t_{d(L),T}$	–	50	140	ns	CAN Normal Mode C_L = 100pF; R_L = 60 Ω; V_{CAN} = 5 V;	P_10.3.29
Propagation Delay TXD HIGH to bus recessive	$t_{d(H),T}$	–	50	140	ns	CAN Normal Mode C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V;	P_10.3.30
Propagation Delay bus dominant to RXD LOW	$t_{d(L),R}$	–	100	115	ns	CAN Normal Mode C_L = 100pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF	P_10.3.31
Propagation Delay bus recessive to RXD HIGH	$t_{d(H),R}$	–	100	115	ns	CAN Normal Mode C_L = 100pF; R_L = 60 Ω V_{CAN} = 5 V; C_{RXD} = 15 pF	P_10.3.32
Propagation Delay Symmetry td(H),TR - td(L),TR	$t_{d,TR,sym}$	–50	–	100	ns	1)CAN Normal Mode CL = 100pF; RL = 60 Ω VCAN = 5 V; C_{RXD} = 15 pF	P_10.3.45
TXD Permanent Dominant Time-out	$t_{TxD_CAN_TO}$	–	4	–	ms	5)CAN Normal Mode	P_10.3.33
BUS Permanent Dominant Time-out	$t_{BUS_CAN_TO}$	–	4	–	ms	5)CAN Normal Mode	P_10.3.34

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1) f_{TXD} = 250 kHz rectangular signal, duty cycle = 50%;
2) Rtest between VS/VCAN and 0V (GND);
3) Wake-up is signalized via INT pin activation in SBC Stop Mode and via VCC1 ramping up with wake from SBC Sleep Mode;
4) Time starts with end of last dominant phase of WUP;
5) Not subject to production test, tolerance defined by internal oscillator tolerance;

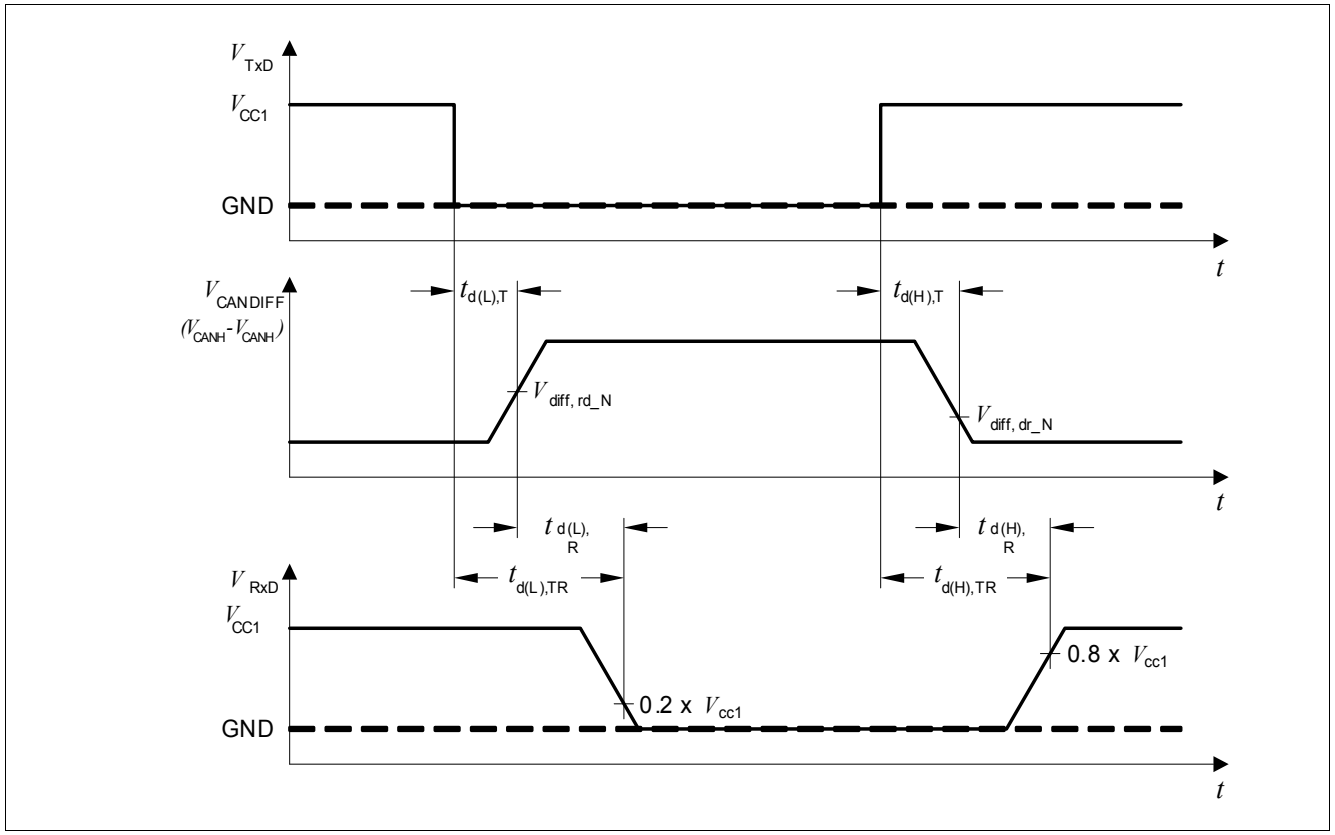


Figure 20 Timing Diagrams for Dynamic Characteristics

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11 LIN Transceiver

11.1 Block Description

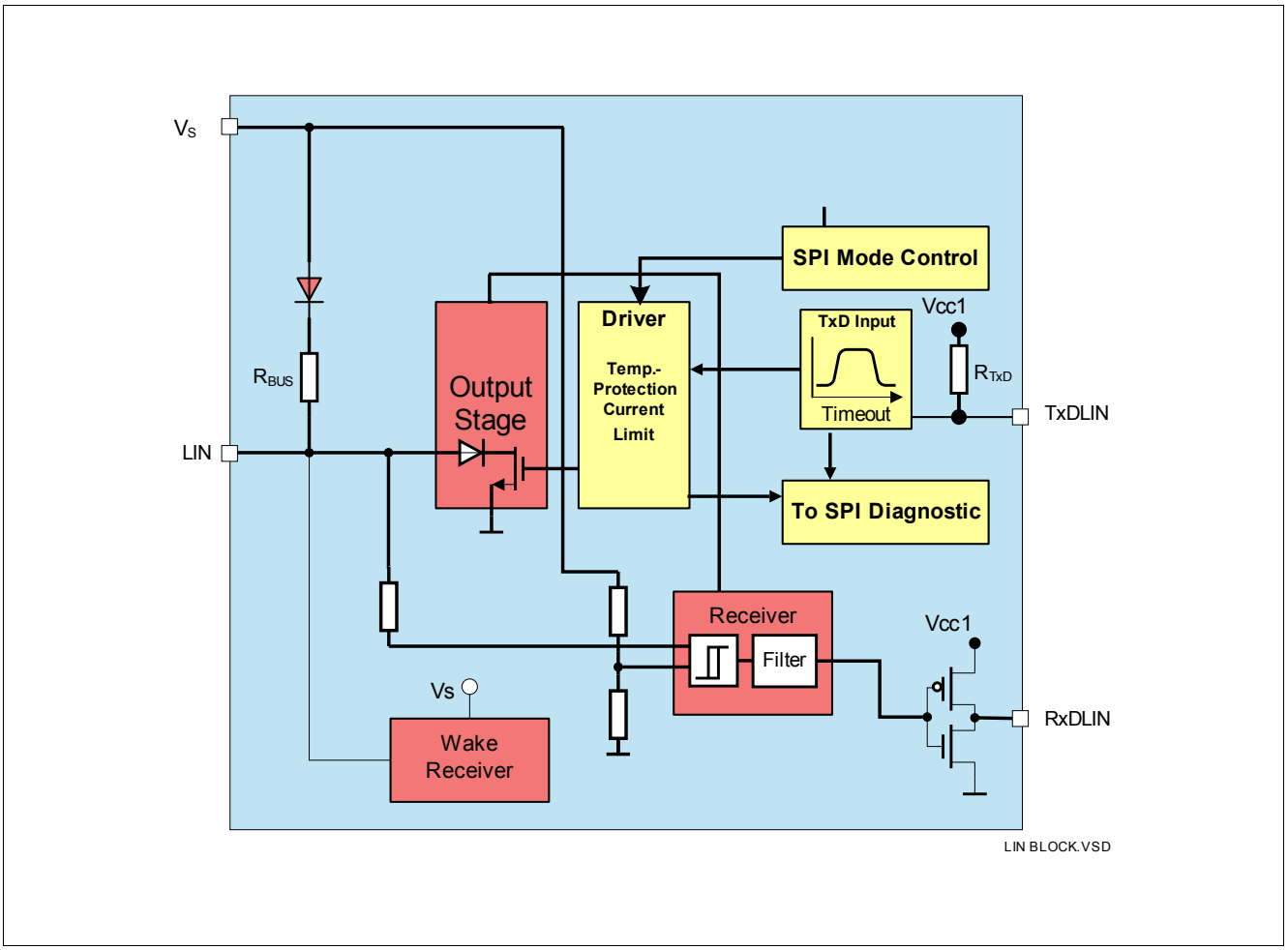


Figure 21 Block Diagram

11.1.1 LIN Specifications

The LIN network is standardized by international regulations. The TLE9266-2QX is compliant to the specification LIN 2.2 (also covers LIN2.2A) and backward compatible to previous LIN specifications LIN2.1, LIN 2.0 or LIN 1.3.

The device is also compliant to the physical layer standard SAE-J2602-2. The SAE-J2602-2 standard differs from the LIN 2.2 standard mainly by the lower data rate (10.4 kbit/s).

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11.2 Functional Description

The LIN Bus is a single wire, bi-directional bus, used for in-vehicle networks. The LIN Transceiver implemented inside the TLE9266-2QX is the interface between the microcontroller and the physical LIN Bus. The digital output data from the microcontroller are driven to the LIN bus via the TXD input pin on the TLE9266-2QX. The transmit data stream on the TXD input is converted to a LIN bus signal with optimized slew rate to minimize the EME level of the LIN network. The RXD output sends back the information from the LIN bus to the microcontroller. The receiver has an integrated filter network to suppress noise on the LIN Bus and to increase the EMI (Electro Magnetic Immunity) level of the transceiver.

Two logical states are possible on the LIN Bus according to the LIN Specification 2.2.

In dominant state, the voltage on the LIN Bus is set close to the GND level. In recessive state, the voltage on the LIN Bus is set close to the supply voltage V_S. By setting the TXD input of the TLE9266-2QX to LOW the transceiver generates a dominant level on the LIN interface pin. The RXD output reads back the signal on the LIN bus and indicates a dominant LIN bus signal with a logical LOW to the microcontroller. Setting the TXD pin to HIGH the transceiver TLE9266-2QX sets the LIN interface pin LIN to the recessive level, at the same time the recessive level on the LIN Bus is indicated by a logical “High” on the RXD output.

Every LIN network consists of a master node and one or more slave nodes. To configure the TLE9266-2QX for master node applications, a resistor in the range of 1 kΩ and a reverse diode must be connected between the LIN bus and the power supply V_S.

11.2.1 LIN OFF Mode

The LIN OFF Mode is the default mode after power-up of the SBC. It is available in all SBC modes and is intended to completely stop LIN activities or when LIN communication is not needed. In LIN OFF Mode, a wake-up event on the bus will be ignored.

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11.2.2 LIN Normal Mode

The LIN Transceiver is enabled via SPI in SBC Normal Mode. LIN Normal Mode is designed for normal data transmission/reception within the LIN network. The mode is available in SBC Normal Mode and in SBC Software Development Mode.

Transmission

The signal from the microcontroller is applied to the TXDLIN input of the SBC. The bus driver switches the LIN output stage to transfer this input signal to the LIN bus line.

Enabling Sequence

The LIN transceiver requires an enabling time $t_{LIN,EN}$ before a message can be sent on the bus. This means that the TXDLIN signal can only be pulled LOW after the enabling time. If this is not ensured, then the TXDLIN needs to be set back to high (=recessive) until the enabling time is completed. Only the next dominant bit will be transmitted on the bus. **Figure 22** shows different scenarios and explanations for CAN enabling.

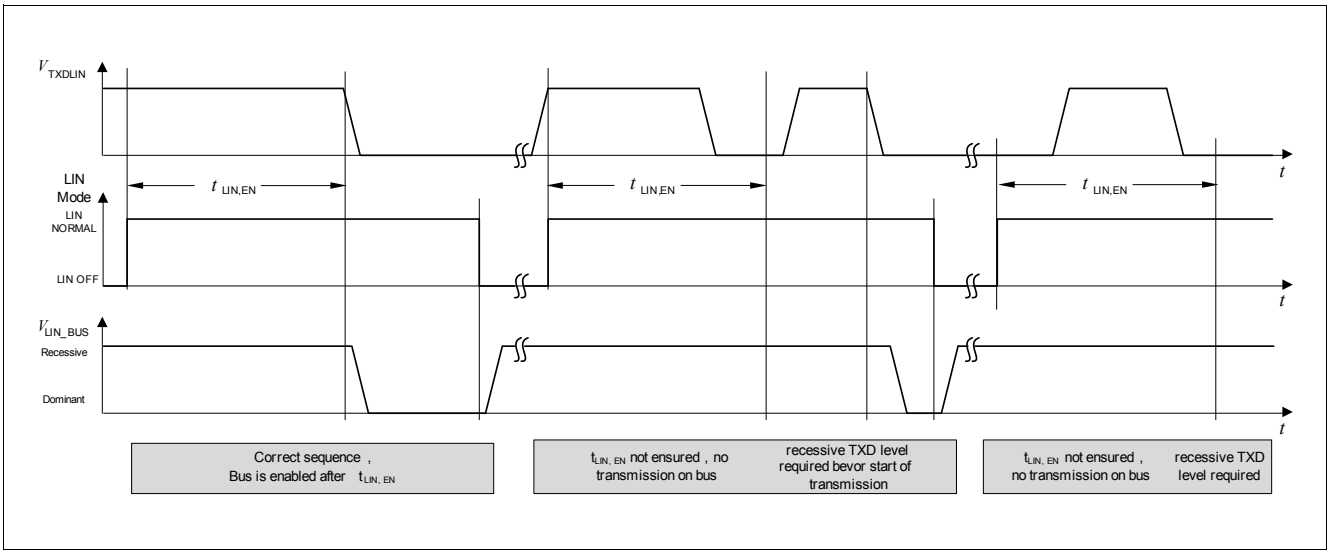


Figure 22 LIN Transceiver Enabling Sequence

Reduced Electromagnetic Emission

To reduce electromagnetic emissions (EME), the bus driver controls LIN slopes symmetrically. The configuration of the different slopes is described in **Chapter 11.2.8**.

Reception

Analog LIN bus signals are converted into digital signals at RXD via the differential input receiver.

11.2.3 LIN Receive Only Mode

In LIN Receive Only Mode (RXD only), the driver stage is de-activated but reception is still possible. This mode is accessible by an SPI command and is available in SBC Normal- and SBC Stop Mode.

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11.2.4 LIN Wake Capable Mode

This mode can be used in SBC Stop, Sleep, Restart and Normal Mode by programming via SPI and it is used to monitor bus activities. It is automatically accessed in SBC Fail-Safe Mode. A valid wake-up signal on the bus (must be a change from dominant to recessive on the LIN bus with a filtering time t > $t_{WK,Bus}$) results in different behavior of the SBC, as described in below **Table 22**. As a signalization to the microcontroller, the RXD_LIN pin is set LOW and will stay LOW until the LIN transceiver is changed to any other mode or until the SBC mode is changed to SBC Sleep-, Stop- or Fail-Safe Mode (automatic rearming - see also below). After the wake-up event the transceiver needs be switched to LIN Normal Mode for communication.

Rearming the Transceiver for Wake Capability

After a BUS wake-up event, the transceiver is woken. However, the **Reserved** transceiver mode bits will still show wake capable (=‘01’) so that the RXD signal will be pulled LOW. There are two possibilities how the LIN transceiver’s wake capable mode is enabled again after a wake-up event:

- The LIN transceiver mode must be toggled, i.e. switched to LIN Normal Mode, LIN Receive Only Mode or LIN OFF, before switching to LIN Wake Capable Mode again.
- Rearming is done automatically when the SBC is changed to SBC Stop-, SBC Sleep-, or SBC Fail-Safe Mode to ensure wake-up capability.

Wake-Up in SBC Stop- and SBC Normal Mode

In SBC Stop Mode, if a wake-up is detected, it is signaled by the INT output and in the **WK_STAT** SPI register. It is also signaled by RxDLIN put to LOW. The same applies for the SBC Normal Mode. The microcontroller should set the device to SBC Normal Mode, there is no automatic transition to Normal Mode.

For functional safety reasons, the watchdog will be automatically enabled in SBC Stop Mode after a Bus wake-up event in case it was disabled before (only if **WD_EN_ WK_BUS** = 1).

Wake-Up in SBC Sleep Mode

Wake-up is possible via a LIN message (filtering time t > $t_{WK,Bus}$). The wake-up automatically transfers the SBC into the SBC Restart Mode and from there to Normal Mode the corresponding RxD pins in set to LOW. The microcontroller is able to detect the LOW signal on RxD and to read the wake source out of the **WK_STAT** register via SPI. No Interrupt is generated when coming out of Sleep Mode. The microcontroller can now switch the LIN transceiver into LIN Normal Mode via SPI to start communication.

Table 15 Action due to a LIN BUS Wake Up

SBC Mode	SBC Mode after Wake	VCC1	INT	RXD
Normal Mode	Normal Mode	ON	LOW	LOW
Stop Mode	Stop Mode	ON	LOW	LOW
Sleep Mode	Restart Mode	Ramping Up	HIGH	LOW
Restart Mode	Restart Mode	ON	HIGH	LOW
Fail-Safe Mode	Restart Mode	Ramping up	HIGH	LOW

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11.2.5 TXD Time - Out

If the TXD signal is dominant for the time t > $t_{TxD_LIN_TO}$, the TXD time-out function deactivates the LIN transmitter output stage temporarily. The transceiver remains in recessive state. The TXD time-out functions prevents the LIN bus from being blocked by a permanent LOW signal on the TXD pin, caused by a failure. The failure is stored in the SPI flag **LIN_FAIL**.

The LIN transmitter stage is activated again after the dominant time-out condition is removed. The level on the TXD must be recessive for at least one clock cycle ($1/f_{CLKSBC}$) to consider the dominant time-out condition is removed. Once this condition is fulfilled, the CAN transceiver requires an enabling time **$t_{LIN,EN}$** before a dominant bit can be sent on the bus again (see also **Figure 22** & **Figure 23**).

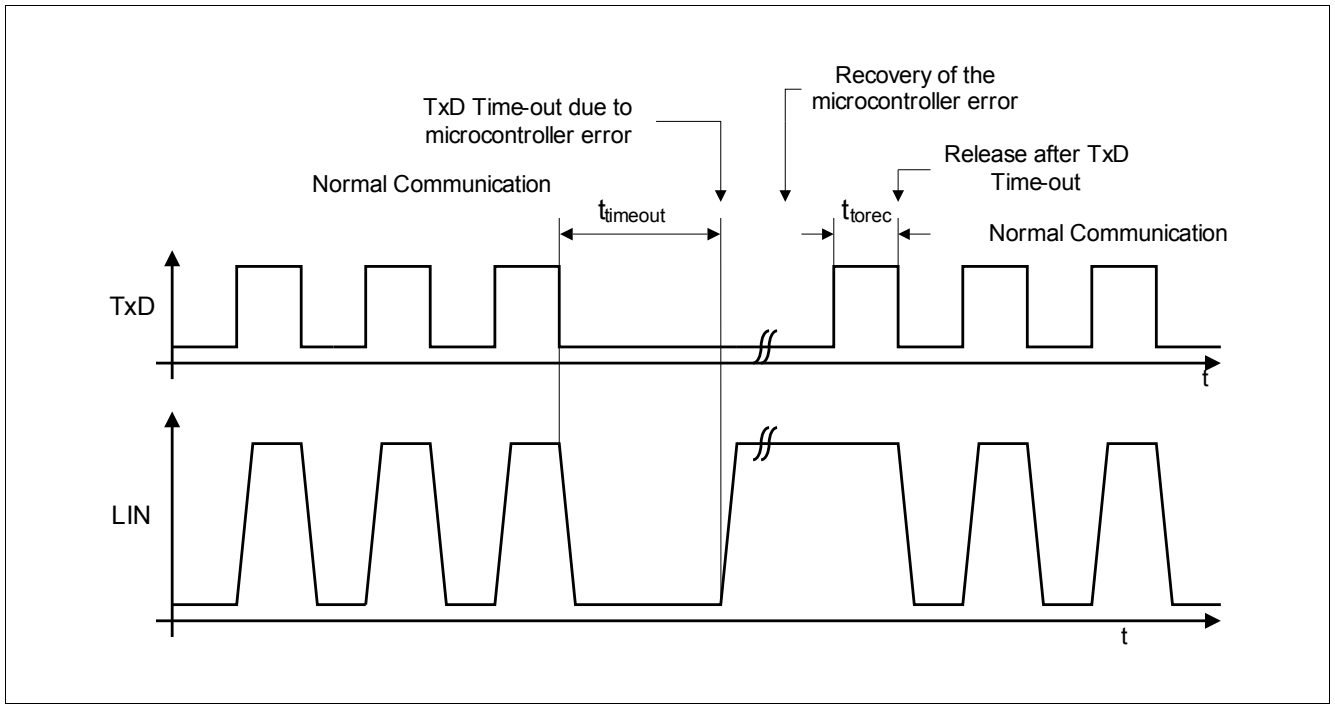


Figure 23 TXD Time-out Function

11.2.6 Bus Dominant Clamping

If the LIN bus signal is dominant for a time t > $t_{BUS_LIN_TO}$, a bus dominant clamping is detected and the SPI bit **LIN_FAIL** is set.

11.2.7 Under-Voltage Detection

In case the supply voltage VS is dropping below the VS under-voltage detection threshold ($V_s < V_{UVD}$), the TLE9266-2QX disables the output and receiver stages. If the power supply VS reaches a higher level than the VS under voltage detection threshold (VS $> V_{UVD}$), the transmitter stage is enabled again. Once this condition is fulfilled, the LIN transceiver requires an enabling time **$t_{LIN,EN}$** before a dominant bit can be sent on the bus again (see also **Figure 22**). A transceiver mode change will only occur if the power supply V_S drops below the power on reset level.

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11.2.8 Slope Selection

The LIN transceiver offers a LIN Low-Slope Mode for 10.4 kBaud communication and a LIN Normal-Slope Mode for 20 kBaud communication. The only difference is the behavior of the transmitter. In LIN Low-Slope Mode, the transmitter uses a lower slew rate to further reduce the EME compared to Normal-Slope Mode. This complies with SAE J2602 requirements.

By default, the device works in LIN Normal-Slope Mode. The selection of LIN Low-Slope Mode is done by an SPI word and will become effective as soon as CSN goes ‘High’. The selection is accessible in SBC Normal Mode only.

11.2.9 Flash Programming via LIN

The device allows LIN flash programming, e.g. of another LIN Slave with a communication of up to 115 kBaud. This feature is enabled by de-activating the slope control mechanism via a SPI command (bit LIN_FLASH) and will become effective as soon as CSN goes ‘High’. The SPI bit can be set in SBC Normal Mode.

Note: It is recommended to perform flash programming only at nominal supply voltage V_S = 13.5V.

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11.3 Electrical Characteristics

Table 16 Electrical Characteristics

V_S = 6 V to 18 V, T_j = -40 °C to +150 °C, R_L = 500 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Receiver Output (RXD pin)							
HIGH Level Output Voltage	$V_{RXD,H}$	0.8 × V_{CC}	–	–	V	I_{RXD} = -1.6 mA; V_{bus} = V_S	P_11.3.1
LOW Level Output Voltage	$V_{RXD,L}$	–	–	0.2 × V_{CC}	V	I_{RXD} = 1.6 mA V_{bus} = 0 V	P_11.3.2
Transmission Input (TXD pin)							
HIGH Level Input Voltage	$V_{TXD,H}$	0.7 × V_{CC}	–	–	V	Recessive State	P_11.3.3
TXD Input Hysteresis	$V_{TXD,hys}$	–	0.12 × V_{CC}	–	mV	1)	P_11.3.4
LOW Level Input Voltage	$V_{TXD,L}$	–	–	0.3 × V_{CC}	V	Dominant State	P_11.3.5
TXD Pull-up Resistance	R_{TXD}	20	40	80	kΩ	V_{TXD} = 0 V	P_11.3.6
LIN Bus Receiver (LIN Pin)							
Receiver Threshold Voltage, Recessive to Dominant Edge	$V_{Bus,rd}$	0.4 × V_S	0.45 × V_S	–	V	$V_{Bus,rec}$ < V_{Bus} < 27 V	P_11.3.7
Receiver Dominant State	$V_{Bus,dom}$	–	–	0.4 × V_S	V	LIN 2.2 Param. 17	P_11.3.8
Receiver Threshold Voltage, Dominant to Recessive Edge	$V_{Bus,dr}$	–	0.55 × V_S	0.60 × V_S	V	$V_{Bus,rec}$ < V_{Bus} < 27 V	P_11.3.9
Receiver Recessive State	$V_{Bus,rec}$	0.6 × V_S	–	–	V	LIN 2.2 Param 18	P_11.3.10
Receiver Center Voltage	$V_{Bus,c}$	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	LIN 2.2 Param 19	P_11.3.11
Receiver Hysteresis	$V_{Bus,hys}$	0.07 × V_S	0.1 × V_S	0.175 × V_S	V	$V_{bus,hys}$ = $V_{bus,dr}$ - $V_{bus,rd}$ LIN 2.2 Param 20	P_11.3.12
Wake-up Threshold Voltage	$V_{Bus,wk}$	0.40 × V_S	0.5 × V_S	0.6 × V_S	V	–	P_11.3.13
Dominant Time for Bus Wake-up	$t_{WK,Bus}$	30	–	150	µs	–	P_11.3.14
LIN Bus Transmitter (LIN Pin)							
Bus Serial Diode Voltage Drop	$V_{serdiode}$	0.4	0.7	1.0	V	1) VTXD = VCC1; LIN 2.2 Param 21	P_11.3.15
Bus Recessive Output Voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TXD} = HIGH Level	P_11.3.16
Bus Short Circuit Current	$I_{BUS,sc}$	40	100	150	mA	V_{BUS} = 13.5 V; LIN 2.2 Param 12	P_11.3.20

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Table 16 Electrical Characteristics (cont'd)

V_S = 6 V to 18 V, T_j = -40 °C to +150 °C, R_L = 500 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Leakage Current Loss of Ground	$I_{BUS,lk1}$	-1000	-450	0	µA	V_S = 0 V; V_{BUS} = -12 V; LIN 2.2 Param 15	P_11.3.21
Leakage Current Loss of Battery	$I_{BUS,lk2}$	–	–	20	µA	V_S = 0 V; V_{BUS} = 18 V; LIN 2.2 Param 16	P_11.3.22
Leakage Current	$I_{BUS,lk3}$	-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; LIN 2.2 Param 13	P_11.3.23
Leakage Current Driver OFF	$I_{BUS,lk4}$	–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V; LIN 2.2 Param 14	P_11.3.24
Bus Pull-up Resistance	R_{BUS}	20	30	47	kΩ	Normal Mode LIN 2.2 Param 26	P_11.3.25
LIN Input Capacitance	C_{BUS}		20	25	pF	1)	P_11.3.26
Receiver propagation delay bus dominant to RXD LOW	$t_{d(L),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RXD} = 20 pF; LIN 2.2 Param 31	P_11.3.27
Receiver propagation delay bus recessive to RXD HIGH	$t_{d(H),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RXD} = 20 pF; LIN 2.2 Param 31	P_11.3.28
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; LIN 2.2 Param 32	P_11.3.29
LIN Transceiver Enabling Time	$t_{LIN,EN}$	–	10	–	µs	2) CSN = HIGH to first valid transmitted TXD dominant	P_11.3.39
Bus Dominant Time Out	$t_{BUS_LIN_TO}$	–	20	–	ms	1)2)	P_11.3.30
TXD Dominant Time Out	$t_{TxD_LIN_TO}$	–	20	–	ms	1)2) V_{TXD} = 0 V	P_11.3.31
TXD Dominant Time Out Recovery Time	t_{torec}	–	10	–	µs	1)2)	P_11.3.32
Duty Cycle D1 (For worst case at 20 kbit/s) LIN 2.2 Normal Slope	D1	0.396	–	–		3) TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 7.0 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus_rec(min)}$/2 t_{bit}; LIN 2.2 Param 27	P_11.3.33
Duty Cycle D2 (for worst case at 20 kbit/s) LIN 2.2 Normal Slope	D2	–	–	0.581		3)TH_{Rec}(min.) = 0.422 × V_S; TH_{Dom}(min.) = 0.284 × V_S; V_S = 7.6 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus_rec(max)}$/2 t_{bit}; LIN 2.2 Param 28	P_11.3.34

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Table 16 Electrical Characteristics (cont'd)

V_S = 6 V to 18 V, T_j = -40 °C to +150 °C, R_L = 500 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Duty Cycle D3 (for worst case at 10.4 kbit/s) SAE J2602 Low Slope	D3	0.417	–	–		3)TH_{Rec}(max) = 0.778 × V_S; TH_{Dom}(max) = 0.616 × V_S; V_S = 7.0 … 18 V; t_{bit} = 96 µs; D3 = $t_{bus_rec(min)}$/2 t_{bit}; LIN 2.2 Param 29	P_11.3.35
Duty Cycle D4 (for worst case at 10.4 kbit/s) SAE J2602 Low Slope	D4	–	–	0.590		3)THRec(min.) = 0.389 × VS; THDom(min.) = 0.251 × VS; VS = 7.6 … 18 V; tbit = 96 µs; D4 = tbus_rec(max)/2 tbit; LIN 2.2 Param 30	P_11.3.36

1) Not subject to production test, specified by design.

2) Not subject to production test, tolerance defined by internal oscillator tolerance

3) Bus load conditions concerning LIN spec 2.1 C_{LIN}, R_{LIN} = 1 nF, 1 kΩ / 6.8 nF, 660 Ω/ 10 nF, 500 Ω

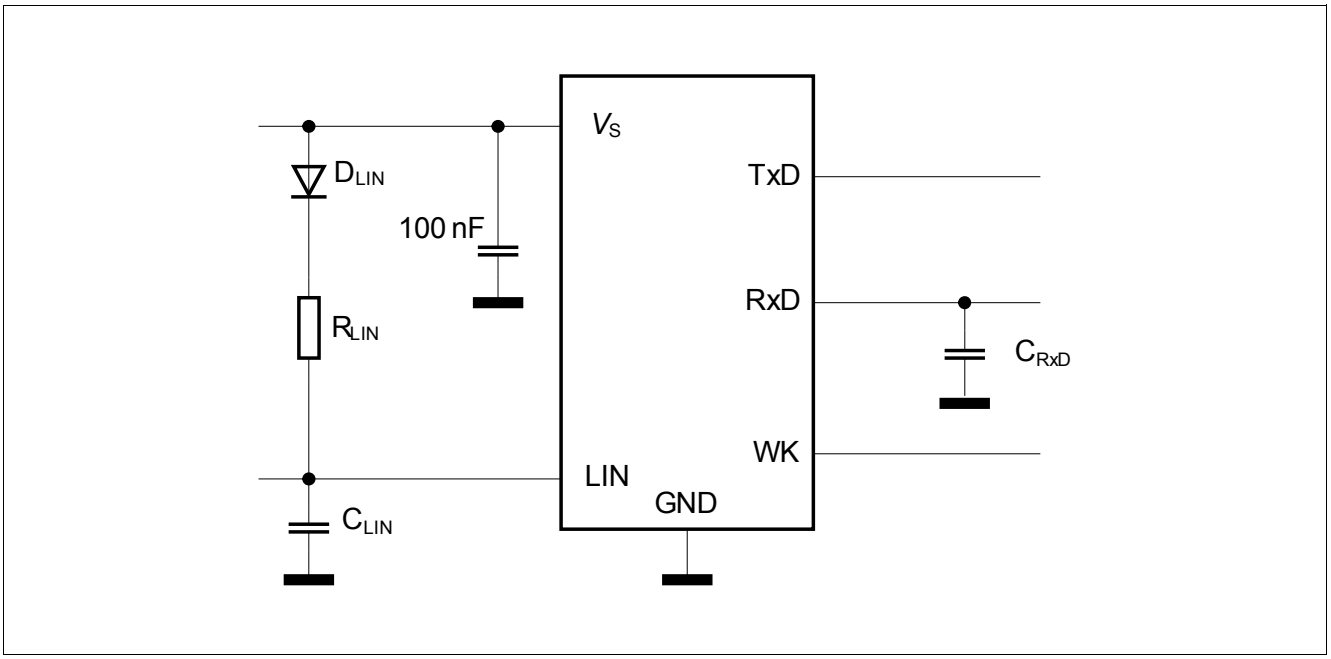


Figure 24 Simplified Test Circuit for Dynamic Characteristics

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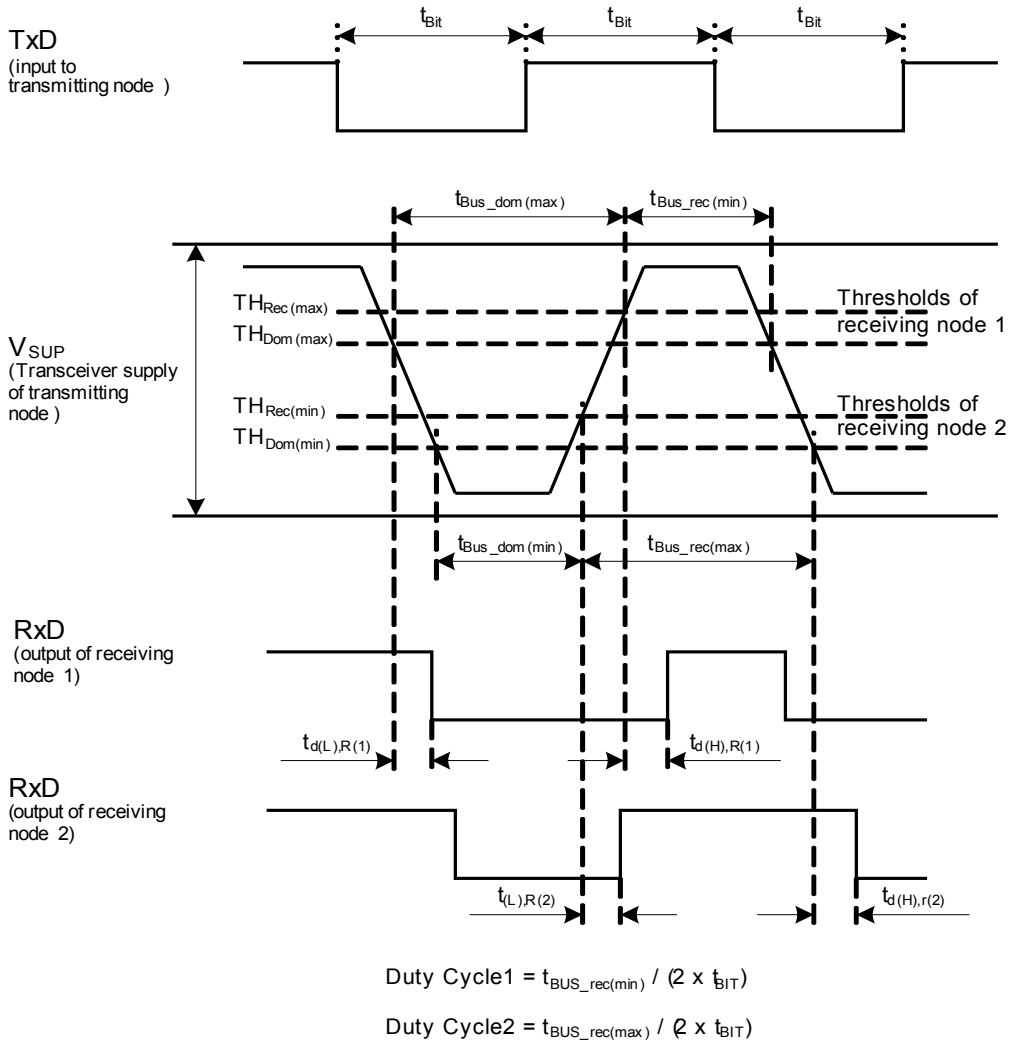


Figure 25 Timing Diagram for Dynamic Characteristics

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12 Wake and Voltage Monitoring Inputs

12.1 Block Description

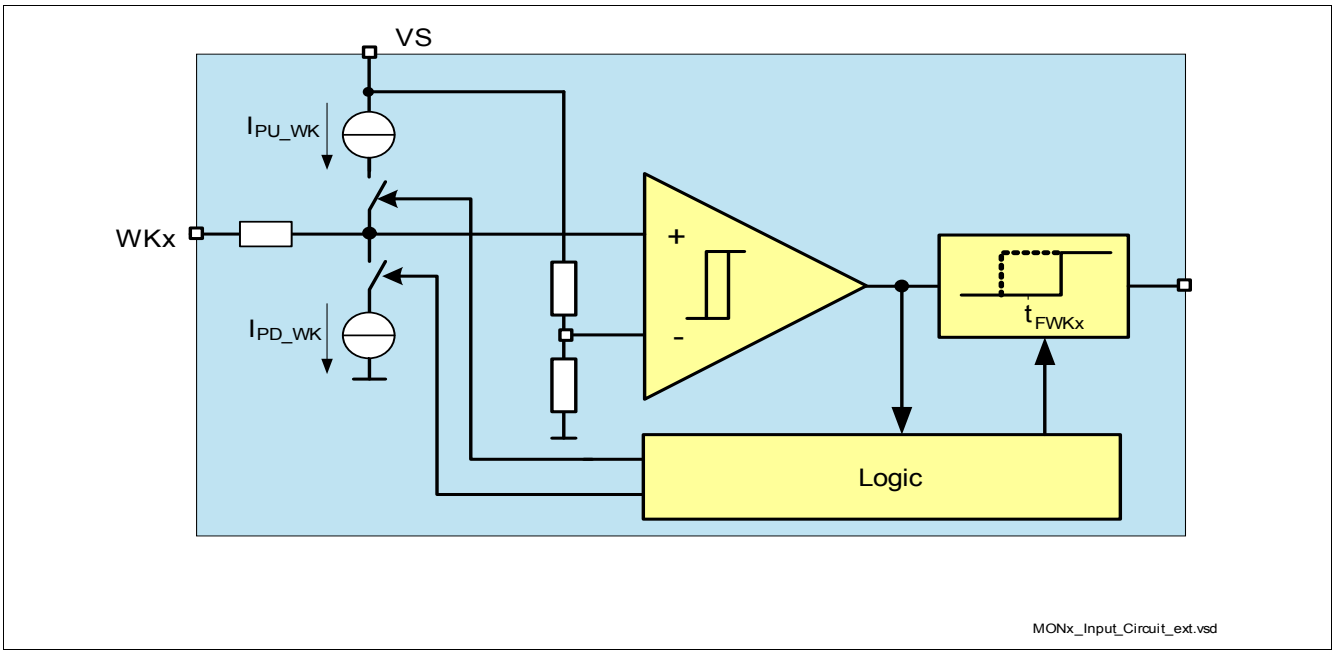


Figure 26 Wake Input Block Diagram

Features

- Three high-voltage inputs (WK1...3) with VS/2 threshold voltage
- Alternate measurement function for high-voltage sensing via WK1 and WK2
- One 5V input with VCC/2 threshold voltage configurable as WK4 or SYNC input
- Selectable SYNC input for external control of cyclic sense / cyclic wake, e.g. via microcontroller
- Wake-up capability for power saving modes
- Level-sensitive wake feature LOW to HIGH and HIGH to LOW
- In SBC Normal- and SBC Stop Mode the level of the WK pin can be read via SPI even if the respective WK is not enabled as a wake source.
- Pull-up and Pull-down current sources, configurable via SPI
- Selectable configuration for cyclic wake / cyclic sense
- Cyclic sense working with TIMER1, TIMER2
- Cyclic sense can be selected to connect to any high-side switch (HS1...6)

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12.2 Functional Description

The SBC can wake up by a voltage level change at the wake inputs. The WK input pins are level sensitive input. This means that both transitions, HIGH to LOW and LOW to HIGH, result in a wake-up. The switching threshold is designed for VS/2 for WK1...3 and VCC1/2 for WK4. The WK input filtering time (16 µs or 64 µs) can be selected via SPI (**WK1_FLT**...4).

The wake-up capability for each WK pin can be enabled or disabled via SPI command in the **WK_CTRL_2** register. When setting the bit WK1_EN, WK2_EN, WK3_EN or WK4_EN to 1, the device wakes up from SBC Sleep Mode with a HIGH to LOW or LOW to HIGH transition on the selected WK input. An interrupt will be generated in SBC Stop Mode and in SBC Normal Mode. From SBC Fail-Safe Mode the device will always go to SBC Restart Mode with a HIGH to LOW or LOW to HIGH transition.

The wake source for a wake via a WKx pin can always be read in the register **WK_STAT** at the bits WK1_WU, WK2_WU, WK3_WU, and WK4_WU.

The actual voltage level of the WK pin (LOW or HIGH) can always be read in SBC Normal and SBC Stop Mode in the register **WK_LVL_STAT**. During cyclic sense, the register show the sampled levels of the respective WK pin.

WK4 is not a default wake source to avoid an unintentional wake if the pin is configured as SYNC.

By selecting the SYNC input, the cyclic sense function can be controlled externally via the microcontroller. It can be configured (SPI registers **TIMER1_CTRL** and **HS_CTRL1**...3) to control either the period, or the on-time or both parameters (see also **Chapter 5.2**).

*Note: It is not possible to select SYNC (ON, OFF or both) for cyclic sense / cyclic wake when WK4 is enabled. In this case the timer is not started and the **SPI_FAIL** bit is set. So first the pin must be configured to SYNC via the bit **WK4_SYNC** before starting cyclic wake / cyclic sense.*

12.2.1 Wake Input Configuration

The WK inputs can be configured independently via the SPI register **WK_PUPD_CTRL**

Note: If there is no pull-up or pull-down configured on the WK input, then the respective input should be tied to GND or VS on board to avoid unintended floating and waking of the pin.

Table 17 Pull-Up / Pull-Down Resistor

WKx_PUPD_1	WKx_PUPD_0	Output Current	
0	0	no resistor	
0	1	pull-down	
1	0	pull-up	
1	1	Automatic switching	If a HIGH level is detected the pull-up is activated, if LOW level is detected the pull down is activated.

During SBC Sleep Mode, the configurations ‘01’, ‘10’ and ‘11’ are not available for WK4. The pull-up/down configurations of WK4 are supplied by VCC1, which is disabled during SBC Sleep Mode. This must be considered by the application.

Note: To avoid an unintentional wake-up at WK4, it is recommended to define the level of WK4 with an external pull-up/down circuitry if possible.

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The filter time configuration of each WK input is done via the SPI register **WK_FLT_CTRL**. The user can choose between static sensing and cyclic sensing with an assigned HS switch or cyclic wake respectively.

Table 18 Wake Filter Time

WKx_FLT_1	WKx_FLT_0	Filter Time	
0	0	Config A	16µs filter Time, no cyclic sense
0	1	Config B	64µs filter Time, no cyclic sense
1	0	Config C	Timer 1, 16µs filter time. Period, on-time and settle time configurable in register **TIMER1_CTRL**
1	1	Config D	Timer 2, 16µs filter time. Period, on-time and settle time configurable in register **TIMER2_CTRL**

Configurations C or D are intended for cyclic sense configuration. With the filter settings, the respective timer needs to be assigned to one or more HS output, which supplies an external circuit connected to the WKx pin, e.g. HS1 controlled by Timer 2 (HS1 = 010) and connected to WK3 via an switch circuitry - see also **Chapter 5.2**.

If SYNC is selected to control the cyclic sense or cyclic wake timing, then the WK4/SYNC pin is automatically configured with a pull down (**WK4_PUPD** = ‘01’) but register values will be kept. When SYNC is selected to stop the on-time, then the default filter time (see **WK_FLT_CTRL**) is selected.

12.2.2 Alternate Measurement Function with WK1 and WK2

12.2.2.1 Block Description

This function provides the possibility to measure a voltage, e.g. the unbuffered battery voltage, with the protected WK1 high-voltage input. The measured voltage is routed out at WK2. It allows for example a voltage compensation for LED lighting by changing the duty cycle of the high-side outputs according to the supply voltage. A simple voltage divider needs to be placed externally to provide the correct voltage level to the microcontroller A/D converter input.

The function is available in SBC Normal Mode and it is disabled in all other modes to allow a low-quiescent current operation.The measurement function can be used instead of the WK1 and WK2 wake and level signalling capability.

The benefits of the function is that the signal is measured by a HV-input pin and that there is no current flowing through the resistor divider during low-power modes.
The functionality is shown in a simplified application diagram in **Figure 4**.

12.2.2.2 Functional Description

This measurement function is by default disabled. In this case, WK1 and WK2 have the regular wake and voltage level signalization functionality. The switch S1 is open for this configuration (see **Figure 4**).

The measurement function can be enabled via the SPI bit **WK_MEAS**.

If **WK_MEAS** is set to ‘1’, then the measurement function is enabled and switch S1 is closed in SBC Normal Mode. S1 is open in all other SBC modes. In this function the pull-up and down currents of WK1 and WK2 are disabled and the internal WK1 and WK2 signals are gated. In addition, the settings for WK1 and WK2 in the registers **WK_PUPD_CTRL**, **WK_FLT_CTRL** and **WK_CTRL_2** are ignored but changing these setting is not prevented. The registers **WK_STAT** and **WK_LVL_STAT** are not updated with respect to the inputs WK1 and WK2.
However, if only WK1 or WK2 are set as wake sources and a SBC Sleep Mode command is sent, then the **SPI_FAIL** flag will be set and the SBC will be changed into SBC Restart Mode. See below table for further details.

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Table 19 Differences between normal WK Function and Measurement Function

Affected settings/modules for WK1 and WK2 inputs	WK_MEAS = 0	WK_MEAS = 1
S1 configuration	'open'	'closed' in SBC Normal Mode, 'open' in all other SBC modes
Internal WK1 & WK2 signal processing	Default wake and level signaling function, WK_STAT, WK_LVL_STAT are updated accordingly	'WK1...2 inputs are gated internally, WK_STAT, WK_LVL_STAT are not updated
WK1_EN, WK2_EN	Wake up via WK1 and WK2 possible if bits are set	setting the bits is ignored and not prevented. If only WK1_EN, WK2_EN are set while trying to go to SBC Sleep Mode, then the SPI_FAIL flag will be set and the SBC will be changed into SBC Restart Mode.
WK_PUPD_CTRL	normal configuration is possible	no pull-up or pull-down enabled
WK_FLT_CTRL	normal configuration is possible	setting the bits is ignored and not prevented

*Note: There is a diode in series to the switch S1 (not shown in the **Figure 4**), which will influence the temperature behavior of the switch.*

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12.3 Electrical Characteristics

Table 20 Electrical Characteristics

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
WK1...WK3 Input Pin Characteristics							
Wake-up/monitoring threshold voltage	V_{WKth}	0.4*V_s	0.5*V_s	0.6*V_s	V	without external serial resistor R_s (with R_s:DV = $I_{PD/PU}$ * R_s);	P_12.3.1
Threshold hysteresis	$V_{WKth,hys}$	0.02*V_s	0.06*V_s	0.12*V_s	V	1)without external serial resistor Rs (with Rs:DV = IPD/PU * Rs);	P_12.3.2
WK pin Pull-up Current	I_{PU_WK}	-20	-10	-3	µA	V_{WK_IN} = 0,6*V_s	P_12.3.3
WK pin Pull-down Current	I_{PD_WK}	3	10	20	µA	V_{WK_IN} = 0.4*V_s	P_12.3.4
Input leakage current	$I_{LK,I}$	-2		2	µA	0 V < V_{WK_IN} < 40V	P_12.3.5
Drop Voltage across S1 switch	$V_{Drop,S1}$	–	1000	–	mV	1)Drop Voltage between WK1 and WK2 when enabled for voltage measurement; I_{WK1} = 500µA; T_j = 25°C	P_12.3.13
Timing							
Wake-up filter time	t_{FWK1}	-	16	-	µs	2)SPI Setting	P_12.3.6
Wake-up filter time	t_{FWK2}	-	64	-	µs	2)SPI Setting	P_12.3.7
WK4/SYNC							
WK4/SYNC threshold voltage	V_{WK4th}	1.5	–	3.5	V	3)SBC Normal- and SBC Stop Mode; without external serial resistor R_s (with R_s:DV = $I_{PD/PU}$ * R_s);	P_12.3.10
Hysteresis of WK4/SYNC input voltage	$V_{WK4,hys}$	–	0.8	–	V	1)	P_12.3.11
Pull-down Resistance at pin WK4/SYNC	R_{SYNC}	20	40	80	kΩ	4)V_{SYNC} = 1V	P_12.3.12

1) Not subject to production test; specified by design

2) Not subject to production test, tolerance defined by internal oscillator tolerance

3) The parameter applies only for SBC Normal and Stop Mode, the lower threshold is lower in SBC Sleep Mode

4) Only applies if pin is configured as SYNC. If configured as WK4 then settings in SPI register **WK_PUPD_CTRL** will apply. The pull-up resistor has the same value as the pull-down resistor.

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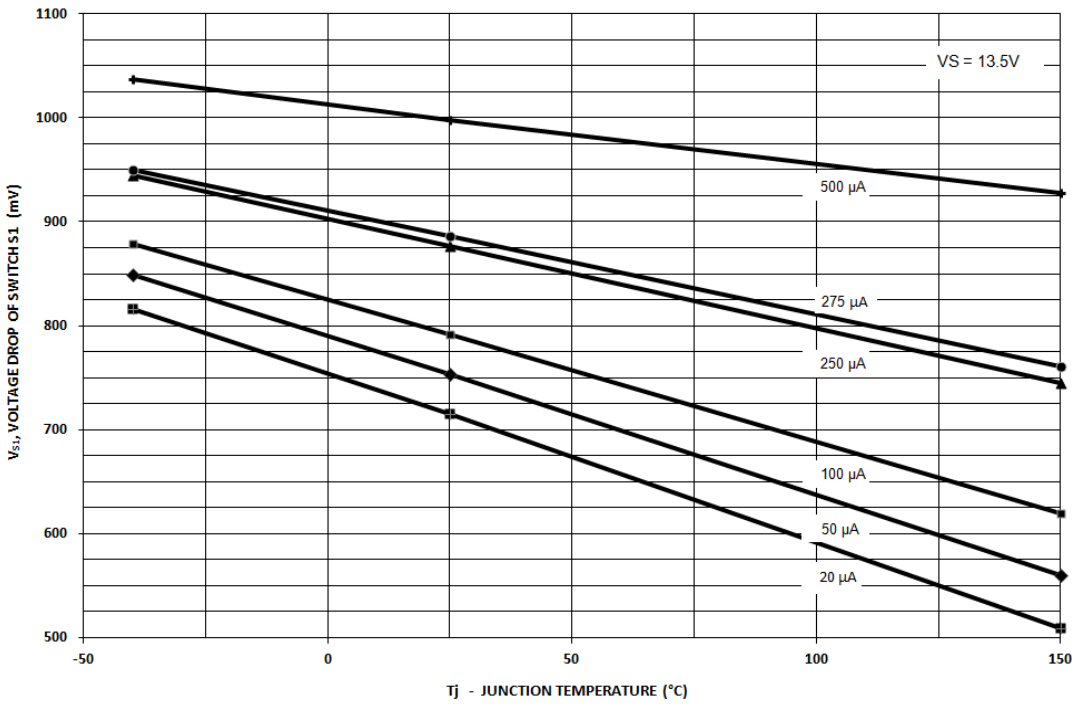


Figure 27 Typical Characteristics of S1 Drop Voltage (between WK1 & WK2) vs. Temperature for different S1 currents

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13 Interrupt Function

13.1 Block and Functional Description

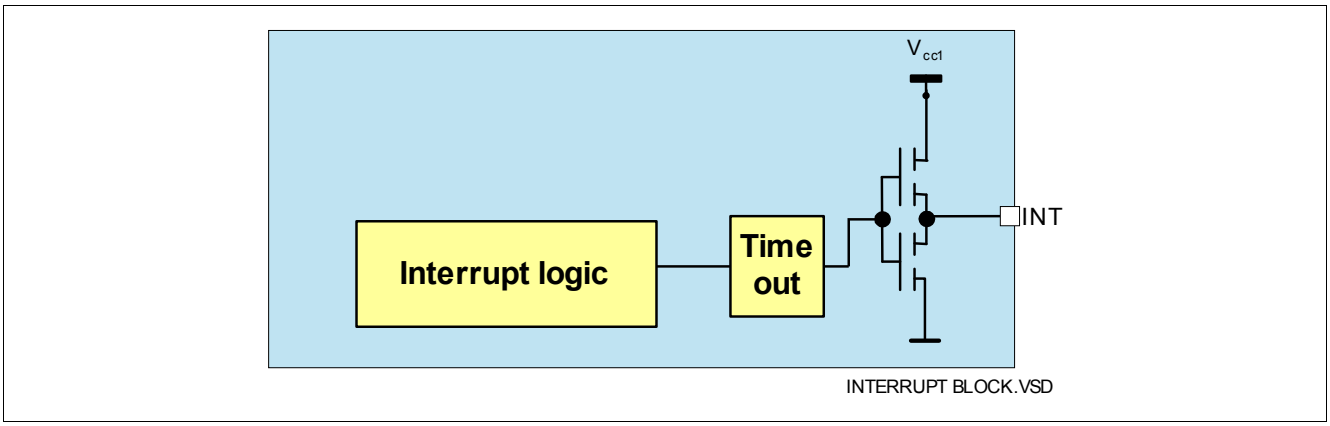


Figure 28 Interrupt Block Diagram

As shown in **Figure 28** INT is designed as a push/pull output stage. An interrupt is triggered and INT is pulled LOW (active LOW) for t_{INT} in SBC Normal- and SBC Stop Mode in case of a wake-up event via:

- LIN
- CAN
- WK1...4
- cyclic wake (Timer1 and Timer2)
- tripping the I_{WD_OFF} threshold on VCC1 in SBC Stop Mode

An interrupt is only triggered if the respective function is also enabled as a wake source in **WK_CTRL_2**.

No Interrupt is generated for a failure detection, e.g. for HSx failure. When the SBC is in Stop Mode and an interrupt is triggered, then the mode is not left automatically.

If the device is in SBC Stop Mode with IVCC1 > I_{WD_OFF} and the watchdog is not disabled, then an interrupt is also generated if IVCC1 > I_{WD_OFF}. The intention is to signal the microcontroller that the watchdog has restarted and needs to be triggered again. The wake signalization of an I_{WD_OFF} threshold crossing can be disabled by clearing the bit **WD_STM_ WK_EN** in **WK_CTRL_1**.

The SPI register **WK_STAT** is updated at every falling edge of the INT pulse. All wake-up events are stored in this register until the register is READ and cleared via SPI command. A second SPI read after reading out the **WK_STAT** register is optional but recommended to verify that the wake-up event is not present anymore. The Interrupt behavior is shown in **Figure 29**.

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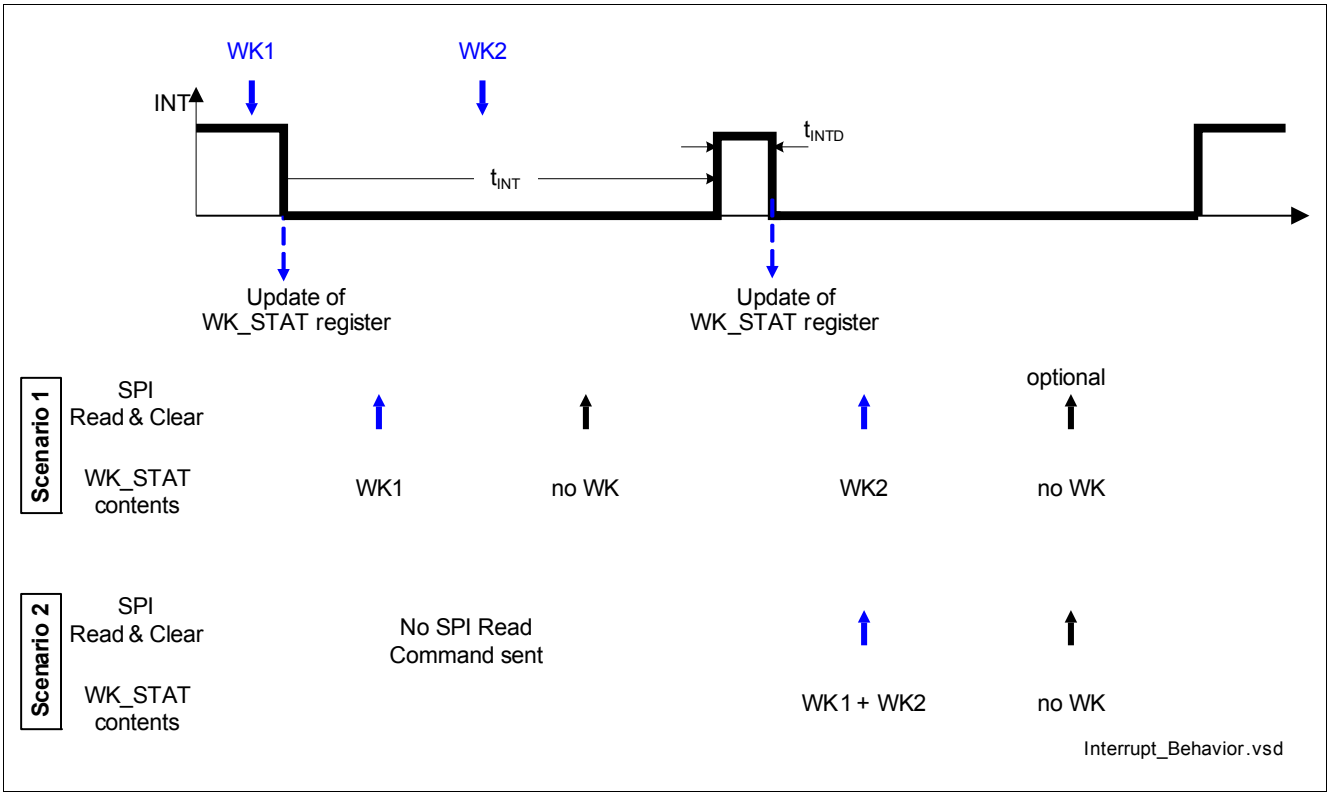


Figure 29 Interrupt Signalization Behavior

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13.2 Electrical Characteristics

Table 21 Interrupt Output

V_S = 6 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Interrupt output; Pin INT							
INT High Output Voltage	$V_{INT,H}$	0.8 × V_{CC1}	–	–	V	I_{INT} = -1 mA; INT = OFF	P_13.2.1
INT LOW Output Voltage	$V_{INT,L}$	–	–	0.2 × V_{CC1}	V	I_{INT} = 1 mA; INT = ON	P_13.2.2
INT Pulse Width	t_{INT}	–	100	–	µs	1)	P_13.2.3
INT Pulse Minimum Delay Time	t_{INTD}	–	100	–	µs	1) between consecutive pulses	P_13.2.4

1) Not subject to production test, tolerance defined by internal oscillator tolerance.

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14 Fail Output

14.1 Block and Functional Description

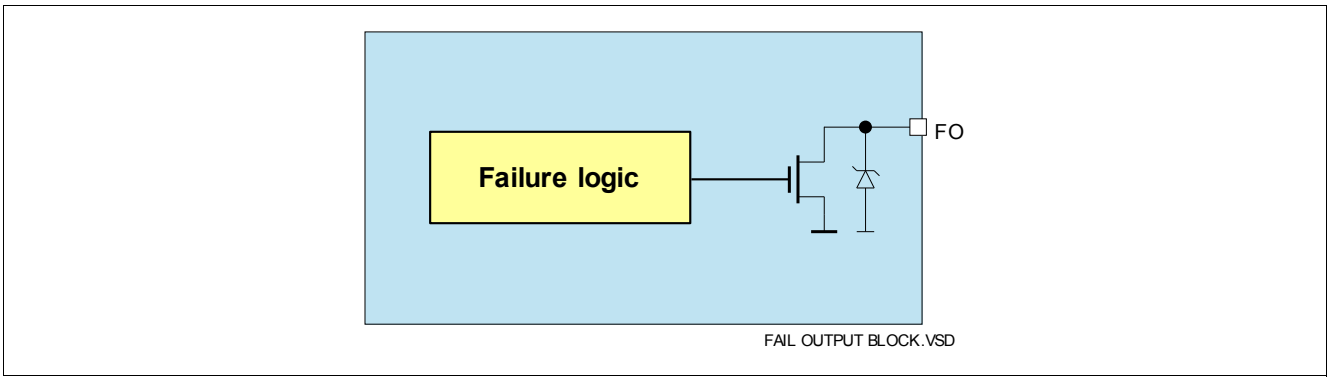


Figure 30 Fail Output Block Diagram

The Fail Output consists of a failure logic block and a low-side switch. In case of failure the FO output is activated (pulled to low) and the SPI bit **FAILURE** in the register **DEV_STAT** is set.

The Fail Output is activated due to following failure conditions:

Failure Conditions

- One watchdog trigger failure
- VCC1 under voltage
- Thermal shutdown TSD2
- SDI stuck at “HIGH” or “LOW”

In order to deactivate the Fail Output the failure conditions (e.g. TSD2, ...) must not be present anymore and the bit **FAILURE** needs to be cleared via SPI command. In case of watchdog fail, the deactivation of the Fail Output is only allowed after a successful WD trigger, which will automatically clear the **WD_FAIL** bits.

Note: The Fail output pin is triggered for any of the above described failure and not only for failures leading to the SBC Fail-Safe Mode.

It is also possible to activate the FO pin manually via the SPI bit **FO_ON**, e.g. for verification purposes. The FO output can also be disabled again by clearing this bit as long as none of the above described failure conditions are present. In this case, the FO will stay activated until the failure is not present anymore.

*Note: The **FAILURE** bit will not be updated in the SPI register **DEV_STAT** if **FO_ON** is set because it is not considered as a failure.*

14.1.1 Inverted Low-Side Logic Option

The Fail Output pin also activates the LSx outputs for the derivative product with the inverted low-side logic. For further details please refer to **Table 10** in **Chapter 9.2.3** and to the **LS_CTRL LS_normal** register.

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14.2 Electrical Characteristics

Table 22 Interrupt Output

V_S = 6 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Fail Output; Pin FO							
FO LOW output voltage (active)	$V_{FO,L}$	–	0.1	0.2	V	I_{FO} = 1mA	P_14.2.1
FO HIGH output current (inactive)	$I_{FO,H}$	0	–	2	µA	V_{FO} = 28V	P_14.2.2

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15 Supervision Functions

15.1 Reset Function

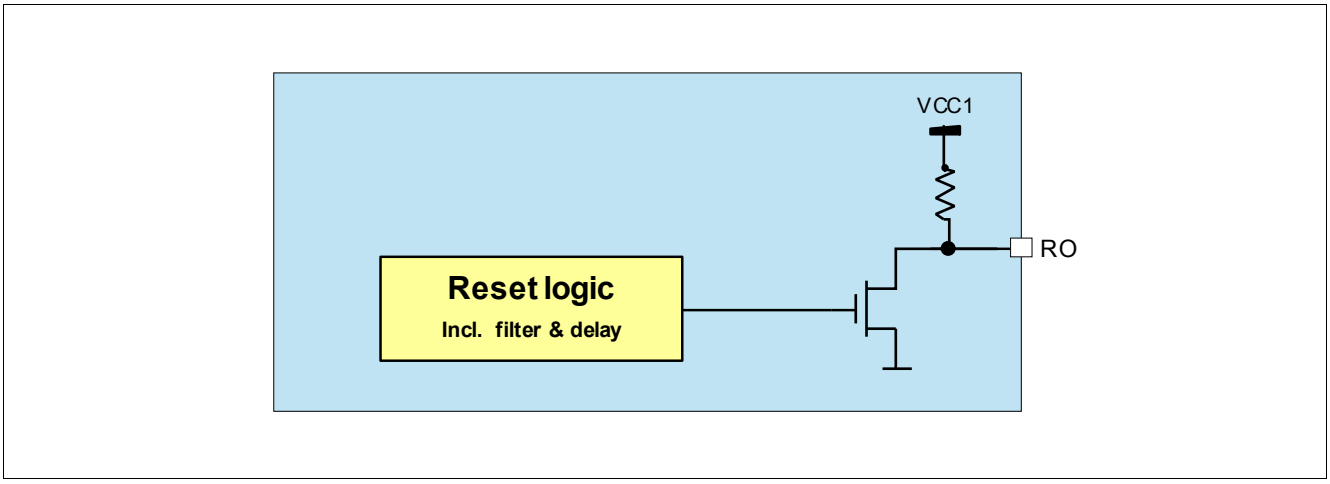


Figure 31 Reset Block Diagram

15.1.1 Reset Output Description

The reset output pin RO provides a reset information to the microcontroller, for example, in the event that the output voltage has fallen below the under voltage threshold $V_{RT1/2/3/4}$. In case of a reset event, the reset output RO is pulled to LOW after the filter time t_{RF} and stays LOW as long as the reset event is present including a reset delay time t_{RD1}. When connecting the SBC to battery voltage, the reset signal remains LOW initially. When the output voltage V_{cc1} has reached the default reset threshold $V_{RT1,f}$, the reset output RO is released to HIGH after the reset delay time t_{rd1}. A reset can also occur due to a watchdog trigger failure. The reset threshold can be adjusted via SPI. The thresholds have a larger tolerance in SBC Stop Mode.
The RO pin has an integrated pull-up resistor.
In case reset is triggered, it will be pulled LOW for V_{cc1} ≥ 1V and for VS ≥ $V_{POR,f}$.

15.1.2 Soft Reset Description

It is also possible to trigger a Soft Reset via an SPI command in order to bring the SBC into a defined state in case of failures. In this case the microcontroller must send a SPI command and set the **MODE** bits to '11' in the **M_S_CTRL** register. As soon as this command becomes valid, the SBC is set back to SBC INIT Mode and all SPI registers are set to their default values (see SPI **Chapter 16.5** and **Chapter 16.6**).
There is no Reset (RO) triggered when the soft reset is executed.

Note: The device must be in SBC Normal Mode when sending this command

15.2 Window Watchdog Function

The watchdog is used to monitor the software execution of the microcontroller and to trigger a reset if the microcontroller stops serving the watchdog due to a lock up in the software. In case of the window watchdog, the microcontroller must trigger the watchdog in a certain time frame, the so called open window, of the selected timeout period.

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The watchdog timing is programmed via SPI command. As soon as the watchdog is programmed, the timer starts with the new setting and the watchdog must be served. Please refer to **Table 23** to match the SBC modes with the respective watchdog modes.

The long open window (t_{LW}) allows the microcontroller to run its initialization sequences and then to trigger the watchdog via the SPI.

The watchdog is served (=triggered) by SPI with a WRITE access to the watchdog register.

In case of a watchdog reset, SBC Restart Mode is entered and RO is pulled low. The SBC transitions automatically to Normal Mode after the reset delay time t_{RD1} and RO is deactivated (pulled HIGH) and the watchdog immediately starts with a long open window.

In SBC Software Development Mode, no reset is generated due to watchdog failure, the watchdog is OFF.

Table 23 Watchdog Functionality by SBC Modes

SBC Mode	Watchdog Mode	Remarks
INIT Mode	Start after Init Mode	Watchdog starts with long open window
Normal Mode	WD Programmable;	–
Stop Mode	Watchdog is fixed	Watchdog OFF depending on setting and current on VCC1
Sleep Mode	OFF	SBC does not remain the set-up.
Restart Mode	OFF	SBC will start with long open window when entering Normal Mode.

15.2.1 Window Watchdog

The watchdog is triggered by sending a valid SPI-WRITE command to the watchdog configuration SPI register **WD_CTRL**. The WD-trigger command is executed when the CSN input becomes HIGH.

A correct watchdog trigger results in starting the window watchdog by a closed window with a width of typically 60% of the selected Window Watchdog Timer period. The closed window is followed by an open window.

The ratio between open and closed window as well as the tolerance of the oscillator defines the “safe trigger area” of the programmed window watchdog time (see **Figure 32**). The safe trigger area is therefore between 72% and 120% of the selected window watchdog timer period. This period, selected via the window watchdog timing bit field (**WD_TIMER**), is in the range of 10 ms to 1000 ms.

A correct watchdog service immediately results in starting the next closed window.

Should the trigger signal meet the closed window, a watchdog reset is created by setting the reset output RO LOW and the SBC switches to SBC Restart Mode.

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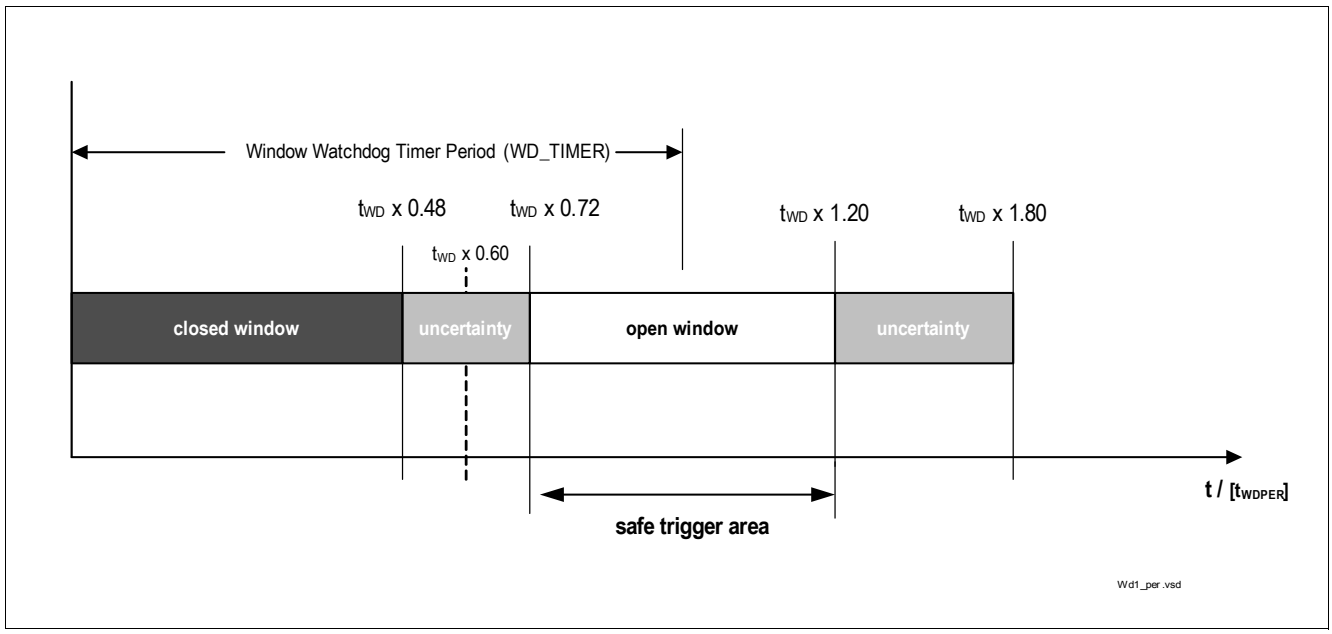


Figure 32 Window Watchdog Definitions

15.2.2 Watchdog Settings

The settings of the watchdog can be changed during the operation of the watchdog. The change is done with a SPI programming into the Watchdog Configuration Bits. The new setting is programmed together with a valid watchdog trigger according to the old settings. The timer with the new settings starts with this SPI command.

The following watchdog settings are available

- WD Setting 1: 10ms
- WD Setting 2: 20ms
- WD Setting 3: 50ms
- WD Setting 4: 100ms
- WD Setting 5: 200ms
- WD Setting 6: 500ms
- WD Setting 7: 1000ms

*Note: After a watchdog trigger failure, the **WD_FAIL** counter is increased. This counter is cleared automatically after a successful watchdog trigger or when entering SBC Software Development Mode. SBC Fail-Safe Mode is entered after 15 sequential watchdog fails.*

15.2.3 Watchdog during SBC Stop Mode

In SBC Stop Mode the watchdog can be disabled. There are 2 options that can be selected via SPI.

- Watchdog is OFF in SBC Stop Mode (**WD_STM_ EN_0** = 1, **WD_STM_ EN_1** = 1)
- Watchdog is OFF if I_{VCC1} < I_{WD_OFF} (**WD_STM_ EN_0** = 0 and/or **WD_STM_ EN_1** = 0)

For WD_STM_EN_x = 0, the watchdog will automatically start if I_{VCC1} > I_{WD_OFF}. In this case, the watchdog will start again with a long open window. Should the current decrease again below the I_{WD_OFF} threshold, then the watchdog is again disabled.

In case the watchdog is enabled in SBC Stop Mode, then the watchdog settings can't be changed. A trial to do this will result the diagnosis bit **SPI_FAIL** to be set. It would also enable the watchdog again in case the watchdog was enabled.

For safety reasons, there is a special sequence to be followed in order to disable the watchdog. If this sequence is not ensured then also the bit **WD_STM_ EN_1** will be cleared and the sequence has to be started again.

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This is shown in **Figure 33**. As soon as the SBC is set to SBC Normal Mode, then the bits WD_STM_EN_1 and WD_STM_ EN_0 are cleared and this sequence must be followed again to switch off the watchdog. Returning to SBC Normal Mode and/or triggering the watchdog in SBC Stop Mode will also enable the watchdog again, which will start with a long open window.

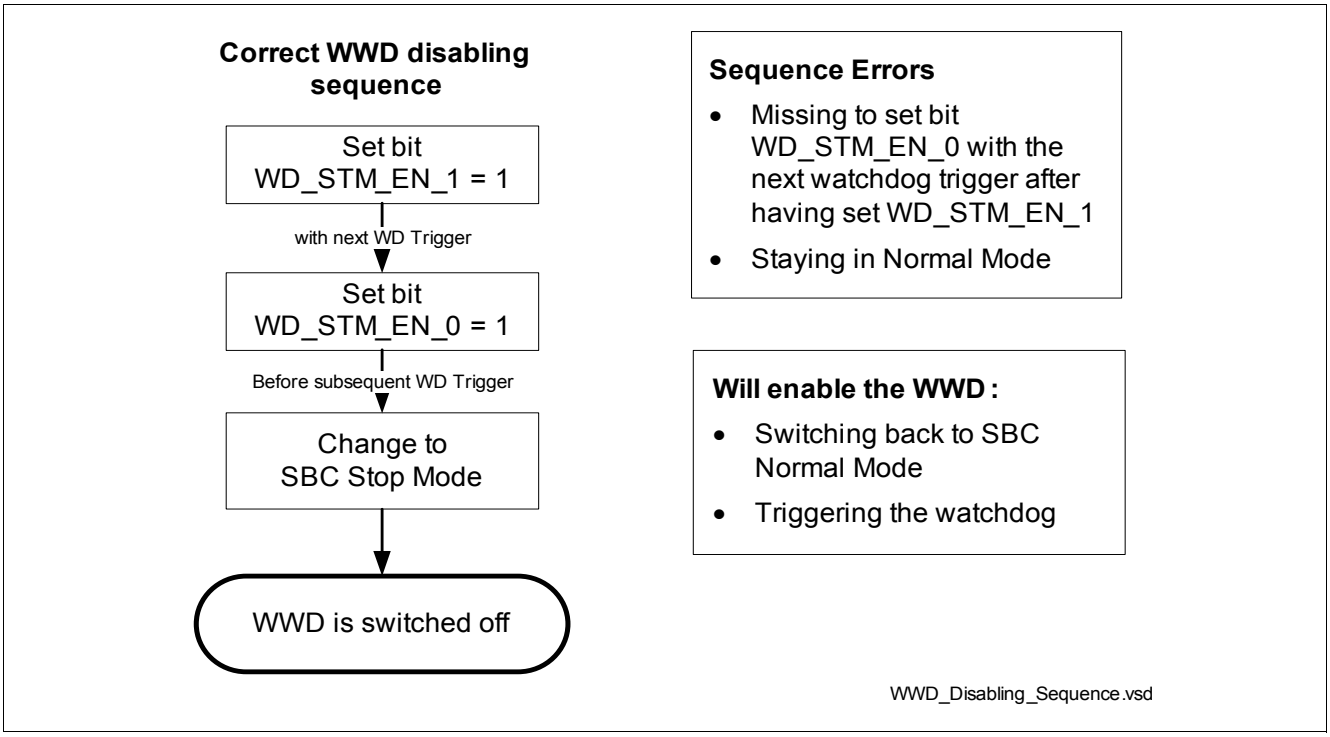


Figure 33 Window Watchdog Disabling Sequence

15.2.4 Watchdog Start in SBC Stop Mode due to Bus Wake

In SBC Stop Mode the watchdog can be disabled. In addition a feature is available which will start the watchdog with any BUS wake during SBC Stop Mode. The feature is enabled by setting the bit **WD_EN_ WK_BUS** = 1 (= default value after POR). The bit can only be changed in SBC Normal Mode and needs to be programmed before entering SBC Stop Mode and it is not reset by the SBC. The sequence described in **Figure 34** needs to be followed to disable the WD.

With the function enabled the watchdog will start again with any wake on CAN or LIN. The wake on CAN and LIN will generate an interrupt and the RxD pin for LIN or CAN is pulled to LOW. With that microcontroller is informed that the watchdog is started independently if the VCC1 load current is below the I_{WD_OFF} threshold or not. The watchdog starts with a long open window. The watchdog can be triggered in SBC Stop Mode or the SBC can be switched to SBC Normal Mode. To disable the watchdog again, the SBC needs to be switched to SBC Normal Mode and the sequence needs to be sent again.

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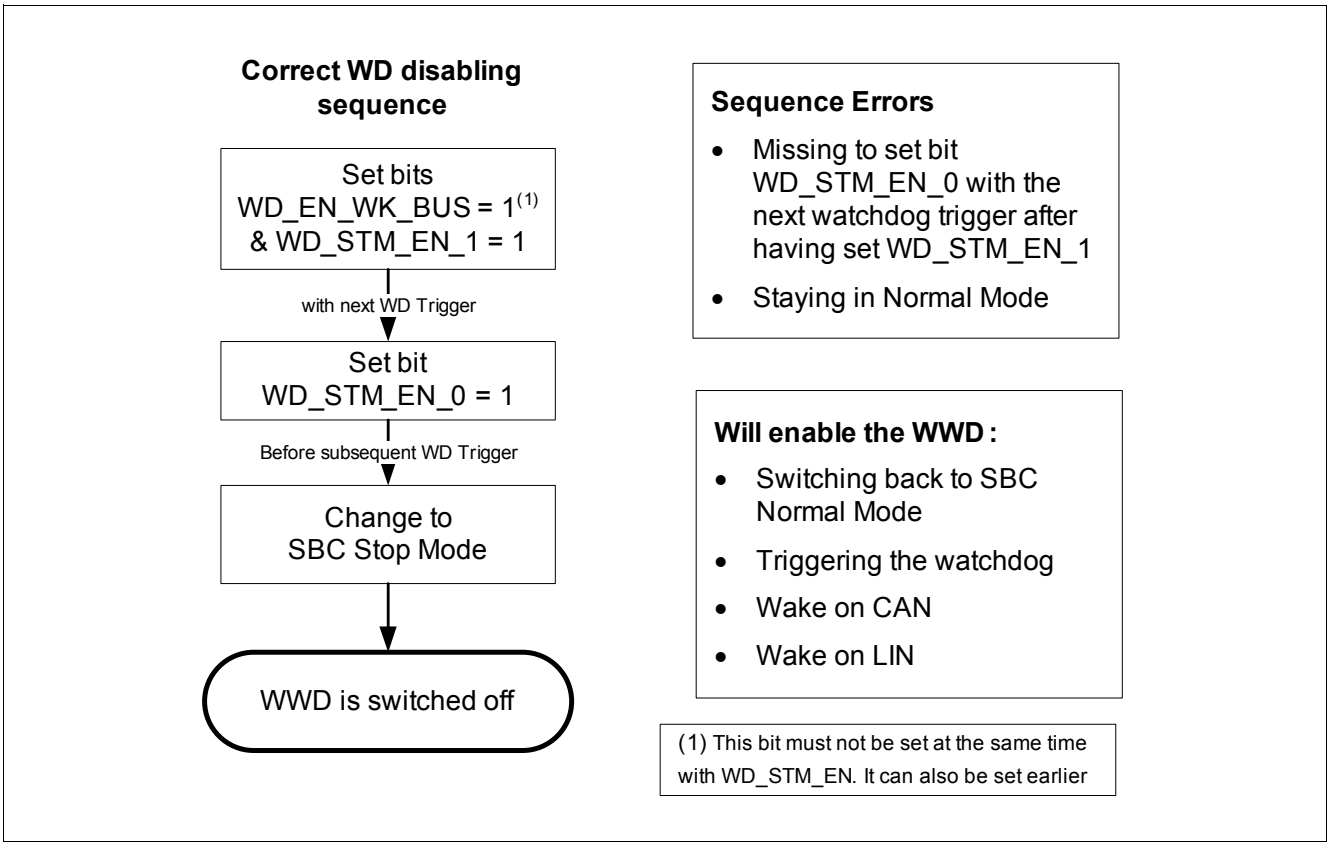


Figure 34 Watchdog Disabling Sequence (with wake via BUS)

15.3 VS Power-On Reset

The VS power-on reset ($V_{POR,f}$) will generate an internal reset to the device. It can be detected via SPI. In case VS < $V_{POR,f}$, the SBC is switched OFF and will restart in INIT mode at the next VS rising.

15.4 Under Voltage VS

If the supply voltage VS reaches the under voltage threshold ($V_{UVD,f}$) the SBC preforms the following measures:

- HS1...6 are switched off depending on the SPI setting (only if SPI bit **HS_UV _SD_EN** is set to ‘0’)
- LIN is switched to high impedance (CAN is not disabled)
- LS1 and LS2 are switched off depending on the SPI setting (only if SPI bit **LS_UV _SD_EN** is set to ‘0’)
- SPI bit **VS_UV** is set and can be READ/cleared via SPI, no other error bits are set

In case the drivers are switched off, the respective SPI bits are cleared and must be turned on again by setting the respective SPI bits. It is recommended to CLEAR the **VS_UV** bit but it is not required to enable the switches again.

*Note: In case the SPI bits **LS_OV_UV _REC** and **HS_OV_UV _REC** are set to ‘1’, the output drivers (LSx, and HSx) resume the previous state once the VS under-voltage condition is removed.*

Note: There is no VS Monitoring available in SBC Stop Mode - due to current consumption saving requirements. However, VS_UV monitoring is enabled as soon as one peripheral (e.g. HS, LIN, CAN, VCC2) is turned on.

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15.5 Over Voltage VS

If the supply voltage VS reaches the over voltage threshold ($V_{OVD,r}$) the SBC does the following measures:

- HS1...6 are switched off depending on the SPI setting (only if SPI bit **HS_OV _SD_EN** is set to '0')
- LS1 and LS2 are switched off depending on the SPI setting (only if SPI bit **LS_OV_UV _REC** is set to '0')
- SPI bit **VS_OV** is set and can be READ/cleared via SPI

In case the drivers are switched off, the respective SPI bits are cleared and must be turned on again by setting the respective SPI bits. It is recommended to CLEAR the **VS_OV** bit but it is not required to enable the switches again.

*Note: In case the SPI bit **LS_OV_UV _REC** is set to '1', the output drivers (HSx, and LSx) resume the previous state once the VS Over-Voltage condition is removed.*

Note: There is no VS Monitoring available in SBC Stop Mode - due to current consumption saving requirements. However, VS_UV monitoring is enabled as soon as one peripheral (e.g. HS, LIN, CAN, VCC2) is turned on.

15.6 VCC1 Under Voltage

As described in **Chapter 15.1**, when the V_{CC1} output voltage reaches the under voltage threshold (V_{RTx}), a reset will be triggered (RO pulled 'LOW') and the SBC will enter SBC Restart Mode.

*Note: The **VCC1_UV** bit is not set in SBC Sleep Mode as VCC1 is switched off in this case.*

15.7 VCC1 Fail & Short Circuit

There are two additional protection features implemented for V_{CC1}:

- Short Circuit detection: If V_{CC1} is not above the $V_{CC1,SC}$ within $t_{VCC1,SC}$ after turning on V_{CC1} or falls below $V_{CC1,SC}$ for more than $t_{VCC1,SC}$, then the SPI bit **VCC1_SC** bit is set. V_{CC1} is turned off and SBC Fail-Safe Mode is entered. The SBC can be activated again via wake on CAN, LIN, WK1-3
- VCC1 failure: In case VCC1 will drop below the threshold $V_{CC1,fail}$ for t > $t_{VCC1,fail}$, the SPI bit **VCC1_FAIL** is set and can be only cleared via SPI
- The thresholds of $V_{CC1,SC}$ and $V_{CC1,fail}$ are identical

*Note: Neither the **VCC1_SC** nor the **VCC1_FAIL** flag is set during power up of VCC1, i.e. it is blanked out.*

15.8 VCC2 Fail & Short Circuit

- Short Circuit detection: in case VCC2 is not above $V_{CC2,SC}$ within $t_{VCC2,SC}$ after turning on VCC2 or falls below $V_{CC2,SC}$ for more than $t_{VCC2,SC}$, then the SPI bit **VCC2_SC _OT** bit is set, and VCC2 is turned off. The filter time (=blanking time) also applies when VCC2 is switched on. VCC2 can be activated again via SPI. It is not necessary to CLEAR the SPI failure bit but it is recommended.
- VCC2 failure: In case VCC2 will drop below the $V_{CC2,fail}$ threshold for t > $t_{VCC2,fail}$, then the SPI bit **VCC2_FAIL** is set and can be only cleared via SPI
- The threshold of $V_{CC2,SC}$ and $V_{CC2,fail}$ are identical

*Note: Neither **VCC2_SC _OT** nor **VCC2_FAIL** flag is set during turn-on or turn-off up of V_{CC2}.*

*Note: If VCC2 is enabled during SBC Sleep Mode and the voltage will decrease below the $V_{CC2,fail}$ threshold, then the **VCC2_FAIL** bit will be set.*

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15.9 Thermal Protection

The thermal protection mechanism is designed in a way that VCC1 will stay active as long as possible in case of high temperature. Following thermal protection features are available and signaled via SPI:

- Thermal Pre warning: Only the SPI bit **TPW** is set when the threshold T_{jPW} is reached. No other actions are taken.
- Over temperature Protection:
  - Over temperature shut down with 2 levels of priority (TSD1 and TSD2).
  - If one output stage or driver (HS1...HS6, LS1...2, LIN, CAN, VCC2) reaches the TSD1 temperature threshold T_{jTSD1}, then it is switched off individually as a first-level protection measure, the respective control bits are reset, the **TSD1** bit and the respective OC_OT bit is set. The other output stages are not affected if their TSD1 threshold is not exceeded.
    Once the OT condition is not present anymore, the respective peripherals are not automatically enabled (except for CAN & LIN - see below) but must be switched on by setting the respective SPI registers.
    It is not required to clear the TSD1 flag and the OC_OT flags (where applicable) to turn on the respective driver but it is recommended.
  - LIN and CAN transceivers: the drivers are automatically switched on again if the OT condition is not present anymore. The user should reset the BUS_FAIL bits via SPI.
  - In case VCC1 reaches the T_{jTSD2} temperature threshold, then the SBC is switched off for 1s and the **TSD2** bit is set. Then the SBC Restart Mode is entered. If 7x TSD2 restarts occur within one minute, then the device is sent to SBC Fail-Safe Mode with the default wake sources LIN, CAN, WK1...WK3 are enabled. The time is counted starting from the first TSD2 event. If the minute passed and less than 7 TSD2 events occurred, then the first event is discarded and the minute is considered to be counted from the second event and so on.
  - Once the respective bits (TPW, TSD1, TSD2) are set, they can be cleared via SPI if the condition is not present anymore.

Note: In case of an TSD1 event for one high-side switch or for one low-side switch, then all high-sides or low-sides are switched off respectively and the OT bits are set for all high-side or low-side switches.

Note: Once a TSD2 event it detected and he SBC is switched off for 1s, then also the Reset Output is pulled LOW to bring the SBC into a defined state.

Note: If the TSD2 counter is different than '000' when entering SBC Stop Mode or SBC Sleep Mode, then there will be a period of not more than one minute (depending when the last TSD2 event occurred) of higher current consumption before the specified low-power current consumption is resumed.

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15.10 Electrical Characteristics

Table 24 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
VCC1 Monitoring, Reset Generator; Pin RO							
Reset Threshold Voltage RT1,f	$V_{RT1,f}$	4.45	4.60	4.70	V	default setting; VCC1 falling	P_15.10.1
Reset Threshold Voltage Stop RT1,f	$V_{RT1ST,f}$	4.40	4.60	4.75	V	default setting; SBC Stop Mode; VCC1 falling	P_15.10.40
Reset Threshold Voltage RT2,f	$V_{RT2,f}$	4.05	4.20	4.30	V	SPI option; VCC1 falling	P_15.10.3
Reset Threshold Voltage Stop RT2,f	$V_{RT2ST,f}$	4.00	4.20	4.35	V	SPI option; SBC Stop Mode; VCC1 falling	P_15.10.42
Reset Threshold Voltage RT3,f	$V_{RT3,f}$	3.65	3.80	3.90	V	SPI option; VS ≥ 4V; VCC1 falling	P_15.10.5
Reset Threshold Voltage Stop RT3,f	$V_{RT3ST,f}$	3.60	3.80	3.95	V	SPI option; SBC Stop Mode; VS ≥ 4V; VCC1 falling	P_15.10.44
Reset Threshold Voltage RT4,f	$V_{RT4,f}$	3.15	3.40	3.50	V	SPI option; VS ≥ 4V; VCC1 falling	P_15.10.7
Reset Threshold Voltage Stop RT4,f	$V_{R0T4ST,f}$	3.10	3.40	3.55	V	SPI option; SBC Stop Mode; VS ≥ 4V; VCC1 falling	P_15.10.46
Reset Threshold Hysteresis	$V_{RT,hys}$	20	100	200	mV	SBC Normal Mode	P_15.10.9
VCC1 Short to GND Threshold Voltage	$V_{CC1,SC}$	–	–	2	V	–	P_15.10.10
VCC1 Short to GND Filter Time	$t_{VCC1,SC}$	–	4		ms	2)	P_15.10.11
VCC1 Fail Threshold Voltage	$V_{CC1,fail}$	–	–	2	V	–	P_15.10.12
VCC1 Fail Filter Time	$t_{VCC1,fail}$	–	2	–	µs	3)	P_15.10.13
Reset LOW Output Voltage	$V_{RO,L}$	–	0.2	0.4	V	I_{RO} = 1 mA for V_{CC1} ≥ 1 V	P_15.10.14
Reset HIGH Output Voltage	$V_{RO,H}$	0.8 x V_{CC1}	–	V_{CC1} + 0.3 V	V	I_{RO} = -20µA	P_15.10.15
Reset Pull-up Resistor	R_{RO}	10	20	40	kΩ	V_{RO} = 0 V	P_15.10.16

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Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Reset Filter Time	t_{RF}	4	10	26	µs	2)VCC1 < VRT1x to RO = L	P_15.10.17
Reset Delay Time	t_{RD1}	1.5	2	2.5	ms	1) 2)	P_15.10.18
VCC2 Monitoring							
VCC2 Short to GND Threshold Voltage	$V_{CC2,SC}$	–	–	2	V	–	P_15.10.19
VCC2 Short to GND Filter Time	$t_{VCC2,SC}$	–	4		ms	2)	P_15.10.20
VCC2 Fail Threshold Voltage	$V_{CC2,fail}$	–	–	2	V	–	P_15.10.21
VCC2 Fail Filter Time	$t_{VCC2,fail}$	–	2	–	µs	3)	P_15.10.22
Watchdog Generator							
Long Open Window	t_{LW}	–	200	–	ms	2)	P_15.10.23
Switch-Off current for WD in Stop Mode	I_{WD_OFF}	0.80		5	mA	–	P_15.10.24
Internal Oscillator	f_{CLKSBC}	0.8	1.0	1.2	MHz	–	P_15.10.25
Power-On Reset, Over / Under Voltage Protection							
VS power-on reset rising	$V_{POR,r}$	–		4.5	V	Vs increasing	P_15.10.26
VS power-on reset falling	$V_{POR,f}$	–		4V	V	Vs decreasing	P_15.10.27
VS Over Voltage Detection threshold	$V_{OVD,r}$	19.5		22	V	rising	P_15.10.28
VS Under Voltage Detection threshold	$V_{UVD,f}$	4.8		5.5	V	falling	P_15.10.29
TEST							
TEST HIGH-input voltage threshold	$V_{TEST,H}$	–	–	0.7 x V_{CC1}	V	–	P_15.10.30
TEST LOW-input voltage threshold	$V_{TEST,L}$	0.3 x V_{CC1}	–	–	V	–	P_15.10.31
Hysteresis of TEST input voltage	$V_{TEST,Hys}$	–	0.12 x V_{CC1}	–	V	3)	P_15.10.32
Pull-down Resistance at pin TEST	R_{TEST}	2.5	5	10	kΩ	V_{TEST} = 0.2 x V_{CC1}	P_15.10.33
TEST Input Filter Time	t_{RF}	–	64	–	µs	2)	P_15.10.34

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Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Over Temperature Shutdown[3]							
Thermal Pre-warning ON Temperature	T_{jPW}	125	145	165	°C	3)	P_15.10.35
Thermal Shutdown TSD1	T_{jTSD1}	165	185	200	°C	3)	P_15.10.36
Thermal Shutdown TSD2	T_{jTSD2}	165	185	200	°C	3)	P_15.10.37
Deactivation time after thermal shutdown TSD2	t_{TSD2}	–	1	–	s	2)	P_15.10.38

1) The reset delay time will start when VCC1 crosses above the selected Vrtx threshold

2) Not subject to production test, tolerance defined by internal oscillator tolerance.

3) Not subject to production test; specified by design.

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16 Serial Peripheral Interface

16.1 SPI Description

The 16-bit wide Control Input Word is read via the data input SDI, which is synchronized with the clock input CLK provided by the microcontroller. The output word appears synchronously at the data output SDO (see **Figure 35**).

The transmission cycle begins when the chip is selected by the input CSN (Chip Select Not), LOW active. After the CSN input returns from LOW to HIGH, the word that has been read is interpreted according to the content. The SDO output switches to tri-state status (HIGH impedance) at this point, thereby releasing the SDO bus for other use.

The state of SDI is shifted into the input register with every falling edge on CLK. The state of SDO is shifted out of the output register after every rising edge on CLK. The SPI of the SBC is not daisy chain capable.

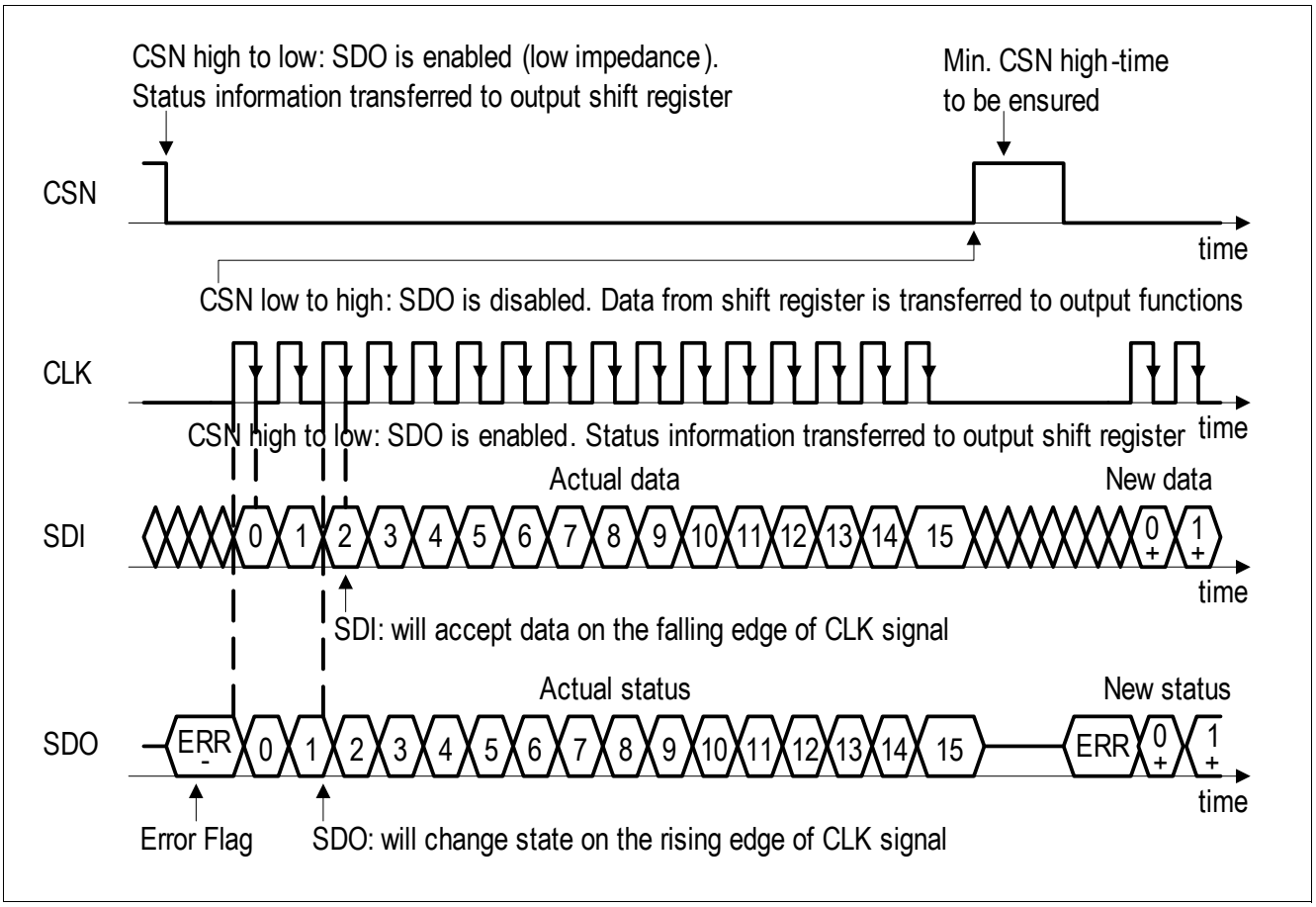


Figure 35 SPI Data Transfer Timing (note the reversed order of LSB and MSB shown in this figure compared to the register description)

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16.2 Failure Signalization in the SPI Data Output

When the microcontroller sends a wrong SPI command, then the SBC ignores the information. In case of invalid SPI commands the diagnosis bit 'SPI_FAIL' is set and the complete SPI WRITE command is ignored (no partial interpretation). The bit can be only reset by actively clearing this bit via SPI command.

Invalid SPI commands leading to the SPI_FAIL bit being set are listed below:

- Illegal state transitions:
  - Going from SBC Stop- to SBC Sleep Mode. In this case the SBC enters in addition the SBC Restart Mode;
  - Attempt to go directly from SBC Init Mode to SBC Stop- or Sleep Mode with the first SPI command. SBC Normal mode will be entered instead;
- Attempting to change the watchdog settings, PWM settings and HS/LS configuration settings or to WRITE to any other control registers during SBC Stop Mode;
  only WD triggering, returning to SBC Normal Mode, and READ & CLEAR commands are valid SPI commands in SBC Stop Mode.
- Attempt to go to SBC Sleep Mode when no wake sources are set (i.e.all bits in the BUS_CTRL and WK_CTRL_2 registers are cleared). In this case the SPI_FAIL bit is set and the SBC enters SBC Restart Mode.
  Note: At least one wake source must be activated in order to avoid a deadlock situation in SBC Sleep Mode, i.e. the SBC would not be able to wake up anymore. No signalization or failure handling is done for the attempt to go to SBC Stop Mode when all bits in the registers BUS_CTRL and WK_CTRL_2 are cleared because the microcontroller can leave this mode via SPI.
- When trying to enter SBC Sleep Mode: if the only wake source is cyclic sense with a timer and this timer is OFF, then the SBC will immediately enter Restart Mode
- Attempt to enter SBC Sleep Mode if WK_MEAS is set to '1' and WK1_EN or WK2_EN are set as the only wake sources. Also in this case the SPI_FAIL bit is set and the SBC enters SBC Restart Mode.
- Trying to turn on LS1..2 during a long open window.
- Setting a longer or equal on-time than the timer period of the respective timer.
- Enabling WK4 as a wake source when SYNC is selected.
- Trying to select SYNC for the on- or off time of TIMER1...2 while WK4_SYNC = '0' will generate a SPI_FAIL and the SPI WRITE command is ignored.

Signalization of the ERR flag (high active) in the SPI data output (see Figure 35):

In addition, the number of received input clocks is supervised to be 0- or 16 clock cycles and the Input / Control Word is discarded in case of a mismatch. The error logic also recognizes if CLK was HIGH during CSN edges. Both errors - 0 bit and 16 bit CLK mismatch or CLK HIGH during CSN edges - are flagged in the following SPI output by a HIGH at the data output (SDO pin, bit ERR) before the first rising edge of the clock is received.

Note: After exiting SBC Fail-Safe Mode, the ERR Flag might not be set correctly due to the failure condition. In this case the flag should be ignored.

Note: It is possible to quickly check for the ERR flag without sending any data bits. i.e. only the CSN is pulled LOW and SDO is observed - no SPI Clocks are sent in this case

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16.3 SPI Programming

For the TLE9266-2QX, 7 bits are used for the address selection (BIT6...0). Bit 7 is used to decide between READ ONLY and READ & CLEAR for the status bits, and between WRITE and READ ONLY for configuration bits. For the actual configuration and status information, 8 data bits (BIT15...8) are used.

Writing, clearing and reading is done byte wise. The SPI status bits are not cleared automatically and must be cleared by the microcontroller, e.g. if the TSD2 was set due to over temperature. The configuration bits will be partially automatically cleared by the SBC - please refer to the individual register description for detailed information. During SBC Restart Mode the SPI communication is ignored by the SBC, i.e. it is not interpreted.

For the **status registers**, the requested information is given in the same SPI command in DO.
For the **control registers**, also the status of the respective bit is shown in the same SPI command, but if the setting is changed this is only shown with the next SPI command (it is only valid after CSN HIGH).

The Status Information is given with each SPI command e.g. watchdog trigger in the status information field. Each bit shows if there is a Status Information set to 1 in one of the Status Register bits. The register **WK_LVL_STAT** is not included in the status Information field. This is listed in **Table 25**.

For example if bit 0 in the Status Information field is set to 1, one or more bits of the register 100001 (**SUP_STAT**) is set to 1. Then this register needs to be read in a second SPI command. The bit in the Status register will be set to 0 when all bits in the register 100001 are set back to 0 (see also **Figure 36**)

Table 25 Status Information Field

Bit in Status Information Field	Corresponding Address Bit	Status Register Description
0	100 0001	SUP_STAT: Supply Status -VS fail, VCCx fail, POR
1	100 0010	THERM_STAT: Thermal Protection Status
2	100 0011	DEV_STAT: Device Status - Mode before wake, WD Fail, SPI Fail, Failure
3	100 0100	BUS_STAT: Bus Failure Status: CAN, LIN,
4	100 0110	WK_STAT: Wake Source Status
5	101 0010	LS_OC_OT_STAT: Low-Side Over Load Status
6	101 0100	HS_OC_OT_STAT: High-Side Over Load Status
7	101 0101	HS_OL_STAT: High-Side Open Load Status

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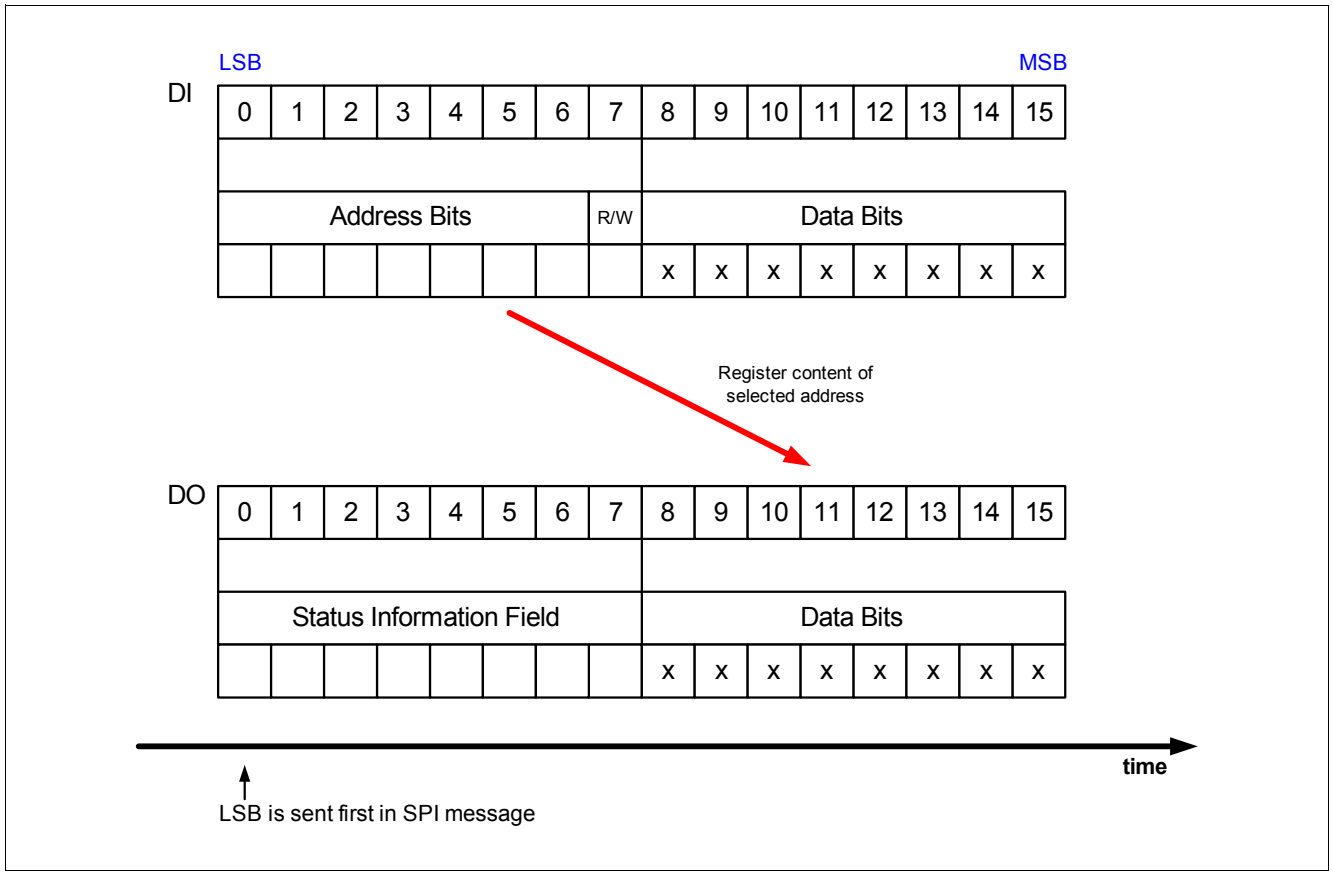


Figure 36 SPI Operation Mode (note the reversed order of LSB and MSB shown in this figure)

16.4 SPI Bit Mapping

, **Figure 37** show the mapping of the registers and , **Figure 38** show the SPI bits of the respective registers.

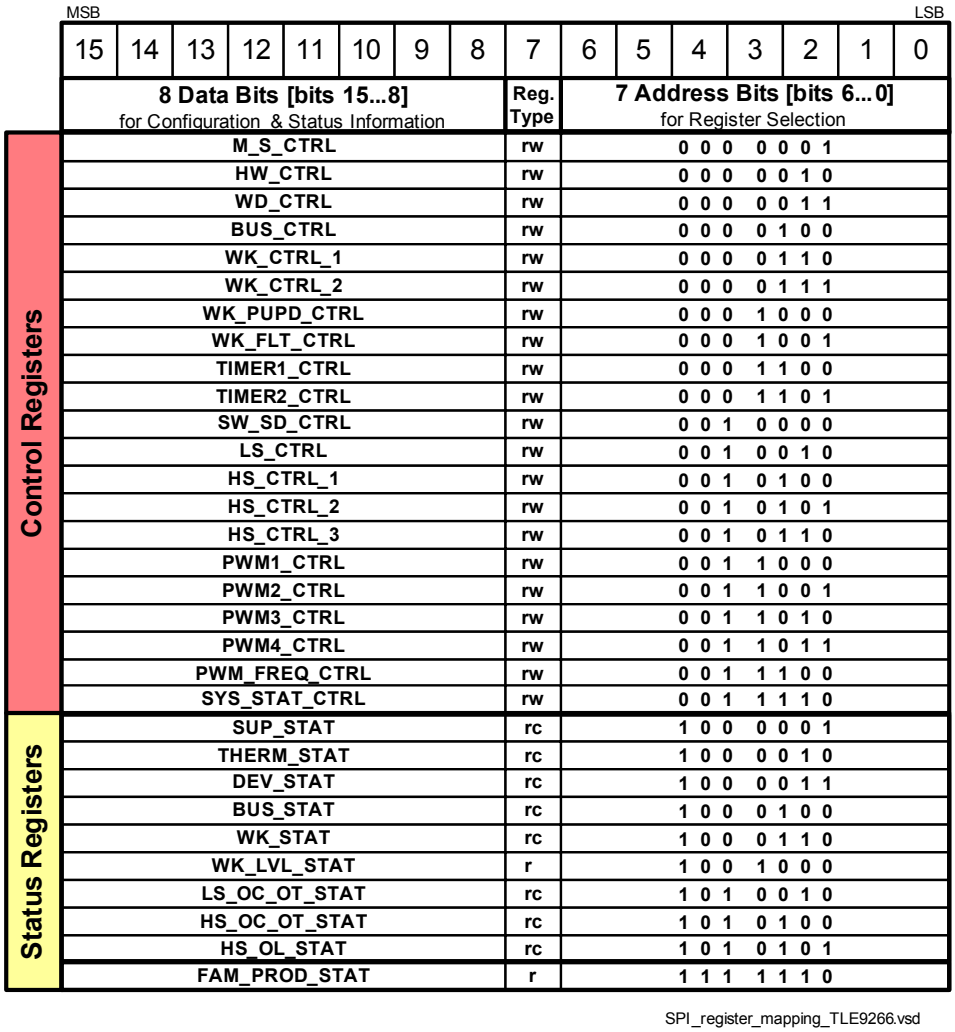
The **Control Registers** '000 0001' to '001 1110' are READ/WRITE Register. Depending on bit 7 the bits are only READ (setting bit 7 to '0') or also written (setting bit 7 to '1'). The new setting of the bit after WRITE can be seen with a new READ / WRITE command.

The registers '100 0001' to '111 1110' are **Status Registers** and can be read or read with clearing the bit (if possible) depending on bit 7. To CLEAR a Data Byte of one of the Status Registers bit 7 must be set to 1. The registers **WK_LVL_STAT**, **FAM_PROD_STAT**, are an exception as they show the actual voltage level at the respective WK pin (LOW/HIGH), or a fixed family/product ID respectively and can thus not be cleared.

When changing to a different SBC mode, certain configurations bits will be cleared automatically:

- The SBC mode bits are updated to the actual status, e.g. when returning to SBC Normal Mode
- When changing to a low-power mode (Stop/Sleep), the diagnosis bits of the switches and transceivers are not cleared.
- The LSx outputs will be switched off when going from SBC Normal to SBC Sleep- or SBC Stop Mode and will not turn on automatically when going back to SBC Normal Mode. The same applies when going into SBC Fail-Safe Mode or SBC Restart Mode.
- HSx will stay on when going to SBC Sleep-/Stop Mode (configuration can only be done in SBC Normal Mode). Diagnosis is active (OC, OL, OT). In case of a failure the switch is turned off and no wake-up is issued
- The configuration bits for HSx and VCC2 are cleared in SBC Restart Mode

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	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
	8 Data Bits [bits 15...8] for Configuration & Status Information								**Reg. Type**	**7 Address Bits [bits 6...0]** for Register Selection						
Control Registers	M_S_CTRL								rw	0	0	0	0	0	0	1
	HW_CTRL								rw	0	0	0	0	0	1	0
	WD_CTRL								rw	0	0	0	0	0	1	1
	BUS_CTRL								rw	0	0	0	0	1	0	0
	WK_CTRL_1								rw	0	0	0	0	1	1	0
	WK_CTRL_2								rw	0	0	0	0	1	1	1
	WK_PUPD_CTRL								rw	0	0	0	1	0	0	0
	WK_FLT_CTRL								rw	0	0	0	1	0	0	1
	TIMER1_CTRL								rw	0	0	0	1	1	0	0
	TIMER2_CTRL								rw	0	0	0	1	1	0	1
	SW_SD_CTRL								rw	0	0	1	0	0	0	0
	LS_CTRL								rw	0	0	1	0	0	1	0
	HS_CTRL_1								rw	0	0	1	0	1	0	0
	HS_CTRL_2								rw	0	0	1	0	1	0	1
	HS_CTRL_3								rw	0	0	1	0	1	1	0
	PWM1_CTRL								rw	0	0	1	1	0	0	0
	PWM2_CTRL								rw	0	0	1	1	0	0	1
	PWM3_CTRL								rw	0	0	1	1	0	1	0
	PWM4_CTRL								rw	0	0	1	1	0	1	1
	PWM_FREQ_CTRL								rw	0	0	1	1	1	0	0
	SYS_STAT_CTRL								rw	0	0	1	1	1	1	0
Status Registers	SUP_STAT								rc	1	0	0	0	0	0	1
	THERM_STAT								rc	1	0	0	0	0	1	0
	DEV_STAT								rc	1	0	0	0	0	1	1
	BUS_STAT								rc	1	0	0	0	1	0	0
	WK_STAT								rc	1	0	0	0	1	1	0
	WK_LVL_STAT								r	1	0	0	1	0	0	0
	LS_OC_OT_STAT								rc	1	0	1	0	0	1	0
	HS_OC_OT_STAT								rc	1	0	1	0	1	0	0
	HS_OL_STAT								rc	1	0	1	0	1	0	1
	FAM_PROD_STAT								r	1	1	1	1	1	1	0

Figure 37 TLE9266-2QX SPI Register Mapping

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Register Short Name	15	14	13	12	11	10	9	8	7	6...0
	Data Bit 15...8								Read-Only (1)	Address A6...A0
	D7	D6	D5	D4	D3	D2	D1	D0		
CONTROL REGISTERS										
M_S_CTRL	MODE_1	MODE_0	reserved	VCC2_ON_1	VCC2_ON_0	reserved	VCC1_RT_1	VCC1_RT_0	read/write	0000001
HW_CTRL	reserved	reserved	FO_ON	reserved	reserved	reserved	reserved	reserved	read/write	0000010
WD_CTRL	reserved	WD_STM_EN_0	reserved	WD_EN_WK_BUS	reserved	WD_TIMER_2	WD_TIMER_1	WD_TIMER_0	read/write	0000011
BUS_CTRL	LIN_FLASH	LIN_LSM	LIN_TXD_TO	LIN_1	LIN_0	reserved	CAN_1	CAN_0	read/write	0000100
WK_CTRL_1	TIMER2_WK_EN	TIMER1_WK_EN	reserved	reserved	WD_STM_WK_EN	WD_STM_EN_1	reserved	reserved	read/write	0000110
WK_CTRL_2	reserved	reserved	WK_MEAS	WK4_SYNC	WK4_EN	WK3_EN	WK2_EN	WK1_EN	read/write	0000111
WK_PUPD_CTRL	WK4_PUPD_1	WK4_PUPD_0	WK3_PUPD_1	WK3_PUPD_0	WK2_PUPD_1	WK2_PUPD_0	WK1_PUPD_1	WK1_PUPD_0	read/write	0001000
WK_FLT_CTRL	WK4_FLT_1	WK4_FLT_0	WK3_FLT_1	WK3_FLT_0	WK2_FLT_1	WK2_FLT_0	WK1_FLT_1	WK1_FLT_0	read/write	0001001
TIMER1_CTRL	reserved	TIMER1_ON_2	TIMER1_ON_1	TIMER1_ON_0	reserved	TIMER1_PER_2	TIMER1_PER_1	TIMER1_PER_0	read/write	0001100
TIMER2_CTRL	reserved	TIMER2_ON_2	TIMER2_ON_1	TIMER2_ON_0	reserved	TIMER2_PER_2	TIMER2_PER_1	TIMER2_PER_0	read/write	0001101
SW_SD_CTRL	reserved	HS_OV_SD_EN	HS_UV_SD_EN	HS_OV_UV_REC	reserved	LS_OV_SD_EN	LS_UV_SD_EN	LS_OV_UV_REC	read/write	0010000
LS_CTRL	reserved	reserved	reserved	reserved	reserved	reserved	LS2	LS1	read/write	0010010
HS_CTRL_1	HS2_SEL	HS2_2	HS2_1	HS2_0	HS1_SEL	HS1_2	HS1_1	HS1_0	read/write	0010100
HS_CTRL_2	reserved	HS4_2	HS4_1	HS4_0	reserved	HS3_2	HS3_1	HS3_0	read/write	0010101
HS_CTRL_3	reserved	HS6_2	HS6_1	HS6_0	reserved	HS5_2	HS5_1	HS5_0	read/write	0010110
PWM1_CTRL	PWM1_DC_7	PWM1_DC_6	PWM1_DC_5	PWM1_DC_4	PWM1_DC_3	PWM1_DC_2	PWM1_DC_1	PWM1_DC_0	read/write	0011000
PWM2_CTRL	PWM2_DC_7	PWM2_DC_6	PWM2_DC_5	PWM2_DC_4	PWM2_DC_3	PWM2_DC_2	PWM2_DC_1	PWM2_DC_0	read/write	0011001
PWM3_CTRL	PWM3_DC_7	PWM3_DC_6	PWM3_DC_5	PWM3_DC_4	PWM3_DC_3	PWM3_DC_2	PWM3_DC_1	PWM3_DC_0	read/write	0011010
PWM4_CTRL	PWM4_DC_7	PWM4_DC_6	PWM4_DC_5	PWM4_DC_4	PWM4_DC_3	PWM4_DC_2	PWM4_DC_1	PWM4_DC_0	read/write	0011011
PWM_FREQ_CTRL	reserved	PWM4_FREQ_0	reserved	PWM3_FREQ_0	reserved	PWM2_FREQ_0	reserved	PWM1_FREQ_0	read/write	0011100
SYS_STAT_CTRL	SYS_STAT_7	SYS_STAT_6	SYS_STAT_5	SYS_STAT_4	SYS_STAT_3	SYS_STAT_2	SYS_STAT_1	SYS_STAT_0	read/write	0011110
STATUS REGISTERS										
SUP_STAT	POR	VS_UV	VS_OV	VCC2_SC_OT	VCC2_FAIL	VCC1_SC	VCC1_FAIL	VCC1_UV	read/clear	1000001
THERM_STAT	reserved	reserved	reserved	TSD2_2	TSD2_1	TSD2_0	TSD1	TPW	read/clear	1000010
DEV_STAT	DEV_ST_1	DEV_ST_0	WD_FAIL_3	WD_FAIL_2	WD_FAIL_1	WD_FAIL_0	SPI_FAIL	FAILURE	read/clear	1000011
BUS_STAT	reserved	LIN_FAIL_1	LIN_FAIL_0	reserved	reserved	CAN_FAIL_1	CAN_FAIL_0	VCAN_UV	read/clear	1000100
WK_STAT	WD_STM_WU	LIN_WU	CAN_WU	TIMER_WU	WK4_WU	WK3_WU	WK2_WU	WK1_WU	read/clear	1000110
WK_LVL_STAT	TEST_LVL		reserved	reserved	WK4_LVL	WK3_LVL	WK2_LVL	WK1_LVL	read	1001000
LS_OC_OT_STAT	reserved	reserved	reserved	reserved	reserved	reserved	LS2_OC_OT	LS1_OC_OT	read/clear	1010010
HS_OC_OT_STAT	reserved	reserved	HS6_OC_OT	HS5_OC_OT	HS4_OC_OT	HS3_OC_OT	HS2_OC_OT	HS1_OC_OT	read/clear	1010100
HS_OL_STAT	reserved	reserved	HS6_OL	HS5_OL	HS4_OL	HS3_OL	HS2_OL	HS1_OL	read/clear	1010101
FAMILY AND PRODUCT REGISTERS										
FAM_PROD_STAT	FAM_3	FAM_2	FAM_1	FAM_0	PROD_3	PROD_2	PROD_1	PROD_0	read	1111110

Figure 38 TLE9266 SPI Bit Mapping

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16.5 SPI Control Registers

READ-/WRITE Operation (see **Chapter 16.3**):

- The ‘POR / Soft Reset Value’ defines the register content after POR or SBC Reset.
- The ‘Restart Value’ defines the register content after SBC Restart Mode, where ‘x’ means the bit is unchanged.
- SPI control bits are in general not cleared or changed automatically. This must be done by the microcontroller via SPI. programming. Exceptions to this behavior are stated at the respective register description and the respective bit type is marked with a ‘h’ meaning that the SBC is able to change the register content.
- Reading a register is done byte wise by setting the SPI bit 7 to “0” (= READ ONLY).
- Writing to a register is done byte wise by setting the SPI bit 7 to “1”.

16.5.1 General Control Registers

M_S_CTRL
Mode- and Supply Control (Address 000 0001_B)
POR / Soft Reset Value: 0000 0000_B; Restart Value: 0000 $00xx_B$

7	6	5	4	3	2	1	0
MODE_1	**MODE_0**	**reserved**	**VCC2_ON_1**	**VCC2_ON_0**	**reserved**	**VCC1_RT_1**	**VCC1_RT_0**
rwh	rwh	r	rwh	rwh	r	rw	rw

Field	Bits	Type	Description
MODE	7:6	rwh	**SBC Mode Control** 00_B SBC Normal Mode (default value) 01_B SBC Sleep Mode 10_B SBC Stop Mode 11_B SBC Reset: Soft Reset is executed (RO is not triggered)
Reserved	5	r	**Reserved, always reads as 0**
VCC2_ON	4:3	rwh	**VCC2 Mode Control** 00_B VCC2 OFF 01_B VCC2 ON in Normal Mode 10_B VCC2 ON in Normal and Stop Mode 11_B VCC2 always ON (incl. Sleep Mode)
Reserved	2	r	**Reserved, always reads as 0**
VCC1_RT	1:0	rw	**VCC1 Reset Threshold Control** 00_B Vrt1 selected (highest threshold - default value) 01_B Vrt2 selected 10_B Vrt3 selected 11_B Vrt4 selected

Note: Trying to enter SBC Sleep Mode without any of the wake sources enabled will result in entering SBC Restart Mode and triggering a Reset.

Note: After entering SBC Restart Mode, the MODE bits will be automatically set to SBC Normal Mode. The VCC2_ON bits will be automatically set to OFF after entering SBC Restart Mode and after OC/OT.

Note: It is not possible to change from Stop to Sleep Mode via SPI Command. See also the State Machine Chapter

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HW_CTRL
Mode- and Supply Control (Address 000 0010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 0000$_B$

7	6	5	4	3	2	1	0
reserved	reserved	FO_ON	reserved	reserved	reserved	reserved	reserved
r	r	rwh	r	r	r	r	r

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
FO_ON	5	rwh	**Failure Output activation** 0_B FO not activated by software, FO can be activated by defined failures 1_B FO activated by software (via SPI)
Reserved	4:0	r	**Reserved, always reads as 0**

*Note: The bit is cleared by the SBC after SBC Restart Mode. Clearing the bit via SPI or via SBC Restart Mode will not disable the FO output, if the failure condition is still present. See also **Chapter 14** for FO activation and deactivation.*

WD_CTRL
Window Watchdog Control (Address 000 0011$_B$)
POR / Soft Reset Value: 0001 0000$_B$; Restart Value: 000x 0xxx$_B$

7	6	5	4	3	2	1	0
reserved	WD_STM_EN_0	reserved	WD_EN_WK_BUS	reserved	WD_TIMER_2	WD_TIMER_1	WD_TIMER_0
r	rwh	r	rw	r	rw	rw	rw

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
WD_STM_EN_0	6	rwh	**Watchdog activation during Stop Mode** 0_B Watchdog is active in Stop Mode as long as Ivcc1 > Iwd_Off 1_B Watchdog is deactivated in SBC Stop Mode
Reserved	5	r	**Reserved, always reads as 0**
WD_EN_WK_BUS	4	rwh	**Watchdog Enable after Bus (CAN/LIN) Wake in SBC Stop Mode** 0_B Watchdog will not start after a CAN/LIN wake 1_B Watchdog starts with a long open window after CAN/LIN wake
Reserved	3	r	**Reserved, always reads as 0**

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Field	Bits	Type	Description
WD_TIMER	2:0	rw	**Window Watchdog Timer Period** 000_B 10ms (POR and Restart value) 001_B 20ms 010_B 50ms 011_B 100ms 100_B 200ms 101_B 500ms 110_B 1000ms 111_B reserved

*Note: The watchdog is only deactivated in SBC Stop Mode when following sequence is ensured: 1.) Set bit WD_STM_ EN_1 in the register WK_CTRL_1 to '1'; 2.) Set bit WD_STM_ EN_0 in the register WD_CTRL to '1' with the next watchdog trigger. If the sequence is not ensured or the watchdog is triggered when the WD is OFF, then the WD will not be stopped or will be enabled again respectively. When returning to SBC Normal Mode, the bits WD_STM_EN_x are cleared. See also **Chapter 15.2.3**.*

*Note: See **Chapter 15.2.4** for more information on the effect of the bit WD_EN_WK_BUS.*

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BUS_CTRL
Bus Control (Address 000 0100$_B$)
POR / Soft Reset Value: 0010 0000$_B$; Restart Value: xxxy y0yy$_B$

7	6	5	4	3	2	1	0
LIN_FLASH	**LIN_LSM**	**LIN_TXD_TO**	**LIN_1**	**LIN_0**	**reserved**	**CAN_1**	**CAN_0**
rw	rw	rw	rwh	rwh	r	rwh	rwh

Field	Bits	Type	Description
LIN_FLASH	7	rw	**LIN Flash Programming Mode** 0_B Slope control mechanism active 1_B Deactivation of slope control for baud rates up to 115kBaud
LIN_LSM	6	rw	**LIN Low-Slope Mode Selection** 0_B LIN Normal-Mode is activated 1_B LIN Low-Slope Mode (10.4kBaud) activated
LIN_TXD_TO	5	rw	**LIN TxD Time-Out Control** 0_B TxD Time-Out feature disabled 1_B TXD Time-Out feature enabled (default value)
LIN	4:3	rwh	**LIN-Module Mode** 00_B LIN OFF 01_B LIN is wake capable 10_B LIN Receive Only Mode 11_B LIN Normal Mode
Reserved	2	r	**Reserved, always reads as 0**
CAN	1:0	rwh	**HS-CAN Module Modes** 00_B CAN OFF 01_B CAN is wake capable 10_B CAN Receive Only Mode 11_B CAN Normal Mode

*Note: Changes in the bits **LIN_FLASH** and **LIN_LSM** will be effective immediately once CSN goes to '1'.'*

Note: The reset values for the LIN and CAN transceivers are marked with 'y' because they will vary depending on the cause of change - see below.

Note: In case either CAN or LIN transceivers are configured to '11' or '10' while going to SBC Sleep Mode, they will be automatically set to wake capable ('01'). If configured to '11' when going to SBC Stop Mode they will be automatically set to wake capable. The SPI bits will be changed to wake capable. If configured to '10' when going to SBC Stop Mode they will be stay in Receive Only Mode.
If they had been configured to wake capable or OFF then the mode will remain unchanged.The Receive Only Mode has to be selected by the user before entering SBC Stop Mode.

Note: Behavior after SBC Restart Mode: If the transceivers had been configured to Normal Mode, or Receive Only Mode, or wake capable then the mode will be changed to wake capable or respectively remain wake capable. If they had been OFF before SBC Restart Mode, then they will remain OFF.

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WK_CTRL_1
Internal Wake Input Control (Address 000 0110$_B$)
POR / Soft Reset Value: 0000 1000$_B$; Restart Value: xx00 x000$_B$

7	6	5	4	3	2	1	0
TIMER2_WK_EN	**TIMER1_WK_EN**	**reserved**	**reserved**	**WD_STM_WK_EN**	**WD_STM_EN_1**	**reserved**	**reserved**
rw	rw	r	r	rw	rwh	r	r

Field	Bits	Type	Description
TIMER2_WK_EN	7	rw	**Timer2 wake source control** 0_B Timer2 wake disabled 1_B Timer2 is enabled as a wake source
TIMER1_WK_EN	6	rw	**Timer1 wake source control** 0_B Timer1 wake disabled 1_B Timer1 is enabled as a wake source
Reserved	5:4	r	**Reserved, always reads as 0**
WD_STM_WK_EN	3	rw	**Watchdog activation Interrupt in Stop Mode** 0_B Watchdog wake via INT in SBC Stop Mode disabled 1_B Watchdog wake via INT in Stop Mode is enabled (default value)
WD_STM_EN_1	2	rwh	**Watchdog activation during SBC Stop Mode** 0_B Watchdog is active in Stop Mode as long as Ivcc1 > Iwd_Off 1_B Watchdog is deactivated in SBC Stop Mode
Reserved	1:0	r	**Reserved, always reads as 0**

Note: The watchdog is only deactivated in SBC Stop Mode when following sequence is ensured: 1.) Set bit WD_STM_ EN_1 in the register WK_CTRL_1 to '1'; 2.) Set bit WD_STM_ EN_0 in the register WD_CTRL to '1' with the next watchdog trigger. If the sequence is not ensured or the watchdog is triggered when the WD is OFF, then the WD will not be stopped or will be enabled again respectively. When returning to SBC Normal Mode, the bits WD_STM_EN_x are cleared. See also Chapter 15.2.3.

*Note: Failure Handling Mechanism: When the device goes to SBC Fail-Safe Mode due to a failure (TSD2, WD-Failure,...), then the wake registers **BUS_CTRL** and **WK_CTRL_2** are reset to following values (=wake sources) '0000 1001' and '000x 0111' in order to ensure that the device can be woken again.*
The selection for WK4_SYNC is unchanged in this case.

*Note: An interrupt will be triggered in SBC Stop Mode if **WD_STM_ WK_EN** is set and if the current on VCC1 crosses above the I_{WD_OFF} threshold. Even though the bit **WD_STM_ WK_EN** is set, an Interrupt will only be triggered if the bits 'WD_STM_EN_x' are set to '0'.*

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WK_CTRL_2
External Wake Source Control (Address 000 0111$_B$)
POR / Soft Reset Value: 0000 0111$_B$; Restart Value: 00xx xxxx$_B$

7	6	5	4	3	2	1	0
reserved	**reserved**	**WK_MEAS**	**WK4_SYNC**	**WK4_EN**	**WK3_EN**	**WK2_EN**	**WK1_EN**
r	r	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
WK_MEAS	5	rw	**WK / Measurement selection** 0_B WK functionality enabled for WK1 and WK2 1_B Measurement functionality enabled; WK1 & WK2 are disable as wake sources, i.e. bits WK1/2_EN bits are ignored
WK4_SYNC	4	rw	**WK4 / SYNC selection** 0_B WK4 active (default value) 1_B SYNC active
WK4_EN	3	rw	**WK4 wake source control** 0_B WK4 wake disabled (default value) 1_B WK4 is enabled as a wake source
WK3_EN	2	rw	**WK3 wake source control** 0_B WK3 wake disabled 1_B WK3 is enabled as a wake source (default value)
WK2_EN	1	rw	**WK2 wake source control** 0_B WK2 wake disabled 1_B WK2 is enabled as a wake source (default value)
WK1_EN	0	rw	**WK1 wake source control** 0_B WK1 wake disabled 1_B WK1 is enabled as a wake source (default value)

Note: WK_MEAS is by default configured for standard WK functionality (WK1 and WK2), i.e. the bits WK1_EN and WK2_EN are ignored in this case. If the bit is set to '1' then the measurement function is enabled during SBC Normal Mode.

Note: WK4 is the default selection. This means it has priority over the SYNC settings.

*Note: The wake sources LIN and CAN are selected in the register **BUS_CTRL** by setting the respective bits to 'wake capable'*

Note: Failure Handling Mechanism: When the device goes to SBC Fail-Safe Mode due to a failure (TSD2, WD-Failure,...), then the wake registers BUS_CTRL and WK_CTRL_2 are reset to following values (=wake sources) '0000 1001' and '000x 0111' in order to ensure that the device can be woken again. The selection for WK4_SYNC is unchanged in this case.

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WK_PUPD_CTRL
Wake Input Level Control (Address 000 1000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
WK4_PUPD_1	**WK4_PUPD_0**	**WK3_PUPD_1**	**WK3_PUPD_0**	**WK2_PUPD_1**	**WK2_PUPD_0**	**WK1_PUPD_1**	**WK1_PUPD_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
WK4_PUPD	7:6	rw	**WK4 Pull-Up / Pull-Down configuration** 00_B No pull-up / pull-down selected 01_B Pull-down resistor selected 10_B Pull-up resistor selected 11_B Automatic switching to pull-up or pull-down
WK3_PUPD	5:4	rw	**WK3 Pull-Up / Pull-Down configuration** 00_B No pull-up / pull-down selected 01_B Pull-down resistor selected 10_B Pull-up resistor selected 11_B Automatic switching to pull-up or pull-down
WK2_PUPD	3:2	rw	**WK2 Pull-Up / Pull-Down configuration** 00_B No pull-up / pull-down selected 01_B Pull-down resistor selected 10_B Pull-up resistor selected 11_B Automatic switching to pull-up or pull-down
WK1_PUPD	1:0	rw	**WK1 Pull-Up / Pull-Down configuration** 00_B No pull-up / pull-down selected 01_B Pull-down resistor selected 10_B Pull-up resistor selected 11_B Automatic switching to pull-up or pull-down

Note: If WK4 is used as SYNC, the settings from register WK_PU_PD_CTRL for WK4 are ignored and the pull-down configuration is used to avoid unintentional activation of a HS by SYNC.
*The configurations pull-up/down or automatic switching are not available for WK4 in SBC Sleep Mode. See also **Chapter 12.2.1**.*

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WK_FLT_CTRL
Wake Input Filter Time Control (Address 000 1001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
WK4_FLT_1	**WK4_FLT_0**	**WK3_FLT_1**	**WK3_FLT_0**	**WK2_FLT_1**	**WK2_FLT_0**	**WK1_FLT_1**	**WK1_FLT_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
WK4_FLT	7:6	rw	**WK4 Filtering time configuration** 00_B Configuration A: Filter with 16µs filter time (static sensing) 01_B Configuration B: Filter with 64µs filter time (static sensing) 10_B Configuration C: Filter is enabled after a settle time defined by timer on-time and a filter time of 16µs (cyclic sensing), Timer1 11_B Configuration D: Filter is enabled after a settle time defined by timer on-time and a filter time of 16µs (cyclic sensing), Timer2
WK3_FLT	5:4	rw	**WK3 Filtering time configuration** 00_B Configuration A: Filter with 16µs filter time (static sensing) 01_B Configuration B: Filter with 64µs filter time (static sensing) 10_B Configuration C: Filter is enabled after a settle time defined by timer on-time and a filter time of 16µs (cyclic sensing), Timer1 11_B Configuration D: Filter is enabled after a settle time defined by timer on-time and a filter time of 16µs (cyclic sensing), Timer2
WK2_FLT	3:2	rw	**WK2 Filtering time configuration** 00_B Configuration A: Filter with 16µs filter time (static sensing) 01_B Configuration B: Filter with 64µs filter time (static sensing) 10_B Configuration C: Filter is enabled after a settle time defined by timer on-time and a filter time of 16µs (cyclic sensing), Timer1 11_B Configuration D: Filter is enabled after a settle time defined by timer on-time and a filter time of 16µs (cyclic sensing), Timer2
WK1_FLT	1:0	rw	**WK1 Filtering time configuration** 00_B Configuration A: Filter with 16µs filter time (static sensing) 01_B Configuration B: Filter with 64µs filter time (static sensing) 10_B Configuration C: Filter is enabled after a settle time defined by timer on-time and a filter time of 16µs (cyclic sensing), Timer1 11_B Configuration D: Filter is enabled after a settle time defined by timer on-time and a filter time of 16µs (cyclic sensing), Timer2

Note: When selecting a filter time configuration, the user must make sure to also assign the respective timer to at least one HS switch during cyclic sense operation

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TIMER1_CTRL
Timer1 Control and Selection (Address 000 1100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 0000$_B$

7	6	5	4	3	2	1	0
reserved	**TIMER1_ ON_2**	**TIMER1_ ON_1**	**TIMER1_ ON_0**	**reserved**	**TIMER1_ PER_2**	**TIMER1_ PER_1**	**TIMER1_ PER_0**
r	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
TIMER1_ ON	6:4	rwh	**Timer1 on-time configuration** 000_B OFF / LOW (timer not running, HSx output is LOW) 001_B 0.1ms on-time / 0.08ms settle time 010_B 0.3ms on-time / 0.27ms settle time 011_B 1.0ms on-time / 0.8ms settle time 100_B 10ms on-time / 0.8ms settle time 101_B 20ms on-time / 0.8ms settle time 110_B OFF / HIGH (timer not running, HSx output is HIGH) 111_B SYNC controlled --> OFF (cyclic sense / cyclic wake end), 0.08ms settle time
Reserved	3	r	**Reserved, always reads as 0**
TIMER1_ PER	2:0	rwh	**Timer1 Period configuration** 000_B 10ms 001_B 20ms 010_B 50ms 011_B 100ms 100_B 200ms 101_B 1s 110_B 2s 111_B SYNC controlled --> ON (cyclic sense / cyclic wake start)

Note: For cyclic wake or cyclic sense, a timer must be first assigned and is then automatically activated as soon as the on-time is configured.

Note: If cyclic sense is selected and the HS switches are cleared during SBC Restart Mode, then also the timer settings (period and on-time) are cleared to avoid incorrect switch detection.

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TIMER2_CTRL
Timer2 Control and selection (Address 000 1101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 0000$_B$

7	6	5	4	3	2	1	0
reserved	**TIMER2_ ON_2**	**TIMER2_ ON_1**	**TIMER2_ ON_0**	**reserved**	**TIMER2_ PER_2**	**TIMER2_ PER_1**	**TIMER2_ PER_0**
r	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
TIMER2_ ON	6:4	rwh	**Timer2 on-time configuration** 000_B OFF / LOW (timer not running, HSx output is LOW) 001_B 0.1ms on-time / 0.08ms settle time 010_B 0.3ms on-time / 0.27ms settle time 011_B 1.0ms on-time / 0.8ms settle time 100_B 10ms on-time / 0.8ms settle time 101_B 20ms on-time / 0.8ms settle time 110_B OFF / HIGH (timer not running, HSx output is HIGH) 111_B SYNC controlled --> OFF (cyclic sense / cyclic wake end), 0.08ms settle time
Reserved	3	r	**Reserved, always reads as 0**
TIMER2_ PER	2:0	rwh	**Timer2 Period configuration** 000_B 10ms 001_B 20ms 010_B 50ms 011_B 100ms 100_B 200ms 101_B 1s 110_B 2s 111_B SYNC controlled --> ON (cyclic sense / cyclic wake start)

Note: For cyclic wake or cyclic sense, a timer must be first assigned and is then automatically activated as soon as the on-time is configured.

Note: If cyclic sense is selected and the HS switches are cleared during SBC Restart Mode, then also the timer settings (period and on-time) are cleared to avoid incorrect switch detection.

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SW_SD_CTRL
Switch Shutdown Control (Address 001 0000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0xxx 0xxx$_B$

7	6	5	4	3	2	1	0
reserved	**HS_OV_SD _EN**	**HS_UV _SD_EN**	**HS_OV_UV _REC**	**reserved**	**LS_OV _SD_EN**	**LS_UV _SD_EN**	**LS_OV_UV _REC**
r	rw	rw	rw	r	rw	rw	rw

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
HS_OV _SD_EN	6	rw	**Shutdown Disabling of HS1...6 in case of VS OV** 0_B shutdown enabled in case of VS OV 1_B shutdown disabled in case of VS OV
HS_UV _SD_EN	5	rw	**Shutdown Disabling of HS1...6 in case of VS UV** 0_B shutdown enabled in case of VS UV 1_B shutdown disabled in case of VS UV
HS_OV_UV _REC	4	rw	**Switch Recovery after removal of VS OV/UV for HS1...6** 0_B Switch recovery is disabled 1_B Previous state before VS OV/UV is enabled after OV/UV condition is removed
Reserved	3	r	**Reserved, always reads as 0**
LS_OV _SD_EN	2	rw	**Shutdown Disabling of LS1...2 in case of VS OV** 0_B shutdown enabled in case of VS OV 1_B shutdown disabled in case of VS OV
LS_UV _SD_EN	1	rw	**Shutdown Disabling of LS1...2 in case of VS UV** 0_B shutdown enabled in case of VS UV 1_B shutdown disabled in case of VS UV
LS_OV_UV _REC	0	rw	**Switch Recovery after removal of VS OV/UV for LS1...2** 0_B Switch recovery is disabled 1_B Previous state before VS OV/UV is enabled after OV/UV condition is removed

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LS_CTRL
Low-Side Switch Control (Address 001 0010$_B$)
POR / Soft Reset Value: 0000 0011$_B$; Restart Value: 0000 0000$_B$

7	6	5	4	3	2	1	0
reserved	**reserved**	**reserved**	**reserved**	**reserved**	**reserved**	**LS2**	**LS1**
r	r	r	r	r	r	rwh	rwh

Field	Bits	Type	Description
Reserved	7:2	r	**Reserved, always reads as 0**
LS2	1	rwh	**LS2 Control** 0_B LS2 Output is “OFF” 1_B LS2 Output is switched on
LS1	0	rwh	**LS1 Control** 0_B LS1 Output is “OFF” 1_B LS1 Output is switched on

Note: The bits for the switches are reset in case of overcurrent and overtemperature.

*Note: The behavior of the low-side switches is different for the inverted low-side logic option. Please see **Chapter 9.2.3** and **Chapter 14.1.1** for further details. The switches will also stay on or will be enabled for TSD2. The respective bits in the register **SW_SD_CTRL** must be set to avoid shutdown due to VS_OV or VS_UV. The bits cannot be cleared if the watchdog timer is in a long open window.*

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HS_CTRL1
High-Side Switch Control 1 (Address 001 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: x000 x000$_B$

7	6	5	4	3	2	1	0
HS2_SEL	**HS2_2**	**HS2_1**	**HS2_0**	**HS1_SEL**	**HS1_2**	**HS1_1**	**HS1_0**
rw	rwh	rwh	rwh	rw	rwh	rwh	rwh

Field	Bits	Type	Description
HS2_SEL	7	rw	**HS2 Open Load & Over Current Detection Configuration** 0_B Small open load detection threshold (0.4mA - 4mA) and small over current threshold are selected 1_B Large open load detection threshold (6mA - 13mA) and large over current threshold are selected
HS2	6:4	rwh	**HS2 configuration** 000_B OFF 001_B ON 010_B Controlled by Timer1 / SYNC 011_B Controlled by Timer2 / SYNC 100_B Controlled by PWM1 101_B Controlled by PWM2 110_B Controlled by PWM3 111_B Controlled by PWM4
HS1_SEL	3	rw	**HS1 Open Load & Over Current Detection Configuration** 0_B Small open load detection threshold (0.4mA - 4mA) and small over current threshold are selected 1_B Large open load detection threshold (6mA - 13mA) and large over current threshold are selected
HS1	2:0	rwh	**HS1 configuration** 000_B OFF 001_B ON 010_B Controlled by Timer1 / SYNC 011_B Controlled by Timer2 / SYNC 100_B Controlled by PWM1 101_B Controlled by PWM2 110_B Controlled by PWM3 111_B Controlled by PWM4

Note: The bits HS1_SEL and HS2_SEL also reconfigure the R_{DS_ON} of HS1/2 to achieve the respective over current and open load settings selection, i.e. the switch is configured with the higher R_{DS_ON} (P_8.3.13) when the lower thresholds for open-load (P_8.3.10) and over current (P_8.3.7) are needed and vice versa.

Note: The bits for the switches are also reset in case of overcurrent and overtemperature as well as for under/over voltage in case the switch recovery bit is not set.

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HS_CTRL2
High-Side Switch Control 2 (Address 001 0101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 0000$_B$

7	6	5	4	3	2	1	0
reserved	**HS4_2**	**HS4_1**	**HS4_0**	**reserved**	**HS3_2**	**HS3_1**	**HS3_0**
r	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
HS4	6:4	rwh	**HS4 configuration** 000_B OFF 001_B ON 010_B Controlled by Timer1 / SYNC 011_B Controlled by Timer2 / SYNC 100_B Controlled by PWM1 101_B Controlled by PWM2 110_B Controlled by PWM3 111_B Controlled by PWM4
Reserved	3	r	**Reserved, always reads as 0**
HS3	2:0	rwh	**HS3 configuration** 000_B OFF 001_B ON 010_B Controlled by Timer1 / SYNC 011_B Controlled by Timer2 / SYNC 100_B Controlled by PWM1 101_B Controlled by PWM2 110_B Controlled by PWM3 111_B Controlled by PWM4

Note: The bits for the switches are also reset in case of overcurrent and overtemperature as well as for under/over voltage in case the switch recovery bit is not set.

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HS_CTRL3
High-Side Switch Control 3 (Address 001 0110$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 0000$_B$

7	6	5	4	3	2	1	0
reserved	**HS6_2**	**HS6_1**	**HS6_0**	**reserved**	**HS5_2**	**HS5_1**	**HS5_0**
r	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
HS6	6:4	rwh	**HS6 configuration** 000_B OFF 001_B ON 010_B Controlled byTimer1 / SYNC 011_B Controlled by Timer2 / SYNC 100_B Controlled by PWM1 101_B Controlled by PWM2 110_B Controlled by PWM3 111_B Controlled by PWM4
Reserved	3	r	**Reserved, always reads as 0**
HS5	2:0	rwh	**HS5 configuration** 000_B OFF 001_B ON 010_B Controlled byTimer1 / SYNC 011_B Controlled by Timer2 / SYNC 100_B Controlled by PWM1 101_B Controlled by PWM2 110_B Controlled by PWM3 111_B Controlled by PWM4

Note: The bits for the switches are also reset in case of overcurrent and overtemperature as well as for under/over voltage in case the switch recovery bit is not set.

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PWM1_CTRL
PWM1 Configuration Control (Address 001 1000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
PWM1_DC_7	**PWM1_DC_6**	**PWM1_DC_5**	**PWM1_DC_4**	**PWM1_DC_3**	**PWM1_DC_2**	**PWM1_DC_1**	**PWM1_DC_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PWM1_DC	7:0	rw	**PWM1 Duty Cycle (bit0=LSB; bit7=MSB)** 0000 0000$_B$ 100% OFF xxxx xxxx $_B$ x% ON 1111 1111$_B$ 100% ON

Note: The min. on-time during PWM is limited by the actual Ton and Toff time of the respective HS switch, e.g. the PWM setting '000 0001' could not be realized.

PWM2_CTRL
PWM2 Configuration Control (Address 001 1001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
PWM2_DC_7	**PWM2_DC_6**	**PWM2_DC_5**	**PWM2_DC_4**	**PWM2_DC_3**	**PWM2_DC_2**	**PWM2_DC_1**	**PWM2_DC_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PWM2_DC	7:0	rw	**PWM2 Duty Cycle (bit0=LSB; bit7=MSB)** 0000 0000$_B$ 100% OFF xxxx xxxx$_B$ x% ON 1111 1111$_B$ 100% ON

Note: The min. on-time during PWM is limited by the actual Ton and Toff time of the respective HS switch, e.g. the PWM setting '000 0001' could not be realized.

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PWM3_CTRL
PWM3 Configuration Control (Address 001 1010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
PWM3_DC_7	**PWM3_DC_6**	**PWM3_DC_5**	**PWM3_DC_4**	**PWM3_DC_3**	**PWM3_DC_2**	**PWM3_DC_1**	**PWM3_DC_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PWM3_DC	7:0	rw	**PWM3 Duty Cycle (bit0=LSB; bit7=MSB)** 0000 0000$_B$ 100% OFF xxxx xxxx$_B$ x% ON 1111 1111$_B$ 100% ON

Note: The min. on-time during PWM is limited by the actual Ton and Toff time of the respective HS switch, e.g. the PWM setting '000 0001' could not be realized.

PWM4_CTRL
PWM4 Configuration Control (Address 001 1011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
PWM4_DC_7	**PWM4_DC_6**	**PWM4_DC_5**	**PWM4_DC_4**	**PWM4_DC_3**	**PWM4_DC_2**	**PWM4_DC_1**	**PWM4_DC_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PWM4_DC	7:0	rw	**PWM4 Duty Cycle (bit0=LSB; bit7=MSB)** 0000 0000$_B$ 100% OFF xxxx xxxx$_B$ x% ON 1111 1111$_B$ 100% ON

Note: The min. on-time during PWM is limited by the actual Ton and Toff time of the respective HS switch, e.g. the PWM setting '000 0001' could not be realized.

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PWM_FREQ_CTRL
PWM Frequency Configuration Control (Address 001 1100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0x0x 0x0x$_B$

7	6	5	4	3	2	1	0
reserved	PWM4_FREQ	reserved	PWM3_FREQ	reserved	PWM2_FREQ	reserved	PWM1_FREQ
r	rw	r	rw	r	rw	r	rw

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
PWM4_ FREQ	6	rw	**PWM4 frequency selection** 0_B 150Hz configuration 1_B 300Hz configuration
Reserved	5	r	**Reserved, always reads as 0**
PWM3_ FREQ	4	rw	**PWM3 frequency selection** 0_B 150Hz configuration 1_B 300Hz configuration
Reserved	3	r	**Reserved, always reads as 0**
PWM2_ FREQ	2	rw	**PWM2 frequency selection** 0_B 150Hz configuration 1_B 300Hz configuration
Reserved	1	r	**Reserved, always reads as 0**
PWM1_ FREQ	0	rw	**PWM1 frequency selection** 0_B 150Hz configuration 1_B 300Hz configuration

SYS_STATUS_CTRL
System Status Control (Address 001 1110$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
SYS_STAT_7	SYS_STAT_6	SYS_STAT_5	SYS_STAT_4	SYS_STAT_3	SYS_STAT_2	SYS_STAT_1	SYS_STAT_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SYS_STAT	7:0	rw	**System Status Control byte (bit0=LSB; bit7=MSB)** Dedicated byte for system configuration, access only by microcontroller

Note: This byte is intended for storing system configurations of the ECU by the microcontroller and is only accessible in SBC Normal Mode. The byte is not accessible by the SBC and is also not cleared after SBC Fail-Safe- or SBC Restart Mode. It allows the microcontroller to quickly store system configuration without loosing the data. The data is stored as long as the SBC is supplied and no POR was issued.

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16.6 SPI Status Information Registers

READ-/WRITE Operation (see **Chapter 16.3**):

- Reading a register is done byte wise by setting the SPI bit 7 to “0” (= READ ONLY)
- Clearing a register is done byte wise by setting the SPI bit 7 to “1”
- SPI status registers are not cleared or changed automatically. This must be done by the microcontroller via SPI command

16.6.1 General Status Registers

SUP_STAT
Supply Voltage Fail Status (Address 100 0001_B)
POR / Soft Reset Value: 1000 0000_B; Restart Value: xxxx $xxxx_B$

7	6	5	4	3	2	1	0
POR	**VS_UV**	**VS_OV**	**VCC2_SC_OT**	**VCC2_FAIL**	**VCC1_SC**	**VCC1_FAIL**	**VCC1_UV**
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
POR	7	rc	**Power-On Reset Detection** 0_B No POR 1_B POR occurred
VS_UV	6	rc	**VS Under-Voltage Detection** 0_B No VS-UV 1_B VS-UV detected
VS_OV	5	rc	**VS Over-Voltage Detection** 0_B No VS-OV 1_B VS-OV detected
VCC2_SC_OT	4	rc	**VCC2 Short to GND (<2V for t>4ms after switch on) or Over Temperature Detection** 0_B No short, no over temperature 1_B VCC2 short to GND or over temperature detected
VCC2_FAIL	3	rc	**VCC2 Failure detection (<2V for t>2µs, any time)** 0_B No VCC2 Fail 1_B VCC2 Fail detected
VCC1_SC	2	rc	**VCC1 Short to GND Detection (<2V for t>4ms after switch on)** 0_B No short 1_B VCC1 short to GND detected
VCC1_FAIL	1	rc	**VCC1 Failure detection (<2V for t>2µs, any time)** 0_B No VCC1 Fail 1_B VCC1 Fail detected
VCC1_UV	0	rc	**VCC1 UV-detection (due to V_{rtx} reset)** 0_B No VCC1 UV detection 1_B VCC1 UV-Fail detected

Note: During SBC Sleep Mode, the bits VCC1_SC, VCC1_FAIL, and VCC1_UV will not be set when VCC1 is OFF

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Note: The default value of the POR bit is set after power-on reset. However it will be cleared after a SBC Soft Reset command.

THERM_STAT
Thermal Protection Status (Address 100 0010_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xxxx\ xxxx_B$

7	6	5	4	3	2	1	0
reserved	**reserved**	**reserved**	**TSD2_2**	**TSD2_1**	**TSD2_0**	**TSD1**	**TPW**
r	r	r	rc	rc	rc	rc	rc

Field	Bits	Type	Description
Reserved	7:5	r	**Reserved, always reads as 0**
TSD2	4:2	rc	**Number of TSD2 Thermal Shut-Down events which caused a restart** 000_B No TSD2 event 001_B 1xTSD2 event, which caused a restart xxx_B .... 111_B 7xTSD2 event (within 1 minute), leading to SBC Fail-Safe Mode
TSD1	1	rc	**Thermal Shut-Down Detection TSD1 Threshold** 0_B No TSD1 fail 1_B TSD1 OT detected
TPW	0	rc	**Thermal Pre warning** 0_B No Thermal Pre warning 1_B Thermal Pre warning detected

Note: TSD1 and TSD2 are not reset automatically, even if the temperature pre warning or TSD1 OT condition is not present anymore. Also TSD2 is not reset after 7xTSD2 to signal to the microcontroller that the device was in Fail-Safe mode. It must be cleared by the microcontroller or it will be changed if a new TSD2 event occurs again. Then the TSD2 register will show '001'. TSD2 is only reset if <7x TSD2 events occurred within one minute. See also ***Chapter 5.1.6***

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DEV_STAT
Device Information Status (Address 100 0011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DEV_STAT_1	**DEV_STAT_0**	**WD_FAIL_3**	**WD_FAIL_2**	**WD_FAIL_1**	**WD_FAIL_0**	**SPI_FAIL**	**FAILURE**
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
DEV_STAT	7:6	rc	**Device Status before SBC Restart Mode** 00_B Cleared (Register must be actively cleared) 01_B Restart due to failure (WD fail, TSD2, VCC1_UV); also after a wake from SBC Fail-Safe Mode; also due to illegal command from Stop to Sleep or Normal to Sleep if no wake source is activated; 10_B SBC Sleep Mode; also if wake sources were still not cleared when going to SBC Sleep mode; 11_B Reserved
WD_FAIL	5:2	rc	**Number of WD-Fail events (max. 15 allowed before SBC Fail-Safe Mode is entered)** 0000_BNo WD Fail 0001_B1x WD Fail $xxx1_B$.... 1111_B 15 WD Fails, causing SBC to enter SBC Fail-Safe Mode
SPI_FAIL	1	rc	**SPI Fail Information** 0_B No SPI fail 1_B Invalid SPI command detected
FAILURE	0	rc	**Activation of Fail Output FO** 0_B No Failure 1_B Failure occurred

Note: The bits DEV_STAT show the status of the device before it went through Restart. Either the device came from regular SBC Sleep Mode or a failure (WD fail, TSD2 fail, VCC_UV fail) occurred (where it could have also have been sent to Sleep and then to Restart).

Note: The SPI_FAIL bit is cleared only by SPI command

Note: The WD_FAIL counter is increased whenever a watchdog failure occurred. The counter is reset after a successful trigger or when Software Development is reached, i.e. TEST = 1; WD_FAIL register will show "15" to signal that SBC Fail-Safe Mode was reached due to 15x Watchdog Failure.
*Also WD_FAIL is not reset automatically to signal the watchdog failure and that the Fail-Safe Mode was entered after15x WD_FAIL. See also **Chapter 5.1.6**. The WD_FAIL register is cleared by a correct watchdog trigger or can be cleared by SPI.*

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BUS_STAT
Bus Communication Status (Address 100 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
reserved	**LIN_FAIL_1**	**LIN_FAIL_0**	**reserved**	**reserved**	**CAN_FAIL_1**	**CAN_FAIL_0**	**VCAN_UV**
r	rc	rc	r	r	rc	rc	rc

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
LIN_FAIL	6:5	rc	**LIN Failure Status** 00_B No error 01_B LIN TSD shutdown 10_B LIN_TXD_DOM: TXD dominant time out for more than 20ms 11_B LIN_BUS_DOM: BUS dominant time out for more than 20ms
Reserved	4:3	r	**Reserved, always reads as 0**
CAN_FAIL	2:1	rc	**CAN Failure Status** 00_B No error 01_B CAN TSD shutdown 10_B CAN_TXD_DOM: TXD dominant time out for more than 20ms 11_B CAN_BUS_DOM: BUS dominant time out for more than 20ms
VCAN_UV	0	rc	**Under voltage CAN Bus Supply** 0_B Normal operation 1_B CAN Supply under voltage detected. Transmitter disabled

Note: VCAN_UV comparator is enabled in SBC Normal Mode if CAN_1 = '1'.

Note: Application Hint for CAN Receive Only Mode:
When the SBC is changed from SBC Normal to Stop Mode and back to Normal while the CAN is in Receive Only Mode, then the VCAN_UV bit will be set unintentionally even if no VCAN-UV condition is present. Clearing of the bit before setting the CAN to Normal Mode is recommended to ensure that no UV occurred.

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WK_STAT
Wake-up Source and Information Status (Address 100 0110$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
WD_STM_WU	LIN_WU	CAN_WU	TIMER_WU	WK4_WU	WK3_WU	WK2_WU	WK1_WU
rw	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
WD_STM_WU	7	rc	**Watch-Dog Wake up during SBC Stop Mode** 0_B No wake up 1_B Wake up
LIN_WU	6	rc	**Wake up via LIN Bus** 0_B No wake up 1_B Wake up
CAN_WU	5	rc	**Wake up via CAN Bus** 0_B No wake up 1_B Wake up
TIMER_WU	4	rc	**Wake up via TimerX** 0_B No wake up 1_B Wake up
WK4_WU	3	rc	**Wake up via WK4** 0_B No wake up 1_B Wake up
WK3_WU	2	rc	**Wake up via WK3** 0_B No wake up 1_B Wake up
WK2_WU	1	rc	**Wake up via WK2** 0_B No wake up 1_B Wake up
WK1_WU	0	rc	**Wake up via WK1** 0_B No wake up 1_B Wake up

*Note: WD_ST_WU is set and signalled as a wake-up event as soon as the load current on VCC1 has exceeded the I_{WD_OFF} threshold. Then the watchdog is started with a long open window if the watchdog was not disabled before going to SBC Stop Mode. The wake-up event signalization can be disabled by clearing the bit **WD_STM_ WK_EN**.*

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WK_LVL_STAT
WK Input Level (Address 100 1000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
TEST_LVL	**reserved**	**reserved**	**reserved**	**WK4_LVL**	**WK3_LVL**	**WK2_LVL**	**WK1_LVL**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
TEST_LVL	7	r	**Status of TEST Pin** 0_B LOW Level (=0) 1_B HIGH Level (=1)
Reserved	6:4	r	**Reserved, always reads as 0**
WK4_LVL	3	r	**Status of WK4** 0_B LOW Level (=0) 1_B HIGH Level (=1)
WK3_LVL	2	r	**Status of WK3** 0_B LOW Level (=0) 1_B HIGH Level (=1)
WK2_LVL	1	r	**Status of WK2** 0_B LOW Level (=0) 1_B HIGH Level (=1)
WK1_LVL	0	r	**Status of WK1** 0_B LOW Level (=0) 1_B HIGH Level (=1)

Note: In cyclic sense or cyclic wake mode, the registers contain the sampled level, i.e. the registers are updated after every sampling.

Note: At the moment the SYNC function is configured then the level of WK4 is stored.

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LS_OC_OT_STAT
Low-Side Switch Overload Status (Address 101 0010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	LS2_OC_OT	LS1_OC_OT
r	r	r	r	r	r	rc	rc

Field	Bits	Type	Description
Reserved	7:2	r	**Reserved, always reads as 0**
LS2_OC_OT	1	rc	**Over-Current & Over-Temperature Detection LS2** 0_B No OC 1_B OC detected
LS1_OC_OT	0	rc	**Over-Current & Over-Temperature Detection LS1** 0_B No OC 1_B OC detected

Note: Both LS switches will be shut down and both bits will be set in case of an over temperature event of one switch.

HS_OC_OT_STAT
High-Side Switch Overload Status (Address 101 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
reserved	reserved	HS6_OC_OT	HS5_OC_OT	HS4_OC_OT	HS3_OC_OT	HS2_OC_OT	HS1_OC_OT
r	r	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
HS6_OC_OT	5	rc	**Over-Current & Over-Temperature Detection HS6** 0_B No OC or OT 1_B OC or OT detected
HS5_OC_OT	4	rc	**Over-Current & Over-Temperature Detection HS5** 0_B No OC or OT 1_B OC or OT detected
HS4_OC_OT	3	rc	**Over-Current & Over-Temperature Detection HS4** 0_B No OC or OT 1_B OC or OT detected
HS3_OC_OT	2	rc	**Over-Current & Over-Temperature Detection HS3** 0_B No OC or OT 1_B OC or OT detected
HS2_OC_OT	1	rc	**Over-Current & Over-Temperature Detection HS2** 0_B No OC or OT 1_B OC or OT detected

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Field	Bits	Type	Description
HS1_OC_OT	0	rc	**Over-Current & Over-Temperature Detection HS1** 0_B No OC or OT 1_B OC or OT detected

Note: All HS switches will be shut down and all bits will be set in case of an over temperature event of one switch.

HS_OL_STAT
High-Side Switch Open-Load Status (Address 101 0101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
reserved	**reserved**	**HS6_OL**	**HS5_OL**	**HS4_OL**	**HS3_OL**	**HS2_OL**	**HS1_OL**
r	r	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
HS6_OL	5	rc	**Open-Load Detection HS6** 0_B No OL 1_B OL detected
HS5_OL	4	rc	**Open-Load Detection HS5** 0_B No OL 1_B OL detected
HS4_OL	3	rc	**Open-Load Detection HS4** 0_B No OL 1_B OL detected
HS3_OL	2	rc	**Open-Load Detection HS3** 0_B No OL 1_B OL detected
HS2_OL	1	rc	**Open-Load Detection HS2** 0_B No OL 1_B OL detected
HS1_OL	0	rc	**Open-Load Detection HS1** 0_B No OL 1_B OL detected

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16.6.2 Family and Product Information Register

FAM_PROD_STAT
SWK Data0 Register (Address 111 1110$_B$)
POR / Soft Reset Value: 0001 yyyy$_B$; Restart Value: 0001 yyyy$_B$

7	6	5	4	3	2	1	0
FAM_3	**FAM_2**	**FAM_1**	**FAM_0**	**PROD_3**	**PROD_2**	**PROD_1**	**PROD_0**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
FAM	7:4	r	**SBC Family Identifier (bit4=LSB; bit7=MSB)** 0 0 0 1$_B$Driver SBC Family
PROD	3:0	r	**SBC Product Identifier (bit0=LSB; bit3=MSB)** 0 0 1 0$_B$ TLE9266 0 0 1 1$_B$TLE9266-2 (inverted Low-Side functionality) 0 1 0 0$_B$TLE9267 (Selective Wake feature = SWK) 0 1 0 1$_B$TLE9267-2 (SWK, inverted Low-Side functionality)

Note: The actual default register value after POR, Soft Reset or Restart of PROD will depend on the respective product. Therefore the value 'y' is specified.

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16.7 Electrical Characteristics

Table 26 Electrical Characteristics: Power Stage

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SPI frequency							
Maximum SPI frequency	$f_{SPI,max}$	–	–	4.0	MHz	1)	P_16.7.1
SPI Interface; Logic Inputs SDI, CLK and CSN							
H-input Voltage Threshold	V_{IH}	–	–	0.7* V_{CC1}	V	–	P_16.7.2
L-input Voltage Threshold	V_{IL}	0.3* V_{CC1}	–	–	V	–	P_16.7.3
Hysteresis of input Voltage	V_{IHY}	–	0.12* V_{CC1}	–	V	1)	P_16.7.4
Pull-up Resistance at pin CSN	R_{ICSN}	20	40	80	kΩ	V_{CSN} = 0.7 x V_{CC1}	P_16.7.5
Pull-down Resistance at pin SDI and CLK	$R_{ICLK/SDI}$	20	40	80	kΩ	$V_{SDI/CLK}$ = 0.2 x V_{CC1}	P_16.7.6
Input Capacitance at pin CSN, SDI or CLK	C_I	–	10	–	pF	1)	P_16.7.7
Logic Output SDO							
H-output Voltage Level	V_{SDOH}	V_{CC1} - 0.4	V_{CC1} - 0.2	–	V	I_{DOH} = -1.6 mA	P_16.7.8
L-output Voltage Level	V_{SDOL}	–	0.2	0.4	V	I_{DOL} = 1.6 mA	P_16.7.9
Tri-state Leakage Current	I_{SDOLK}	-10	–	10	µA	V_{CSN} = V_{CC1}; 0 V < V_{DO} < V_{CC1}	P_16.7.10
Tri-state Input Capacitance	C_{SDO}	–	10	15	pF	1)	P_16.7.11
Data Input Timing[1)]							
Clock Period	t_{pCLK}	250	–	–	ns	–	P_16.7.12
Clock HIGH Time	t_{CLKH}	125	–	–	ns	–	P_16.7.13
Clock LOW Time	t_{CLKL}	125	–	–	ns	–	P_16.7.14
Clock LOW before CSN LOW	t_{bef}	125	–	–	ns	–	P_16.7.15
CSN Setup Time	t_{lead}	250	–	–	ns	–	P_16.7.16
CLK Setup Time	t_{lag}	250	–	–	ns	–	P_16.7.17
Clock LOW after CSN HIGH	t_{beh}	125	–	–	ns	–	P_16.7.18
SDI Set-up Time	t_{DISU}	100	–	–	ns	–	P_16.7.19
SDI Hold Time	t_{DIHO}	50	–	–	ns	–	P_16.7.20
Input Signal Rise Time at pin SDI, CLK and CSN	t_{rIN}	–	–	50	ns	–	P_16.7.21
Input Signal Fall Time at pin SDI, CLK and CSN	t_{fIN}	–	–	50	ns	–	P_16.7.22
Delay Time for Mode Changes[2)]	$t_{Del,Mode}$	–	–	4	µs	–	P_16.7.23

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Table 26 Electrical Characteristics: Power Stage (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Minimum CSN HIGH Time	$t_{CSN(high)}$	3	–	–	µs	–	P_16.7.24
Data Output Timing[1]							
SDO Rise Time	t_{rSDO}	–	30	80	ns	C_L = 100 pF	P_16.7.25
SDO Fall Time	t_{fSDO}	–	30	80	ns	C_L = 100 pF	P_16.7.26
SDO Enable Time	t_{ENSDO}	–	–	50	ns	low impedance	P_16.7.27
SDO Disable Time	t_{DISSDO}	–	–	50	ns	high impedance	P_16.7.28
SDO Valid Time	t_{VASDO}	–	–	50	ns	C_L = 100 pF	P_16.7.29

1) Not subject to production test; specified by design

2) Applies to all mode changes triggered via SPI commands. Not subject to production test; tolerance defined by internal oscillator tolerance

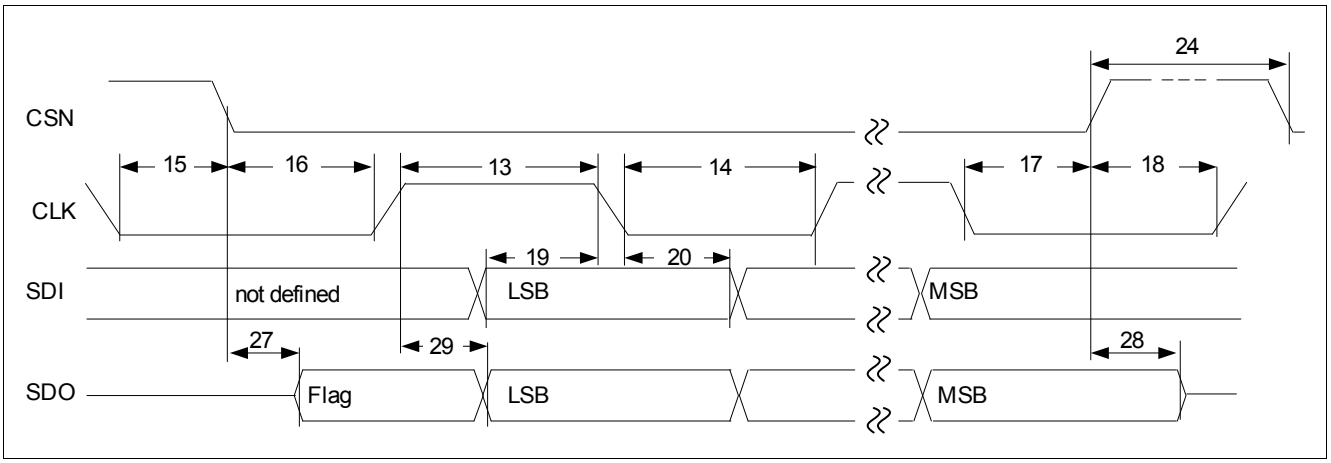


Figure 39 SPI Timing Diagram

Note: Numbers in drawing correlate to the last 2 digits of the Number field in the Electrical Characteristics table.

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17 Application Information

17.1 Application Diagram

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

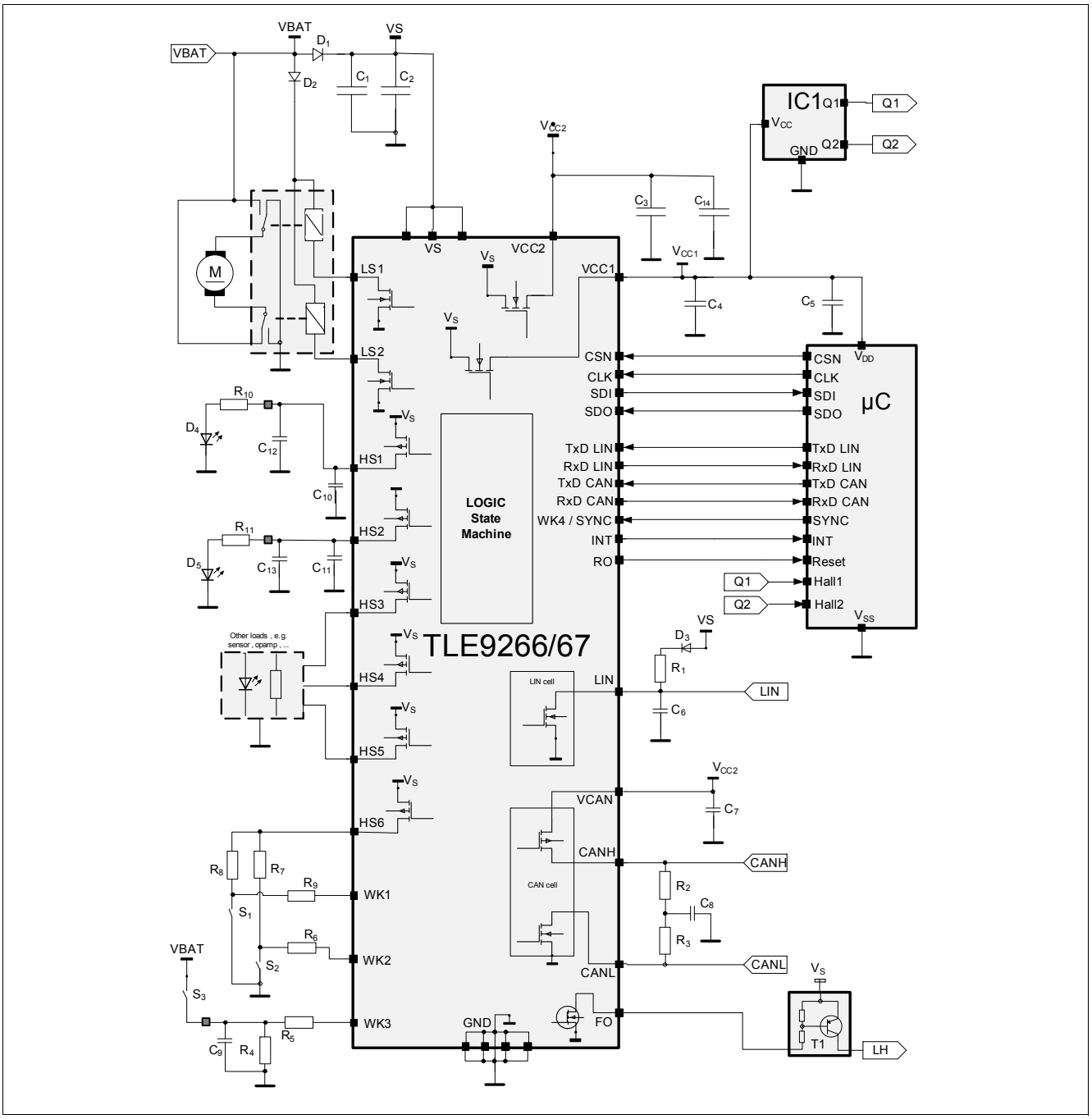


Figure 40 Simplified Application Diagram

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Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the actual application.

Table 27 Bill of Material for Figure 40

Ref.	Typical Value	Purpose / Comment
Capacitances		
C1	68µF	Buffering capacitor to cut off battery spikes, depending on application
C2	100nF	EMC, blocking capacitor
C3	10µF low ESR	As required by application, min. 470nF for stability
C4	10µF low ESR	As required by application, min. 470nF for stability
C5	100nF ceramic	spike filtering, improve stability of supply
C6	1nF / OEM dependent	LIN master termination
C7	100nF	EMC improvement, blocking capacitor
C8	4.7nF / OEM dependent	Split termination stability
C9	10nF	As required by application, for off-board connections
C10	47pF	As required by application, mandatory for off-board connections; place close to pin
C11	47pF	As required by application, mandatory for off-board connections; place close to pin
C12	33nF	As required by application, mandatory for off-board connections, especially when used in high-ohmic configuration or for HS3...6; place close to connector
C13	33nF	As required by application, mandatory for off-board connections, especially when used in high-ohmic configuration or for HS3...6; place close to connector
C14	47nF	As required by application, mandatory for off-board connections, place close to connector
Resistances		
R1	1kΩ / OEM dependent	LIN master termination (if configured as a LIN master)
R2	60Ω / OEM dependent	CAN bus termination
R3	60Ω / OEM dependent	CAN bus termination
R4	10kΩ	Wetting current of the switch, as required by application
R5	10kΩ	Limit the WK pin current, e.g. for ISO pulses
R6	10kΩ	Limit the WK pin current, e.g. for ISO pulses
R7	10kΩ	Wetting current of the switch, as required by application
R8	10kΩ	Wetting current of the switch, as required by application
R9	10kΩ	Limit the WK pin current, e.g. for ISO pulses
R10	depending on LED config.	LED current limitation, as required by application
R11	depending on LED config.	LED current limitation, as required by application
Relay		
Relay	e.g. FTR-P4CN012W1	Relay for motor control, controlled by LS1/2
Active Components		
D1	e.g. BAS 3010A	Reverse polarity protection
D2	e.g. BAS 3010A	Reverse polarity protection

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Table 27 Bill of Material for Figure 40 (cont'd)

Ref.	Typical Value	Purpose / Comment
D3	e.g. BAS70	Requested by LIN standard; reverse polarity protection of network
D4	LED	As required by application, configure series resistor accordingly
D5	LED	As required by application, configure series resistor accordingly
T1	e.g. BCR191W	High active FO control
µC	e.g. XC2xxx	Microcontroller

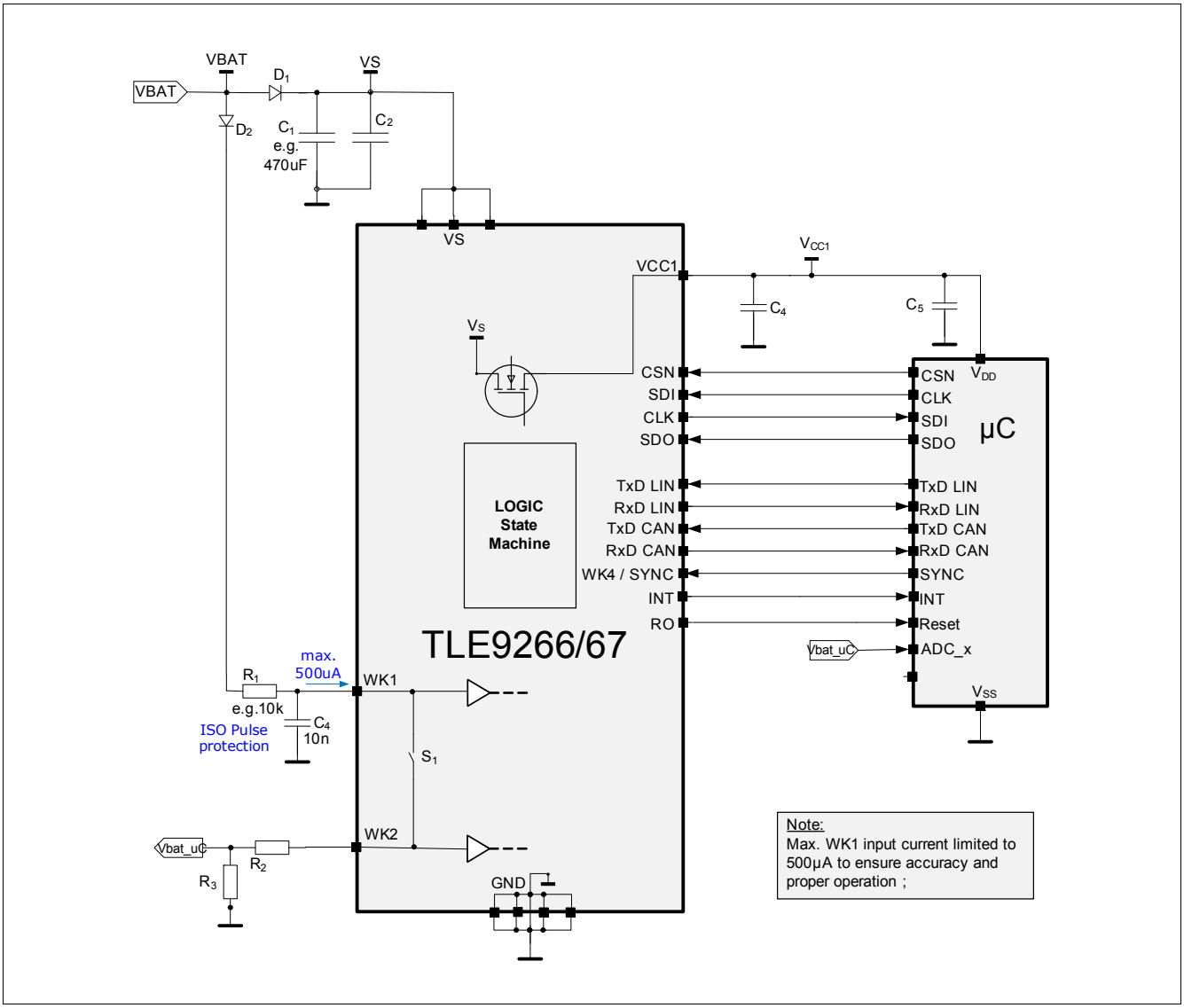


Figure 41 Simplified Application Diagram with the Alternate Measurement Function via WK1 and WK2

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.WK1 must be connected to signal to be measured and WK2 is the output to the microcontroller supervision function. The maximum current into WK1 must be <500µA. The minimum current into WK1 should be >5µA to ensure proper operation.

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17.2 ESD and EMC Tests

Tests for ESD robustness according to IEC61000-4-2 “gun test” (150pF, 330Ω) have been performed.

The results and test condition are available in a test report. The values for the test are listed in **Table 28**.

Table 28 ESD “Gun Test”

Performed Test	Result	Unit	Remarks
ESD at pin CANH, CANL, LIN, VS[1)], WK1..3[1)], HSx[1)], VCC2[1)] versus GND	>6	kV	[2)]positive pulse
ESD at pin CANH, CANL, LIN, VS[1)], WK1..3[1)], HSx[1)], VCC2[1)] versus GND	< -6	kV	[2)]negative pulse

1) ESD Test “Gun Test” is specified with external components for pins VS, WK1..3, HSx and VCC2. See the application diagram in **Chapter 17.1** for more information.

2) ESD susceptibility “ESD GUN” according LIN EMC 1.3 Test Specification, Section 4.3 (IEC 61000-4-2). Tested by external test house (IBEE Zwickau, EMC Test report Nr. 02-13-13)

EMC and ESD susceptibility tests according to SAE J2962-2 (2010) have been performed. Tested by external test house (UL LLC, Test report Nr. 2012-787 & 2013-238)

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17.3 Thermal Behavior of Package

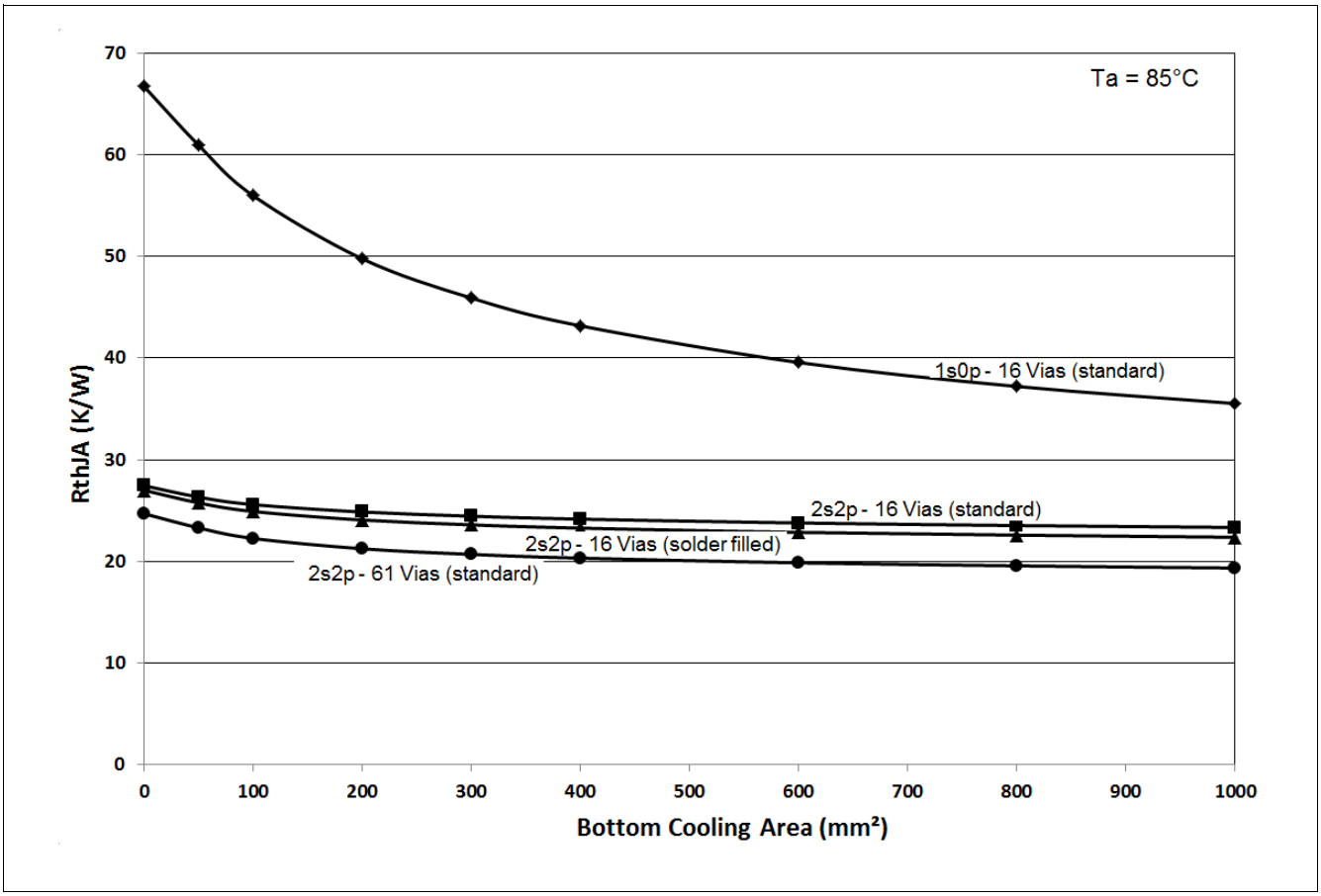


Figure 42 Thermal Resistance (Rth_{J-A}) vs. Cooling Area

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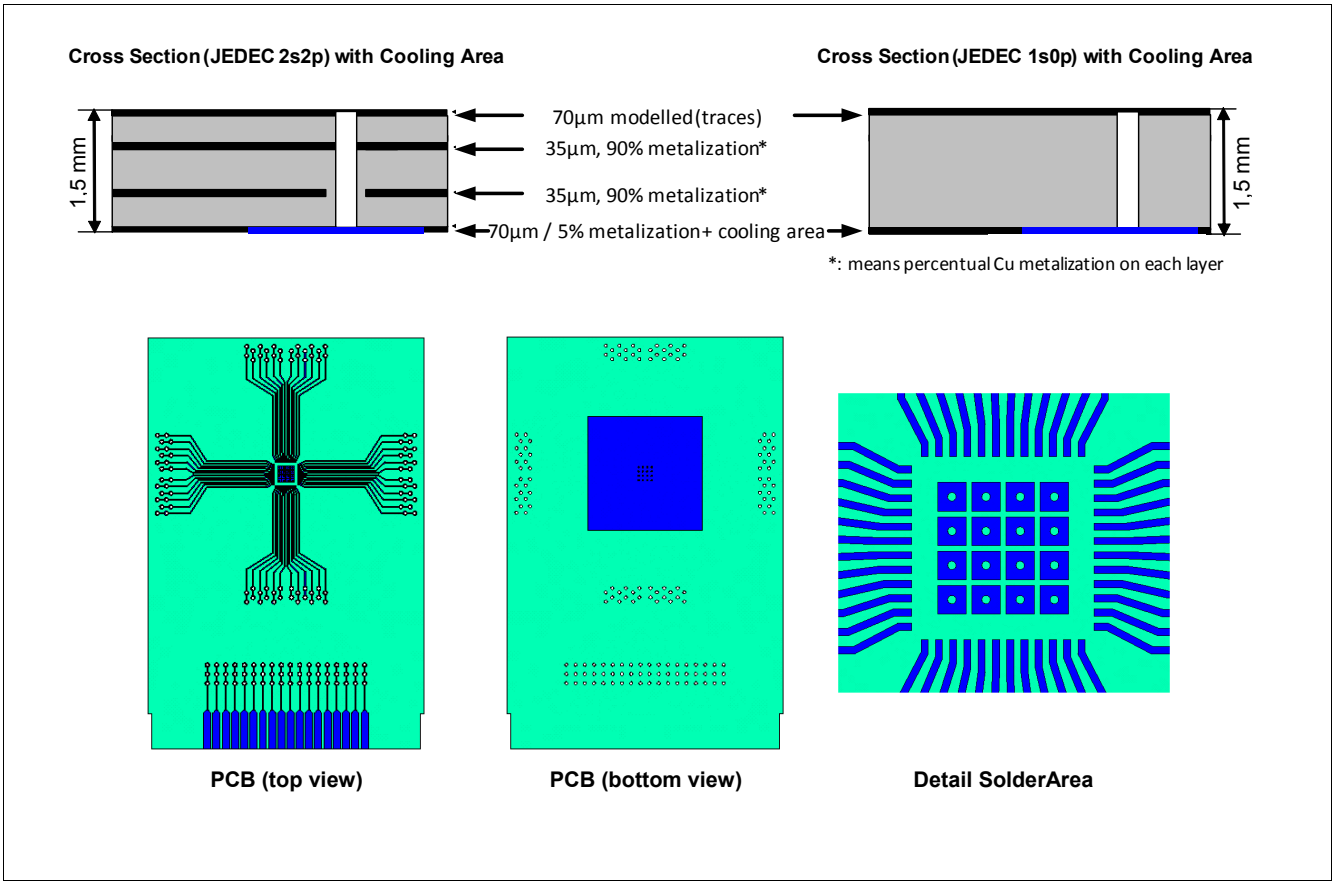


Figure 43 Board Setup

Board setup is defined according to JESD 51-2,-5,-7.
Board: 76.2x114.3x1.5mm³ with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm^2 cooling area on the bottom layer (70µm).

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18 Package Outlines

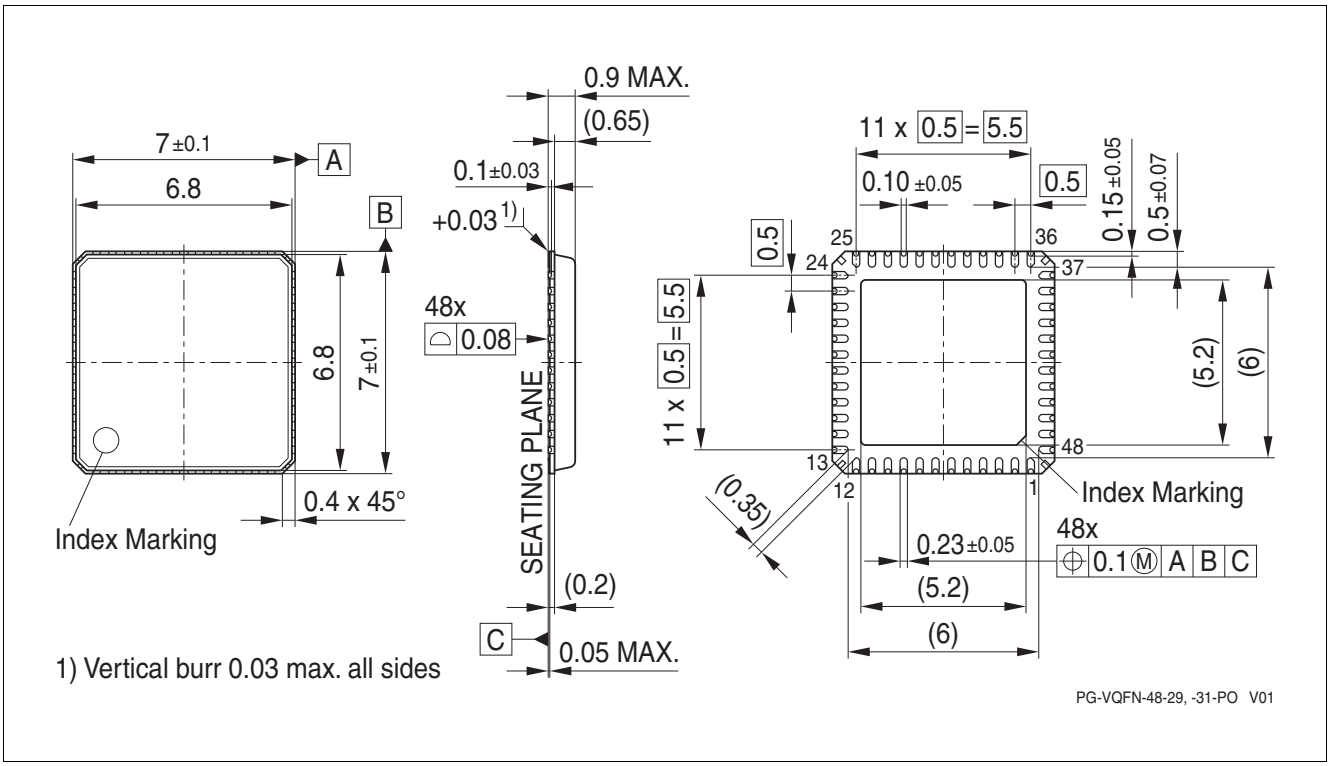


Figure 44 PG-VQFN-48-31

Note: For assembly recommendations please also refer to the documents "Recommendations for Board Assembly (VQFN and IQFN)" and "VQFN48 Layout Hints" on the Infineon website (**www.infineon.com**).

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

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19 Revision History

Revision	Date	Changes
Rev. 1.1 changes vs. Rev 1.0:		
v1.1	2014-02-01	- Voltage Regulators 1 & 2: Updated Block Diagrams **Figure 10** & **Figure 12** and corrected axis format of **Figure 13**; - High-Side Switches: Updated Block Diagram **Figure 14**, added description for the Ron configuration to achieve selection of different open-load and over-current thresholds in **Chapter 8.2** and with footnote [1)] in **Chapter 8.3** (numbering of other footnotes increased sequentially); - Low-Side Switches: Updated Block Diagram **Figure 15**; - Serial Peripheral Interface: added note in HS_CTRL_1 register explaining that HSx_SEL bit is reconfiguring the R_{DS_ON} to achieve selection of respective open-load and over-current threshold; - Application Information: updated **Figure 43** showing cooling area of cross section in same color as bottom view;
v1.0	2013-07-01	Initial Release

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