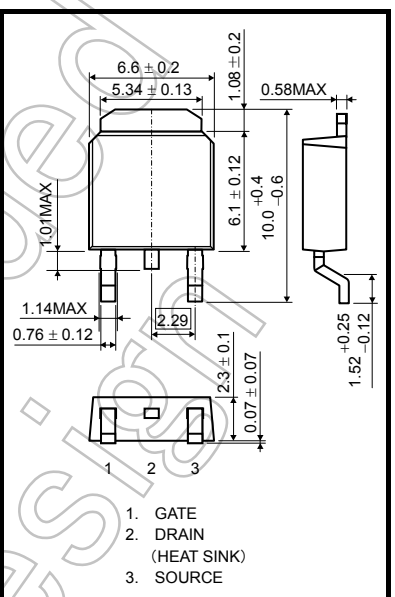
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π-MOSVII)

# TK7P50D

## Switching Regulator Applications

- Low drain-source ON-resistance: $R_{DS\ (ON)}$ = 1.0 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 2.5 S (typ.)
- Low leakage current: $I_{DSS}$ = 10 μA (max) ($V_{DS}$ = 500 V)
- Enhancement-mode: $V_{th}$ = 2.4 to 4.4 V ($V_{DS}$ = 10 V, $I_D$ = 1 mA)

Unit: mm




| | |
|---|---|
| JEDEC | — |
| JEITA | — |
| TOSHIBA | 2-7K1A |

Weight : 0.36 g (typ.)

## Absolute Maximum Ratings (Ta = 25°C)

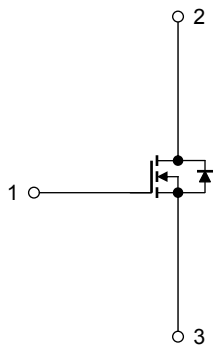
| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | 500 | V |
| Gate-source voltage | | $V_{GSS}$ | ±30 | V |
| Drain current | DC (Note 1) | $I_D$ | 7 | A |
| | Pulse (t = 1 ms) (Note 1) | $I_{DP}$ | 28 | |
| Drain power dissipation (Tc = 25°C) | | $P_D$ | 100 | W |
| Single pulse avalanche energy (Note 2) | | $E_{AS}$ | 105 | mJ |
| Avalanche current | | $I_{AR}$ | 7 | A |
| Repetitive avalanche energy (Note 3) | | $E_{AR}$ | 10 | mJ |
| Channel temperature | | $T_{ch}$ | 150 | °C |
| Storage temperature range | | $T_{stg}$ | −55 to 150 | °C |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Thermal Characteristics

| Characteristics | Symbol | Max | Unit |
|---|---|---|---|
| Thermal resistance, channel to case | $R_{th\ (ch-c)}$ | 1.25 | °C/W |
| Thermal resistance, channel to ambient | $R_{th\ (ch-a)}$ | 125 | °C/W |

Internal Connection




Note 1: Please use devices on conditions that the channel temperature is below 150°C.

Note 2: $V_{DD}$ = 90 V, $T_{ch}$ = 25°C (initial), L = 3.64 mH, $R_G$ = 25 Ω, $I_{AR}$ = 7 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic sensitive device. Please handle with caution.

Start of commercial production
2009-12

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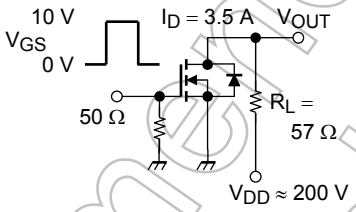
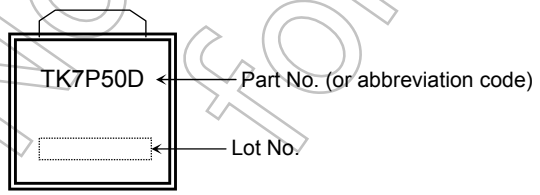
## Electrical Characteristics (Ta = 25°C)

| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±30 V, $V_{DS}$ = 0 V | — | — | ±1 | μA |
| Drain cut-off current | | $I_{DSS}$ | $V_{DS}$ = 500 V, $V_{GS}$ = 0 V | — | — | 10 | μA |
| Drain-source breakdown voltage | | $V_{(BR)DSS}$ | $I_D$ = 10 mA, $V_{GS}$ = 0 V | 500 | — | — | V |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 2.4 | — | 4.4 | V |
| Drain-source ON-resistance | | $R_{DS(ON)}$ | $V_{GS}$ = 10 V, $I_D$ = 3.5 A | — | 1.0 | 1.22 | Ω |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 3.5 A | 0.7 | 2.5 | — | S |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1 MHz | — | 600 | — | pF |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 4 | — | |
| Output capacitance | | $C_{oss}$ | | — | 70 | — | |
| Switching time | Rise time | $t_r$ |   Duty ≤ 1%, $t_w$ = 10 μs | — | 18 | — | ns |
| | Turn-on time | $t_{on}$ | | — | 40 | — | |
| | Fall time | $t_f$ | | — | 8 | — | |
| | Turn-off time | $t_{off}$ | | — | 55 | — | |
| Total gate charge | | $Q_g$ | $V_{DD}$ ≈ 400 V, $V_{GS}$ = 10 V, $I_D$ = 7 A | — | 12 | — | nC |
| Gate-source charge | | $Q_{gs}$ | | — | 7 | — | |
| Gate-drain charge | | $Q_{gd}$ | | — | 5 | — | |

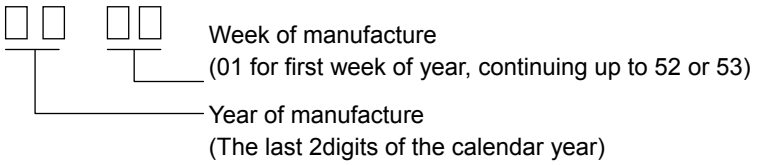
## Source-Drain Ratings and Characteristics (Ta = 25°C)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Continuous drain reverse current (Note 1) | $I_{DR}$ | — | — | — | 7 | A |
| Pulse drain reverse current (Note 1) | $I_{DRP}$ | — | — | — | 28 | A |
| Forward voltage (diode) | $V_{DSF}$ | $I_{DR}$ = 7 A, $V_{GS}$ = 0 V | — | — | −1.7 | V |
| Reverse recovery time | $t_{rr}$ | $I_{DR}$ = 7 A, $V_{GS}$ = 0 V, $dI_{DR}/dt$ = 100 A/μs | — | 1200 | — | ns |
| Reverse recovery charge | $Q_{rr}$ | | — | 7 | — | μC |

## Marking (Note 4)




Note 4: * Weekly code: (Four digits)

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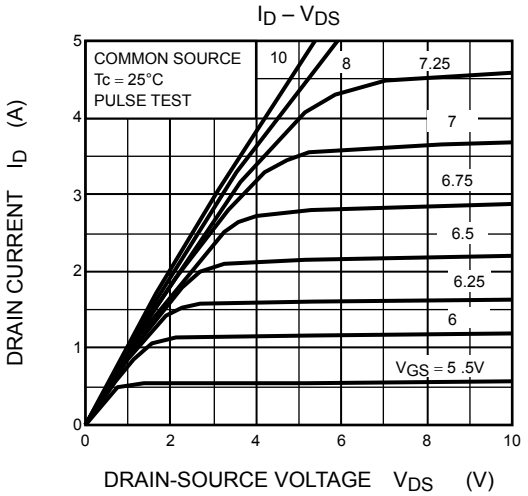


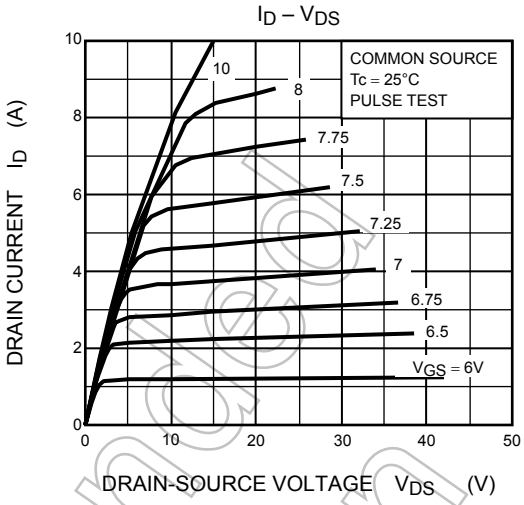


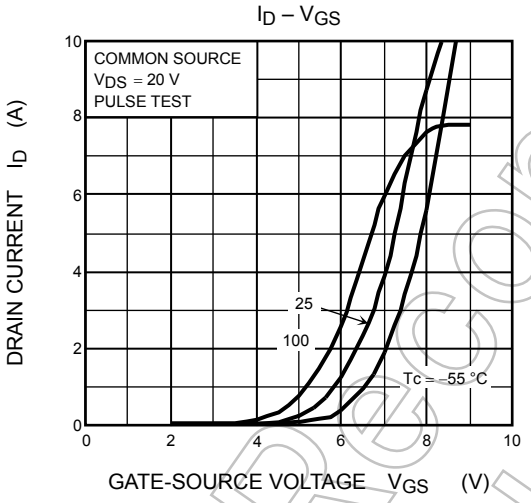


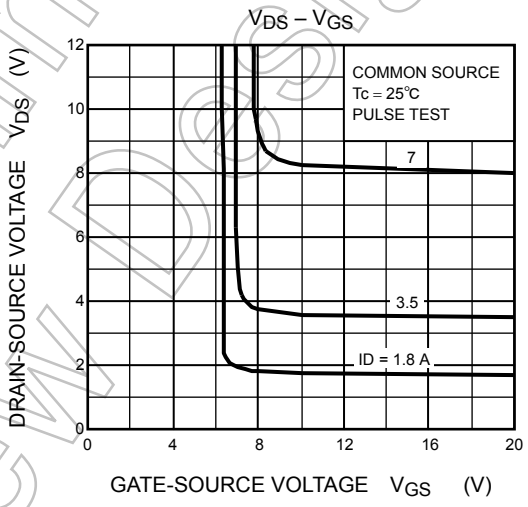


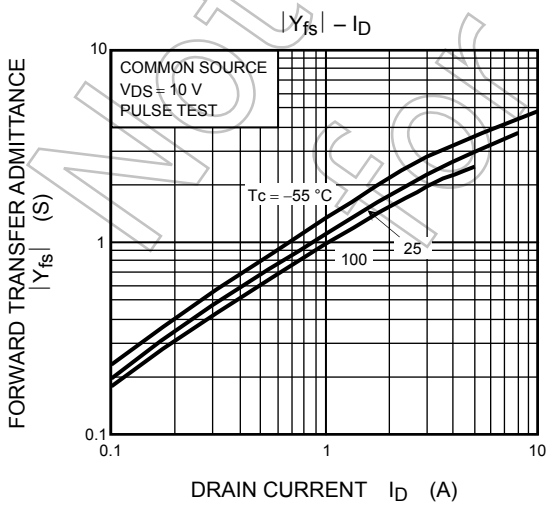


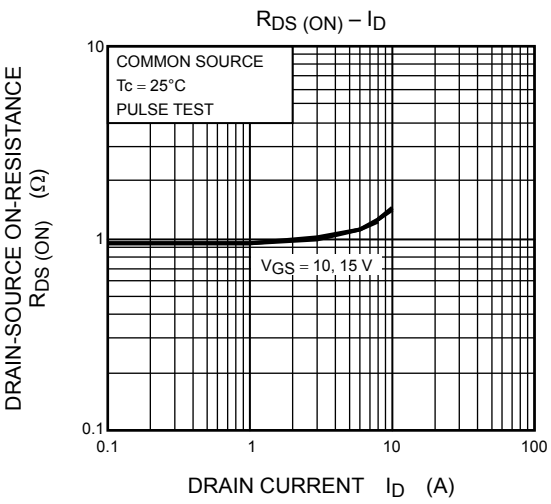


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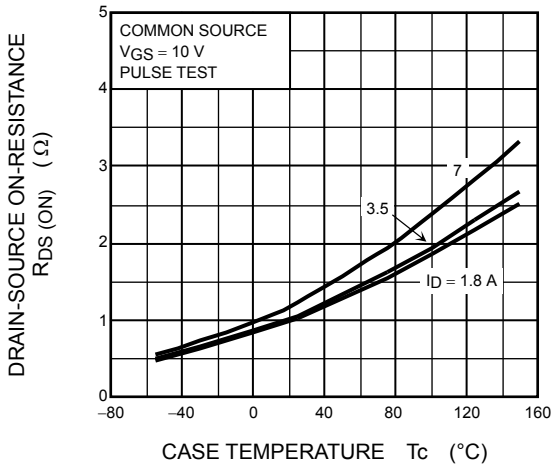
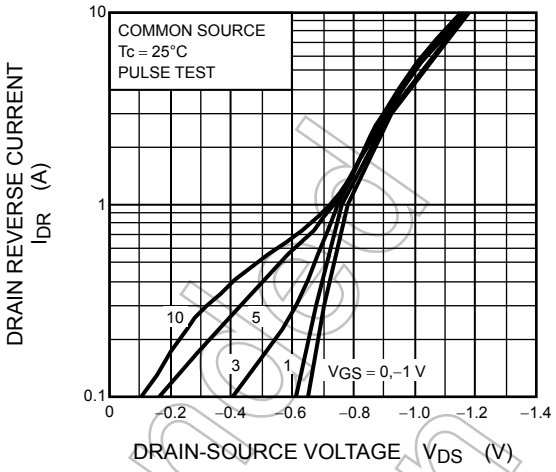
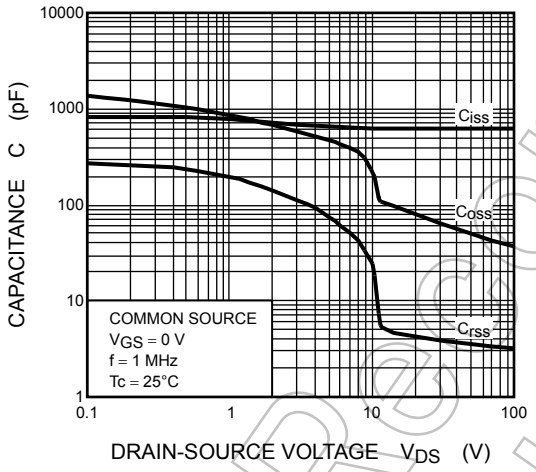
$R_{DS\ (ON)}$ – Tc



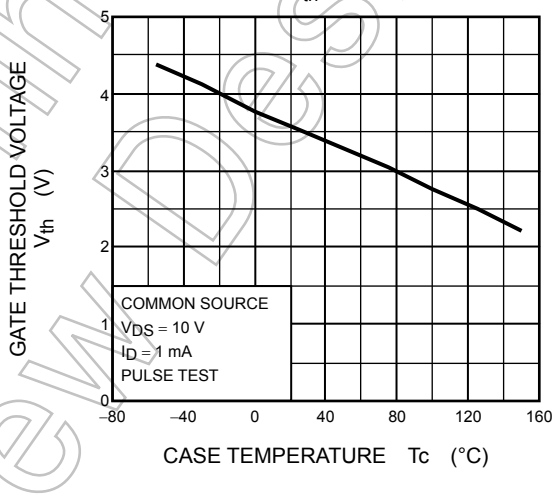

$I_{DR}$ – $V_{DS}$



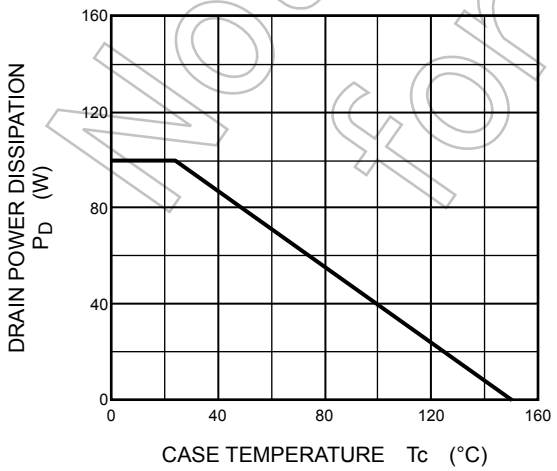

CAPACITANCE – $V_{DS}$



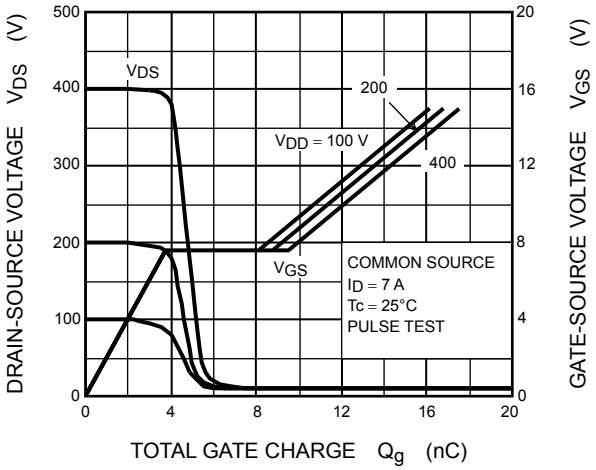

$V_{th}$ – Tc




$P_D$ – Tc




DYNAMIC INPUT / OUTPUT CHARACTERISTICS

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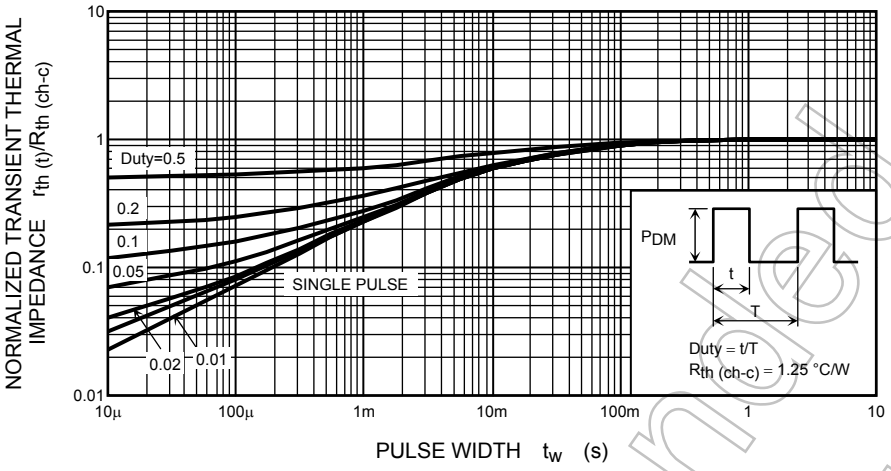
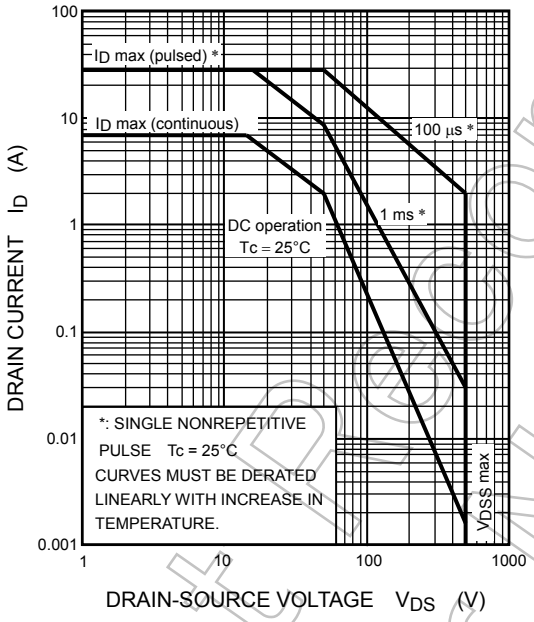
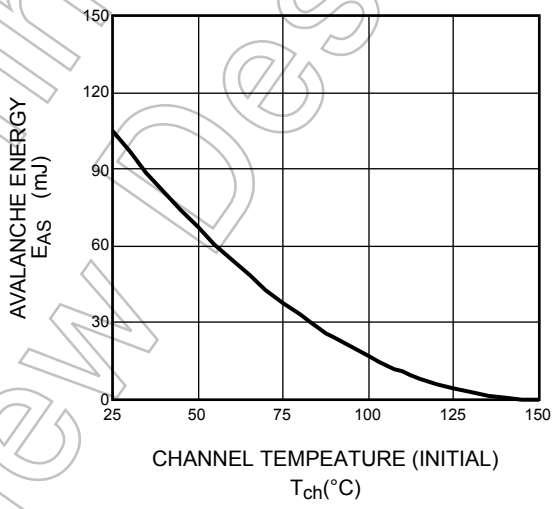
$r_{th} - t_w$

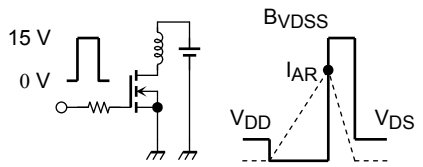



SAFE OPERATING AREA




$E_{AS} - T_{ch}$




TEST CIRCUIT WAVEFORM

$R_G = 25\ \Omega$
$V_{DD} = 90$ V, L = 3.64 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left( \frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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