ANALOG DEVICES

Circuit Note
CN-0270

Circuits from the Lab® Reference Designs

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Devices Connected/Referenced	
AD5700, AD5700-1	Low Power HART® Modem
AD5420	16-Bit 4 mA to 20 mA DAC

Complete 4 mA to 20 mA HART Solution

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0270 Evaluation Board (EVAL-CN0270-EB1Z) includes
USB-SWD/UART-EMUZ

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 uses the AD5700, the industry's lowest power and smallest footprint HART[1]-compliant IC modem and the AD5420, a 16-bit current-output DAC, to form a complete HART-compatible 4 mA to 20 mA solution, typical of line-powered transmitter applications

For additional space savings, the AD5700-1 offers a 0.5% precision internal oscillator.

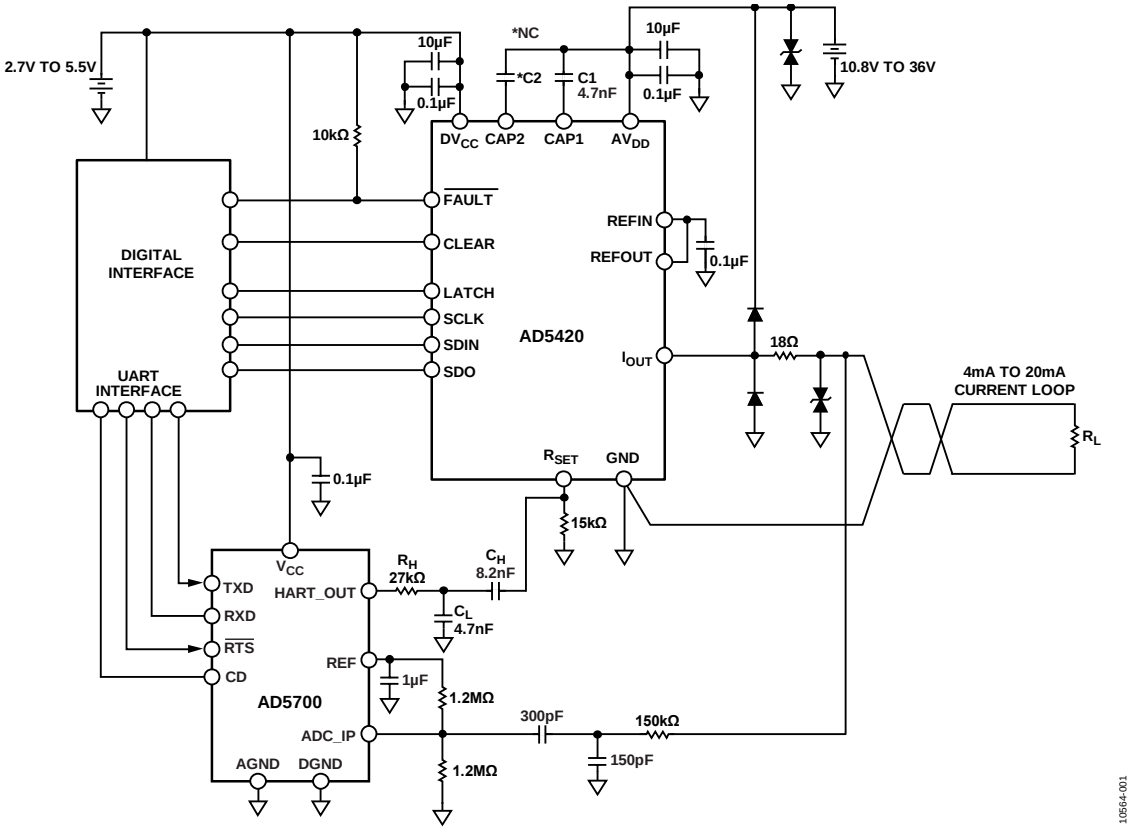

Figure 1. AD5420 HART-Enabled Circuit Simplified Schematic

[1] HART® is a registered trademark of the HART Communication Foundation.

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This circuit adheres to the HART physical layer specifications as defined by the HART Communication Foundation, for example, the analog rate of change and noise during silence specifications.

For many years, 4 mA to 20 mA communication has been used in process control instrumentation. This communication method is reliable and robust, and offers high immunity to environmental interference over long communication distances. A limitation, however, is that only 1-way communication of one process variable at a time is possible.

The development of the highway addressable remote transducer (HART) standard provided highly capable 2-way digital communication, simultaneously with the 4 mA to 20 mA analog signaling used by traditional instrumentation equipment. This allows for features such as remote calibration, fault interrogation, and transmission of additional process variables. Put simply, HART is a digital two-way communication in which a 1 mA peak-to-peak frequency-shift-keyed (FSK) signal is modulated on top of the 4 mA to 20 mA analog current signal.

CIRCUIT DESCRIPTION

Figure 1 shows the manner in which the AD5420 can be combined with the AD5700 HART modem and a UART interface to construct a HART-capable 4 mA to 20 mA current output. Such a circuit is popular in line-powered field transmitters in which a variety of input signals (RTD, TC, and ohm) are converted into a scalable analog, 4 mA to 20 mA output signal.The HART_OUT signal from the AD5700 is attenuated and ac-coupled into the R_{SET} pin of the AD5420. If the external R_{SET} resistor is not being used, an alternative method of connecting the AD5420 and the AD5700 can be found in Application Note AN-1065, where the AD5700 HART modem output is coupled into the AD5420 via the CAP2 pin. While the method described in this circuit note requires the use of the external R_{SET} resistor, it provides better power supply rejection performance than the alternative application note solution. The use of either solution results in the AD5700 HART modem output modulating the 4 mA to 20 mA analog current (as shown in Figure 2) without affecting the dc level of the current. The diode protection circuitry (D1 to D4) is discussed in more detail in the Transient Voltage Protection section.

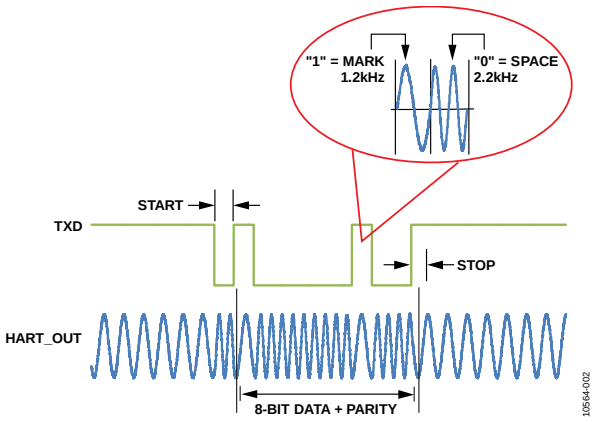

Figure 2. AD5700/AD5700-1 Sample Modulator Waveform

Determining the Values of the External Components

C1 and C2 can be used in conjunction with the digital slew rate control functionality of the part to control the slew rate of the I_{OUT} signal of the AD5420. In determining the absolute values of the capacitors, ensure that the FSK output from the modem is passed undistorted. Thus, the bandwidth presented to the modem output signal must pass the 1200 Hz and 2200 Hz frequencies. Figure 3 shows a circuit that achieves this requirement. In this case, C2 is left open-circuit.

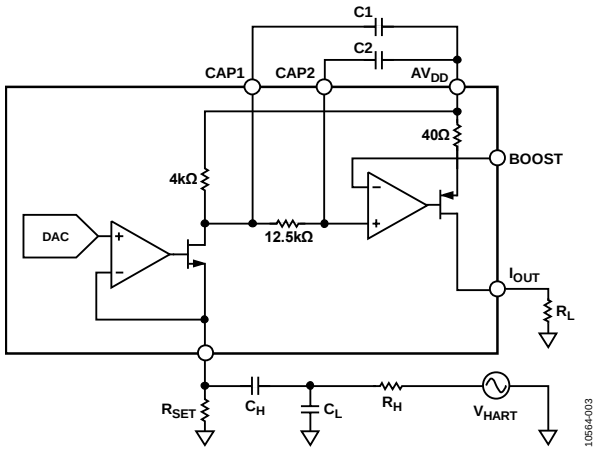

Figure 3. AD5420/AD5410 and AD5700 HART Modem Connection

The low-pass and high-pass filter circuitry is formed through the interaction of R_H, C_L, C_H, and C1, along with some internal circuitry in the AD5420. In calculating the values of these components, the low-pass and high-pass frequency cutoff point targets were >10 kHz and <500 Hz, respectively. Figure 4 shows a plot of the simulated frequency response, while Table 1 shows the effect on the frequency response of increasing each component while the remaining component values are kept constant.

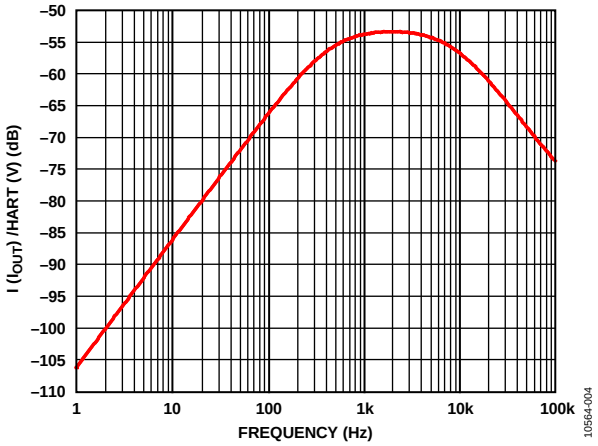

Figure 4. Simulated Frequency Response

Table 1. Effect on Frequency Response of Individual Component Value Increase

Component	C1	C_H	C_L	R_H
f_L (Hz)	↓	↓	↓	↓
f_H (kHz)	↓	No change	No change	No change
G (dB)	↓	↑	↓	↓

The output of the modem is an FSK signal consisting of 1200 Hz and 2200 Hz shift frequencies. This signal must translate to a 1 mA peak-to-peak current signal. To achieve this, the signal amplitude at the R_{SET} pin must be attenuated. This is due to the internal current gain configuration in the AD5420 design. Assuming that the modem output amplitude is 500 mV peak-to-peak, its output must be attenuated by 500/150 = 3.33. This attenuation is achieved by means of R_H and C_L.

The measurements in this circuit note were completed using the following component values:

- C1 = 4.7 nF
- R_H = 27 kΩ
- C_L = 4.7 nF
- C_H = 8.2 nF

Figure 5 shows the individual 1200 Hz and 2200 Hz shift frequencies measured across a 500 Ω load resistor. Channel 1 shows the modulated HART signal coupled into the AD5420 output (set to output 4 mA), while Channel 2 shows the AD5700 TXD signal.

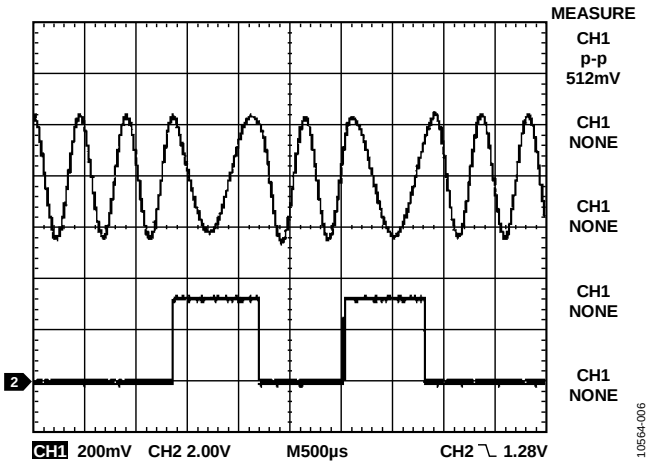

Figure 5. FSK Waveforms Measured Across a 500 Ω Load

HART Compliance

For the circuit in Figure 1 to be HART-compliant, it must meet the HART physical layer specifications. There are numerous physical layer specifications included in the HART specification documents. The two that are most important in this case are the output noise during silence and the analog rate of change.

Output Noise During Silence

When a HART device is not transmitting (silent), it should not couple noise onto the network in the HART extended frequency band. Excessive noise may interfere with reception of HART signals by the device itself or other devices on the network.

The voltage noise measured across a 500 Ω load must contain no more than 2.2 mV rms of combined broadband and correlated noise in the extended frequency band. This noise was measured by connecting the HCF_TOOL-31 filter (available from the HART Communication Foundation) across the 500 Ω load and by connecting the output of the filter to a true rms meter (see Figure 6). An oscilloscope was also used to examine the output waveform peak-to-peak voltage.

The AD5420 output current was set to 4 mA, 12 mA, and 20 mA. No discernible differences in noise were measured. The rms values measured, with and without the HCF_TOOL-31 band-pass filter, were 115 µV rms and 252 µV rms, respectively. Both of these values are well within the required specifications of 2.2 mV rms (with HART filter) and 138 mV rms (broadband noise without HART filter).

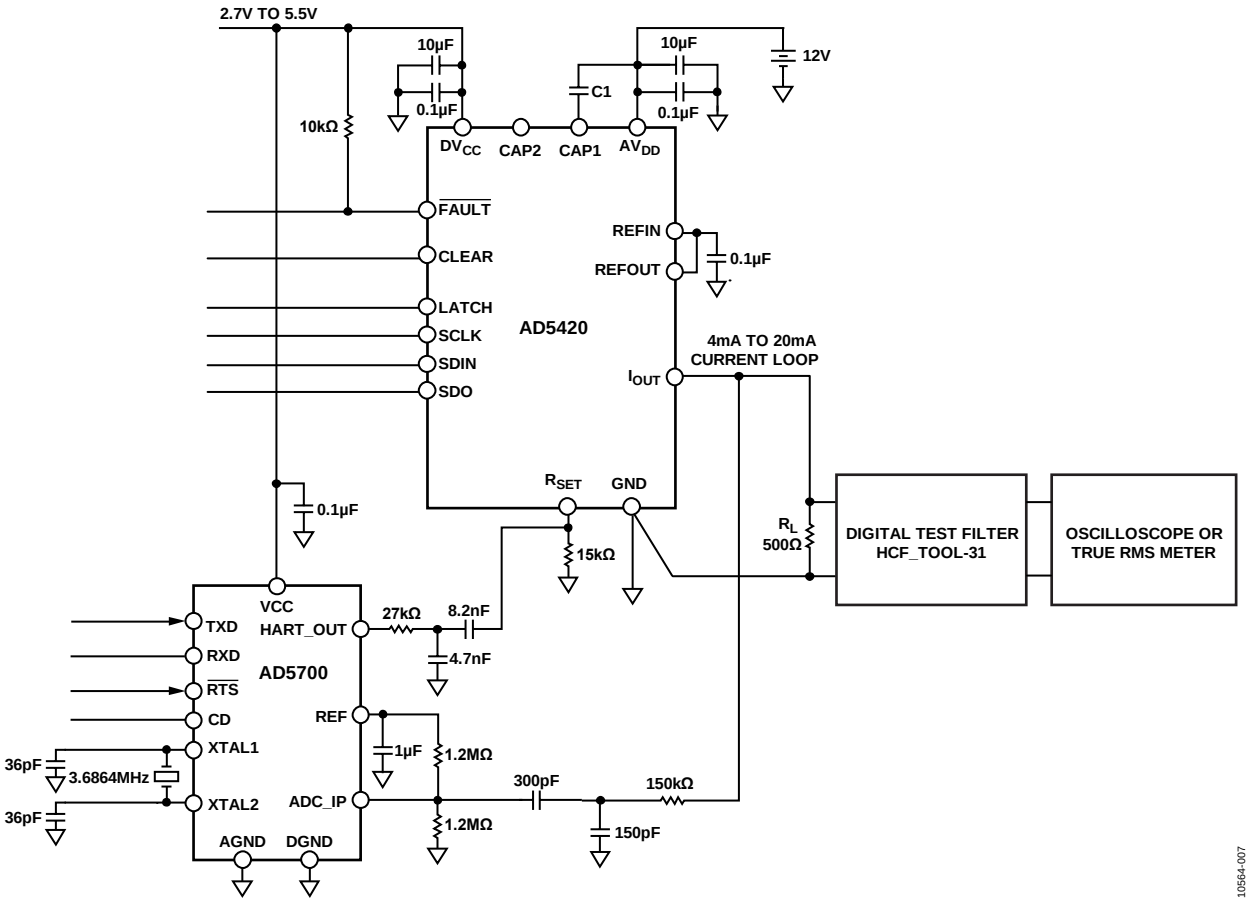

Figure 6. HART Specifications Test Circuit

Figure 7 and Figure 8 show the oscilloscope plots for 4 mA and 12 mA output current, respectively. Note that the filter has a pass-band gain of 10. Channel 1 and Channel 2 show the input and output of the filter, respectively.

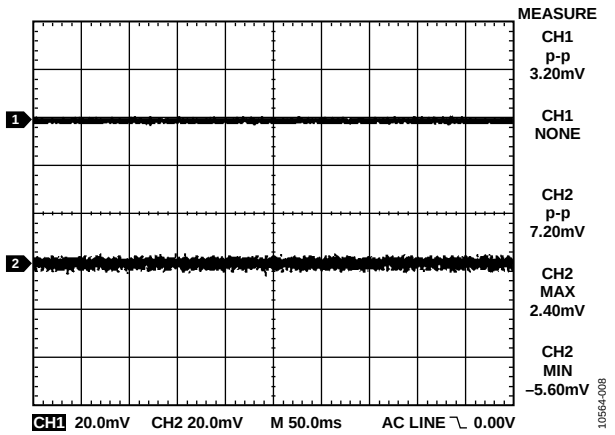

Figure 7. Noise at Input (CH1) and Output (CH2) of HART Filter with 4 mA Output Current

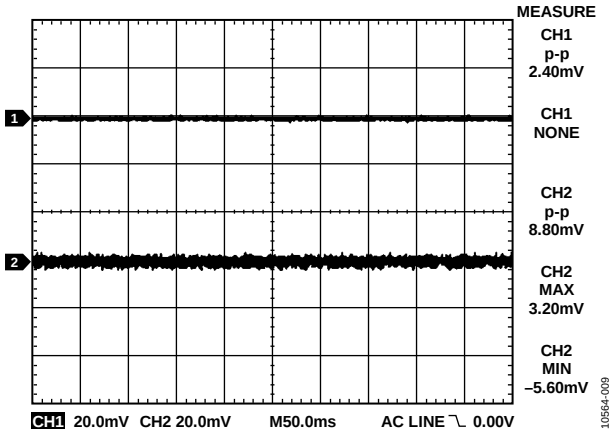

Figure 8. Noise at Input (CH1) and Output (CH2) of HART Filter with 12 mA Output Current

Analog Rate of Change

This specification ensures that when a device regulates current, the maximum rate of change of analog current does not interfere with HART communications. Step changes in current disrupt HART signaling. The same test circuit shown in Figure 6 was used. For this test, the AD5420 was programmed to output a cyclic waveform, switching from 4 mA to 20 mA with no delay at either value, to ensure the maximum rate of change. To meet the HART specifications, the waveform at the output of the filter must not exhibit a peak voltage greater than 150 mV. Meeting this requirement ensures that the maximum bandwidth of the analog signaling is within the specified dc to 25 Hz frequency band.

The normal time for the output of the AD5420 to change from 4 mA to 20 mA is about 10 µs. This is obviously too fast and would cause major disruption to a HART network. To reduce the rate of change, the AD5420 employs two features: connecting capacitors at the CAP1 and CAP2 pins, and an internal digital slew rate control function (refer to the AD5420 data sheet for details).

It requires very large capacitor values at CAP1 and CAP2 to reduce the bandwidth below 25 Hz. The optimum solution is to use a combination of the external capacitors and the digital slew rate control function of the AD5420. The two capacitors, C1 and C2, have the effect of reducing the rate of change of the analog signal; however, not sufficiently enough to meet the specification. Enabling the slew rate control feature offers the flexibility to set the rate of change.

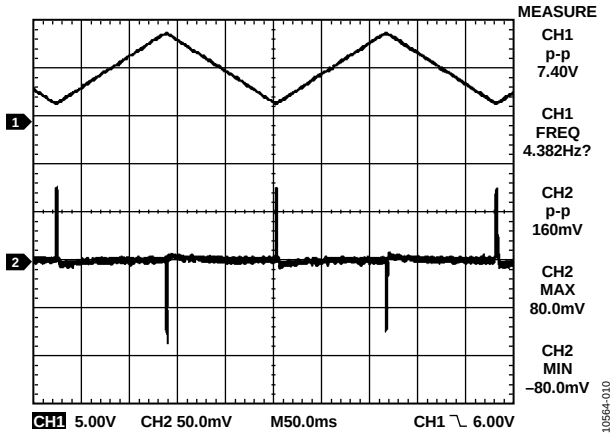

Figure 9. AD5420 Output (CH1) and HART Filter Output (CH2), SR Clock = 3, SR Step = 2, C1 = 4.7 nF, C2 = NC

Figure 9 shows the output of the AD5420 and the output of the HART filter. The peak voltage at the output of the filter is within specification at 80 mV. The slew rate settings are SR CLOCK = 3 and SR STEP = 2, setting the transition time from 4 mA to 20 mA at approximately 120 ms. C1 is 4.7 nF and C2 is unconnected. If this rate of change is too slow, the slew time can be reduced. However, this has the effect of increasing the peak voltage at the output of the filter. The capacitor connected from CAP1 to AV_{DD} can be used to counteract this.

Figure 10 shows the results of changing the slew rate control settings to SR CLOCK = 5 and SR STEP = 2, while leaving the C1 capacitor value unchanged at 4.7 nF. This results in a transition time of approximately 240 ms. The peak amplitude at the output of the filter can be reduced further by increasing the value of C1, configuring a slower slew rate, or a combination of both.

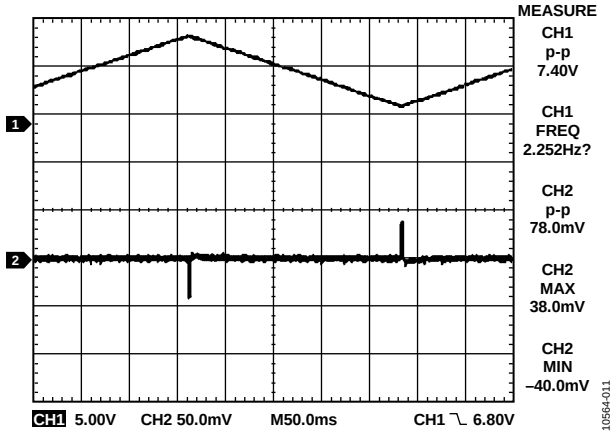

Figure 10. AD5420 Output (CH1) and HART Filter Output (CH2), SR Clock = 5, SR Step = 2, C1 = 4.7 nF, C2 = NC

Transient Voltage Protection

The AD5420 contains ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5420 from excessively high voltage transients, external power diodes and a surge current limiting resistor may be required, as shown in Figure 1. The constraint on the resistor value, (shown in Figure 1 as 18 Ω), is that during normal operation, the output level at I_{OUT} must remain within its voltage compliance limit of AV_{DD} − 2.5 V, and the two protection diodes and resistor must have appropriate power ratings. With 18 Ω, for a 4 mA to 20 mA output, the compliance limit at the terminal is decreased by $V = I_{MAX} \times R = 0.36$ V. Further protection can be provided with transient voltage suppressors (TVS) or transorbs. These are available as both unidirectional and bidirectional suppressors, and in a wide range of standoff and breakdown voltage ratings. Size the TVS with the lowest breakdown voltage possible while not conducting in the functional range of the current output. It is recommended that all remotely connected nodes be protected.

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. The *i*Coupler family of products from Analog Devices, Inc., provides voltage isolation in excess of 2.5 kV. Further information on *i*Coupler products is available at www.analog.com/icouplers. To reduce the number of isolators required, nonessential signals, such as CLEAR, can be connected to GND; $\overline{\text{FAULT}}$ and SDO can be left unconnected, reducing the isolation requirements to only three signals. However, note that either $\overline{\text{FAULT}}$ or SDO are required to provide access to the fault detection features of the AD5420.

COMMON VARIATIONS

A common variation on the circuit shown in Figure 1 is to use the AD5422 (LFCSP version), which is similar to the AD5420, but has a voltage output channel as well as a current output channel, and is therefore a popular choice in PLC/DCS type applications. Circuit Note CN-0065 provides extra information on an IEC 61000 compliant solution for a fully isolated output module using the AD5422 and the ADuM1401 digital isolator.

Circuit Note CN-0233 contains information on providing power and data isolation using the ADuM3471 PWM controller and transformer driver with quad-channel isolators. Circuit Note CN-0278 and Circuit Note CN-0321 both feature HART solutions using the AD5422 and AD5700. These devices have voltage and current output capability.

If multiple channels are required, the AD5755-1 quad voltage and current output DAC may be used. This product has innovative on-chip dynamic power control that minimizes package power dissipation in current mode. Each channel has a corresponding C_{HART} pin so that HART signals can be coupled to the current output of the AD5755-1.

The AD5421 and the AD5700 HART modem can be combined if the requirement is a loop-powered 4 mA to 20 mA HART solution. This circuit is detailed in Circuit Note CN-0267 and is available as an evaluation board.

CIRCUIT EVALUATION AND TEST

The circuit was tested using the EVAL-CN0270-EB1Z circuit board. The Analog Devices J-Link OB emulator (USB-SWD/UART-EMUZ) is used to interface the evaluation board to a PC running the evaluation software. The test setup is shown on Figure 11.

Equipment Needed

The following equipment is needed:

- CN-0270 evaluation board (EVAL-CN0270-EB1Z)
- CN-0270 evaluation board software (ftp://ftp.analog.com/pub/cftl/CN0270/)
- J-Link OB emulator (USB-SWD/UART-EMUZ) included with EVAL-CN0270-EB1Z.
- PC running Windows® XP or higher with USB port
- 10.8 V to 36 V power supply
- Digital test filter (HCF_TOOL-31 available from the HART Communication Foundation)
- Load resistor, 500 Ω
- Oscilloscope, Tektronix DS1012B or equivalent

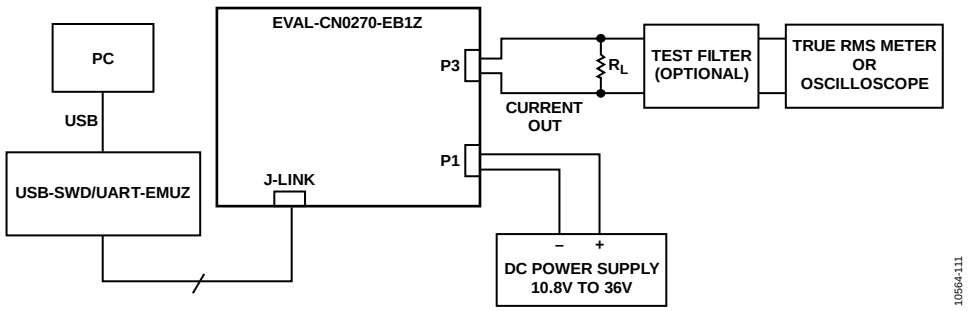

Figure 11. Test Setup Block Diagram

For the output noise during silence tests, as described previously, the AD5700 modem was not transmitting (silent). The AD5420 was set to output the required current and passed through the HCF (HART Communication Foundation) band-pass filter. The output noise was then measured using a Tektronix TDS1012B oscilloscope.

The analog rate of change specification ensures that when the AD5420 regulates current, the maximum rate of change of analog current does not interfere with HART communications. Step changes in current disrupt HART signaling.

For this test, the AD5420 was programmed to output a cyclic waveform switching from 4 mA to 20 mA with no delay at either value to ensure the maximum rate of change. The slew rate settings used were SR CLOCK = 3 and SR STEP = 2, with C1 set to 4.7 nF and C2 open circuit. Measurements were also completed whereby the slew rate was reduced even further by changing the SR CLOCK setting to 5 rather than 3 and leaving all other settings and component values unchanged.

Details of the software operation can be found in the CN-0270 Software User Guide.

LEARN MORE

CN0270 Design Support Package:
http://www.analog.com/CN0270-DesignSupport

Maurice Egan, *Configuring the AD5420 for HART Communication Compliance*, Application Note AN-1065, Analog Devices.

HART Communication Foundation

Data Sheets and Evaluation Boards

AD5420 Data Sheet and Evaluation Board

AD5700 Data Sheet and Evaluation Board

AD5700-1 Data Sheet and Evaluation Board

REVISION HISTORY

7/14—Rev. A to Rev. B

Changes to Figure 1 1
Changes to Figure 6 4
Changes to Common Variations Section, Circuit Evaluation and Test Section, and Figure 11 6

5/12—Rev. 0 to Rev. A

Changes to Circuit Function and Benefits Section 1
Changes to Circuit Description Section 2
Changes to Common Variations 6

4/12—Revision 0: Initial Version