

# NLX1G97

## Configurable Multifunction Gate

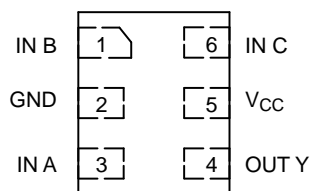
The NLX1G97 MiniGate™ is an advanced high-speed CMOS multifunction gate. The device allows the user to choose logic functions MUX, AND, OR, NAND, NOR, INVERT and BUFFER. The device has Schmitt-trigger inputs, thereby enhancing noise immunity.

The NLX1G97 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

### Features

- High Speed:  $t_{PD} = 3.3 \text{ ns}$  (Typ) @  $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 1 \mu\text{A}$  (Maximum) at  $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These are Pb-Free Devices

### PIN ASSIGNMENTS



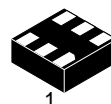
(Top View)



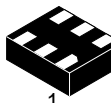
**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)

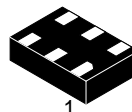
### MARKING DIAGRAMS



ULLGA6  
1.0 x 1.0  
CASE 613AD



ULLGA6  
1.2 x 1.0  
CASE 613AE



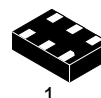
ULLGA6  
1.45 x 1.0  
CASE 613AF



UDFN6  
1.0 x 1.0  
CASE 517BX



UDFN6  
1.2 x 1.0  
CASE 517AA



UDFN6  
1.45 x 1.0  
CASE 517AQ



F = Specific Device Code  
M = Date Code

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NLX1G97

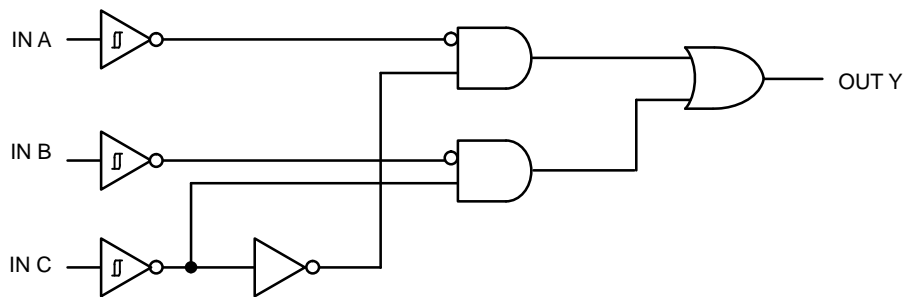


Figure 1. Function Diagram

PIN ASSIGNMENT

1	IN B
2	GND
3	IN A
4	OUT Y
5	V <sub>CC</sub>
6	IN C

FUNCTION TABLE\*

Input			Output
A	B	C	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	H
H	H	L	H
H	H	H	H

\*To select a logic function, please refer to “Logic Configurations section”.

LOGIC CONFIGURATIONS

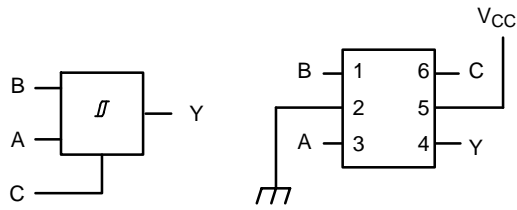


Figure 2. 2-Input MUX

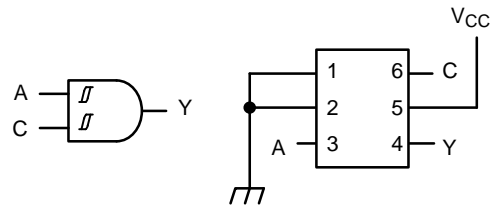


Figure 3. 2-Input AND (When B = "L")

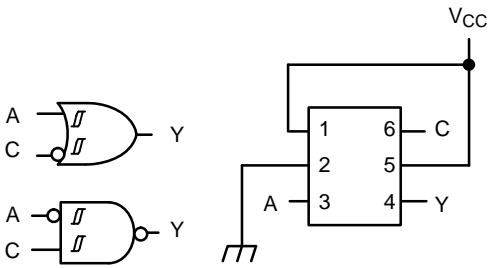


Figure 4. 2-Input OR with Input C Inverted (When B = "H")

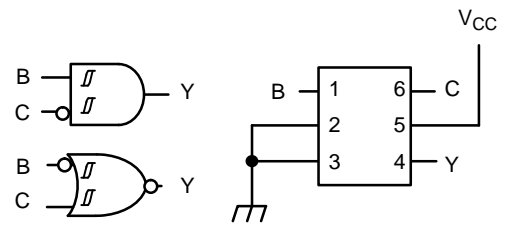


Figure 5. 2-Input AND with Input C Inverted (When A = "L")

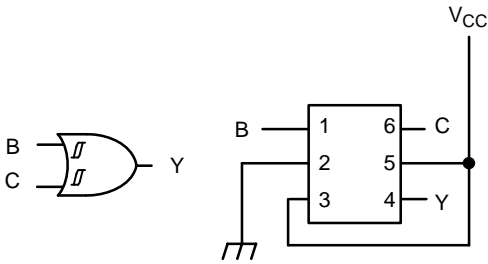


Figure 6. 2-Input OR (When A = "H")

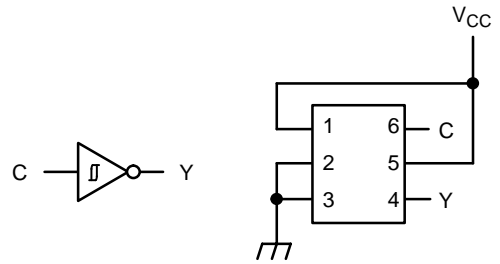


Figure 7. Inverter (When A = "L" and B = "H")

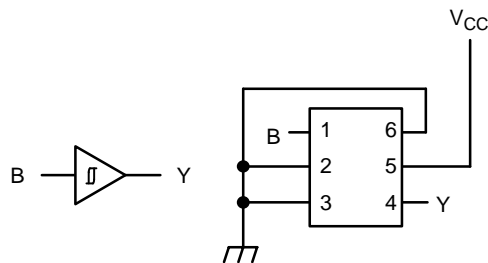


Figure 8. Buffer (When A = C = "L")

# NLX1G97

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0	V
$V_{IN}$	DC Input Voltage	-0.5 to +7.0	V
$V_{OUT}$	DC Output Voltage	-0.5 to +7.0	V
$I_{IK}$	DC Input Diode Current $V_{IN} < GND$	-50	mA
$I_{OK}$	DC Output Diode Current $V_{OUT} < GND$	-50	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$	mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$	mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
$T_J$	Junction Temperature Under Bias	150	°C
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V
$I_{LATCHUP}$	Latchup Performance Above $V_{CC}$ and Below GND at 125°C (Note 5)	$\pm 500$	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage	1.65	5.5	V
$V_{IN}$	Digital Input Voltage	0	5.5	V
$V_{OUT}$	Output Voltage	0	5.5	V
$T_A$	Operating Free-Air Temperature	-55	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	0 0 0	No Limit No Limit No Limit	nS/V

# NLX1G97

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ +85°C		T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V <sub>T+</sub>	Positive Threshold Voltage		1.65	0.79		1.16		1.16		1.16	V
			2.3	1.11		1.56		1.56		1.56	
			3.0	1.5		1.87		1.87		1.87	
			4.5	2.16		2.74		2.74		2.74	
			5.5	2.61		3.33		3.33		3.33	
V <sub>T-</sub>	Negative Threshold Voltage		1.65	0.35		0.62	0.35		0.35		V
			2.3	0.58		0.87	0.58		0.58		
			3.0	0.84		1.19	0.84		0.84		
			4.5	1.41		1.9	1.41		1.41		
			5.5	1.78		2.29	1.78		1.78		
V <sub>H</sub>	Hysteresis Voltage		1.65	0.30		0.62	0.30	0.62	0.30	0.62	V
			2.3	0.40		0.8	0.40	0.8	0.40	0.8	
			3.0	0.53		0.87	0.53	0.87	0.53	0.87	
			4.5	0.71		1.04	0.71	1.04	0.71	1.04	
			5.5	0.8		1.2	0.8	1.2	0.8	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> = V <sub>T-MIN</sub> or V <sub>T+MAX</sub> I <sub>OH</sub> = -50 μA	1.65 – 5.5	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1		V <sub>CC</sub> – 0.1		V
		V <sub>IN</sub> = V <sub>T-MIN</sub> or V <sub>T+MAX</sub>									
		I <sub>OH</sub> = -4 mA	1.65	1.2			1.2		1.2		
		I <sub>OH</sub> = -8 mA	2.3	1.9			1.9		1.9		
		I <sub>OH</sub> = -16 mA	3.0	2.4			2.4		2.4		
		I <sub>OH</sub> = -24 mA	3.0	2.3			2.3		2.3		
		I <sub>OH</sub> = -32 mA	4.5	3.8			3.8		3.8		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>T-MIN</sub> or V <sub>T+MAX</sub> I <sub>OL</sub> = 50 μA	1.65 – 5.5			0.1		0.1		0.1	V
		V <sub>IN</sub> = V <sub>T-MIN</sub> or V <sub>T+MAX</sub>									
		I <sub>OL</sub> = 4 mA	1.65			0.45		0.45		0.45	
		I <sub>OL</sub> = 8 mA	2.3			0.3		0.3		0.3	
		I <sub>OL</sub> = 16 mA	3.0			0.4		0.4		0.4	
		I <sub>OL</sub> = 24 mA	3.0			0.55		0.55		0.55	
		I <sub>OL</sub> = 32 mA	4.5			0.55		0.55		0.55	
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5 V	0 to 5.5			±0.1		±1.0		±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			1.0		10		10	μA

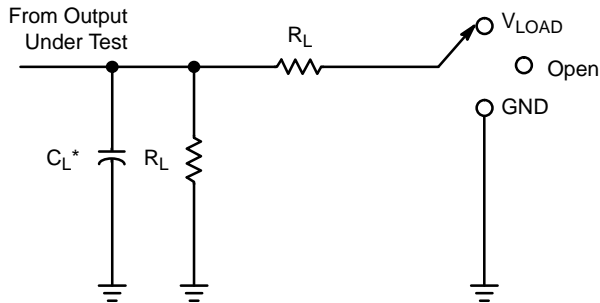
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r = t_f = 3.0$  ns)

Symbol	Parameter	$V_{CC}$ (V)	Test Condition	$T_A = 25^\circ\text{C}$			$T_A \leq +85^\circ\text{C}$		$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay, Any Input to Output Y (See Test Circuit)	1.65 – 1.95		3.2	8.6	14.4	3.2	14.4	3.2	14.4	ns
		2.3 – 2.7		2.0	5.1	8.3	2.0	8.3	2.0	8.3	
		3.0 – 3.6		1.5	3.9	6.3	1.5	6.3	1.5	6.3	
		4.5 – 5.5		1.1	3.3	5.1	1.1	5.1	1.1	5.1	
$C_{IN}$	Input Capacitance				3.5						pF
$C_{PD}$	Power Dissipation Capacitance (Note 6)	5.0	$f = 10$ MHz		22						pF

6.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$ .  $C_{PD}$  is used to determine the no-load dynamic power consumption:  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

**TEST CIRCUIT AND VOLTAGE WAVEFORMS**



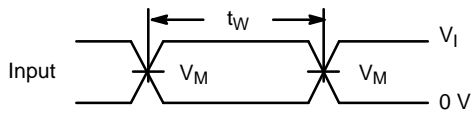
Test	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

\* $C_L$  includes probes and jig capacitance.

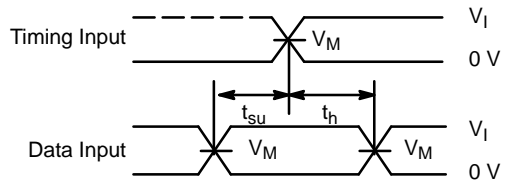
**Figure 9. Load Circuit**

$V_{CC}$	Inputs		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_A$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5.5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V

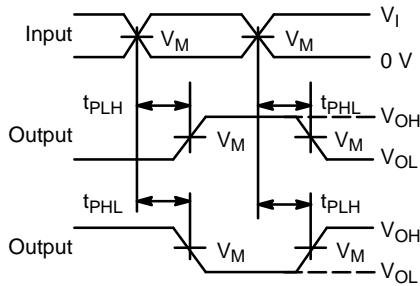
# NLX1G97



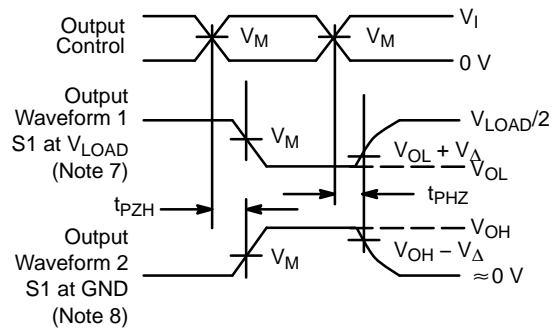
**Figure 10. Voltage Waveforms Pulse Duration**



**Figure 11. Voltage Waveforms Setup and Hold Times**



**Figure 12. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs**



**Figure 13. Voltage Waveforms Enable and Disable Times Low- and High-Level Enabling**

7. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
8. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
9. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ .
10. The outputs are measured one at a time, with one transition per measurement.
11. All parameters are waveforms are not applicable to all devices.

## ORDERING INFORMATION

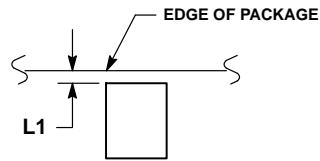
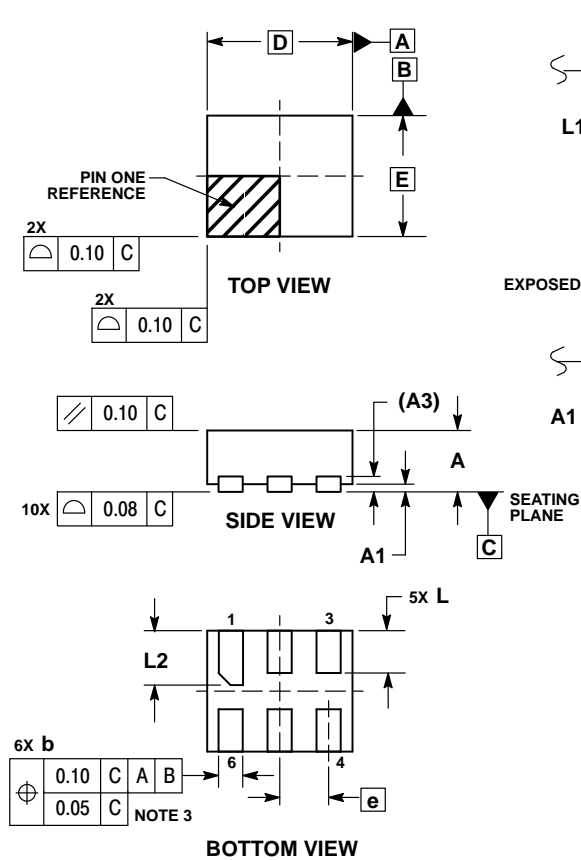
Device	Package	Shipping†
NLX1G97AMX1TCG	ULLGA6 – 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G97BMX1TCG	ULLGA6 – 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G97CMX1TCG	ULLGA6 – 0.35P (Pb-Free)	3000 / Tape & Reel
NLX1G97MUTCG	UDFN6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G97AMUTCG (In Development)	UDFN6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G97CMUTCG (In Development)	UDFN6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

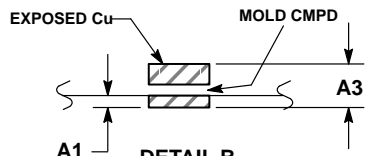
# NLX1G97

## PACKAGE DIMENSIONS

UDFN6 1.2x1.0, 0.4P  
CASE 517AA  
ISSUE O



**DETAIL A**  
Bottom View  
(Optional)

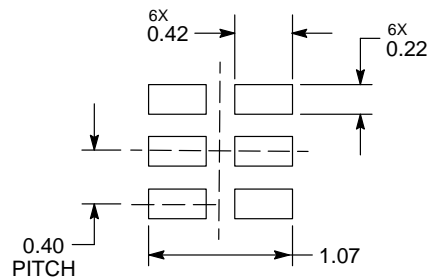


**DETAIL B**  
Side View  
(Optional)

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
  4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.15	0.25
D	1.20	BSC
E	1.00	BSC
e	0.40	BSC
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50

### MOUNTING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

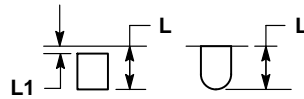
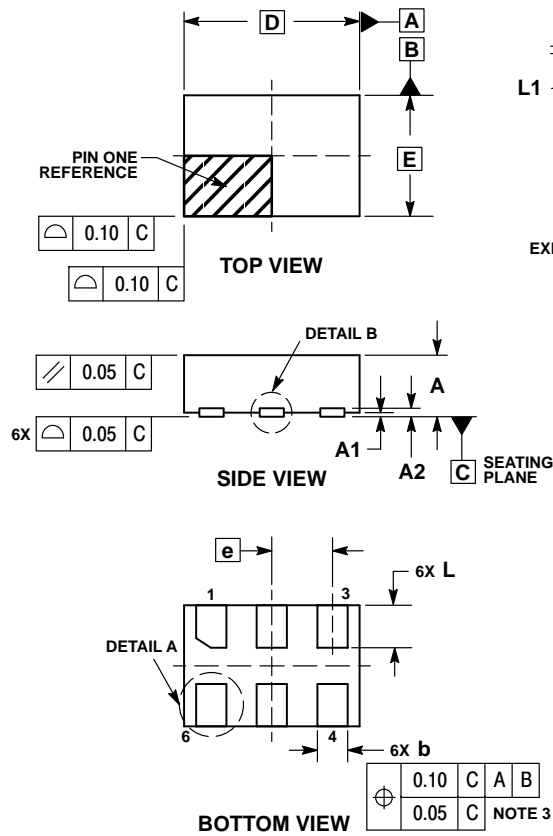
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



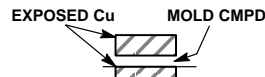
# NLX1G97

## PACKAGE DIMENSIONS

UDFN6 1.45x1.0, 0.5P  
CASE 517AQ  
ISSUE O



**DETAIL A**  
OPTIONAL  
CONSTRUCTIONS



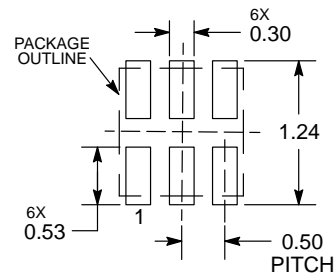
**DETAIL B**  
OPTIONAL  
CONSTRUCTIONS

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	—	0.15

### MOUNTING FOOTPRINT



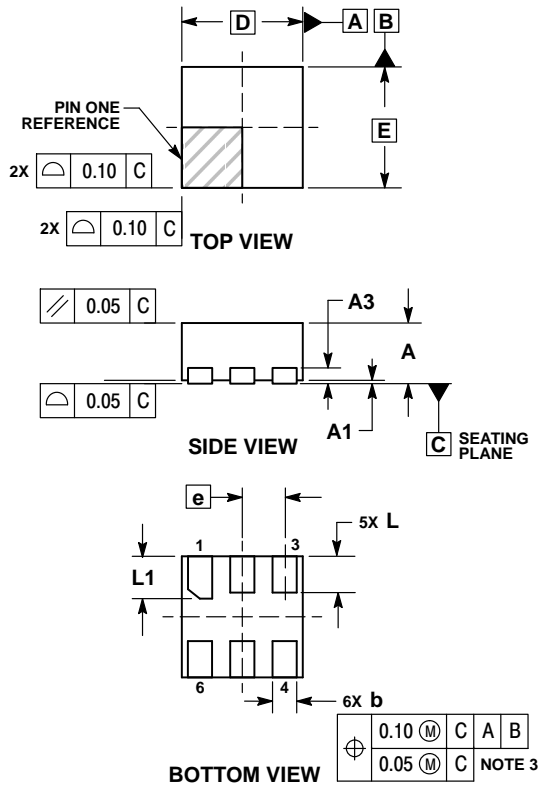
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NLX1G97

## PACKAGE DIMENSIONS

UDFN6 1.0x1.0, 0.35P  
CASE 517BX  
ISSUE O

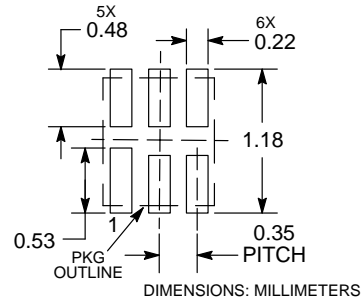


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.12	0.22
D	1.00	BSC
E	1.00	BSC
e	0.35	BSC
L	0.25	0.35
L1	0.30	0.40

### RECOMMENDED SOLDERING FOOTPRINT\*

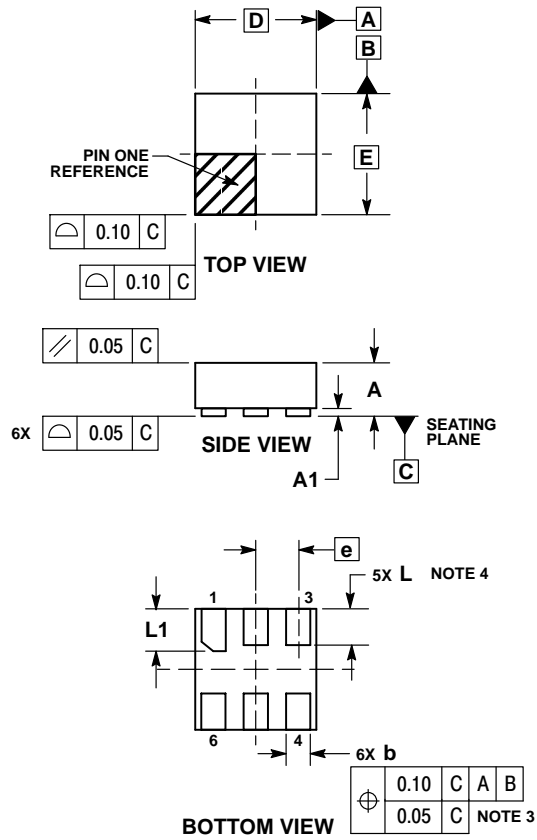


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NLX1G97

## PACKAGE DIMENSIONS

ULLGA6 1.0x1.0, 0.35P  
CASE 613AD  
ISSUE A

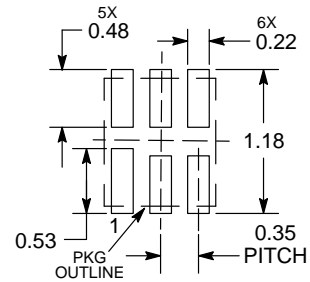


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

### MOUNTING FOOTPRINT SOLDERMASK DEFINED\*



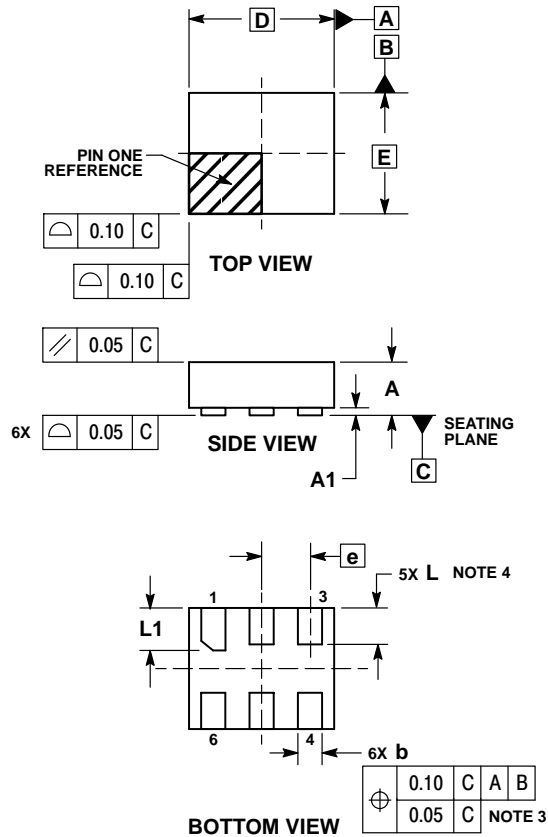
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NLX1G97

## PACKAGE DIMENSIONS

ULLGA6 1.2x1.0, 0.4P  
CASE 613AE  
ISSUE A

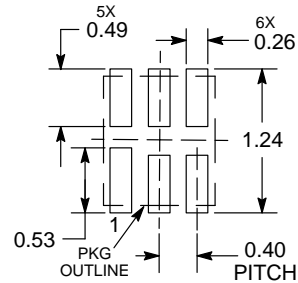


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.35	0.45

### MOUNTING FOOTPRINT SOLDERMASK DEFINED\*



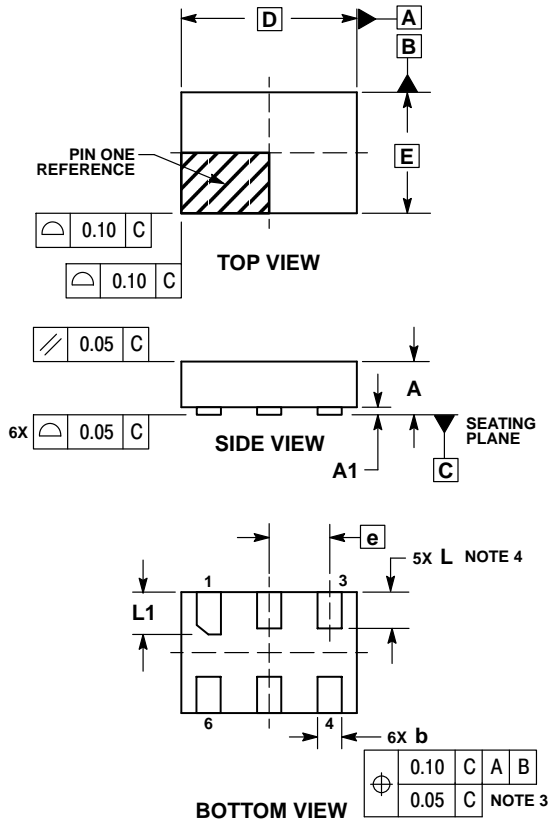
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NLX1G97

## PACKAGE DIMENSIONS

ULLGA6 1.45x1.0, 0.5P  
CASE 613AF  
ISSUE A

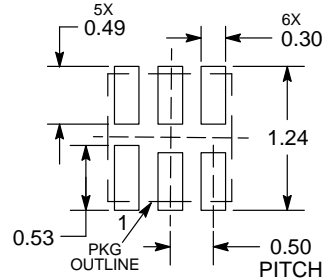


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	0.00	0.05
A1	0.15	0.25
b	1.45 BSC	
D	1.00 BSC	
E	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

### MOUNTING FOOTPRINT SOLDERMASK DEFINED\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

MiniGate is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marketing.pdf](http://www.onsemi.com/site/pdf/Patent-Marketing.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

NLX1G97/D