IMY120R036AM2H

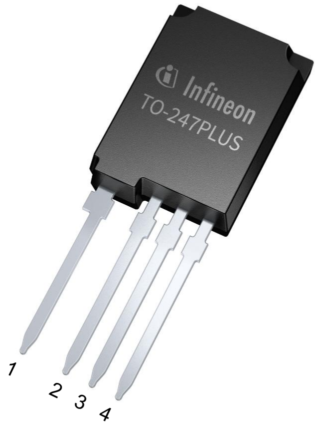
CoolSiC™ Hybrid Discrete

Final datasheet

CoolSiC™ Hybrid Discrete : CoolSiC™ 1200 V SiC MOSFET G2 co-packed with soft, fast recovery Emitter Controlled 7 diode for reverse-polarity protection

Features

- V_{DSS} = 1200 V at T_{vj} = 25°C
- I_{DDC} = 31 A at T_C = 100°C
- $R_{DS(on)}$ = 36 mΩ at V_{GS} = 18 V, T_{vj} = 25°C
- Reverse-polarity protection diode with I_F = 76 A at T_c = 100°C
- Very low switching losses
- Optimized for MPPT boost converter in solar applications
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.2 V
- Robust against parasitic turn on, 0 V turn-off gate voltage can be applied
- Soft and low Q_{rr} diode with V_F = 1.6 V at T_c = 175°C
- Suitable Infineon gate drivers can be found under https://www.infineon.com/gdfinder



Halogen-free

Green

Lead-free

RoHS

Potential applications

- String inverter

Product validation

- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

Pin definition:

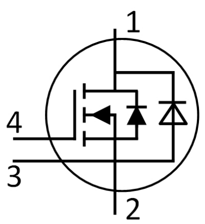
1 – Drain

2 – Source

3 – Kelvin sense contact

4 – Gate

Note: the source and sense pins are not exchangeable, their exchange might lead to malfunction (only for 4pin, TO263-7L)



Type	Package	Marking
IMY120R036AM2H	PG-TO247-4-U10	12M2HA036

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1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}	Wave soldering 1.6 mm (0.063 in.) from case for 10 s			260	°C
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W
MOSFET thermal resistance, junction-case	$R_{th(j-c)}$			0.67	0.87	K/W
Reverse-polarity protection diode thermal resistance, junction-case	$R_{th(j-c)}$			0.31	0.42	K/W
Comparative Tracking Index	*CTI*	IEC 60112 (material group 1 according to IEC 60664-1)	600			V

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	$V_{GS} = 18$ V	$T_c = 25$ °C	44	A
			$T_c = 100$ °C	31	
Peak drain current, t_p limited by $T_{vj(max)}$ [1)]	I_{DM}	$V_{GS} = 18$ V		155	A
Gate-source voltage, max. transient voltage[2)]	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$		-10...25	V
Gate-source voltage, max. static voltage	V_{GS}			-7...23	V
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		$T_c = 25$ °C	171	W
			$T_c = 100$ °C	86	

1) Verified by design
2) The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		15...18	V
Recommended turn-off gate voltage	$V_{GS(off)}$		-5...0	V

Table 4 **Characteristic values**

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 18.2 A	T_{vj} = 25 °C, $V_{GS(on)}$ = 18 V		36	45	mΩ
			T_{vj} = 150 °C, $V_{GS(on)}$ = 18 V		77		
			T_{vj} = 175 °C, $V_{GS(on)}$ = 18 V		89		
			T_{vj} = 25 °C, $V_{GS(on)}$ = 15 V		47		
Gate-source threshold voltage	$V_{GS(th)}$	I_D = 5.7 mA, $V_{DS} = V_{GS}$ (tested after 1 ms pulse at V_{GS} = 20 V)	T_{vj} = 25 °C	3.5	4.2	5.1	V
			T_{vj} = 175 °C		3.2		
Zero gate-voltage drain current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	T_{vj} = 25 °C			170	µA
			T_{vj} = 175 °C		930		
Gate leakage current	I_{GSS}	V_{DS} = 0 V	V_{GS} = 23 V			120	nA
			V_{GS} = -10 V			-120	
Forward transconductance	g_{fs}	I_D = 18.2 A, V_{DS} = 20 V			13.9		S
Internal gate resistance	$R_{G,int}$	f = 1 MHz, V_{AC} = 25 mV			1.8		Ω
Input capacitance	C_{iss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			1473		pF
Output capacitance	C_{oss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			84		pF
Reverse transfer capacitance	C_{rss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			3.5		pF
C_{oss} stored energy	E_{oss}	Calculated based on $C_{oss} = f(V_{DD})$			34		µJ
Output charge	Q_{oss}	Calculated based on $C_{oss} = f(V_{DD})$			116		nC
Effective output capacitance, energy related	$C_{o(er)}$	V_{DS} = 0...800 V, V_{GS} = 0 V, Calculated based on E_{oss}			106		pF
Effective output capacitance, time related	$C_{o(tr)}$	I_D = constant, V_{DS} = 0...800 V, V_{GS} = 0 V, Calculated based on Q_{oss}			146		pF
Total gate charge	Q_G	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = 0/18 V, turn-on pulse			37		nC
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = 0/18 V, turn-on pulse			8.5		nC
Gate-drain charge	Q_{GD}	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = 0/18 V, turn-on pulse			8.2		nC
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.8 Ω, L_σ = 12 nH	T_{vj} = 25 °C		11.2		ns
			T_{vj} = 175 °C		10.8		

(table continues...)

Table 4 (continued) Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Rise time	t_r	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.8 Ω, L_σ = 12 nH	T_{vj} = 25 °C		7.6		ns
			T_{vj} = 175 °C		8		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.8 Ω, L_σ = 12 nH	T_{vj} = 25 °C		18		ns
			T_{vj} = 175 °C		20		
Fall time	t_f	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.8 Ω, L_σ = 12 nH	T_{vj} = 25 °C		12.8		ns
			T_{vj} = 175 °C		12.8		
Turn-on energy	E_{on}	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.8 Ω, L_σ = 12 nH	T_{vj} = 25 °C		154		µJ
			T_{vj} = 175 °C		155		
Turn-off energy	E_{off}	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.8 Ω, L_σ = 12 nH	T_{vj} = 25 °C		33		µJ
			T_{vj} = 175 °C		37		
Total switching energy	E_{tot}	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.8 Ω, L_σ = 12 nH	T_{vj} = 25 °C		187		µJ
			T_{vj} = 175 °C		192		
Turn-on energy at -5 V	E_{on}	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.8 Ω, L_σ = 12 nH	T_{vj} = 25 °C		144		µJ
			T_{vj} = 175 °C		143		
Turn-off energy at -5 V	E_{off}	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.8 Ω, L_σ = 12 nH	T_{vj} = 25 °C		33		µJ
			T_{vj} = 175 °C		38		
Total switching energy at -5 V	E_{tot}	V_{DD} = 800 V, I_D = 18.2 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.8 Ω, L_σ = 12 nH	T_{vj} = 25 °C		177		µJ
			T_{vj} = 175 °C		181		
Virtual junction temperature	T_{vj}			-40		175	°C

***Note**:* *Characteristics at T_{vj} = 25°C, unless otherwise specified.*
Dynamic test circuit see Figure F, 2nd device SiC Schottky diode IDWD20G120C5.

3 Reverse-polarity protection diode

Table 5 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Diode forward current, limited by T_{vjmax}	I_F	limited by bondwire	T_c = 25 °C	98	A
			T_c = 100 °C	76	

(table continues...)

Table 5 (continued) Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Diode pulsed current, t_p limited by T_{vjmax}	I_{Fpulse}			225	A
Power dissipation	P_{tot}		T_c = 25 °C	356	W
			T_c = 100 °C	178	

Table 6 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Diode forward voltage	V_F	I_F = 75 A	T_{vj} = 25 °C		1.65	2.15	V
			T_{vj} = 175 °C		1.6		
Diode reverse recovery charge	Q_{rr}	I_F = 18.2 A, V_{DD} = 800 V, $R_{G,ext}$ = 2.8 Ω, Opposite MOSFET V_{GS} = 0/18 V, Q_{rr} includes also Q_C	T_{vj} = 25 °C		2.9		µC
			T_{vj} = 175 °C		7.4		
Diode peak reverse recovery current	I_{rrm}	I_F = 18.2 A, V_{DD} = 800 V, $R_{G,ext}$ = 2.8 Ω, Opposite MOSFET V_{GS} = 0/18 V	T_{vj} = 25 °C		116		A
			T_{vj} = 175 °C		158		
Diode reverse recovery energy	E_{rec}	I_F = 18.2 A, V_{DD} = 800 V, $R_{G,ext}$ = 2.8 Ω, Opposite MOSFET V_{GS} = 0/18 V, Q_{rr} includes also Q_C	T_{vj} = 25 °C		1.7		mJ
			T_{vj} = 175 °C		4.6		
Virtual junction temperature	T_{vj}			-40		175	°C

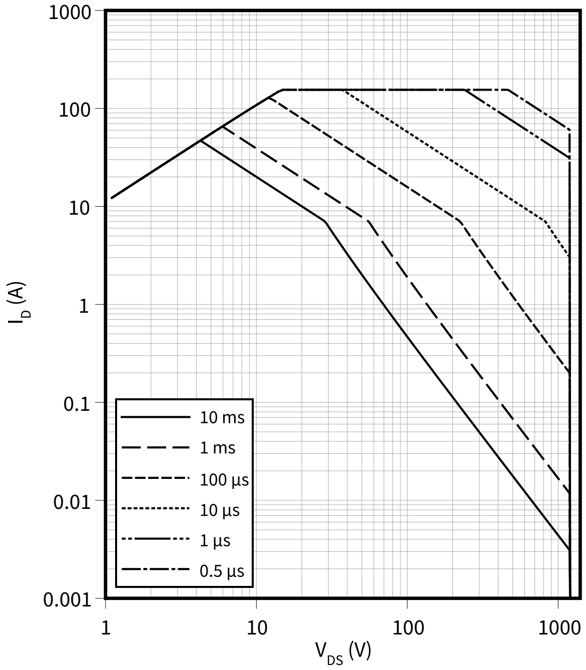
***Note**: Dynamic test circuit see Figure G, 2nd device: reverse-polarity protection co-packed diode, V_{GS} = 0 V.*

4 Characteristics diagrams

Safe operating area (SOA)

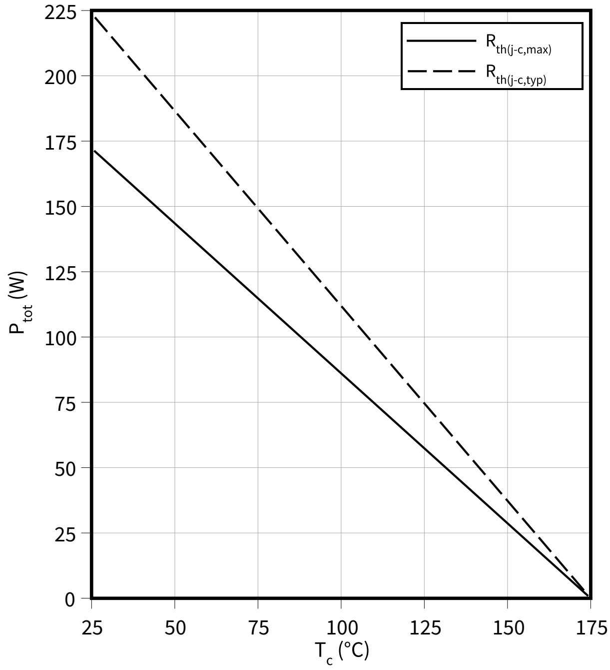
$I_D = f(V_{DS})$

$T_{vj} \le 175$ °C, $T_c = 25$ °C



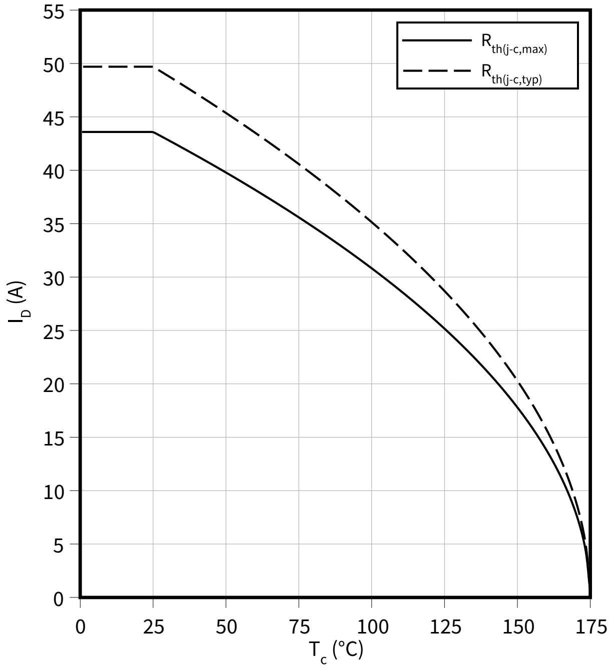
Power dissipation as a function of case temperature limited by bond wire

$P_{tot} = f(T_c)$



Maximum DC drain to source current as a function of case temperature limited by bond wire

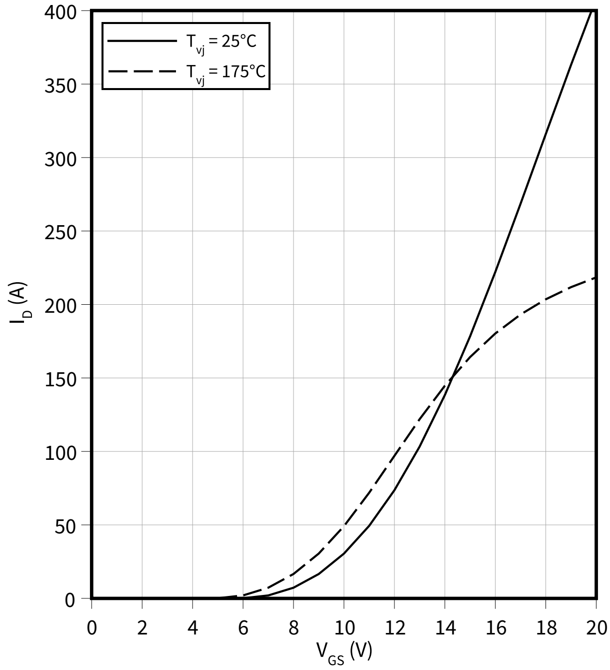
$I_D = f(T_c)$



Typical transfer characteristic

$I_D = f(V_{GS})$

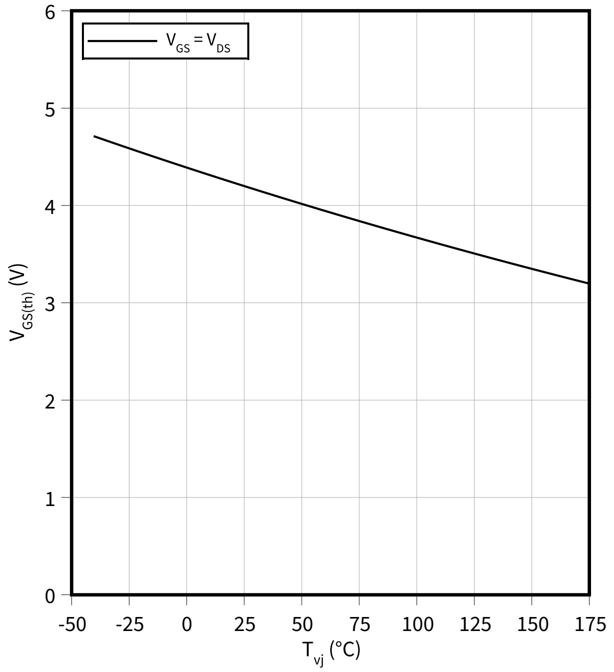
$V_{DS} = 20$ V, $t_p = 20$ µs



Typical gate-source threshold voltage as a function of junction temperature

$V_{GS(th)} = f(T_{vj})$

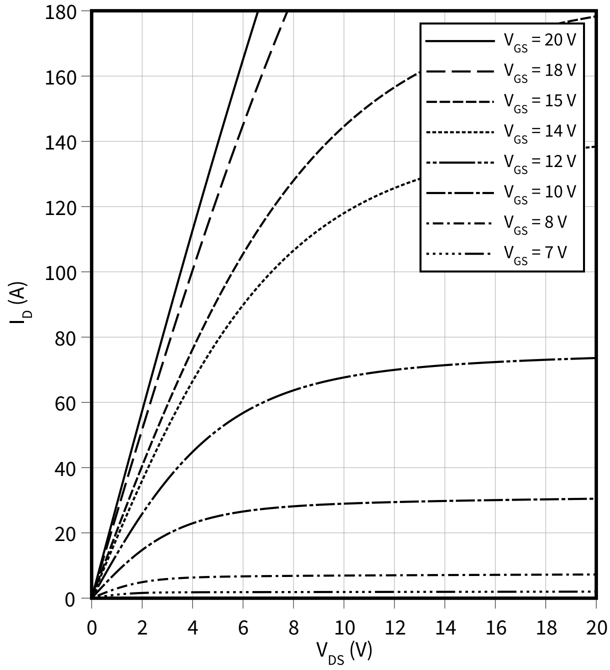
$I_D = 5.7$ mA



Typical output characteristic, V_{GS} as a parameter

$I_D = f(V_{DS})$

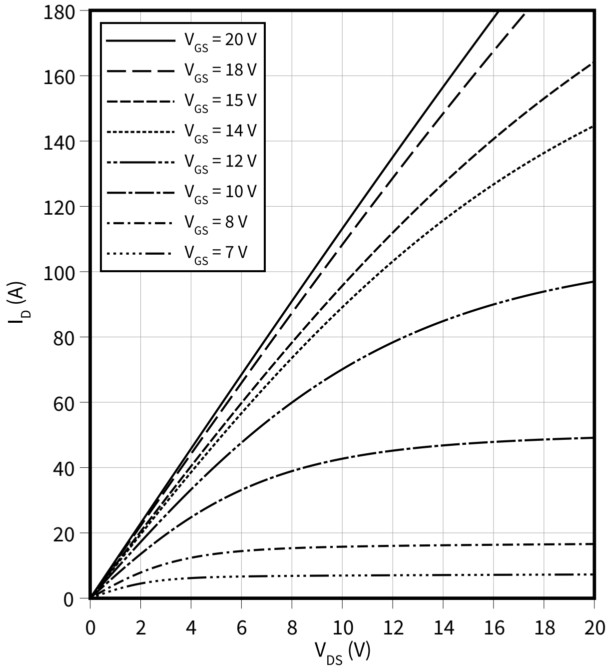
$T_{vj} = 25$ °C, $t_p = 20$ µs



Typical output characteristic, V_{GS} as a parameter

$I_D = f(V_{DS})$

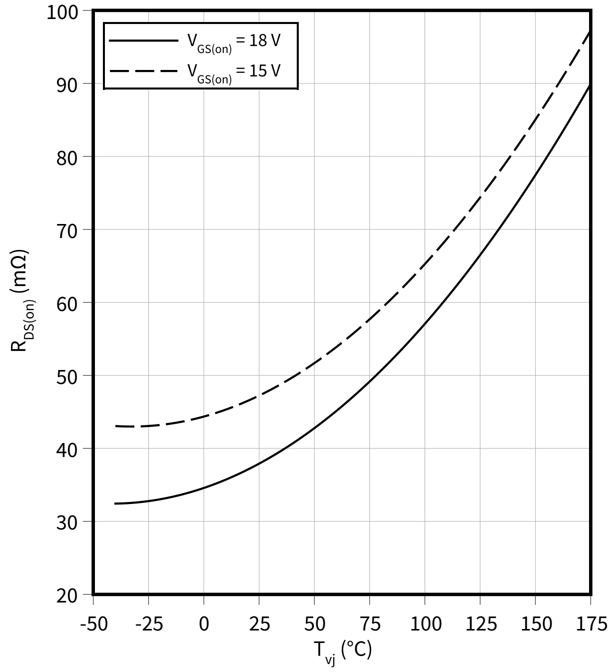
$T_{vj} = 175$ °C, $t_p = 20$ µs



Typical on-state resistance as a function of junction temperature

$R_{DS(on)} = f(T_{vj})$

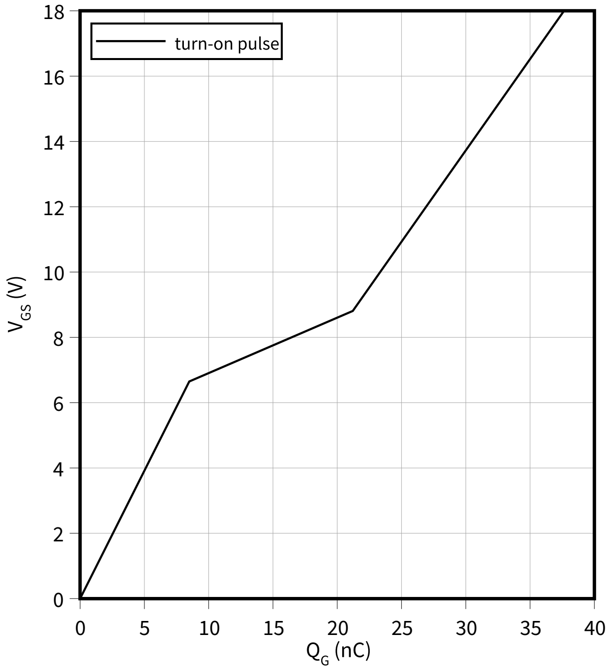
$I_D = 18.2$ A



Typical gate charge

$V_{GS} = f(Q_G)$

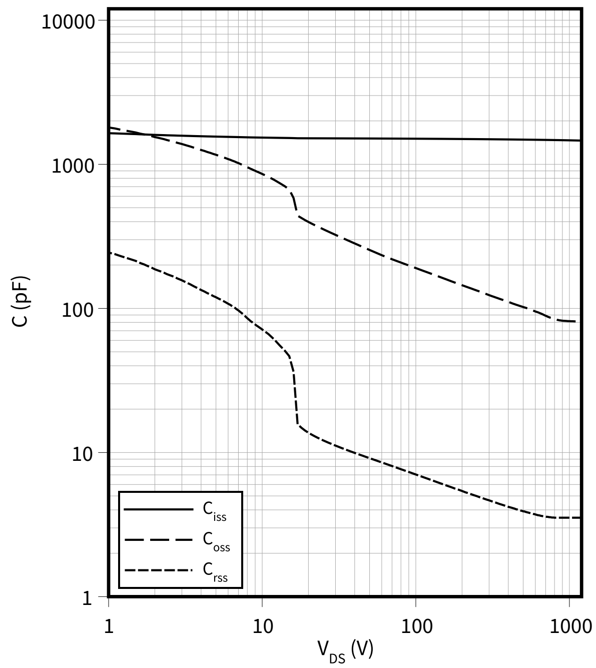
$I_D = 18.2$ A, $V_{DS} = 800$ V



Typical capacitance as a function of drain-source voltage

$C = f(V_{DS})$

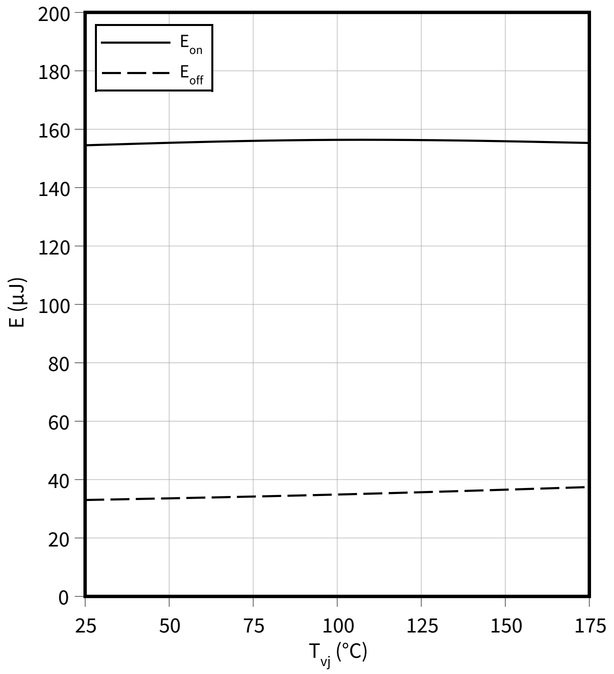
$f = 100$ kHz, $V_{GS} = 0$ V



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device external SiC diode

$E = f(T_{vj})$

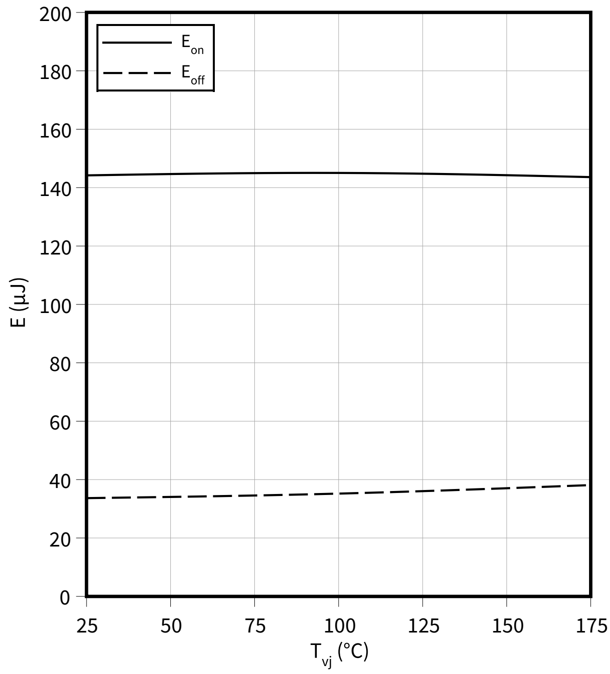
$V_{GS} = 0/18$ V, $I_D = 18.2$ A, $R_{G,ext} = 2.8\ \Omega$, $V_{DD} = 800$ V



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device external SiC diode

$E = f(T_{vj})$

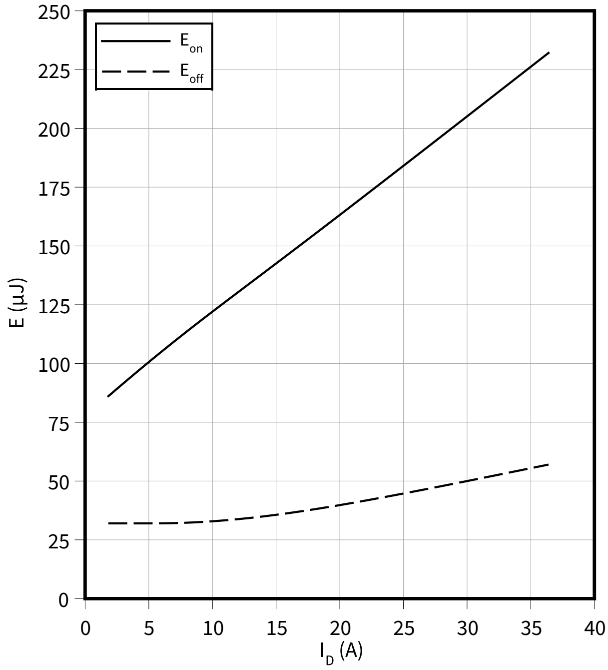
$V_{GS} = -5/18$ V, $I_D = 18.2$ A, $R_{G,ext} = 2.8\ \Omega$, $V_{DD} = 800$ V



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device external SiC diode

$E = f(I_D)$

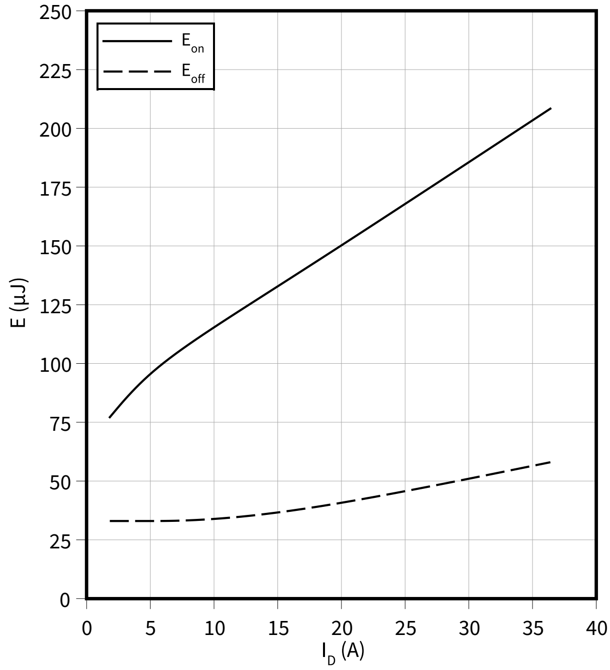
V_{GS} = 0/18 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2.8 Ω, V_{DD} = 800 V



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device external SiC diode

$E = f(I_D)$

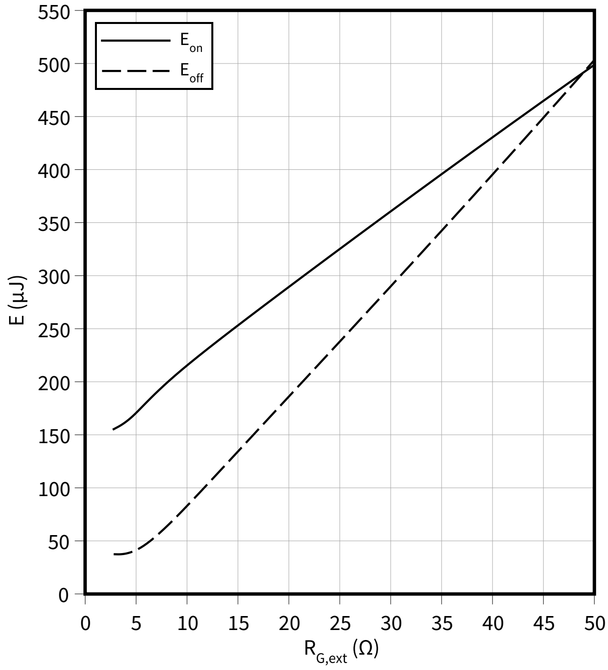
V_{GS} = -5/18 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2.8 Ω, V_{DD} = 800 V



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device external SiC diode

$E = f(R_{G,ext})$

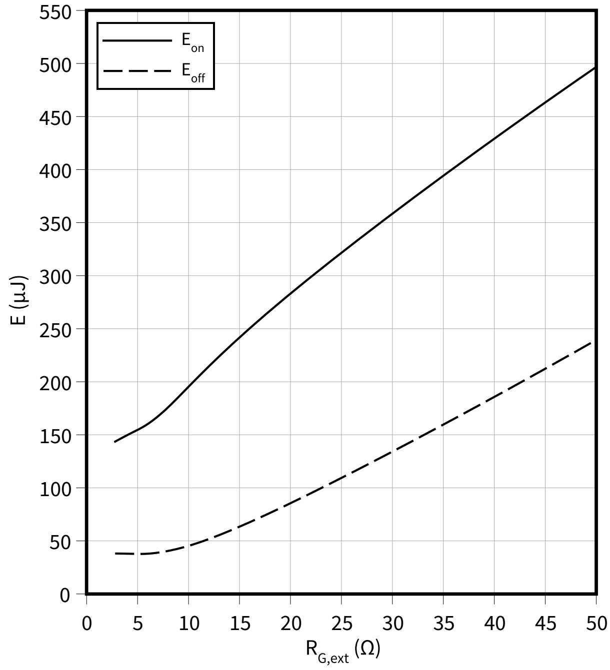
V_{GS} = 0/18 V, I_D = 18.2 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device external SiC diode

$E = f(R_{G,ext})$

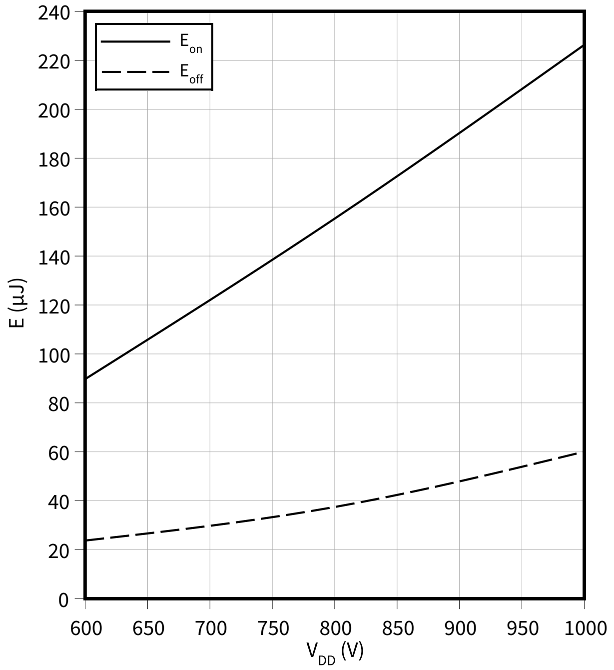
V_{GS} = -5/18 V, I_D = 18.2 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching energy as a function of DC link voltage, test circuit in Fig. F, 2nd device external SiC diode

$E = f(V_{DD})$

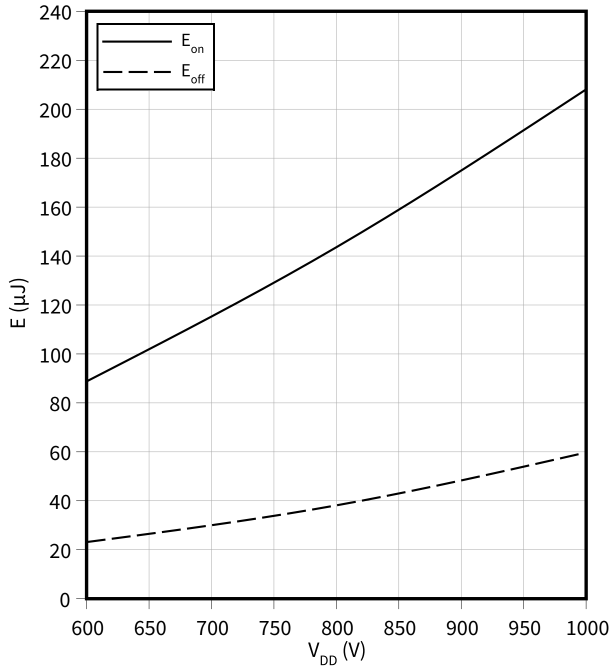
V_{GS} = 0/18 V, I_D = 18.2 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.8 Ω



Typical switching energy as a function of DC link voltage, test circuit in Fig. F, 2nd device external SiC diode

$E = f(V_{DD})$

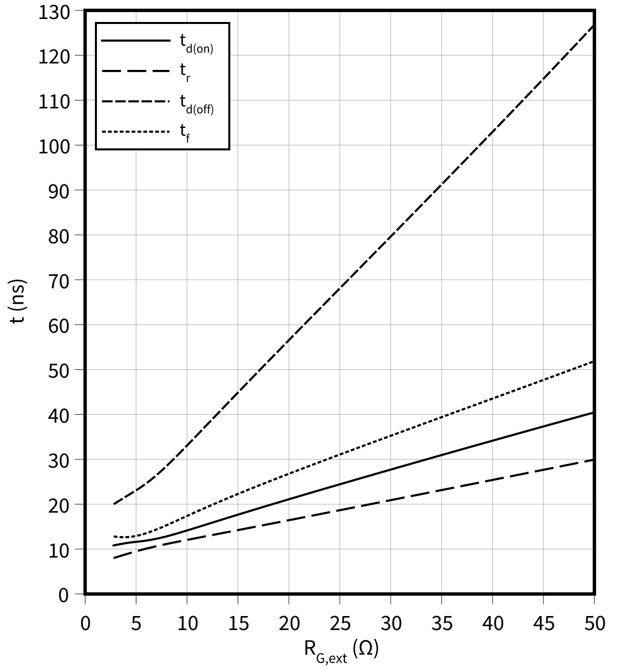
V_{GS} = -5/18 V, I_D = 18.2 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.8 Ω



Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device external SiC diode

$t = f(R_{G,ext})$

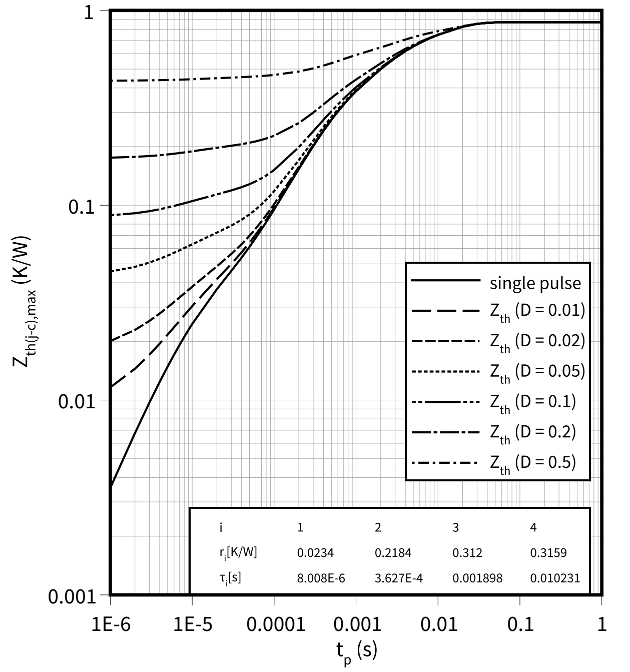
V_{GS} = 0/18 V, I_D = 18.2 A, T_{vj} = 175 °C, V_{DD} = 800 V



Max. transient thermal impedance (MOSFET)

$Z_{th(j-c),max} = f(t_p)$

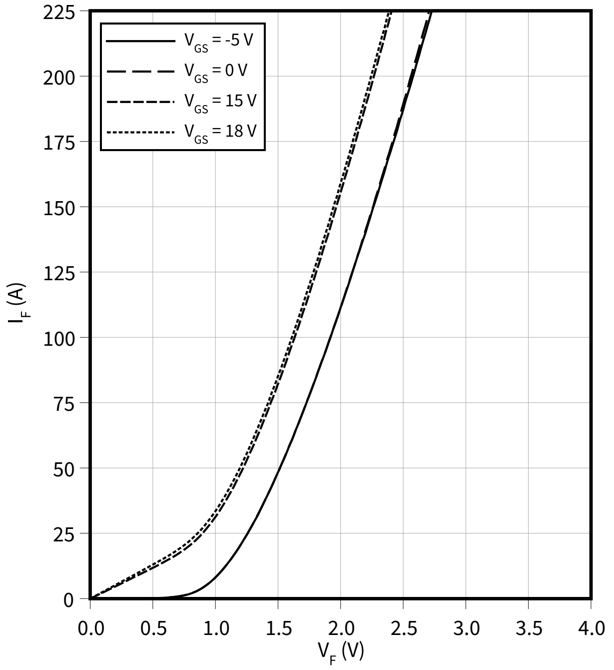
$D = t_p/T$



Typical diode forward current as a function of forward voltage, V_{GS} as a parameter

$I_F = f(V_F)$

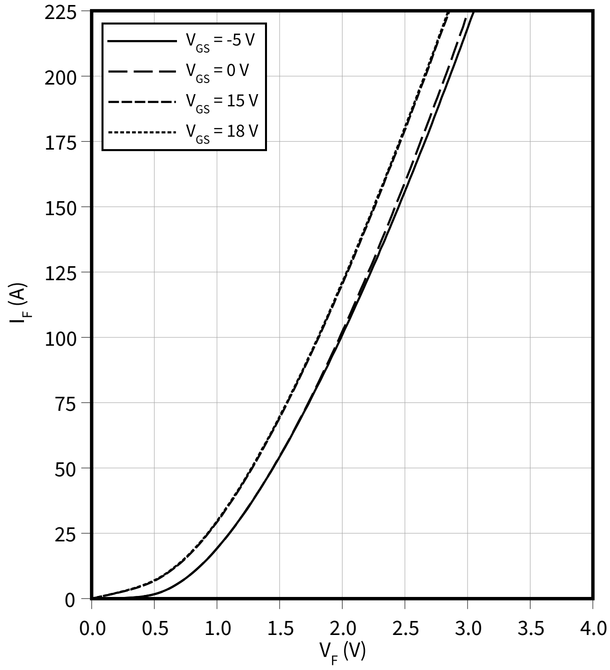
$t_p = 20\ \mu s$, $T_{vj} = 25\ °C$



Typical diode forward current as a function of forward voltage, V_{GS} as a parameter

$I_F = f(V_F)$

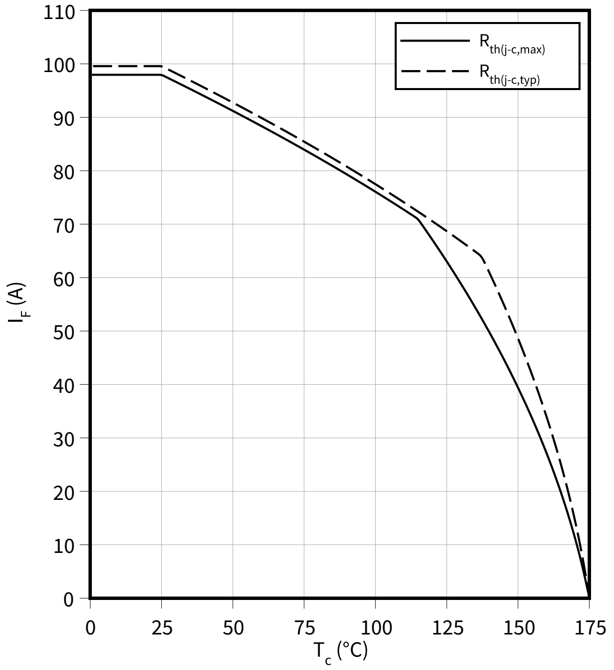
$t_p = 20\ \mu s$, $T_{vj} = 175\ °C$



Maximum diode forward current as a function of case temperature limited by bond wire

$I_F = f(T_c)$

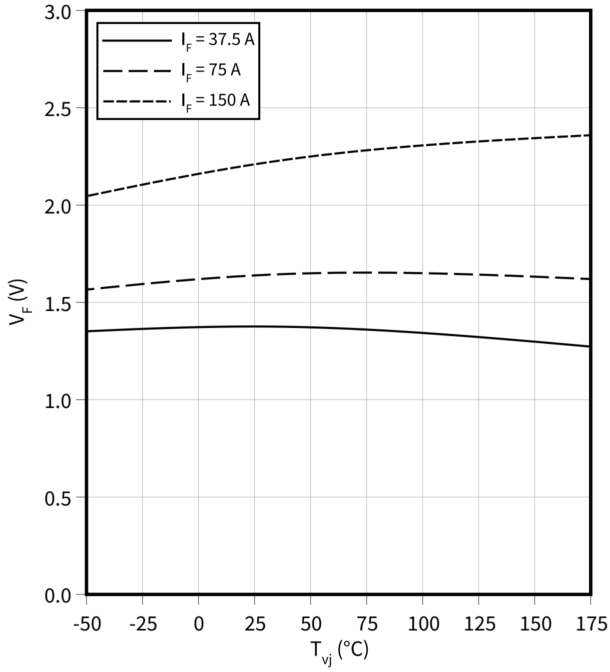
$V_{GS} = 0\ V$



Typical diode forward voltage as function of junction temperature

$V_F = f(T_{vj})$

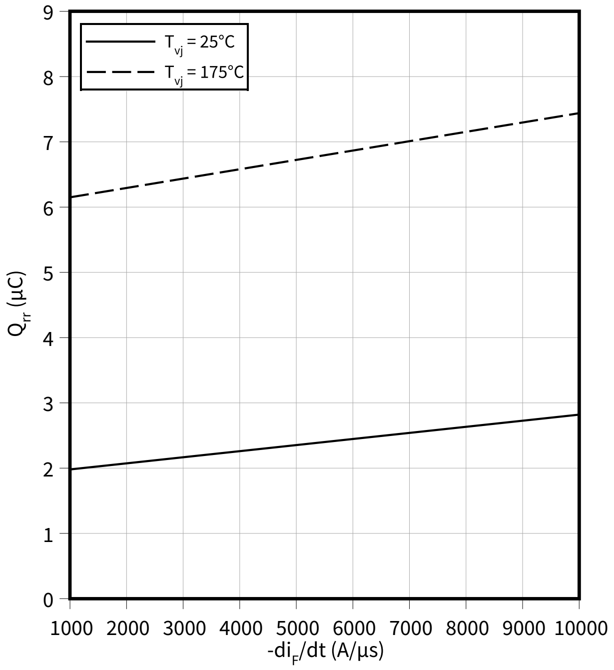
$V_{GS} = 0\ V$



Typical reverse recovery charge as function of diode current slope, test circuit in Fig. G, 2nd device reverse-polarity protection co-packed diode

$Q_{rr} = f(-di_F/dt)$

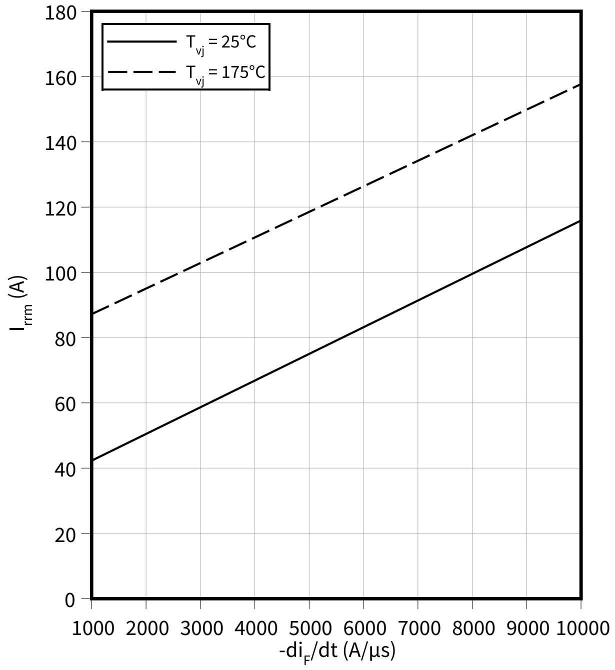
$V_{GS} = 0/18$ V, $V_{DD} = 800$ V, $I_F = 18.2$ A



Typical reverse recovery current as function of diode current slope, test circuit in Fig. G, 2nd device reverse-polarity protection co-packed diode

$I_{rrm} = f(-di_F/dt)$

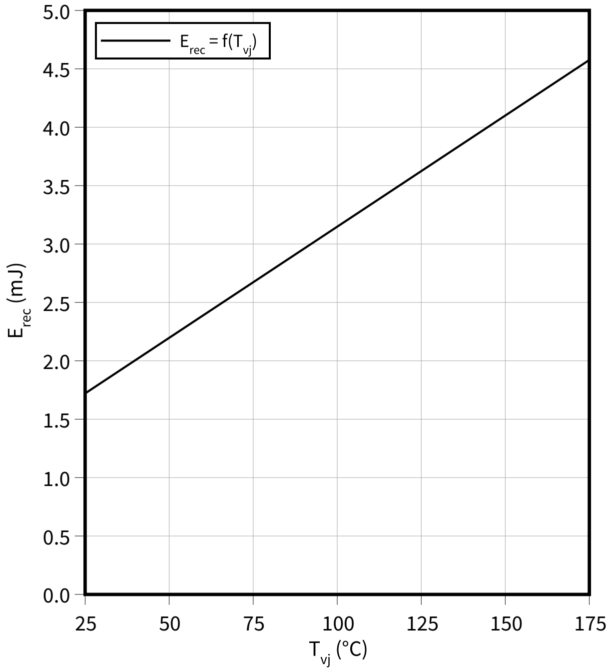
$V_{GS} = 0/18$ V, $V_{DD} = 800$ V, $I_F = 18.2$ A



Typical reverse energy losses as function of junction temperature, test circuit in Fig. G, 2nd device reverse-polarity protection co-packed diode

$E_{rec} = f(T_{vj})$

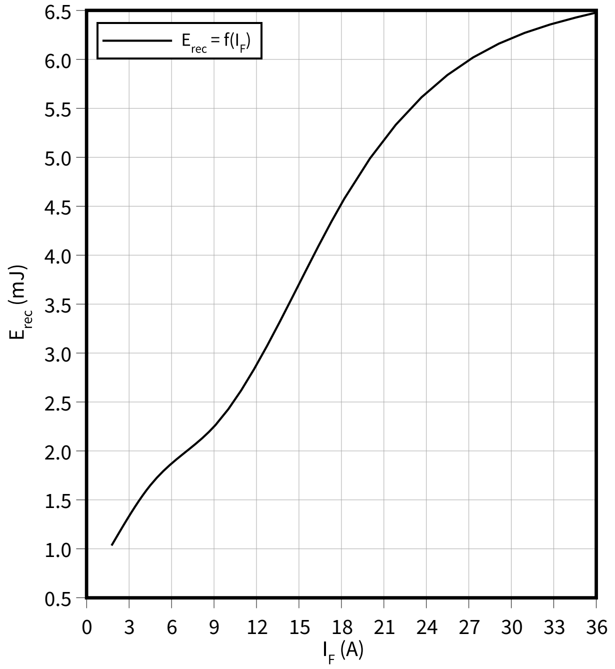
$V_{GS} = 0/18$ V, $R_{G,ext} = 2.8$ Ω, $V_{DD} = 800$ V, $I_F = 18.2$ A



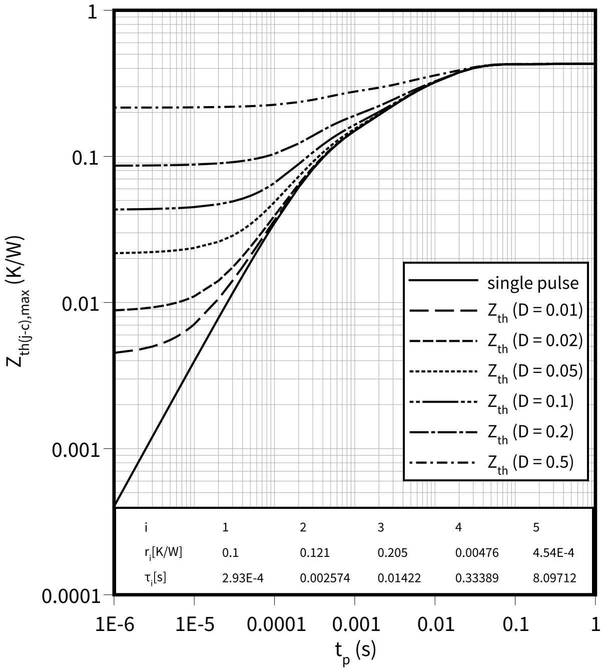
Typical reverse energy losses as function of diode current, test circuit in Fig. G, 2nd device reverse-polarity protection co-packed diode

$E_{rec} = f(I_F)$

$V_{GS} = 0/18$ V, $T_{vj} = 175$ °C, $R_{G,ext} = 2.8$ Ω, $V_{DD} = 800$ V

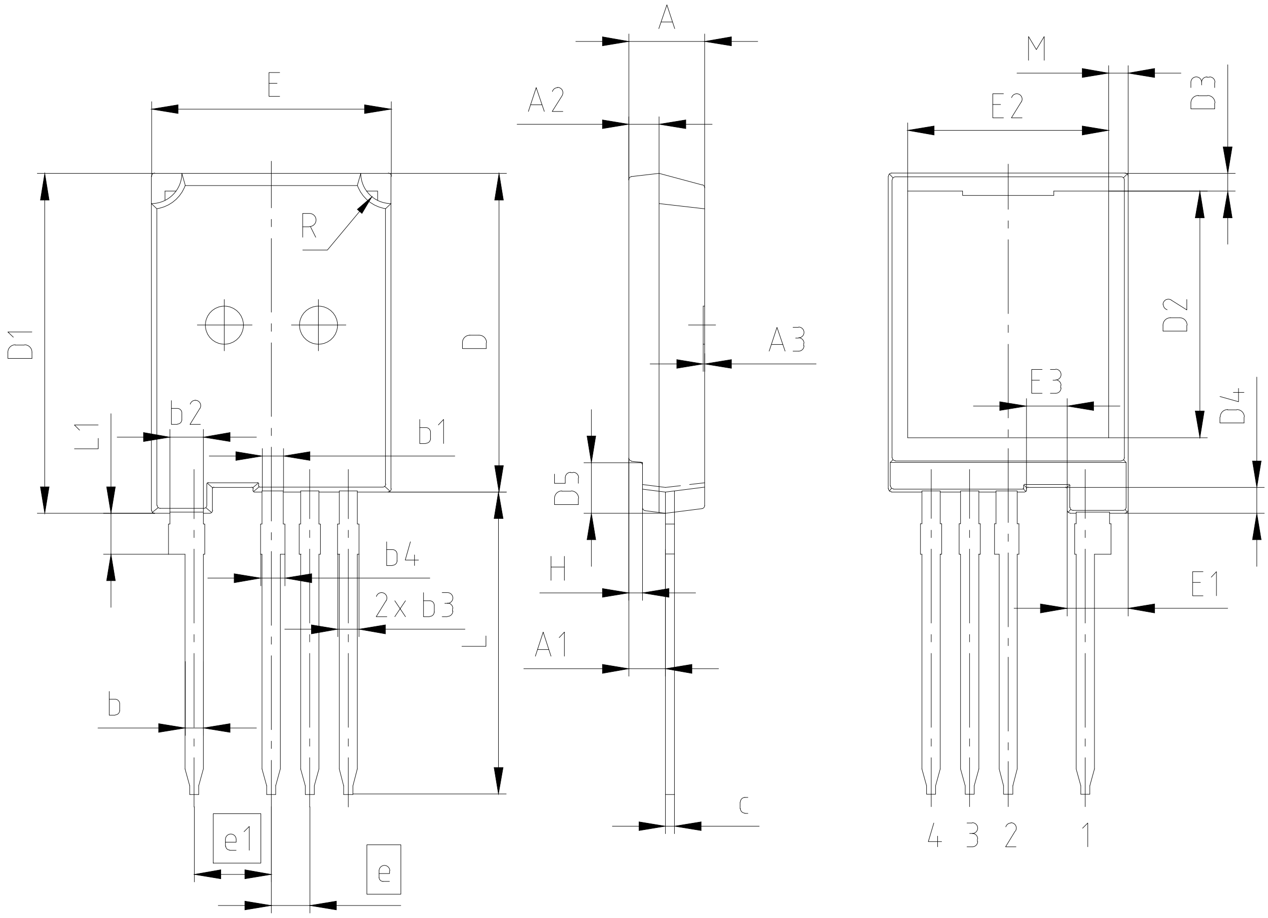


Max. transient thermal impedance (protection diode) $Z_{th(j\text{-}c),max} = f(t_p)$ $D = t_p/T$	



i	1	2	3	4	5
r_i[K/W]	0.1	0.121	0.205	0.00476	4.54E-4
τ_i[s]	2.93E-4	0.002574	0.01422	0.33389	8.09712

5 Package outlines



NOTES:
PACKAGE SURFACE ROUTE BETWEEN PIN 1 & PIN 2 WILL BE 5.1 mm MIN.
ALL b... AND c DIMENSIONS INCLUDING PLATING EXPECT AREA OF CUTTING

PACKAGE - GROUP NUMBER: **PG-TO247-4-U10**

DIMENSIONS	**MILLIMETERS**		**DIMENSIONS**	**MILLIMETERS**	
	MIN.	MAX.		MIN.	MAX.
A	4.90	5.10	**E**	15.70	15.90
A1	2.31	2.51	**E1**	3.90	4.10
A2	1.90	2.10	**E2**	13.10	13.50
b	1.16	1.29	**E3**	2.58	2.78
b1	1.36	1.49	**e**	2.54	
b2	2.16	2.29	**e1**	5.08	
b3	1.16	1.45	**H**	0.80	1.00
b4	1.16	1.65	**N**	4	
c	0.59	0.66	**L**	19.80	20.10
D	20.90	21.10	**L1**	2.55	2.85
D1	22.30	22.50	**M**	0.97	1.57
D2	15.95	16.55	**R**	1.90	2.10
D3	1.00	1.35			
D4	1.60	1.80			
D5	3.24	3.44			

Figure 1

6 Testing conditions

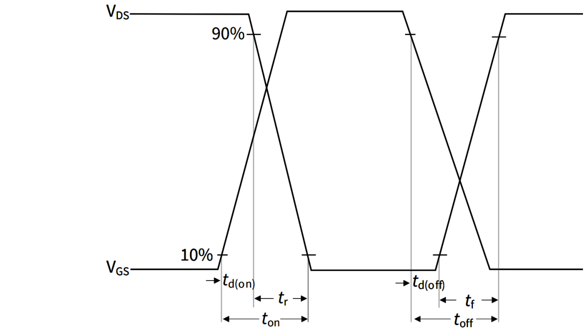


Figure A. **Definition of switching times**

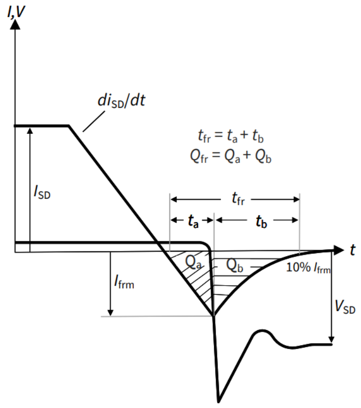


Figure B. **Definition of body diode switching characteristics**

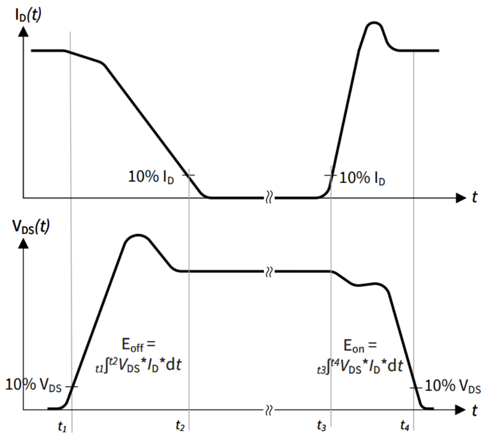


Figure C. **Definition of switching losses**

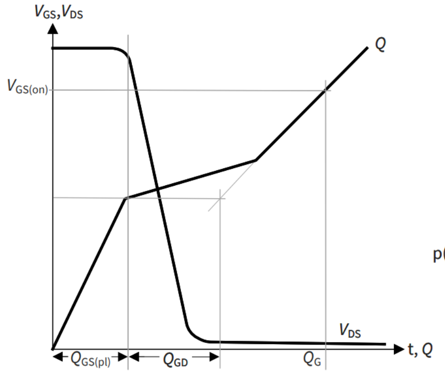


Figure D. **Definition of QGD**

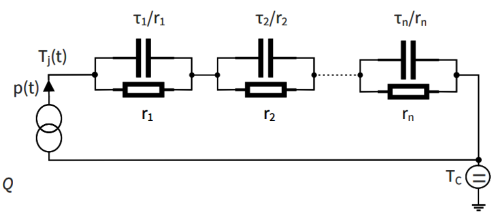


Figure E. **Thermal equivalent circuit**

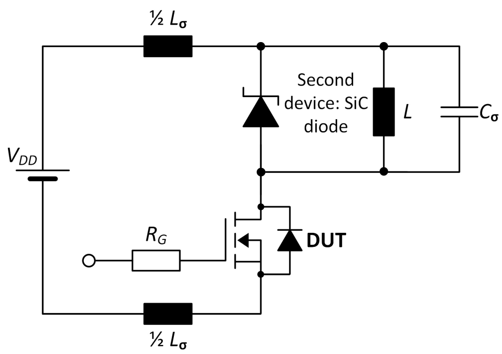


Figure F. **Dynamic test circuit for MOSFET**
Parasitic inductance L_σ
Parasitic capacitance C_σ

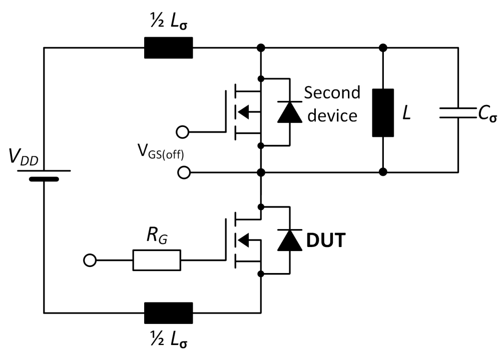


Figure G. **Dynamic test circuit for reverse -polarity protection diode**
Parasitic inductance L_σ
Parasitic capacitance C_σ

Figure 2

Revision history

Document revision	Date of release	Description of changes
0.10	2025-03-12	Target datasheet
0.20	2025-08-08	Preliminary datasheet
1.00	2025-11-20	Final datasheet

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