3.3V, PRECISION, 33MHz to 500MHz PROGRAMMABLE LVPECL AND LVDS BUS CLOCK SYNTHESIZER

Precision Edge®
SY89532L
SY89533L

FEATURES

- **Integrated synthesizer plus fanout buffers, clock drivers , and translator in a single 64-pin package**
- **3.3V ±10% power supply**
- **Low jitter: <50ps cycle-to-cycle**
- **Low pin-to-pin skew: <50ps**
- **33MHz to 500MHz output frequency range**
- **Direct interface to crystal: 14MHz to 18MHz**
- **LVPECL output (SY89532L), LVPECL/LVDS outputs (SY89533L)**
- **TTL/CMOS compatible control logic**
- **3 independently programmable output frequency banks:**
  - **9 differential output pairs @BankB (LVPECL/LVDS)**
  - **2 differential output pairs @BankA (LVPECL)**
  - **2 differential output pairs @BankC (LVPECL)**
- **ExtVCO input allows synthesizer and crystal interface to be bypassed**
- **Available in 64-pin EPAD-TQFP**

Precision Edge®

DESCRIPTION

The SY89532 and SY89533L programmable clock synthesizer/drivers are a 3.3V, high-frequency, precision PLL-based clock driver family optimized for multi-frequency, multi-processor server and synchronous computing applications that require the highest precision. These devices integrate the following blocks into a single monolithic IC:

- PLL (Phase-Lock-Loop)-based synthesizer
- Fanout buffers
- Clock generator (dividers)
- Logic translation (LVPECL, LVDS)

This level of integration minimizes the additive jitter and part-to-part skew associated with the discrete alternative, resulting in superior system-level timing as well as reduced board space and power. For applications that must interface to a reference clock, see the SY89534/5.

APPLICATIONS

- **Servers**
- **Workstations**
- **Parallel processor-based systems**
- **Other high-performance computing**
- **Communications**

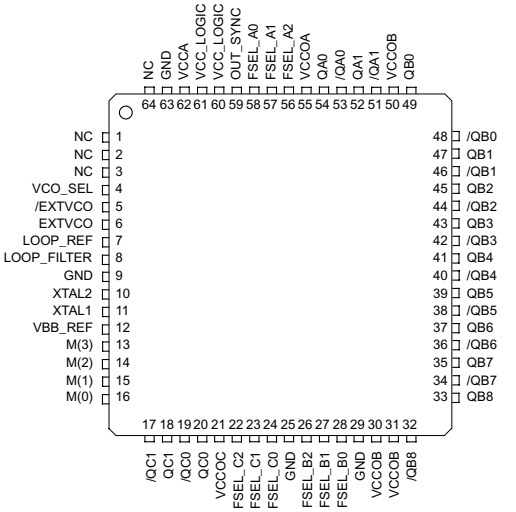
PRODUCT SELECTION GUIDE

	Input		Output		
Device	Crystal	Reference	BankA	BankB	BankC
SY89532L	X		LVPECL	LVPECL	LVPECL
SY89533L	X		LVPECL	LVDS	LVPECL
SY89534L[1]		X	LVPECL	LVPECL	LVPECL
SY89535L[1]		X	LVPECL	LVDS	LVPECL

Note:

1.Refer to SY89534/35L data sheet for details.

PACKAGE/ORDERING INFORMATION



64-Pin EPAD-TQFP (H64-1)

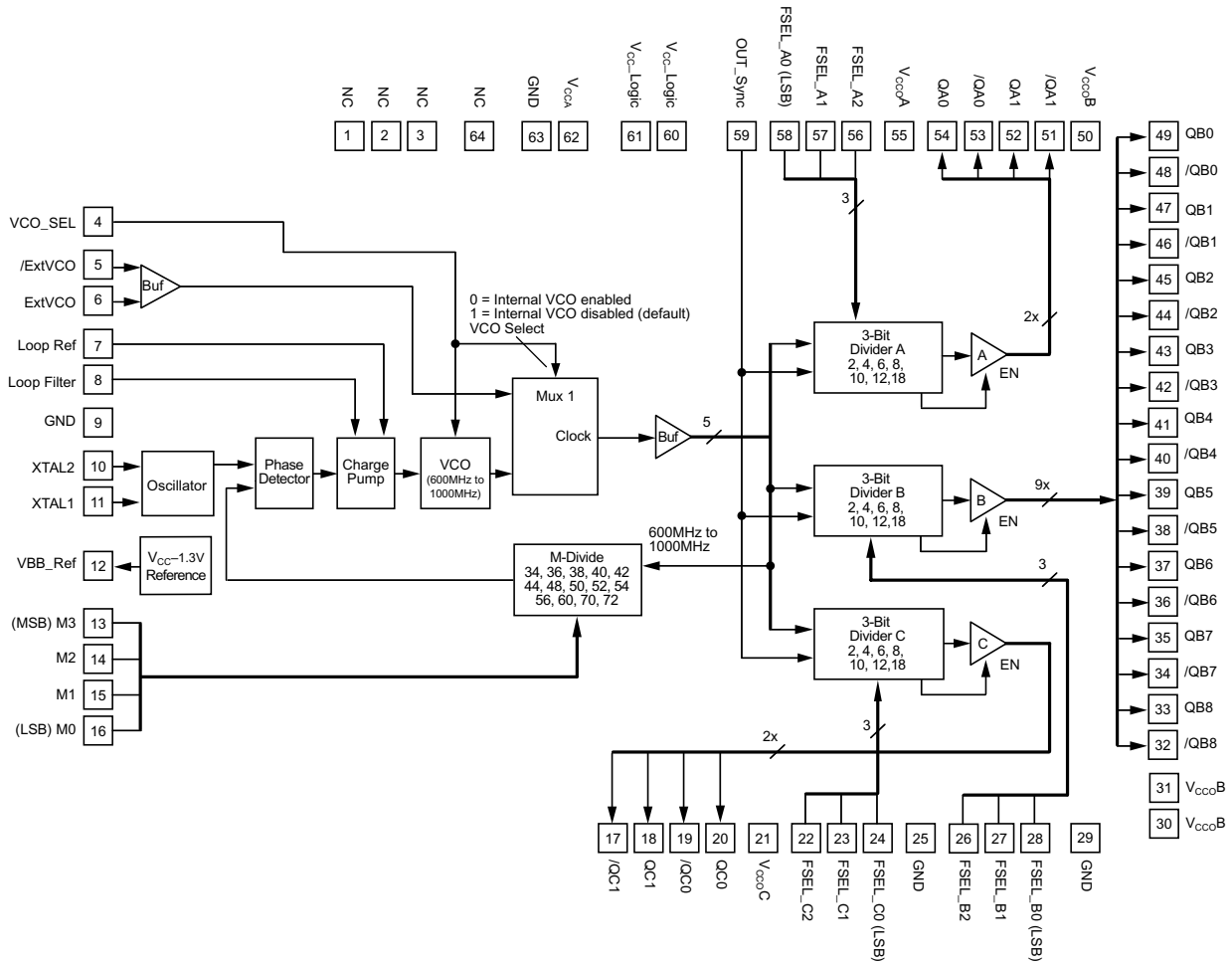
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89532LHC	H64-1	Commercial	SY89532LHC	Sn-Pb
SY89532LHCTR[2]	H64-1	Commercial	SY89532LHC	Sn-Pb
SY89533LHC	H64-1	Commercial	SY89533LHC	Sn-Pb
SY89533LHCTR[2]	H64-1	Commercial	SY89533LHC	Sn-Pb
SY89532LHZ	H64-1	Commercial	SY89532LHZ with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89532LHZTR[2, 3]	H64-1	Commercial	SY89532LHZ with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89533LHZ	H64-1	Commercial	SY89533LHZ with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89533LHZTR[2, 3]	H64-1	Commercial	SY89533LHZ with Pb-Free bar-line indicator	Pb-Free Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Power

Pin Number	Pin Name	Functional Description
60, 61	V_{CC_Logic}	Power for Core Logic: Connect to 3.3V supply. 3.3V power pins are not internally connected on the die, and must be connected together on the PCB.
62	V_{CCA}	Power for PLL: Connect to "quiet" 3.3V supply. 3.3V power pins are not internally connected on the die, and must be connected together on the PCB.
55 30, 31, 50 21	$V_{CCO}A$ $V_{CCO}B$ $V_{CCO}C$	Power for Output Drivers: Connect all V_{CCO} pins to 3.3V supply. V_{CCO} pins are not connected internally on the die.
9, 25, 63, 29 (exposed pad)	GND	Ground: Exposed pad must be soldered to a ground plane.

Configuration

Pin Number	Pin Name	Functional Description
4	VCO_SEL	LVTTL/CMOS-Compatible Input: Selects between internal or external VCO. For external VCO, leave floating. Default condition is logic HIGH. Internal 25kΩ pull-up. When tied LOW, internal VCO is selected.
7	LOOP REF	Analog Input/Output: Provides the reference voltage for PLL loop filter.
8	LOOP FILTER	Analog Input/Output: Provides the loop filter for PLL. See "External Loop Filter Considerations" for loop filter values.
13,14,15,16	M (3:0)	LVTTL/CMOS-Compatible Input: Used to change the PLL (Phase-Lock Loop) feedback divider. Internal 25kΩ pull-up. (M0 = LSB). Default is logic HIGH. See "Feedback Divide Select" table.
22, 23, 24	FSEL_C (2:0)	LVTTL/CMOS-Compatible Input: Bank C post divide select. Internal 25kΩ pull-up. Default is logic HIGH. See "Post-Divide Frequency Select" table.
26, 27, 28	FSEL_B (2:0)	LVTTL/CMOS-Compatible Input: Bank B post divide select. Internal 25kΩ pull-up. Default is logic HIGH. See "Post-Divide Frequency Select" table.
56, 57, 58	FSEL_A (2:0)	LVTTL/CMOS-Compatible Input: Bank A post divide select. Internal 25kΩ pull-up. Default is logic HIGH. See "Post-Divide Frequency Select." FSEL_A0 = LSB.
59	OUT_SYNC	Banks A,B,C output synchronous control: (LVTTL/CMOS compatible). Internal 25kΩ pull-up. After any bank has been programmed, toggle with a HIGH-LOW-HIGH pulse to resynchronize all output banks.

Input/Output

Pin Number	Pin Name	Functional Description
1, 2, 3	NC	No Connect: Leave floating.
10, 11	XTAL2, XTAL1	Crystal Input. Directly connect a series resonant crystal across inputs.
12	VBB_REF	Reference Output Voltage. Used for single-ended input. Maximum sink/source current = 0.5mA.
5, 6	/EXT_VCO, EXT_VCO	Differential "Any In" Compatible Input Pair. Allows for external VCO connection. The "Any In" input structure accepts many popular logic types. See "Input Interface for ExtVCO Pins" section for intercace diagrams. Can leave unconnected if using internal VCO.
51, 52, 53, 54	QA1 to QA0	Bank A 100k LVPECL Output Drivers: Output frequency is controlled by FSEL_A (0:2). Terminate outputs with 50Ω to V_{CC} –2V. See "Output Termination Recommendations" section for termination detail.
32–49	QB8 to QB0	Bank B Output Drivers: SY89532: 100k LVPECL output drivers. SY89533: Differential LVDS outputs. See "Output Termination Recommendations" section for termination detail. Output frequency is controlled by FSEL_B (0:2).
17, 18, 19, 20	QC1 to QC0	Bank C 100k LVPECL Output Drivers: Output frequency is controlled by FSEL_C (0:2). Terminate outputs with 50Ω to V_{CC}–2V. See "Output Termination Recommendations" section.
64	NC	No Connect: Leave floating.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
All V_{CC}	V_{CC} Pin Potential to Ground Pin	–0.5 to +4.0	V
V_{IN}	Input Voltage (except XTAL 1,2 pins)	–0.5 to V_{CCI}	V
$V_{XTAL\ 1,2}$	XTAL 1, 2 Input Voltage	(V_{CC}–1.9V) to V_{CC}	V
I_{OUT}	DC Output Current –LVPECL outputs –LVDS outputs	–50 ±10	mA mA
T_{LEAD}	Lead Temperature (soldering, 20sec.)	260	°C
T_{store}	Storage Temperature	–65 to +150	°C
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient) With Die attach soldered to GND: –Still-Air (TQFP) –200lfpm (TQFP) –500lfpm (TQFP)	 23 18 15	 °C/W °C/W °C/W
	With Die attach NOT soldered to GND:[2] –Still-Air (TQFP) –200lfpm (TQFP) –500lfpm (TQFP)	44 36 30	°C/W °C/W °C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case)	4.3	°C/W

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. It is recommended that the user always solder the exposed die pad to a ground plane for enhanced heat dissipation.

DC ELECTRICAL CHARACTERISTICS

Power Supply

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CCA}[1] V_{CC_LOGIC}	PLL and Logic Supply Voltage	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V
V_{CCO}A/C	Bank A and C V_{CC} Output	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V
V_{CCO}B	Bank B V_{CC} Output LVPECL/LVDS	 3.0	 3.3	 3.6	 3.0	 3.3	 3.6	 3.0	 3.3	 3.6	 V
I_{CC}	Total Supply Current[2] SY89533L LVDS	— —	— 275	260 330	— —	225 285	260 330	— —	— 300	260 330	mA mA

Notes:

1. V_{CCA}, V_{CC_LOGIC}, V_{CCO}A/C. V_{CCO}B are *not* internally connected together inside the device. They must be connected together on the PCB.
2. No load. Outputs floating, Banks A, B, and C enabled.

DC ELECTRICAL CHARACTERISTICS

LVCMOS/LVTTL Input Control Logic

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V
V_{IL}	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V
I_{IH}	Input HIGH Current	—	—	—	—	—	150	—	—	—	µA
I_{IL}	Input LOW Current	—	—	—	–300	—	—	—	—	—	µA

ExtVCO (pins 5, 6) INPUT (All V_{CC} pins = +3.3V ±10%)

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{ID}	Differential Input Voltage	100(1) 200(2)	— —	— —	100(1) 200(2)	— —	— —	100(1) 200(2)	— —	— —	mV mV
V_{IH}	Input HIGH Voltage	—	—	V_{CC} +0.3	—	—	V_{CC} +0.3	—	—	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage	–0.3	—	—	–0.3	—	—	–0.3	—	—	V

Notes:

1. V_{IN} < 2.4V
2. V_{IN} < V_{CC} +0.3V

100K LVPECL Outputs

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage(1)	V_{CC}–1.075	—	V_{CC}–0.830	V_{CC}–1.075	—	V_{CC}–0.830	V_{CC}–1.075	—	V_{CC}–0.830	V
V_{OL}	Output LOW Voltage(1)	V_{CC}–1.860	—	V_{CC}–1.570	V_{CC}–1.860	—	V_{CC}–1.570	V_{CC}–1.860	—	V_{CC} –1.570	V
V_{BB}	Output Reference Voltage	V_{CC}–1.26	V_{CC}–1.32	V_{CC}–1.38	V_{CC}–1.26	V_{CC}–1.32	V_{CC}–1.38	V_{CC}–1.26	V_{CC}–1.32	V_{CC}–1.38	V

Note:

1. 50Ω to V_{CC} –2V. Banks A, B, and C enabled.

LVDS Outputs (SY89533L) Bank B QB0:8(2)

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OD}	Output Voltage Swing(2, 3)	250	—	450	250	—	450	250	—	450	mV
V_{OH}	Output HIGH Voltage	—	—	1.475	—	—	1.475	—	—	1.475	V
V_{OL}	Output LOW Voltage	0.925	—	—	0.925	—	—	0.925	—	—	V
V_{OCM}	Output Common Mode Voltage(2)	1.125	—	1.375	1.125	—	1.375	1.125	—	1.375	V
ΔV_{OCM}	Change in Common Mode Voltage(2)	–50	—	50	–50	—	50	–50	—	50	mV

Notes:

2. 100Ω termination across differential pair.
3. 

AC ELECTRICAL CHARACTERISTICS

$V_{CC\_LOGIC} = V_{CCA} = V_{CCO}A/B/C = +3.3V \pm 10\%$

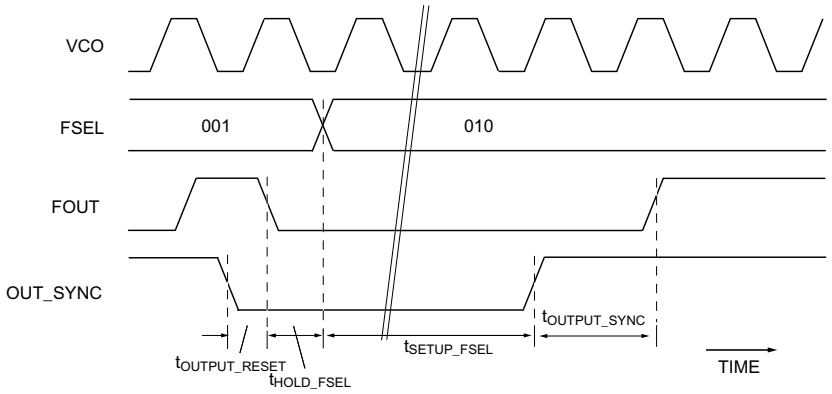
Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{IN}	Xtal Input Frequency Range(1)	—	—	—	14	—	18	—	—	—	MHz
f_{OUT}	Output Frequency Range										
	Internal VCO	—	—	—	33.33	—	500	—	—	—	MHz
	External VCO	—	—	—	—	—	622.08	—	—	—	MHz
t_{VCO}	VCO Frequency Range	600	—	1000	600	—	1000	600	—	1000	MHz
	External VCO Frequency	—	—	1250	—	—	1250	—	—	1250	MHz
t_{skew}	Within Device(2)	—	—	—	—	—	50	—	—	50	ps
	Pin-to-Pin Skew, Bank-to-Bank										
	(Within Same Logic Type)	—	0	50	—	0	50	—	0	50	ps
	(Between Logic Types)	—	60	150	—	60	150	—	60	150	ps
	Part-to-Part Skew(3)	—	—	—	—	—	200	—	—	200	ps
t_{LOCK}	Maximum PLL Lock Time	—	—	—	—	—	10	—	—	10	ms
t_{JITTER}	Cycle-to-Cyle Jitter(4) (pk-to-pk)	—	—	—	—	25	50	—	—	—	ps
	Total Jitter(5) (rms)	—	—	—	—	20	50	—	—	50	ps
t_{pw} (min)	Minimum Pulse Width	—	—	—	50	—	—	50	—	—	ns
	Target PLL Loop Bandwidth										
	Feedback Divider Ratio: 72(6)	—	1.0	—	—	1.0	—	—	1.0	—	MHz
	Feedback Divider Ratio: 34(6)	—	2.0	—	—	2.0	—	—	2.0	—	MHz
	External VCO Clock Input	—	—	1.25	—	—	1.25	—	—	1.25	GHz
t_{DC}	f_{OUT} Duty Cycle	—	—	—	45	50	55	45	50	55	%
t_r, t_f	Output Rise/Fall Time										ps
	(20% to 80%) LVPECL_Out	—	—	400	—	250	400	—	—	400	
	(SY89533L) LVDS_Out	—	—	450	—	300	450	—	—	450	
t_{OUTPUT_RESET} (See Timing Diagrams)		—	—	—	—	—	10	—	—	—	ns
t_{HOLD_FSEL}		—	—	—	5	—	—	—	—	—	ns
t_{SETUP_FSEL}		—	—	—	5	—	—	—	—	—	ns
t_{OUTPUT_SYNC}		—	—	—	1	—	—	—	—	—	VCO clock cycle
FSEL-to-Valid Output Transition Time		—	—	—	—	—	1	—	—	—	µs
$t_{SETUP\_OUT\_SYNC}$		—	—	—	500	—	—	—	—	—	ps

Notes:

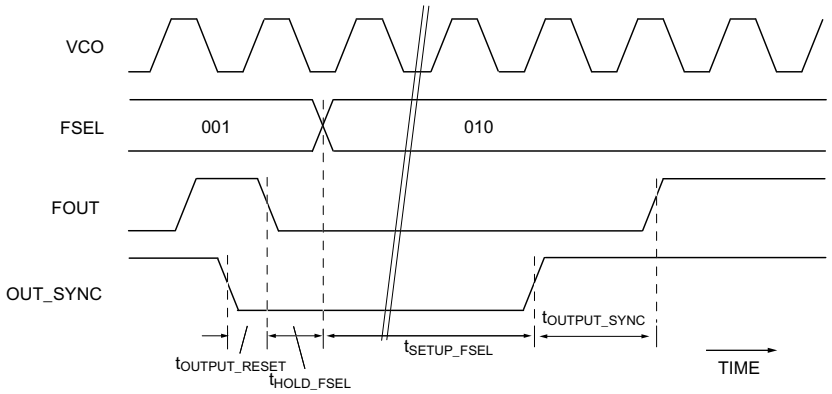
1. Fundamental mode crystal.
2. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature.
3. The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature.
4. Cycle-to-cycle jitter definition: The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n - T_{n+1}$ where T is the time between rising edges of the output signal.
5. Loop filter values shown in Figure 3.
6. Using recommended loop filter components. See “Functional Description, External Loop Filter Considerations.”

TIMING DIAGRAMS

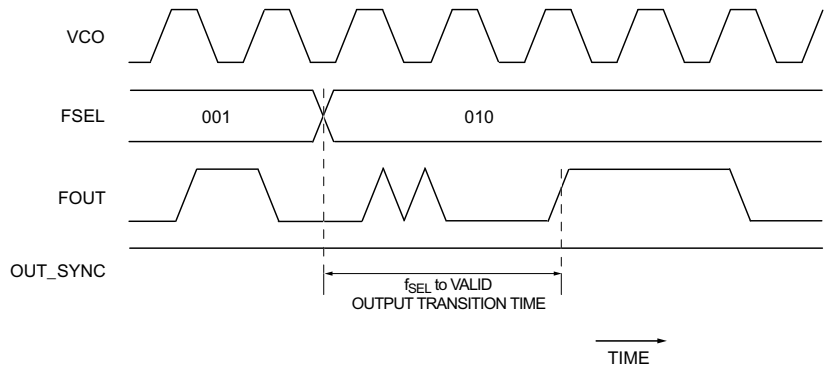
Conditions: Internal VCO, unless otherwise stated.



Frequency Programming (Internal VCO Clock)



Frequency Programming (External VCO Clock)



Output Frequency Update to Valid Output

FUNCTIONAL DESCRIPTION

At the core of the SY89532/33L clock synthesizer is a precision PLL driven by 14MHz to 18MHz series resonant crystal. For users who wish to supply a TTL or LVPECL clock input, please use the SY89534L or SY89535L. The PLL output is sent to three banks of outputs. Each bank has its own programmable frequency divider, and the design is optimized to provide very low skew between banks, and very low jitter.

PLL Programming and Operation

IMPORTANT: If the internal VCO will be used, VCO_SEL **must** be tied LOW, and ExtVCO pins can be left unconnected.

The internal VCO range is 600MHz to 1000MHz, and the feedback ratio is selectable via the MSEL divider control (M3:0 pins). If the designer wishes to use the internal VCO, the VCO_SEL pin must be tied low. The feedback ratio can be changed without powering the chip down. The PLL output is fed to three banks of outputs: Bank A, Bank B, and Bank C. Banks A and C each have two differential LVPECL output pairs. Bank B has nine differential output pairs. On the SY89532L, Bank B is LVPECL. On the SY89533L, Bank B is LVDS.

Each bank has a separate frequency divider circuit that can be reprogrammed on the fly. The FSEL_x0:2 (where x is A,B, or C) pins control the divider value. The FSEL divider can be programmed in ratios from 2 to 18, and the outputs of Banks A,B, and C can be synchronized after programming by pulsing the OUT_SYNC pin HIGH-LOW-HIGH.

To determine the correct settings for SY89532/33L follow these steps:

1. Refer to the "Suggested Selections for Specific Customer Applications" section for common applications, as well as the formula used to compute the output frequency.
2. Determine the desired output frequency, such as 66MHz.
3. Choose a crystal frequency between 14MHz and 18MHz. In this example, we choose 18MHz for the crystal frequency. This results in an input/output ratio of 66/18.
4. Refer to the "Feedback Divide Select Table" and the "Post-Divide Frequency Select Table" to find values for MSEL and FSEL such that MSEL/FSEL equals the same 66/18 ratio. In this example, values of MSEL=44 and FSEL=12 work.
5. Make sure that XTAL (the crystal frequency) multiplied by MSEL is between 600MHz and 1000MHz.

The user may need to experiment with different crystal frequencies to satisfy these requirements.

External VCO Operation

If the designer wishes to use an external VCO, the VCO_SEL pin can be left floating or tied HIGH, and the external VCO signal is connected to the ExtVCO differential input pair. The ExtVCO input structure is designed to accept many popular logic types. See “Input Interface for ExtVCO Pins” section for interface diagrams. A SONET OC-48 compliant 622.08MHz clock is a good example of an application requiring an external VCO. For this application, use a VCXO to supply the 1244.16MHz. to the ExtVCO pins, and set VCO_SEL to HIGH. To save power and reduce noise, the internal VCO is shut down when VCO_SEL is HIGH.

ExtVCO Input Interface

The flexible ExtVCO inputs are designed to accept any differential or single-ended input signal within 300mV above V_{CC} and 300mV below ground.

Do not leave unused ExtVCO inputs floating. Tie either the true or complement inputs to ground, but not both. A logic zero is achieved by connecting the complement input to ground with the true input floating. For a TTL input, tie a 2.5kΩ resistor between the complement input and ground. See “Input Interface for ExtVCO Pins” section, Figures 5a through 5j.

Input Levels

LVDS, CML and HSTL differential signals may be connected directly to the ExtVCO inputs. Depending on the actual worst case voltage seen, the minimum input voltage swing varies as illustrated in the following table:

Input Voltage Range	Minimum Voltage Swing
0 to 2.4V	100mV
0 to V_{CC} +0.3	200mV

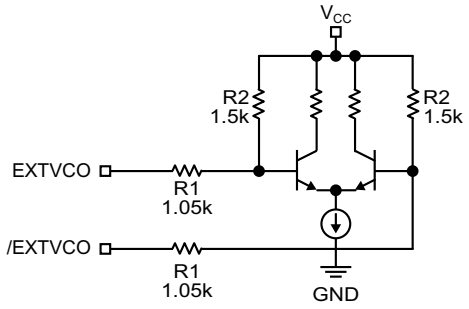


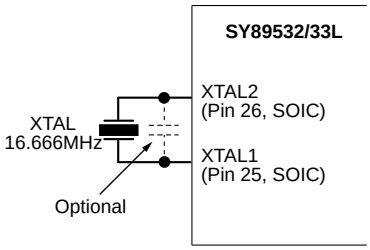
Figure 1. Simplified Input Structure

Crystal Input and Oscillator Interface

The SY89532/33L features a fully integrated on-board oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design, and thus, a series-resonant crystal is preferred, but not required.

A parallel-resonant crystal can be used with the SY89532/33L with only a minor error in the desired frequency. A parallel-resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial.

As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the SY89532/33L as possible to avoid any board level parasitics. In addition, trace lengths should be matched. Figure 2 shows how to interface with a crystal. Table 1 illustrates the crystal specifications. Certain crystals may require a 10pf capacitor across XTAL1 and XTAL2 for proper operation. This is normally not required, but it is recommended that provisions be made for it.



Quartz Crystal Selection:
(1) Raltron Series Resonant: AS-16.666-S-SMD-T-MI
(2) Raltron Parallel Resonant: AS-16.666-18-SMD-T-MI

Figure 2. Crystal Interface

External Loop Filter Considerations

The SY89532/33L features an external PLL loop filter that allows the user to tailor the PLL's behavior to their application and operating environment. We recommend using ceramic capacitors with NPO or X7R dielectric, as they have very low effective series resistance. For applications that require ultra-low cycle-to-cycle jitter, use the components shown in Figure 3. The PLL loop bandwidth is a function of feedback divider ratio, and the external loop filter allows the user to compensate. For instance, the PLL's loop bandwidth can be decreased by using a smaller resistor in the loop filter. This results in less noise from the PLL input, but potentially more noise from the VCO. Refer to "AC Electrical Characteristics" for target PLL loop bandwidth. The designer should take care to keep the loop filter components on the same side of the board and as close as possible to the SY89532/33L's LOOP_REF and LOOP_FILTER pins. To insure minimal noise pick up on the loop filter, it is desirable to cut away the ground plane directly underneath the loop filter component pads and traces. However, the benefit may not be significant in all applications and one must be careful to not alter the characteristic impedance of nearby traces.

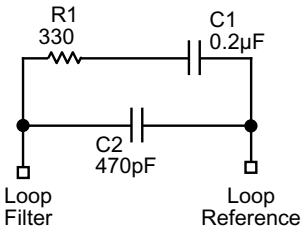


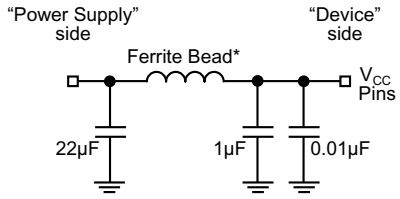
Figure 3. External Loop Filter Connection

OUTPUT FREQUENCY: 14MHz-18MHz				
MODE OF OSCILLATION: FUNDAMENTAL				
	Min.	**Typ.**	**Max.**	**Unit**
Frequency Tolerance @25°C	—	±30	±50	PPM
Frequency Stability over 0°C to 70°C	—	±50	±100	ppm
Operating Temperature Range	–20	—	+70	°C
Storage Temperature Range	–55	—	+125	°C
Aging (per yr/1st 3yrs)	—	—	±5	ppm
Load Capacitance	—	18 (or series)	—	pF
Equivalent Series Resistance (ESR)	—	—	50	Ω
Drive Level	—	100	—	µW

Table 1. Quartz Crystal Oscillator Specifications

Power Supply Filtering Techniques

As with any high-speed integrated circuit, power supply filtering is very important. At a minimum, V_{CC}A, V_{CC}_Logic, and all V_{CCO} pins should be individually connected using a via to the power supply plane, and separate bypass capacitors should be used for each pin. To achieve optimal jitter performance, each power supply pin should use separate instances of the circuit shown in Figure 4.



*For V_{CC}_Analog, V_{CC_TTL}, V_{CC1}, use ferrite bead = 200mA, 0.45 DC, Murata P/N BLM21A1025

*For V_{CC_OUT} use ferrite bead = 3A, 0.025 DC, Murata, P/N BLM31P005

*Component size: 0805

Figure 4. Power Supply Filtering

Output Logic Characteristics

See "Output Termination Recommendations" for illustrations. In cases where single-ended output is desired, the designer should terminate the unused complimentary output in the same manner as the normal output that is begin used. Unused LVPECL output pairs can be left floating. Unused LVDS output pairs (SY89533L) should be terminated w/100Ω across the pair. Unused output banks can be switched off by tying the appropriate FSEL pins to ground. Unused output pairs that are in a bank that is disabled can be left floating, regardless of output driver type.

LVPECL operation:

- Typical voltage swing is 700mV$_{PP}$ to 800mV$_{PP}$ into 50Ω.
- Common mode voltage is V_{CC}–1.3V, typical.
- 100Ω termination across the output pair is NOT recommended for LVPECL.

LVDS operation (Bank B, SY89533L):

- Typical voltage swing is 250mV$_{PP}$ to 450mV$_{PP}$ into effective 50Ω.
- Common mode voltage is 1.25V, typical.
- 100Ω termination across differential output pair is fine.

Thermal Considerations

This part has an exposed die pad for enhanced heat dissipation. We strongly recommend soldering the exposed pad to a ground plane. Where this is not possible, we recommend maintaining at least 500lfpm air flow.

For additional information on exposed-pad characteristics and implementation details, see Amkor Technology's write-up at www.amkor.com.

POST-DIVIDE FREQUENCY SELECT TABLE (FSEL)

FSEL_A2[1] (MSB)	FSEL_A1[1]	FSEL_A0[1] (LSB)	Output Divider
0	0	0	TBD
0	0	1	VCO ÷ 2
0	1	0	VCO ÷ 4
0	1	1	VCO ÷ 6
1	0	0	VCO ÷ 8
1	0	1	VCO ÷ 10
1	1	0	VCO ÷ 12
1	1	1	VCO ÷ 18

Note:

1. Same dividers apply to FSEL_B (0:2) and FSEL_C (0:2).

FEEDBACK DIVIDE SELECT TABLE (MSEL)

M3	M2	M1	M0	VCO Frequency[1]
0	0	0	0	Ref x 34
0	0	0	1	Ref x 36
0	0	1	0	Ref x 38
0	0	1	1	Ref x 40
0	1	0	0	Ref x 42
0	1	0	1	Ref x 44
0	1	1	0	Ref x 48
0	1	1	1	Ref x 50
1	0	0	0	Ref x 52
1	0	0	1	Ref x 54
1	0	1	0	Ref x 56
1	0	1	1	Ref x 60
1	1	1	0	Ref x 70
1	1	1	1	Ref x 72

Note:

1. Ref = Crystal Frequency.

SUGGESTED SELECTIONS FOR SPECIFIC CUSTOMER APPLICATIONS

Protocol	Rate (MHz)	FSEL (Post Divider)	MSEL (Feedback Div.)	XTAL (MHz)	FOUT
PCI	33	18	36	16.67	33
Fast Ethernet	100	6	40	15	100
1/8 FC	133	6	52	15.36	133
ESCON	200	4	50	16	200

$$FOUT = \frac{(XTAL \times MSEL)}{FSEL}$$

Notes:

1. 600MHz < (XTAL x MSEL) < 1000MHz.
2. Where two settings provide the user with the identical desired frequency, the setting with the higher input reference frequency (and lower feedback divider) will usually have lower output jitter. However, the reference input frequency, as well as the VCO frequency, must be kept within their respective ranges.

INPUT INTERFACE FOR EXTVCO PINS

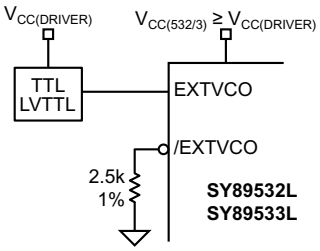


Figure 5a. 5V, 3.3V "TTL"

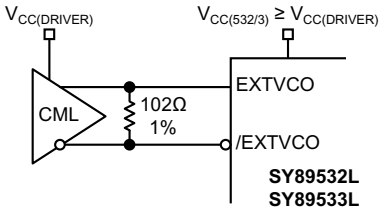


Figure 5b. CML-DC Coupled

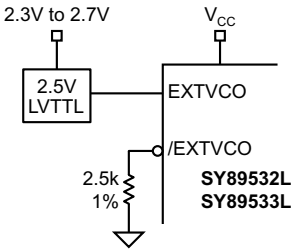


Figure 5c. 2.5V "LVTTL"

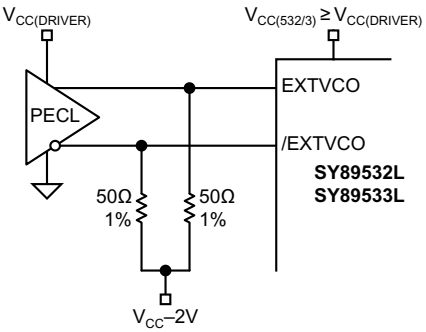


Figure 5d. 3.3V LVPECL-DC Coupled

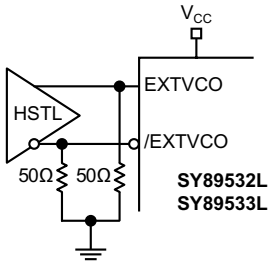


Figure 5e. HSTL

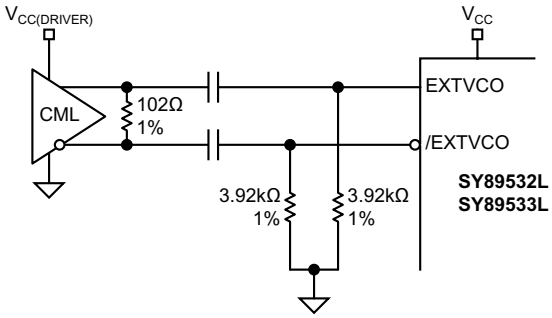


Figure 5f. CML-AC Coupled–Short Trace Lengths

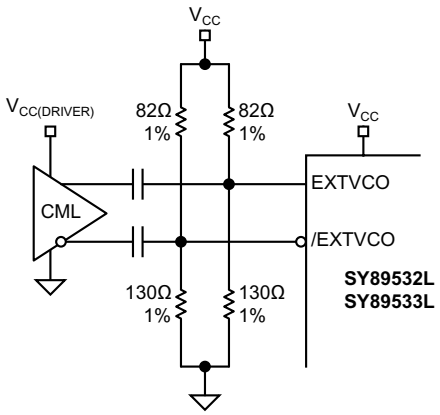


Figure 5g. CML-AC Coupled–Long Trace Lengths

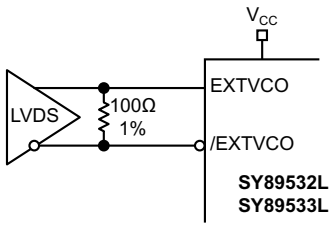


Figure 5h. LVDS

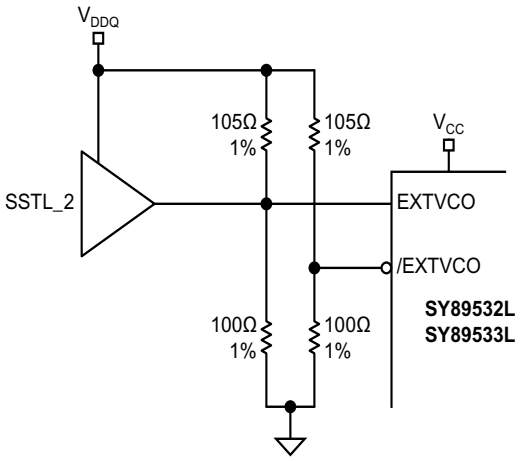


Figure 5i. SSTL_2

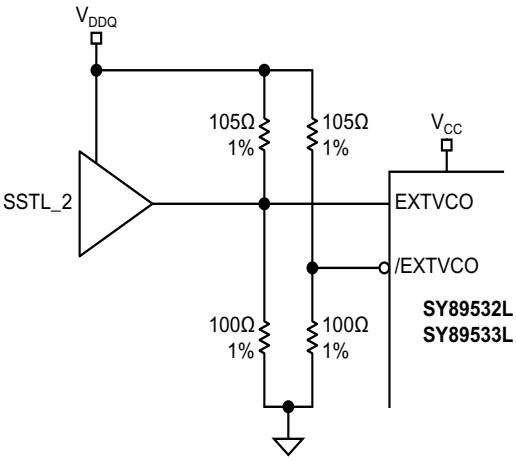


Figure 5j. SSTL_3

OUTPUT TERMINATION RECOMMENDATIONS

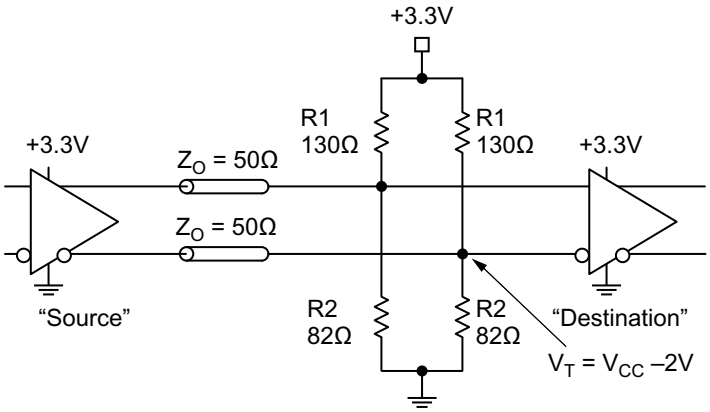


Figure 6. PECL Parallel Termination–Thevenin Equivalent

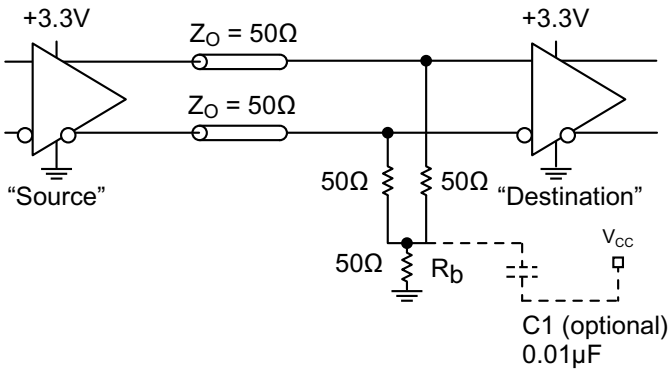


Figure 7. LVPECL Three-Resistor "Y–Termination"

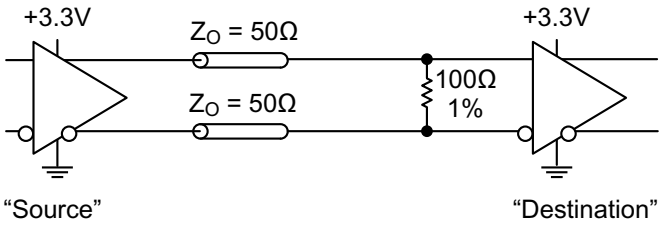
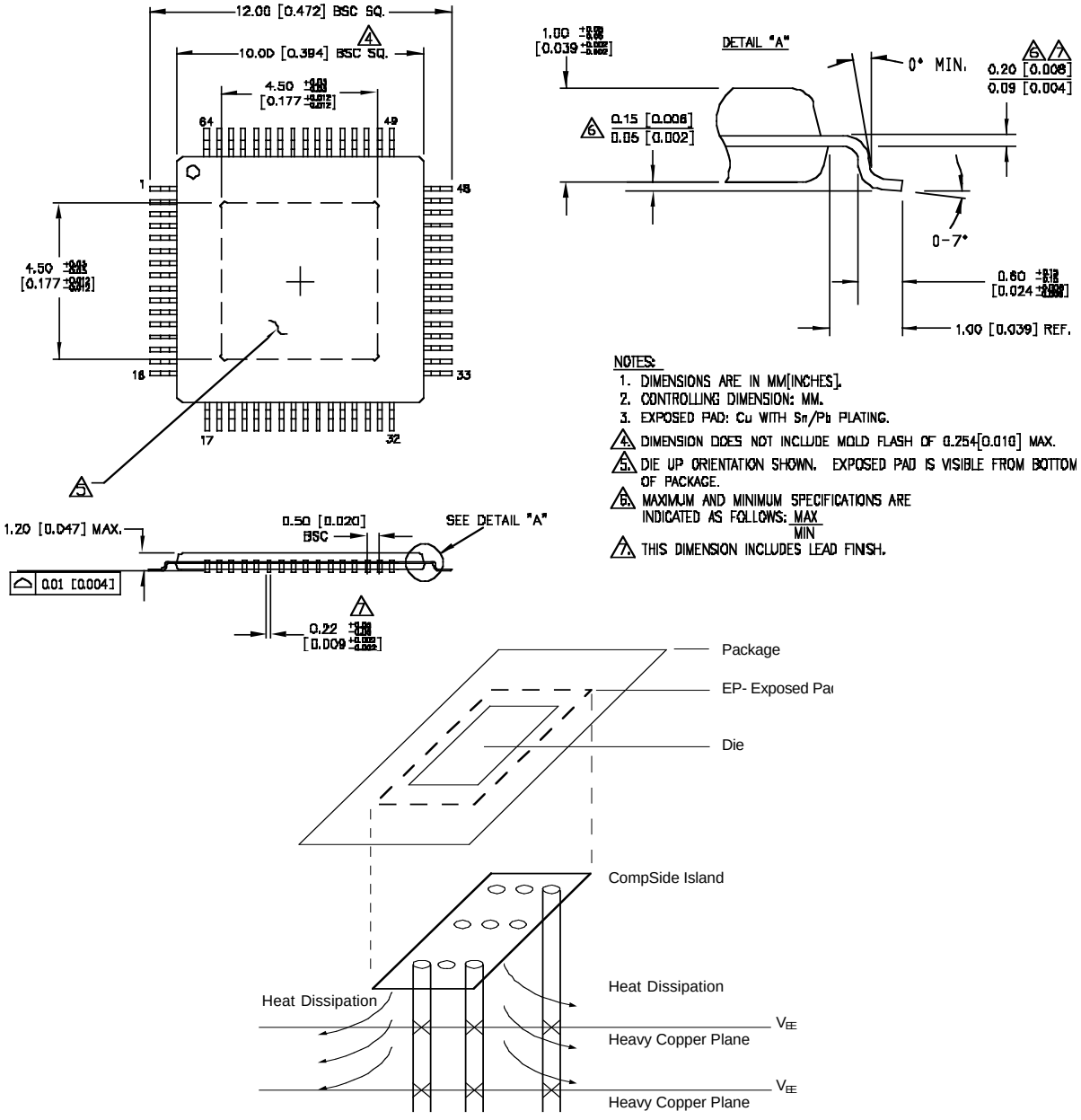


Figure 8. SY89533L LVDS Differential Termination

Notes:

1. PECL Y-termination is a power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_T. For +3.3V systems R_b = 46Ω to 50Ω.

64-PIN EPAD-TQFP (DIE UP) (H64-1)



PCB Thermal Consideration for 64-Pin EPAD-TQFP Package

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