



BUK7J2R4-80M

N-channel 80 V, 2.4 mOhm, Standard level MOSFET in LPAK56E

3 July 2024

Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 14 low ohmic split-gate technology, for ultra-low R_{DSon} capability, housed in a LPAK56E package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
 - 175 °C rating suitable for thermally demanding environments
- Trench 14 split-gate technology:
 - Reduced cell pitch enables enhanced power density and efficiency with lower R_{DSon} in same footprint
 - Fast and efficient switching with optimal damping and low spiking
- LPAK Gull Wing leads:
 - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joints
- LPAK copper clip technology:
 - Improved reliability, with reduced R_{th} , R_{DSon} and package inductance
 - Increases maximum current capability and improved current spreading

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motor, lighting and solenoid control
- Ultra high-performance power switching

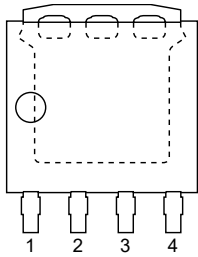
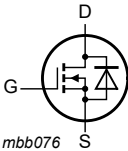
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	231	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	294	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	1.3	1.9	2.4	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 40\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 13 ; Fig. 14	42.5	85	127	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56E; Power-SO8 (SOT1023)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7J2R4-80M	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56E); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7J2R4-80M	72M480J

8. Limiting values

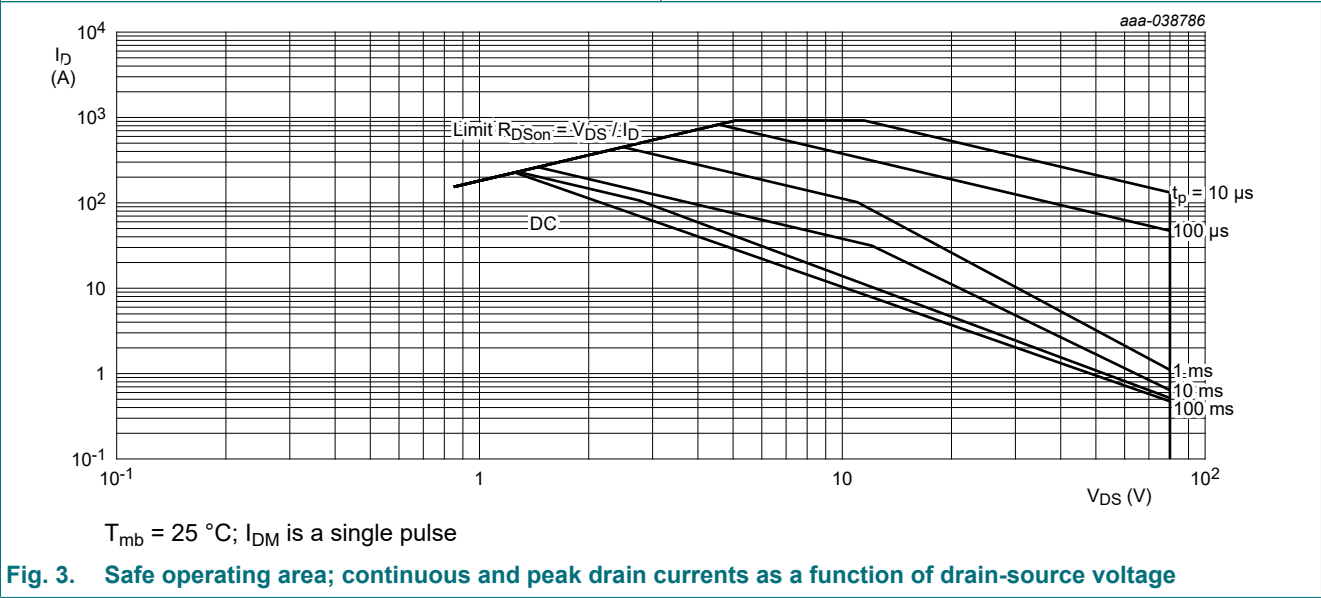
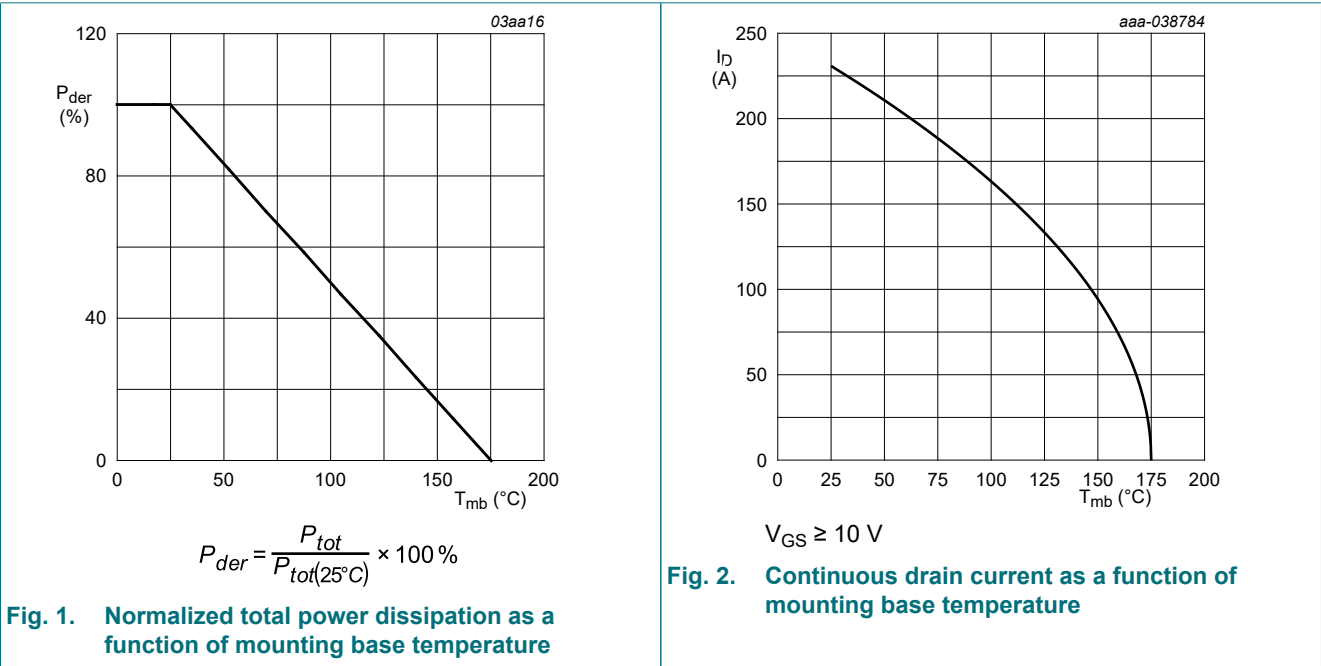
Table 5. Limiting values

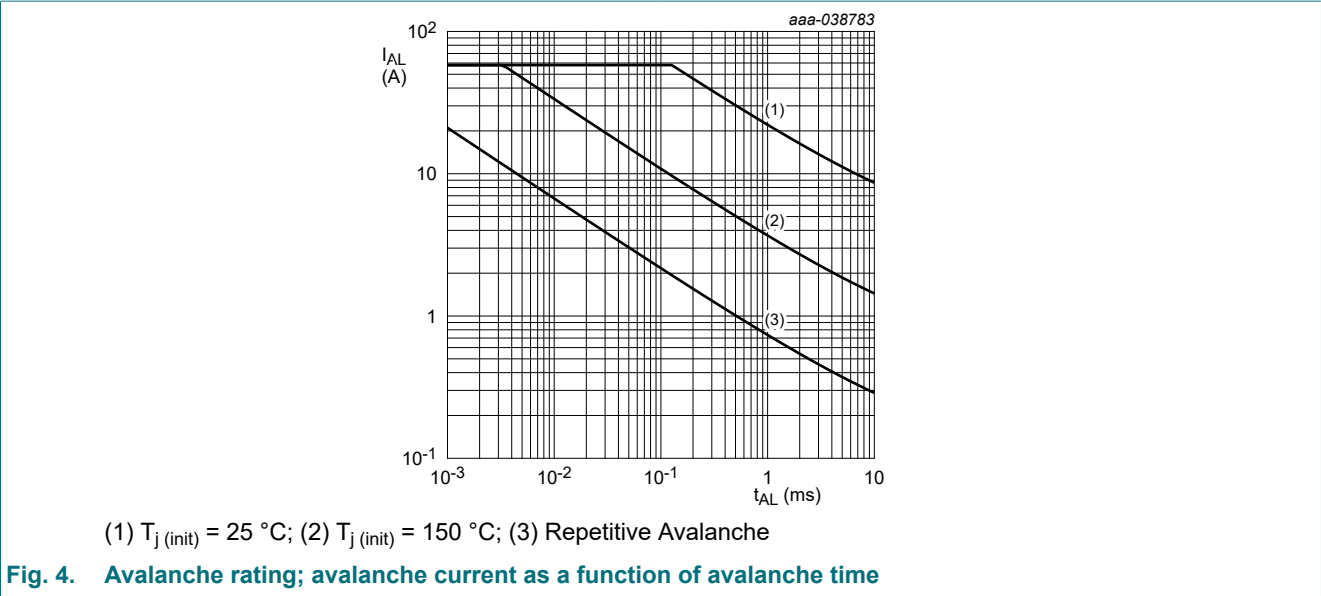
In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
VDS	drain-source voltage	25 °C ≤ Tj ≤ 175 °C	-	80	V
VGS	gate-source voltage		-20	20	V
Ptot	total power dissipation	Tmb = 25 °C; Fig. 1	-	294	W
ID	drain current	VGS = 10 V; Tmb = 25 °C; Fig. 2	-	231	A
		VGS = 10 V; Tmb = 100 °C; Fig. 2	-	163	A
IDM	peak drain current	pulsed; tp ≤ 10 μs; Tmb = 25 °C; Fig. 3	-	923	A
Tstg	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
IAS	non-repetitive avalanche current	Vsup = 80 V; VGS = 10 V; Tj(init) = 25 °C; RGS = 50 Ω	[1]	58	A
Source-drain diode					
IS	source current	Tmb = 25 °C	-	231	A
ISM	peak source current	pulsed; tp ≤ 10 μs; Tmb = 25 °C	-	923	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 58 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[1] [2] [3]	-	383	mJ

- [1] Protected by 100% test.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.



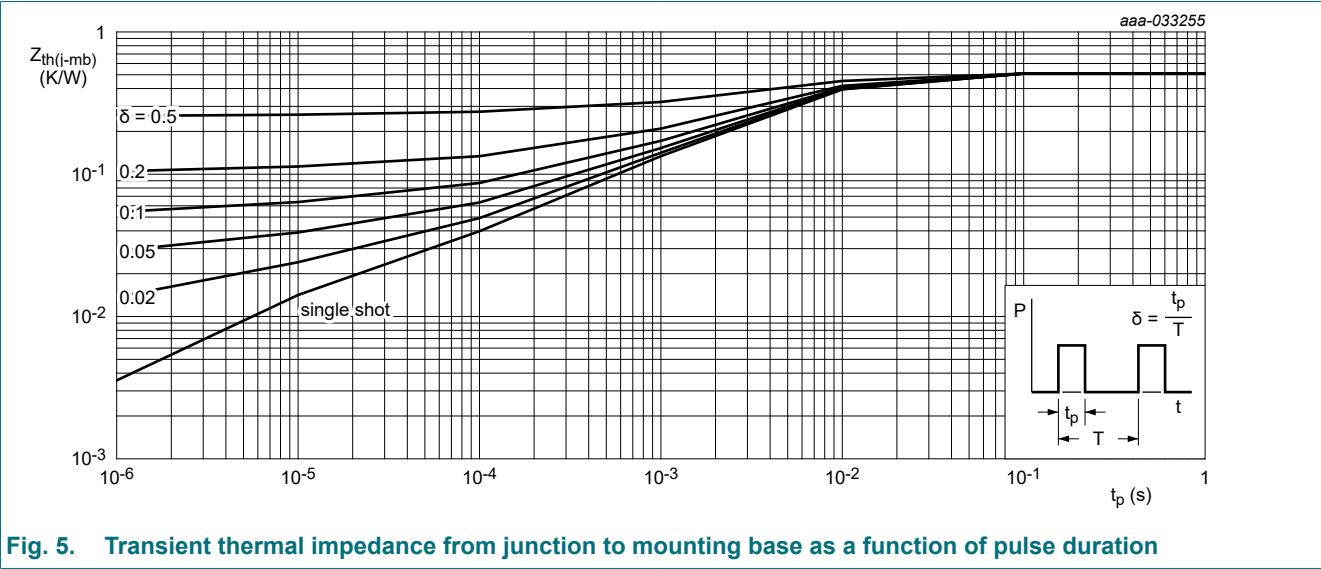


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.45	0.51	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	24	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.



10. Characteristics

Table 7. Characteristics
T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		80	87	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -40 °C		-	85	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C		72	84	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C; Fig. 9		2	3	4	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C; Fig. 10		1	1.9	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = -55 °C; Fig. 10		-	3.3	4.6	V
I _{DSS}	drain leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _j = 25 °C		-	0.01	1	μA
		V _{DS} = 80 V; V _{GS} = 0 V; T _j = 125 °C		-	3	100	μA
		V _{DS} = 80 V; V _{GS} = 0 V; T _j = 175 °C		-	76	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11		1.3	1.9	2.4	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 105 °C; Fig. 12		2	3.1	3.8	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 125 °C; Fig. 12		2.2	3.4	4.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 12		2.8	4.4	5.5	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C		0.4	0.8	1.6	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; Fig. 13 ; Fig. 14		42.5	85	127	nC
Q _{GS}	gate-source charge			8.8	22	35	nC
Q _{GD}	gate-drain charge			5.8	16.5	38	nC
C _{iss}	input capacitance	V _{DS} = 40 V; V _{GS} = 0 V; f = 1 MHz; Fig. 15		3510	5850	8191	pF
C _{oss}	output capacitance			554	1385	2493	pF
C _{rss}	reverse transfer capacitance			4	44	102	pF
t _{d(on)}	turn-on delay time	V _{DS} = 40 V; R _L = 1.6 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω		-	19	-	ns
t _r	rise time			-	18	-	ns
t _{d(off)}	turn-off delay time			-	53	-	ns
t _f	fall time			-	29	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.79	1	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 40 V; Fig. 17		-	38	-	ns
Q _r	recovered charge			-	33	-	nC

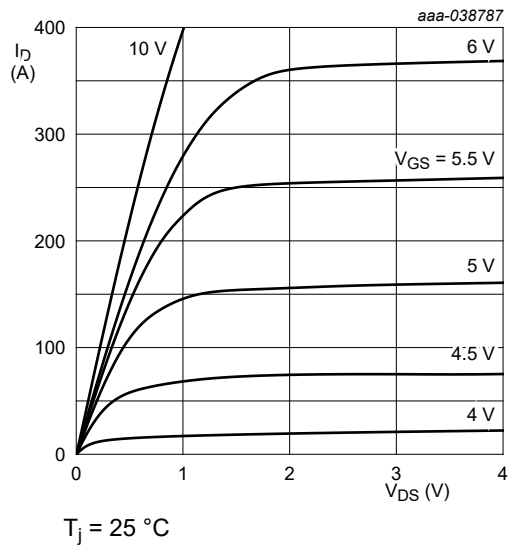


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

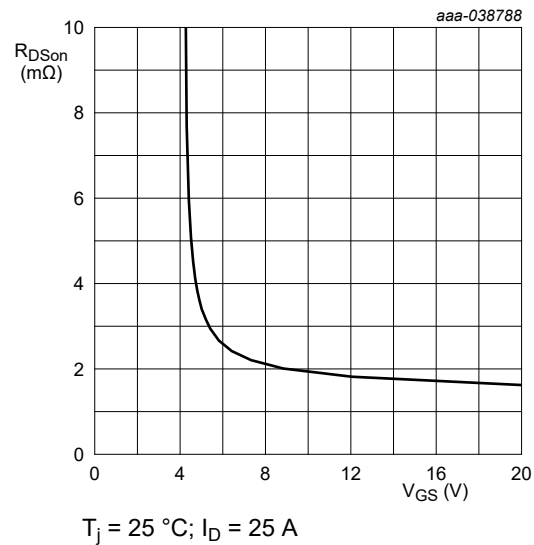


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

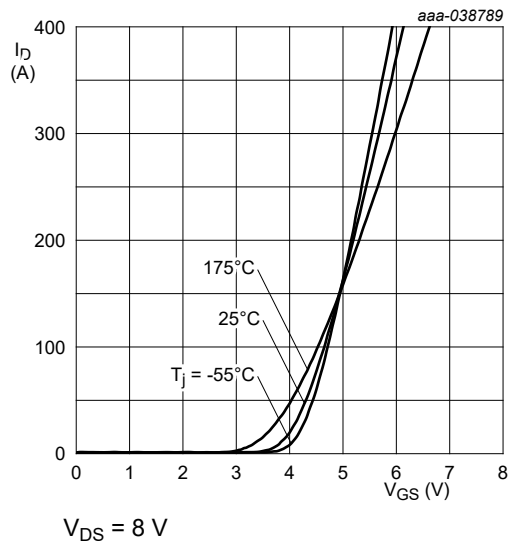


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

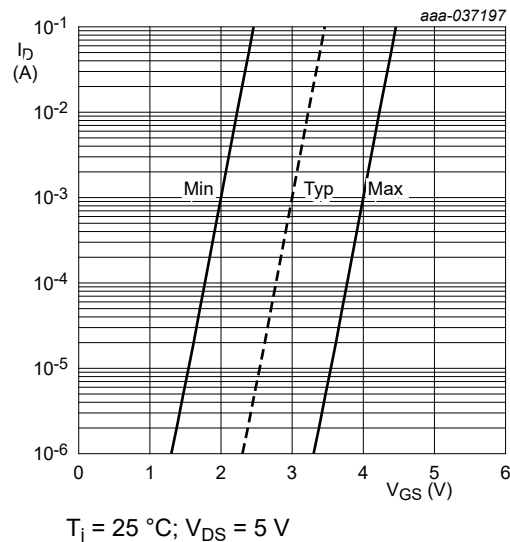


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

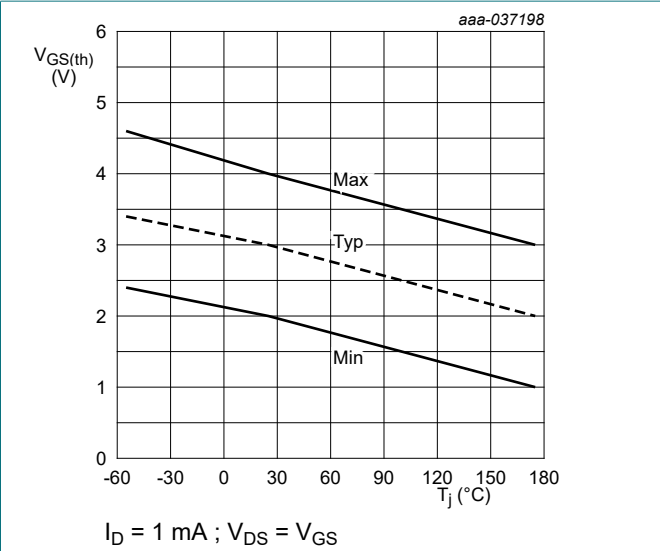


Fig. 10. Gate-source threshold voltage as a function of junction temperature

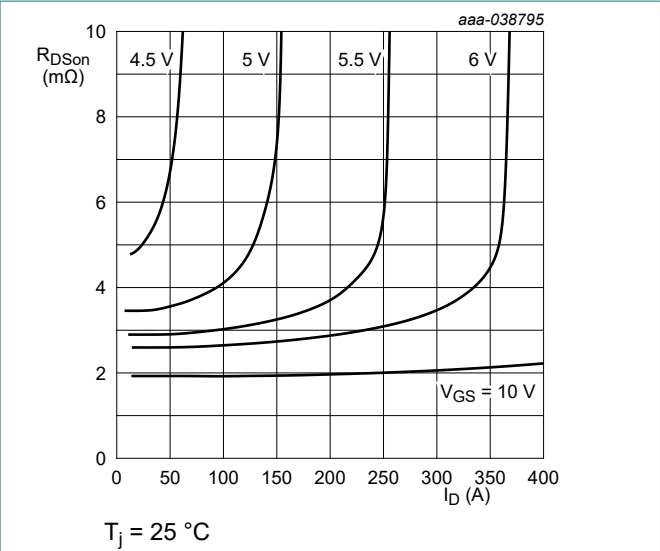


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

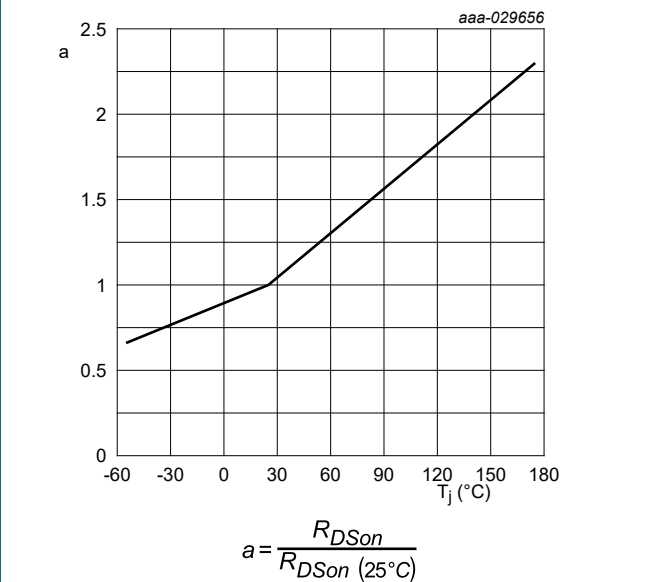


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

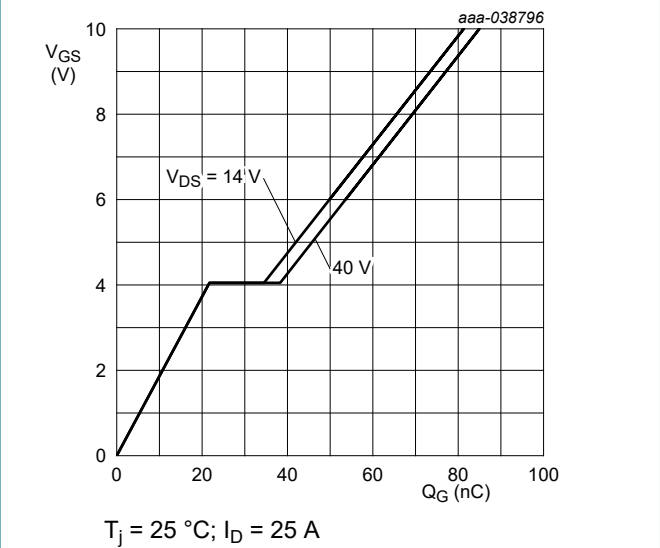


Fig. 13. Gate-source voltage as a function of gate charge; typical values

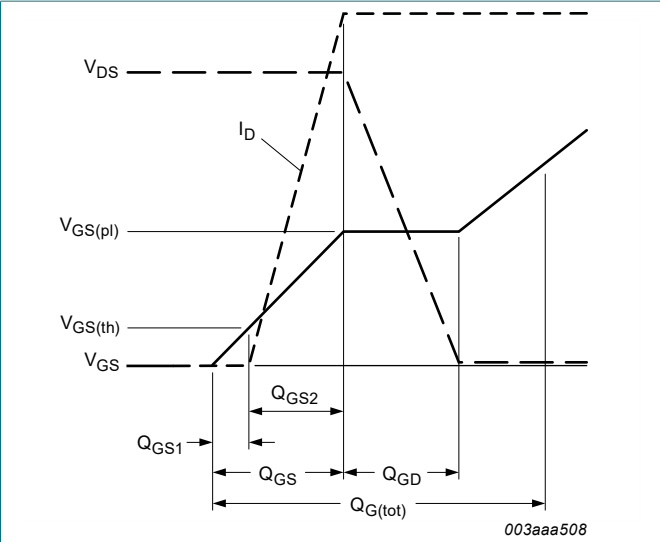


Fig. 14. Gate charge waveform definitions

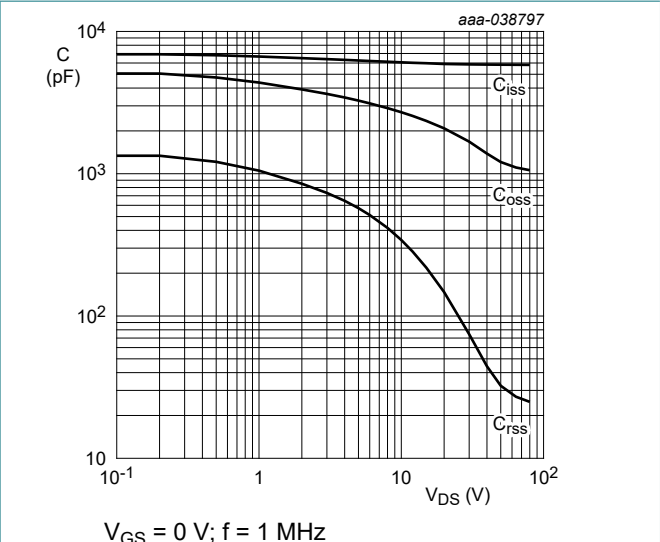


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

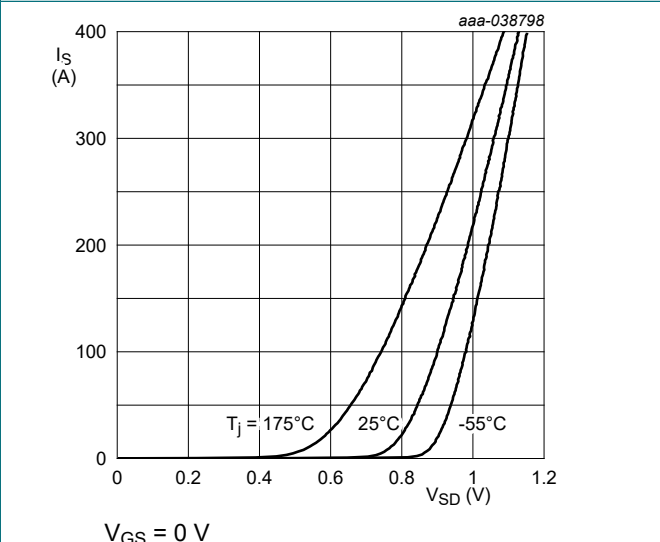


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

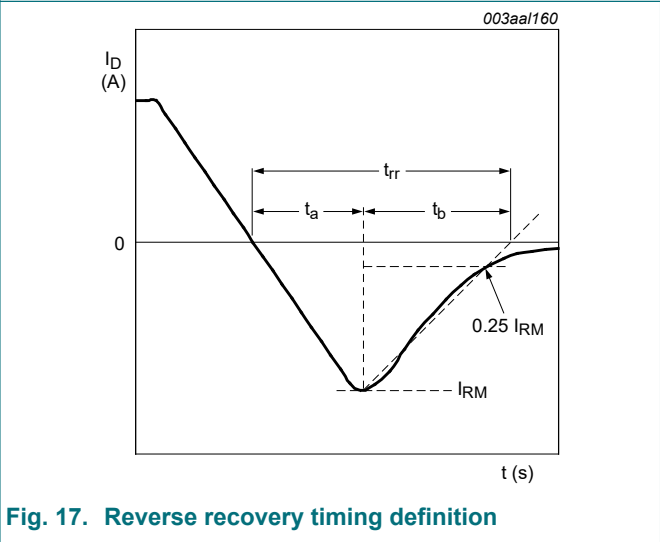


Fig. 17. Reverse recovery timing definition

11. Package outline

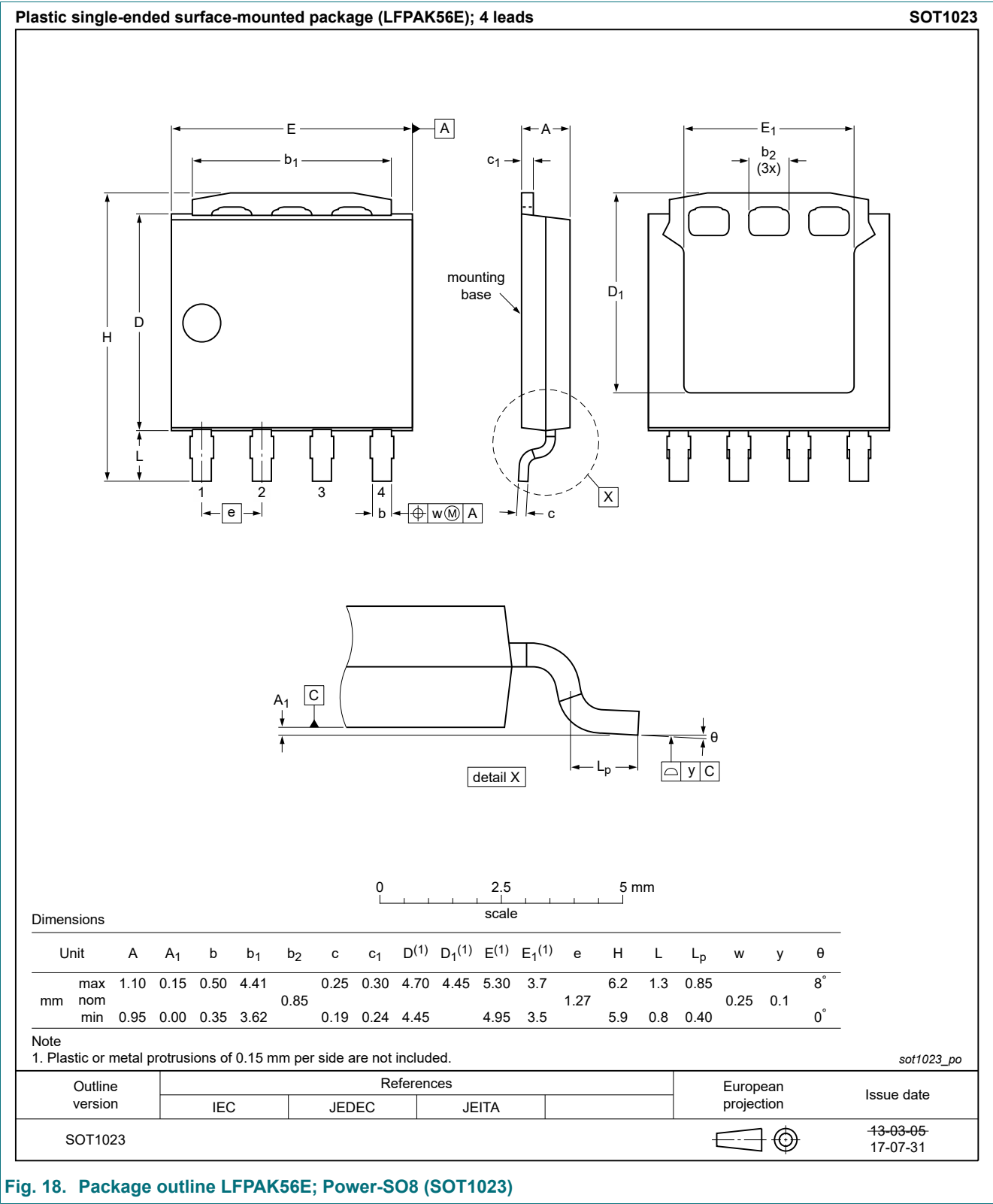
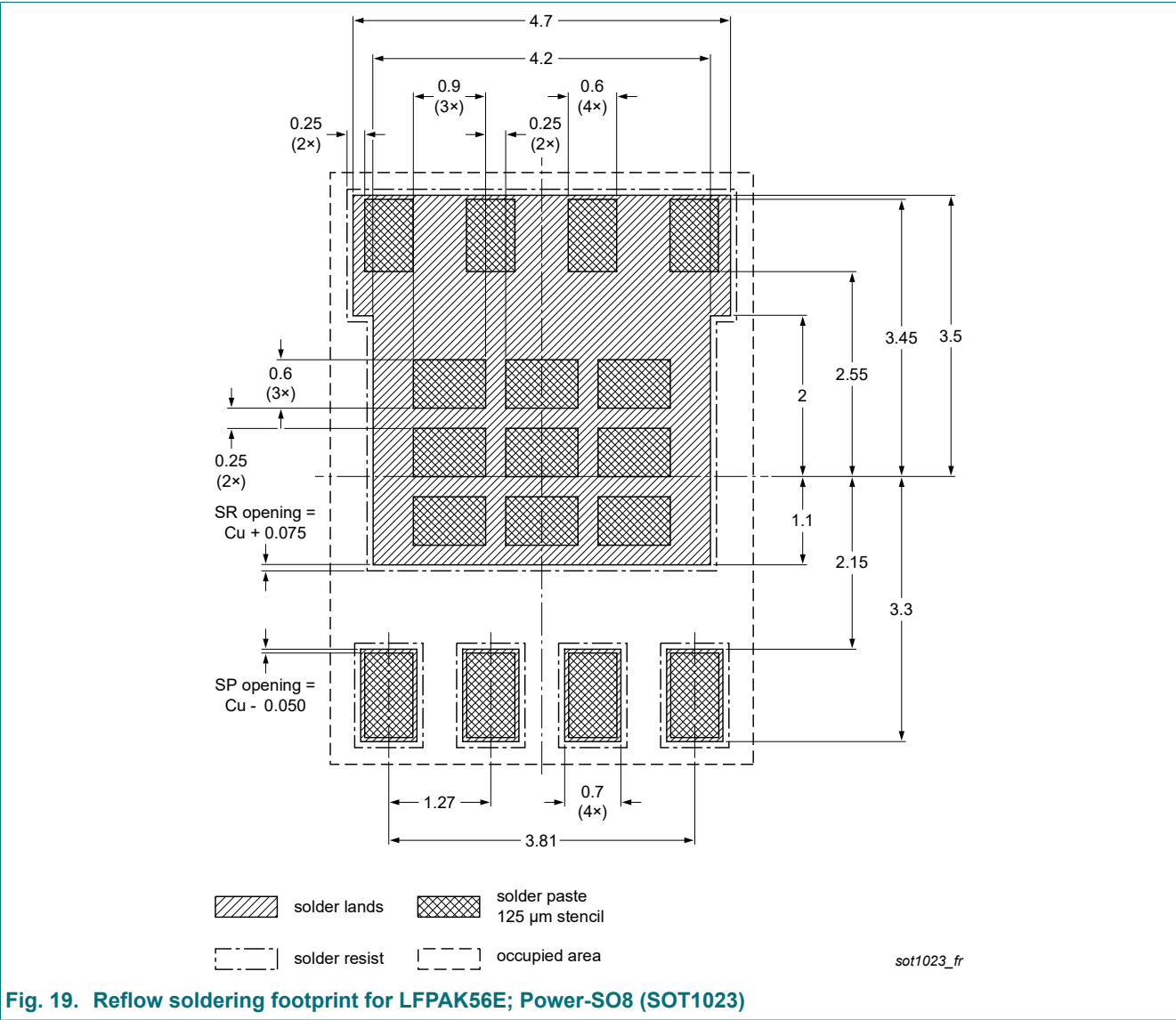


Fig. 18. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering



13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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- [2] The term 'short data sheet' is explained in section "Definitions".
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