

**Ultra Low Output Voltage Linear N-FET Controller****AP2160****General Description**

The AP2160 is an ultra low output voltage N-FET linear regulator controller. The output voltage can be adjusted down to 0.5V. A Power-On-Reset (POR) circuit monitors supply voltage to prevent wrong operations. A POK pin indicates the output status. It can control other converters for power sequence. The AP2160 can be enabled by other power systems.

The AP2160 integrates a 0.5V reference voltage with 1% accuracy to provide tight regulation to the output voltage. The regulator also features enable control, open drain power good signal, under-voltage protection and soft start.

The AP2160 is available in 6-pin SOT-23-6 standard package.

**Features**

- 0.5V Reference Voltage with 1% Accuracy
- Adjustable Output Voltage down to 0.5V
- Low ESR Output Capacitor (MLCC and POSCAP) Applicable
- Enable Control for the Output Voltage and Low Shutdown Current
- Under-voltage Short Circuit Protection
- Fast Transient Response
- Power Good Monitoring and Signaling for the Output
- Drive N-Channel MOSFETs

**Applications**

- Notebook PC Computers
- Desktop Computers
- Battery Powered Devices
- Portable Instruments

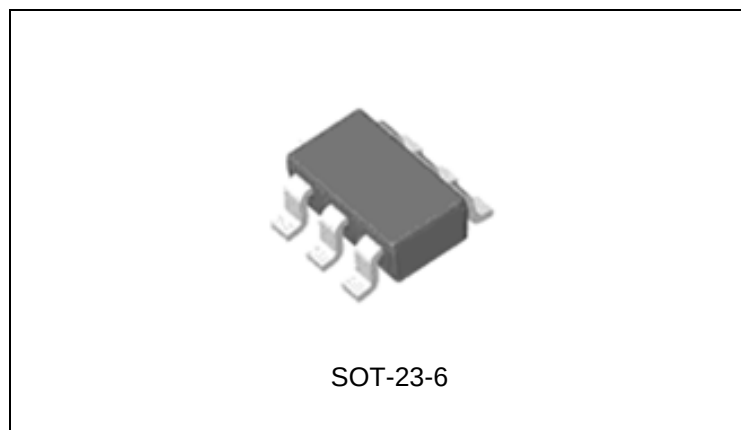


Figure 1. Package Type of AP2160

## Ultra Low Output Voltage Linear N-FET Controller

**AP2160**

### Pin Configuration

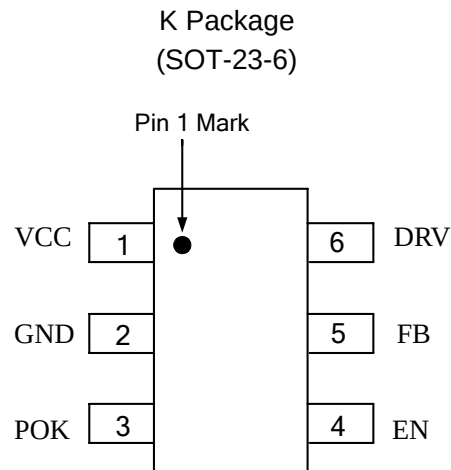


Figure 2. Pin Configuration of AP2160 (Top View)

### Pin Description

| Pin Number | Pin Name | Function                         |
|------------|----------|----------------------------------|
| 1          | VCC      | Input voltage                    |
| 2          | GND      | Common ground pin                |
| 3          | POK      | Power OK output pin              |
| 4          | EN       | H: Normal operation; L: Shutdown |
| 5          | FB       | Output voltage feedback pin      |
| 6          | DRV      | Gate drive to N-FET              |

# Ultra Low Output Voltage Linear N-FET Controller

**AP2160**

## Functional Block Diagram

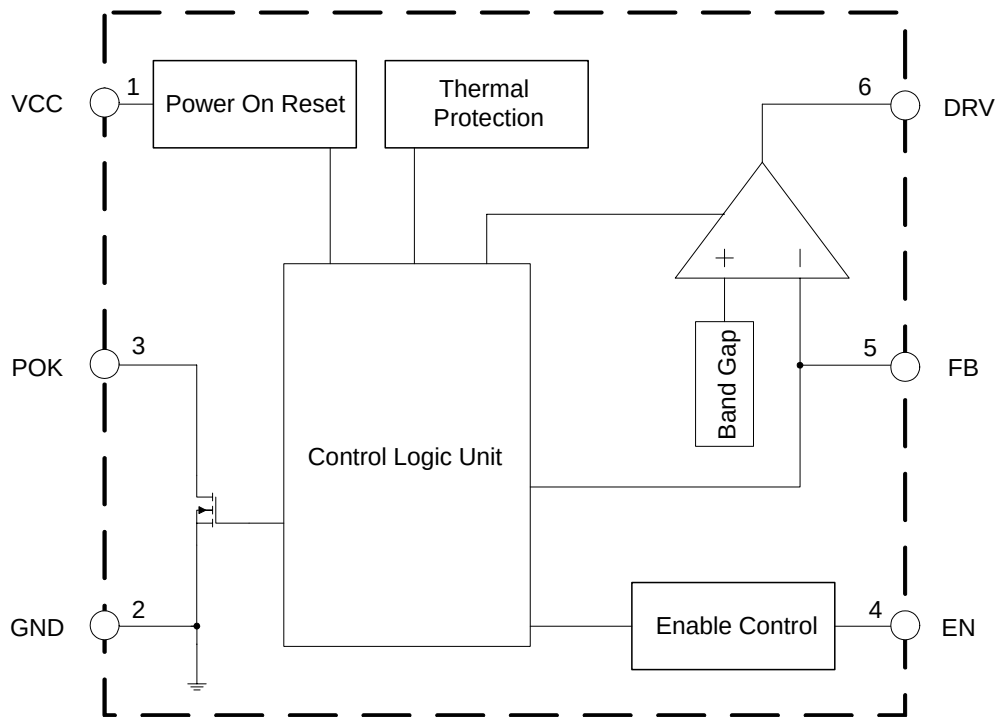
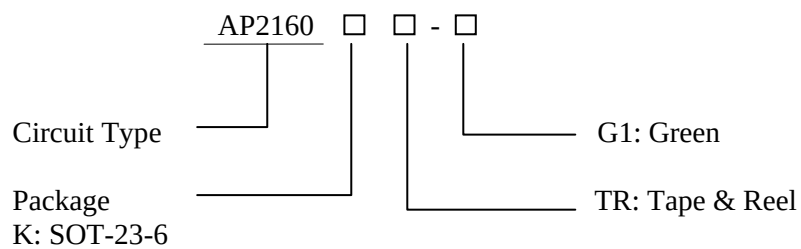


Figure 3. Functional Block Diagram of AP2160

## Ordering Information



| Package  | Temperature Range | Part Number  | Marking ID | Packing Type |
|----------|-------------------|--------------|------------|--------------|
| SOT-23-6 | -40 to 85°C       | AP2160KTR-G1 | GJC        | Tape & Reel  |

BCD Semiconductor's Pb-free products, as designated with "G1" suffix in the part number, are RoHS compliant and green.

**Ultra Low Output Voltage Linear N-FET Controller****AP2160****Absolute Maximum Ratings (Note 1)**

| Parameter                                | Symbol     | Value                | Unit |
|------------------------------------------|------------|----------------------|------|
| VCC to GND                               | $V_{CC}$   | -0.3 to 7            | V    |
| DRV to GND                               | $V_{DRV}$  | -0.3 to $V_{CC}+0.3$ | V    |
| POK to GND                               | $V_{POK}$  | -0.3 to $V_{CC}+0.3$ | V    |
| FB to GND                                | $V_{FB}$   | -0.3 to $V_{CC}+0.3$ | V    |
| EN to GND                                | $V_{EN}$   | -0.3 to $V_{CC}+0.3$ | V    |
| Operating Junction Temperature           | $T_J$      | 150                  | °C   |
| Power Dissipation (25°C)                 | $P_D$      | 0.4                  | W    |
| Operating Temperature Range              | $T_{OPR}$  | -40 to 85            | °C   |
| Storage Temperature Range                | $T_{STG}$  | -65 to 150           | °C   |
| Lead Temperature (Soldering, 10 Seconds) | $T_{LEAD}$ | 260                  | °C   |
| ESD (Machine Model)                      |            | 200                  | V    |
| ESD (Human Body Model)                   |            | 2000                 | V    |

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

**Recommended Operating Conditions**

| Parameter                                  | Symbol   | Min | Max | Unit |
|--------------------------------------------|----------|-----|-----|------|
| Supply Voltage (between VCC and GND)       | $V_{CC}$ | 4.5 | 5.5 | V    |
| System Input Voltage (between VIN and GND) | $V_{IN}$ | 0.5 | 5.5 | V    |
| Ambient Operating Temperature Range        | $T_A$    | -40 | 85  | °C   |

**Ultra Low Output Voltage Linear N-FET Controller****AP2160****Electrical Characteristics** $V_{IN}=1.5V$ ,  $V_{OUT}=1.05V$ ,  $V_{EN}=V_{CC}$ ,  $T_A=25^{\circ}C$ ,  $C_{IN}=4.7\mu F$ ,  $C_{OUT}=22\mu F$ , unless otherwise specified.

| Parameter                              | Symbol          | Conditions                             | Min   | Typ  | Max   | Units       |
|----------------------------------------|-----------------|----------------------------------------|-------|------|-------|-------------|
| Supply Voltage Range                   | $V_{CC}$        |                                        | 4.5   |      | 5.5   | V           |
| Input Voltage UVLO Threshold           | $V_{UVLO}$      | $V_{FB}=0.48V$ , $V_{CC}$ rising       |       | 3.70 |       | V           |
| Input Voltage UVLO Hysteresis          | $V_{HYST}$      | $V_{FB}=0.48V$ , $V_{CC}$ falling      |       | 0.25 |       | V           |
| Supply Current                         | $I_{CC}$        | $V_{EN}=V_{CC}=5V$                     |       | 0.42 | 0.6   | mA          |
| Shutdown Current                       | $I_{SD}$        | $V_{EN}=0V$                            | -1    |      | 1     | $\mu A$     |
| Feedback Voltage                       | $V_{FB}$        | $V_{EN}=V_{CC}=5V$                     | 0.495 | 0.5  | 0.505 | V           |
| Feedback Pin Input Current             | $I_{FB}$        | $V_{FB}=0.5V$                          | -100  |      | 100   | nA          |
| EN Pin Logic High Threshold Voltage    | $V_{EN-H}$      | $V_{CC}=5V$ , $V_{EN}$ rising          | 1.3   |      |       | V           |
|                                        | $V_{EN-L}$      | $V_{CC}=5V$ , $V_{EN}$ falling         |       |      | 0.5   |             |
| EN Pin Input Current                   | $I_{EN}$        | $I_{OUT}=0mA$ , $V_{IN}=5V$            | -1    |      | 1     | $\mu A$     |
| Output Voltage UVLO Threshold          | $V_{TH(UV)}$    | $V_{FB}$ Falling                       | 0.2   | 0.25 | 0.3   | V           |
| DRV Output Current                     | $I_{DRV(SS)}$   | Sourcing, $V_{FB}=0V$                  |       | 20   |       | $\mu A$     |
|                                        | $I_{DRV(SRC)}$  | Sourcing, $V_{FB}=0.48V$               |       | 2.2  |       | mA          |
|                                        | $I_{DRV(SINK)}$ | Sinking, $V_{FB}=0.52V$                |       | 9.0  |       |             |
| DRV Pin Output Voltage                 | $V_{DRV}$       | $V_{FB}=0.48V$ ,<br>$V_{EN}=V_{CC}=5V$ | 4.9   |      | 5.0   | V           |
|                                        |                 | $V_{FB}=0.52V$ ,<br>$V_{EN}=V_{CC}=5V$ | 0.8   | 1.15 | 1.5   |             |
| POK Threshold Voltage for Power not OK | $V_{PNOK}$      | $V_{FB}$ falling                       | 84%   | 88%  | 91%   | $V_{FB}$    |
| POK Low Voltage                        |                 | POK sinks 1mA                          |       | 200  | 250   | mV          |
| POK Delay Time                         | $t_{DELAY}$     |                                        | 0.8   | 2    | 10    | ms          |
| Thermal Shutdown Temperature           | $T_{SD}$        |                                        |       | 150  |       | $^{\circ}C$ |
| Thermal Shutdown Hysteresis            |                 |                                        |       | 40   |       | $^{\circ}C$ |



## Typical Performance Characteristics

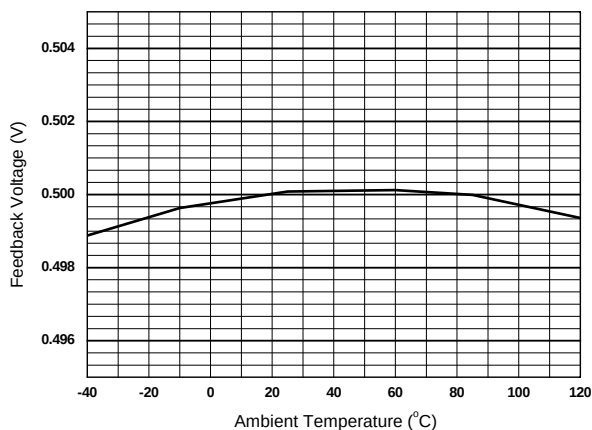


Figure 4. Feedback Voltage vs. Ambient Temperature

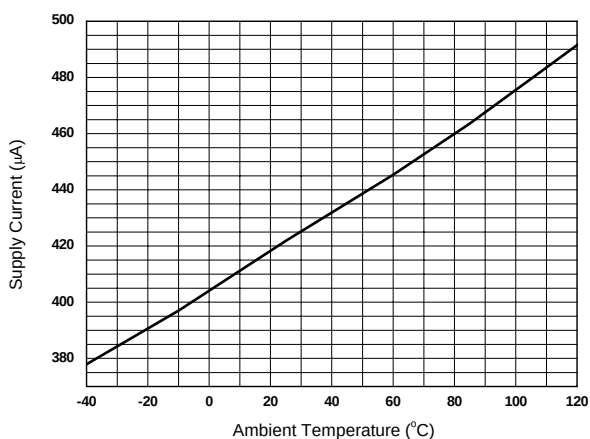


Figure 5. Supply Current vs. Ambient Temperature

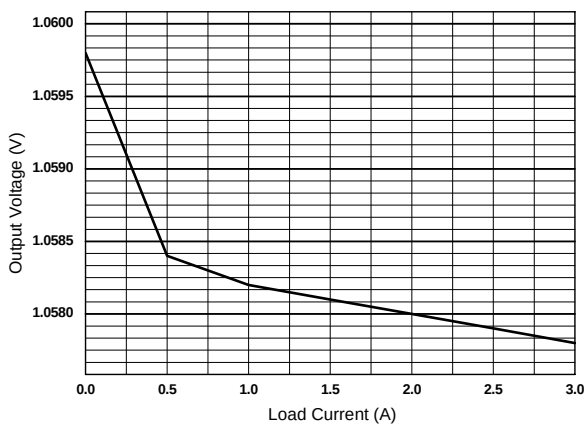


Figure 6. Output Voltage vs. Load Current

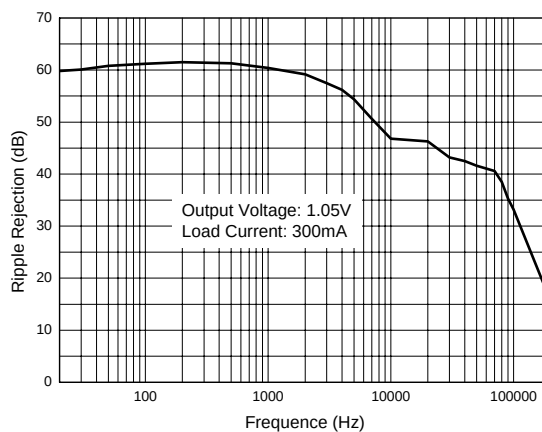


Figure 7. Ripple Rejection vs. Frequency

**Ultra Low Output Voltage Linear N-FET Controller****AP2160****Function Description****1. Power-On-Reset**

A Power-On-Reset (POR) circuit monitors input voltages at VCC pin to prevent wrong logic controls. The POR function initiates a soft-start process after the supply voltages exceed input voltage UVLO threshold during powering on. The POR function also pulls low the POK pin regardless of the output voltage when the VCC voltage falls below the input voltage UVLO threshold minus input voltage UVLO hysteresis.

**2. Output Voltage Regulation**

An error amplifier working with a temperature compensated 0.5V reference and an output NMOS regulates output to the preset voltage. The error amplifier designed with high bandwidth and DC gain

provides very fast transient response and excellent load regulation.

**3. Under-Voltage Protection (UVP)**

AP2160 monitors the voltage on FB pin after soft-start process finishing. Therefore the UVP is disabled during soft-start. When the voltage on FB pin falls below the output voltage UVLO Threshold, the UVP circuit shuts down the output immediately.

**4. Thermal Shutdown**

A thermal shutdown circuit limits the junction temperature of AP2160. When the junction temperature exceeds 150°C, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature drops by 40°C.

# Ultra Low Output Voltage Linear N-FET Controller

## AP2160

### Typical Application

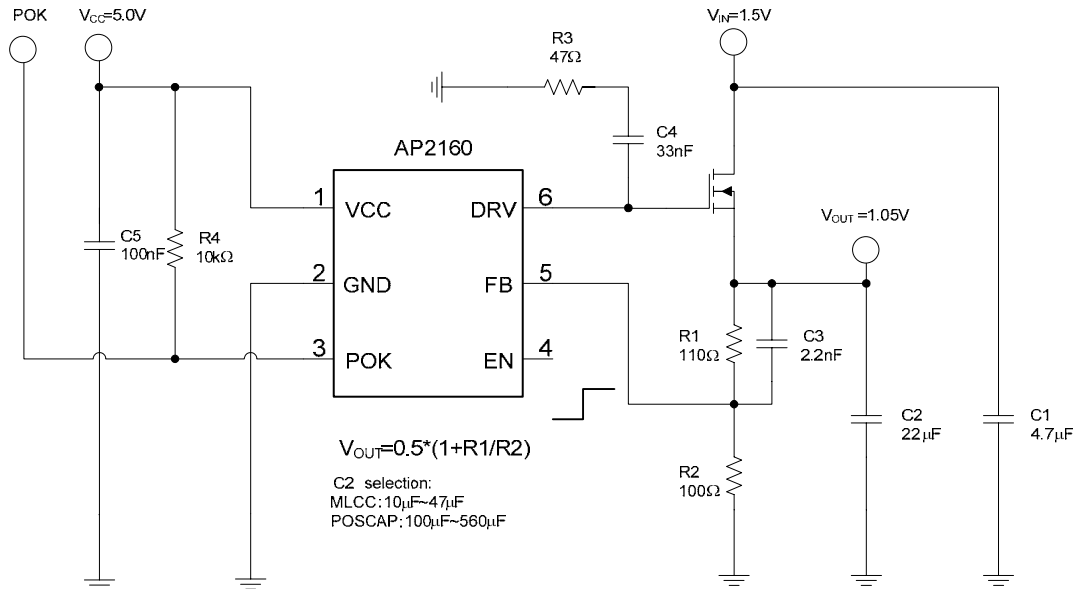
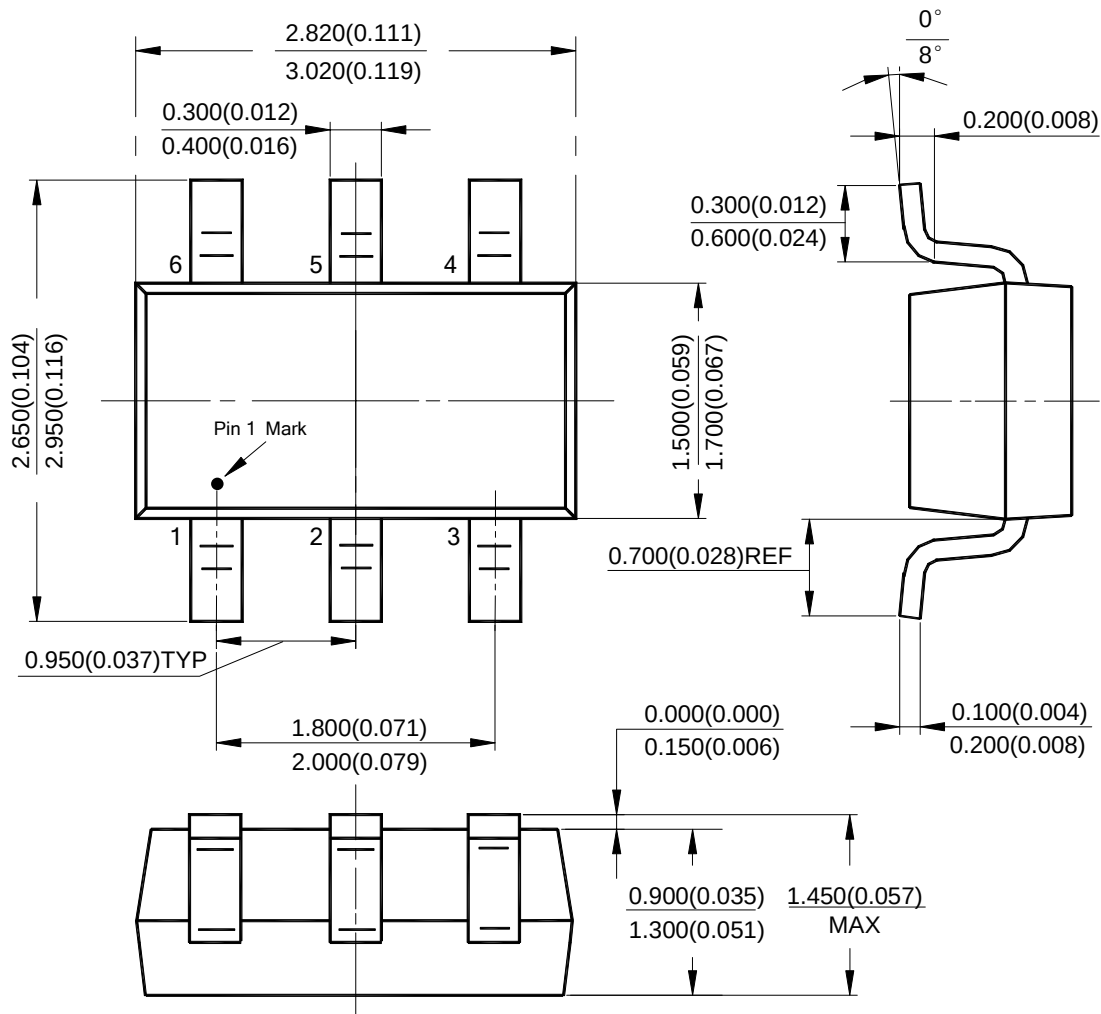


Figure 8. Typical Application Circuit of AP2160



**Ultra Low Output Voltage Linear N-FET Controller****AP2160****Mechanical Dimensions****SOT-23-6****Unit: mm(inch)**



## **BCD Semiconductor Manufacturing Limited**

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