



# 4Gb / 8Gb LPDDR4 / LPDDR4X Combo

## Table of Contents-

|        |                                                              |    |
|--------|--------------------------------------------------------------|----|
| 1.     | GENERAL DESCRIPTION .....                                    | 6  |
| 2.     | FEATURES .....                                               | 6  |
| 3.     | ORDER INFORMATION .....                                      | 7  |
| 4.     | BALL ASSIGNMENT .....                                        | 8  |
| 4.1    | Single-Die-Package (SDP) VFBGA 100 Ball Assignment .....     | 8  |
| 4.2    | Single-Die-Package (SDP) TFBGA 200 Ball Assignment .....     | 9  |
| 4.3    | Dual-Die-Package (DDP) TFBGA 200 Ball Assignment .....       | 10 |
| 5.     | BALL/PAD/PIN CONFIGURATION .....                             | 11 |
| 5.1    | Ball/Pad/Pin Description .....                               | 11 |
| 5.2    | Addressing Table .....                                       | 12 |
| 6.     | BLOCK DIAGRAM .....                                          | 13 |
| 6.1    | Block diagram of single chip .....                           | 13 |
| 6.2    | Block diagram of Dual-Die-Package (DDP) .....                | 14 |
| 7.     | FUNCTIONAL DESCRIPTION .....                                 | 15 |
| 7.1    | Simplified LPDDR4/LPDDR4X State Diagram .....                | 15 |
| 7.1.1  | Simplified Bus Interface State Diagram .....                 | 16 |
| 7.2    | Power-up, Initialization, and Power-Off Procedure .....      | 18 |
| 7.2.1  | Voltage Ramp and Device Initialization .....                 | 18 |
| 7.2.2  | Reset Initialization with Stable Power .....                 | 20 |
| 7.2.3  | Power-off Sequence .....                                     | 20 |
| 7.2.4  | Uncontrolled Power-Off Sequence .....                        | 21 |
| 7.3    | Mode Register Definition .....                               | 22 |
| 7.3.1  | MR0 Register Information (MA[5:0] = 00 <sub>H</sub> ) .....  | 23 |
| 7.3.2  | MR1 Register Information (MA[5:0] = 01 <sub>H</sub> ) .....  | 24 |
| 7.3.3  | MR2 Register Information (MA[5:0] = 02 <sub>H</sub> ) .....  | 26 |
| 7.3.4  | MR3 Register Information (MA[5:0] = 03 <sub>H</sub> ) .....  | 27 |
| 7.3.5  | MR4 Register Information (MA[5:0] = 04 <sub>H</sub> ) .....  | 28 |
| 7.3.6  | MR5 Register Information (MA[5:0] = 05 <sub>H</sub> ) .....  | 28 |
| 7.3.7  | MR6 Register Information (MA[5:0] = 06 <sub>H</sub> ) .....  | 29 |
| 7.3.8  | MR7 Register Information (MA[5:0] = 07 <sub>H</sub> ) .....  | 29 |
| 7.3.9  | MR8 Register Information (MA[5:0] = 08 <sub>H</sub> ) .....  | 29 |
| 7.3.10 | MR9 Register Information (MA[5:0] = 09 <sub>H</sub> ) .....  | 29 |
| 7.3.11 | MR10 Register Information (MA[5:0] = 0A <sub>H</sub> ) ..... | 29 |
| 7.3.12 | MR11 Register Information (MA[5:0] = 0B <sub>H</sub> ) ..... | 30 |
| 7.3.13 | MR12 Register Information (MA[5:0] = 0C <sub>H</sub> ) ..... | 30 |
| 7.3.14 | MR13 Register Information (MA[5:0] = 0D <sub>H</sub> ) ..... | 32 |
| 7.3.15 | MR14 Register Information (MA[5:0] = 0E <sub>H</sub> ) ..... | 33 |
| 7.3.16 | MR15 Register Information (MA[5:0] = 0F <sub>H</sub> ) ..... | 35 |
| 7.3.17 | MR16 Register Information (MA[5:0] = 10 <sub>H</sub> ) ..... | 36 |
| 7.3.18 | MR17 Register Information (MA[5:0] = 11 <sub>H</sub> ) ..... | 36 |
| 7.3.19 | MR18 Register Information (MA[5:0] = 12 <sub>H</sub> ) ..... | 37 |
| 7.3.20 | MR19 Register Information (MA[5:0] = 13 <sub>H</sub> ) ..... | 37 |
| 7.3.21 | MR20 Register Information (MA[5:0] = 14 <sub>H</sub> ) ..... | 37 |
| 7.3.22 | MR21 Register Information (MA[5:0] = 15 <sub>H</sub> ) ..... | 38 |
| 7.3.23 | MR22 Register Information (MA[5:0] = 16 <sub>H</sub> ) ..... | 38 |
| 7.3.24 | MR23 Register Information (MA[5:0] = 17 <sub>H</sub> ) ..... | 39 |
| 7.3.25 | MR24 Register Information (MA[5:0] = 18 <sub>H</sub> ) ..... | 39 |
| 7.3.26 | MR25 Register Information (MA[5:0] = 19 <sub>H</sub> ) ..... | 40 |



|          |                                                                                     |     |
|----------|-------------------------------------------------------------------------------------|-----|
| 7.3.27   | MR26~29 Registers (Reserved) (MA[5:0] = 1A <sub>H</sub> -1D <sub>H</sub> ) .....    | 40  |
| 7.3.28   | MR30 Register Information (MA[5:0] = 1E <sub>H</sub> ) .....                        | 40  |
| 7.3.29   | MR31 Register (Reserved) (MA[5:0] = 1F <sub>H</sub> ) .....                         | 40  |
| 7.3.30   | MR32 Register Information (MA[5:0] = 20 <sub>H</sub> ) .....                        | 40  |
| 7.3.31   | MR33~38 Registers (Reserved) (MA[5:0] = 21 <sub>H</sub> -26 <sub>H</sub> ) .....    | 40  |
| 7.3.32   | MR39 Register Information (MA[5:0] = 27 <sub>H</sub> ) .....                        | 41  |
| 7.3.33   | MR40 Register Information (MA[5:0] = 28 <sub>H</sub> ) .....                        | 41  |
| 7.3.34   | MR41~50 Registers (Reserved) (MA[5:0] = 29 <sub>H</sub> -32 <sub>H</sub> ) .....    | 41  |
| 7.3.35   | MR51 Register Information (MA[5:0] = 33 <sub>H</sub> ) .....                        | 41  |
| 7.4      | Command Definitions and Timing Diagrams .....                                       | 42  |
| 7.4.1    | Activate Command .....                                                              | 42  |
| 7.4.1.1  | 8-Bank Device Operation .....                                                       | 42  |
| 7.4.2    | Core Timing .....                                                                   | 43  |
| 7.4.3    | Read and Write Access Operations .....                                              | 44  |
| 7.4.4    | Read Preamble and Postamble .....                                                   | 44  |
| 7.4.5    | Burst Read Operation .....                                                          | 45  |
| 7.4.6    | Read Timing .....                                                                   | 49  |
| 7.4.7    | tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation .....                              | 49  |
| 7.4.7.1  | tLZ(DQS) and tHZ(DQS) Calculation for ATE (Automatic Test Equipment) – LPDDR4 ..... | 50  |
| 7.4.7.2  | tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment) – LPDDR4 .....   | 52  |
| 7.4.7.3  | tRPRE Calculation for ATE (Automatic Test Equipment) – LPDDR4 .....                 | 54  |
| 7.4.7.4  | tRPST Calculation for ATE (Automatic Test Equipment) – LPDDR4 .....                 | 55  |
| 7.4.8    | tDQSCK Timing Table .....                                                           | 56  |
| 7.4.9    | Write Preamble and Postamble .....                                                  | 57  |
| 7.4.10   | Burst Write Operation .....                                                         | 58  |
| 7.4.11   | Write Timing .....                                                                  | 61  |
| 7.4.11.1 | tWPRE Calculation for ATE (Automatic Test Equipment) .....                          | 62  |
| 7.4.11.2 | tWPST Calculation for ATE (Automatic Test Equipment) .....                          | 63  |
| 7.4.12   | Read and Write Latencies .....                                                      | 64  |
| 7.4.13   | Write and Masked Write operation DQS controls (WDQS Control) .....                  | 64  |
| 7.4.13.1 | WDQS Control Mode 1 - Read Based Control .....                                      | 65  |
| 7.4.13.2 | WDQS Control Mode 2 - WDQS_on/off .....                                             | 65  |
| 7.4.14   | Postamble and Preamble merging behavior .....                                       | 70  |
| 7.4.14.1 | Read to Read Operation .....                                                        | 70  |
| 7.4.14.2 | Write to Write Operation .....                                                      | 83  |
| 7.4.15   | Masked Write Operation .....                                                        | 93  |
| 7.4.15.1 | Masked Write Timing constraints for BL16 .....                                      | 95  |
| 7.4.16   | Data Mask (DM) and Data Bus Inversion (DBI <sub>dc</sub> ) Function .....           | 97  |
| 7.4.17   | Precharge Operation .....                                                           | 100 |
| 7.4.17.1 | Burst Read Operation Followed by Precharge .....                                    | 101 |
| 7.4.17.2 | Burst Write Operation Followed by Precharge .....                                   | 102 |
| 7.4.17.3 | Auto-Precharge Operation .....                                                      | 102 |
| 7.4.17.4 | Burst Read with Auto-Precharge .....                                                | 103 |
| 7.4.17.5 | Burst Write with Auto-Precharge .....                                               | 104 |
| 7.4.18   | Auto-Precharge Operation .....                                                      | 105 |
| 7.4.18.1 | Delay time from Write to Read with Auto-Precharge .....                             | 106 |
| 7.4.19   | Refresh command .....                                                               | 110 |
| 7.4.19.1 | Burst Read operation followed by Per Bank Refresh .....                             | 116 |
| 7.4.20   | Refresh Requirement .....                                                           | 117 |
| 7.4.21   | Self Refresh Operation .....                                                        | 118 |
| 7.4.21.1 | Self Refresh Entry and Exit .....                                                   | 118 |
| 7.4.21.2 | Power Down Entry and Exit during Self Refresh .....                                 | 120 |
| 7.4.21.3 | Partial Array Self-Refresh (PASR) .....                                             | 121 |
| 7.4.21.4 | Command input Timing after Power Down Exit .....                                    | 122 |
| 7.4.21.5 | Self Refresh Timing Table .....                                                     | 123 |
| 7.4.22   | MRR, MRW, MPC Command during tXSR, tRFC .....                                       | 124 |



|          |                                                                                  |     |
|----------|----------------------------------------------------------------------------------|-----|
| 7.4.23   | Mode Register Read (MRR) .....                                                   | 125 |
| 7.4.23.1 | MRR after Read and Write command .....                                           | 127 |
| 7.4.23.2 | MRR after Power-Down Exit .....                                                  | 129 |
| 7.4.24   | Mode Register Write (MRW) Operation .....                                        | 130 |
| 7.4.24.1 | Mode Register Write .....                                                        | 130 |
| 7.4.25   | VREF Current Generator (VRCG) .....                                              | 132 |
| 7.4.26   | CA VREF Training .....                                                           | 133 |
| 7.4.27   | DQ VREF Training .....                                                           | 138 |
| 7.4.28   | Command Bus Training .....                                                       | 143 |
| 7.4.28.1 | Training Sequence for single-rank systems .....                                  | 144 |
| 7.4.28.2 | Training Sequence for multi-rank systems .....                                   | 144 |
| 7.4.28.3 | Relation between CA input pin DQ output pin .....                                | 145 |
| 7.4.28.4 | Timing Diagram .....                                                             | 145 |
| 7.4.28.5 | Command Bus Training AC Timing Table .....                                       | 150 |
| 7.4.29   | Frequency Set Point .....                                                        | 151 |
| 7.4.29.1 | Frequency set point update Timing .....                                          | 152 |
| 7.4.30   | Mode Register Write-WR Leveling Mode .....                                       | 156 |
| 7.4.30.1 | Write Leveling Procedure .....                                                   | 156 |
| 7.4.30.2 | Input Clock Frequency Stop and Change .....                                      | 158 |
| 7.4.30.3 | Write Leveling Setup and Hold Time .....                                         | 159 |
| 7.4.31   | RD DQ Calibration .....                                                          | 160 |
| 7.4.31.1 | RD DQ Calibration Training Procedure .....                                       | 160 |
| 7.4.31.2 | DQ Read Training Example .....                                                   | 163 |
| 7.4.31.3 | MPC of Read DQ Calibration after Power-Down Exit .....                           | 164 |
| 7.4.32   | DQS-DQ Training .....                                                            | 165 |
| 7.4.32.1 | FIFO Pointer Reset and Synchronism .....                                         | 166 |
| 7.4.33   | DQS Interval Oscillator .....                                                    | 171 |
| 7.4.33.1 | Interval Oscillator matching error .....                                         | 173 |
| 7.4.33.2 | DQS Interval Oscillator Readout Timing .....                                     | 174 |
| 7.4.34   | READ Preamble Training .....                                                     | 176 |
| 7.4.35   | Multi-Purpose Command (MPC) .....                                                | 177 |
| 7.4.36   | Thermal Offset .....                                                             | 181 |
| 7.4.37   | Temperature Sensor .....                                                         | 181 |
| 7.4.38   | ZQ Calibration .....                                                             | 183 |
| 7.4.38.1 | ZQCal Reset .....                                                                | 183 |
| 7.4.38.2 | ZQ External Resistor, Tolerance, and Capacitive Loading .....                    | 184 |
| 7.4.39   | Pull Up/Pull Down Driver Characteristics and Calibration – LPDDR4 .....          | 184 |
| 7.4.40   | On Die Termination for Command/Address Bus – LPDDR4 .....                        | 185 |
| 7.4.40.1 | ODT Mode Register and ODT State Table – LPDDR4 .....                             | 185 |
| 7.4.40.2 | ODT Mode Register and ODT Characteristics – LPDDR4 .....                         | 186 |
| 7.4.40.3 | ODT for Command/Address update time .....                                        | 189 |
| 7.4.41   | On-Die Termination .....                                                         | 190 |
| 7.4.41.1 | ODT Mode Register .....                                                          | 190 |
| 7.4.41.2 | Asynchronous ODT .....                                                           | 190 |
| 7.4.41.3 | ODT during Write Leveling .....                                                  | 192 |
| 7.4.42   | On Die Termination for DQ, DQS and DMI .....                                     | 193 |
| 7.4.43   | Output Driver and Termination Resistor Temperature and Voltage Sensitivity ..... | 196 |
| 7.4.44   | Power-Down Mode .....                                                            | 197 |
| 7.4.44.1 | Power-Down Entry and Exit .....                                                  | 197 |
| 7.4.45   | Input Clock Stop and Frequency Change .....                                      | 204 |
| 7.4.46   | Truth Tables .....                                                               | 206 |
| 7.4.47   | TRR Mode - Target Row Refresh .....                                              | 208 |
| 7.4.47.1 | TRR Mode Operation .....                                                         | 208 |
| 7.4.48   | Post Package Repair (PPR) .....                                                  | 210 |
| 7.4.48.1 | Fail Row Address Repair .....                                                    | 210 |
| 8.       | ELECTRICAL CHARACTERISTIC .....                                                  | 212 |
| 8.1      | Absolute Maximum DC Ratings .....                                                | 212 |



|          |                                                                                  |     |
|----------|----------------------------------------------------------------------------------|-----|
| 8.2      | AC & DC Operating Conditions .....                                               | 212 |
| 8.2.1    | Recommended DC Operating Conditions – LPDDR4 .....                               | 212 |
| 8.2.2    | Input Leakage Current.....                                                       | 212 |
| 8.2.3    | Input/Output Leakage Current .....                                               | 212 |
| 8.2.4    | Operating Temperature Range.....                                                 | 213 |
| 8.3      | AC and DC Input/Output Measurement levels .....                                  | 213 |
| 8.3.1    | DC electrical characteristics .....                                              | 213 |
| 8.3.1.1  | Input Level for CKE.....                                                         | 213 |
| 8.3.1.2  | Input Level for Reset_n and ODT_CA.....                                          | 214 |
| 8.3.2    | AC Over/Undershoot .....                                                         | 214 |
| 8.3.2.1  | LPDDR4/LPDDR4X AC Over/Undershoot.....                                           | 214 |
| 8.3.3    | Differential Input Voltage .....                                                 | 215 |
| 8.3.3.1  | Differential Input Voltage for CK.....                                           | 215 |
| 8.3.3.2  | Peak voltage calculation method.....                                             | 216 |
| 8.3.3.3  | Single-Ended Input Voltage for Clock.....                                        | 217 |
| 8.3.3.4  | Differential Input Slew Rate Definition for Clock .....                          | 218 |
| 8.3.3.5  | Differential Input Cross Point Voltage – LPDDR4 .....                            | 219 |
| 8.3.3.6  | Differential Input Voltage for DQS .....                                         | 220 |
| 8.3.3.7  | Peak voltage calculation method.....                                             | 221 |
| 8.3.3.8  | Single-Ended Input Voltage for DQS.....                                          | 222 |
| 8.3.3.9  | Differential Input Slew Rate Definition for DQS .....                            | 223 |
| 8.3.3.10 | Differential Input Cross Point Voltage.....                                      | 224 |
| 8.3.4    | Input level for ODT_CA input.....                                                | 225 |
| 8.3.5    | Single Ended Output Slew Rate .....                                              | 225 |
| 8.3.6    | Differential Output Slew Rate .....                                              | 226 |
| 8.3.7    | Overshoot and Undershoot for LVSTL.....                                          | 227 |
| 8.3.8    | Driver Output Timing Reference load.....                                         | 228 |
| 8.3.9    | LVSTL (Low Voltage Swing Terminated Logic) IO System for 1.1V VDDQ .....         | 228 |
| 8.4      | Input/Output Capacitance .....                                                   | 230 |
| 8.5      | IDD Specification Parameters and Test Conditions .....                           | 231 |
| 8.5.1    | IDD Measurement Conditions.....                                                  | 231 |
| 8.5.2    | IDD Specifications .....                                                         | 247 |
| 8.5.2.1  | LPDDR4 IDD Specification Parameters and Operating Conditions – Single Die.....   | 247 |
| 8.5.2.2  | LPDDR4X IDD Specification Parameters and Operating Conditions – Single Die ..... | 250 |
| 8.6      | Electrical Characteristics and AC Timing .....                                   | 253 |
| 8.6.1    | Clock Specification .....                                                        | 253 |
| 8.6.1.1  | Definition for tCK(avg) and nCK .....                                            | 253 |
| 8.6.1.2  | Definition for tCK(abs).....                                                     | 253 |
| 8.6.1.3  | Definition for tCH(avg) and tCL(avg) .....                                       | 254 |
| 8.6.1.4  | Definition for tCH(abs) and tCL(abs) .....                                       | 254 |
| 8.6.1.5  | Definition for tJIT(per) .....                                                   | 254 |
| 8.6.1.6  | Definition for tJIT(cc).....                                                     | 254 |
| 8.6.2    | Clock AC Timing.....                                                             | 255 |
| 8.6.3    | Temperature Derating for AC timing .....                                         | 255 |
| 8.6.4    | CA Rx voltage and timing .....                                                   | 256 |
| 8.6.5    | DRAM Data Timing .....                                                           | 259 |
| 8.6.6    | DQ Rx voltage and timing.....                                                    | 261 |
| 9.       | SINGLE-ENDED MODE FOR CLOCK AND STROBE .....                                     | 265 |
| 9.1      | Combination of Mode Register setting and ODT termination .....                   | 265 |
| 9.2      | Restriction of Single-ended mode .....                                           | 265 |
| 9.3      | Switching sequence between Differential and Single-ended.....                    | 266 |
| 9.4      | VRCG Enable timing.....                                                          | 270 |
| 9.5      | Command bus training procedure.....                                              | 271 |
| 9.6      | Reference level for Single-ended mode .....                                      | 273 |
| 9.7      | AC parameters for Single Ended (SE) .....                                        | 274 |
| 10.      | LPDDR4X SPECIFIC REQUIREMENT .....                                               | 275 |





|         |                                                                                            |     |
|---------|--------------------------------------------------------------------------------------------|-----|
| 10.1    | Mode Register Definition – LPDDR4X .....                                                   | 275 |
| 10.1.1  | MR0 Register Information (MA[5:0] = 00 <sub>H</sub> ) .....                                | 276 |
| 10.1.2  | MR3 Register Information (MA[5:0] = 03 <sub>H</sub> ) .....                                | 277 |
| 10.1.3  | MR12 Register Information (MA[5:0] = 0C <sub>H</sub> ) .....                               | 278 |
| 10.1.4  | MR14 Register Information (MA[5:0] = 0E <sub>H</sub> ) .....                               | 280 |
| 10.1.5  | MR22 Register Information (MA[5:0] = 16 <sub>H</sub> ) .....                               | 282 |
| 10.2    | Pull Up/Pull Down Driver Characteristics and Calibration - LPDDR4X .....                   | 283 |
| 10.3    | ODT Mode Register and ODT Characteristics - LPDDR4X .....                                  | 283 |
| 10.4    | On Die Termination for DQ, DQS and DMI - LPDDR4X .....                                     | 285 |
| 10.5    | Output Driver and Termination Resistor Temperature and Voltage Sensitivity - LPDDR4X ..... | 287 |
| 10.6    | AC & DC Operating Conditions for LPDDR4X .....                                             | 288 |
| 10.6.1  | Recommended DC Operating Conditions .....                                                  | 288 |
| 10.6.2  | Single Ended Output Slew Rate .....                                                        | 288 |
| 10.7    | Differential Output Slew Rate .....                                                        | 289 |
| 10.8    | VREF Specifications - LPDDR4X .....                                                        | 290 |
| 10.8.1  | CA Internal VREF Specifications for LPDDR4X .....                                          | 290 |
| 10.8.2  | DQ Internal VREF Specifications for LPDDR4X .....                                          | 291 |
| 10.9    | Power-up, Initialization, and Power-Off Procedure – LPDDR4X .....                          | 292 |
| 10.10   | On Die Termination for Command/Address Bus - LPDDR4X .....                                 | 293 |
| 10.10.1 | ODT Mode Register and ODT State Table .....                                                | 293 |
| 10.11   | Core Timing - LPDDR4X .....                                                                | 294 |
| 10.12   | Burst READ Operation - LPDDR4X ATE Condition .....                                         | 294 |
| 10.12.1 | tLZ(DQS) and tHZ(DQS) Calculation for ATE (Automatic Test Equipment) – LPDDR4X .....       | 294 |
| 10.12.2 | tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment) – LPDDR4X .....         | 296 |
| 10.12.3 | tRPRE Calculation for ATE (Automatic Test Equipment) – LPDDR4X .....                       | 298 |
| 10.12.4 | tRPST Calculation for ATE (Automatic Test Equipment) – LPDDR4X .....                       | 299 |
| 10.13   | Differential Input Cross Point Voltage – LPDDR4X .....                                     | 300 |
| 10.13.1 | Differential Input Cross Point Voltage .....                                               | 300 |
| 10.14   | LVSTL (Low Voltage Swing Terminated Logic) IO System for 0.6V VDDQ .....                   | 301 |
| 11.     | PACKAGE DIMENSIONS .....                                                                   | 302 |
| 11.1    | VFBGA 100 Ball .....                                                                       | 302 |
| 11.2    | TFBGA 200 Ball .....                                                                       | 303 |
| 12.     | REVISION HISTORY .....                                                                     | 304 |



## 1. GENERAL DESCRIPTION

This datasheet specifies LPDDR4/LPDDR4X combo SDRAM with either one of following configurations.

Single-Die-Package (SDP) 32Mb x 16DQ x 8-banks x 1 channel with 4 Gb (4,294,967,296 bits) density.

Dual-Die-Package (DDP) 32Mb x 16DQ x 8-banks x 2 channels with 8 Gb (8,589,934,592 bits) density.

The LPDDR4/LPDDR4X combo SDRAM uses a 2 or 4 clocks architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information. Each command uses 1, 2 or 4 clock cycle, during which command information is transferred on the positive edge of the clock. See command truth table for details.

The LPDDR4/LPDDR4X combo SDRAM will operate as LPDDR4 mode while the VDDQ supply voltage is 1.1 Voltage or as LPDDR4X mode while the VDDQ supply voltage is 0.6 Voltages.

While the LPDDR4/LPDDR4X combo SDRAM operate as LPDDR4X mode, some specifications different to the LPDDR4 mode are defined in section of “**LPDDR4X SPECIFIC REQUIREMENT**”.

## 2. FEATURES

- |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>• Power supply (VDD1, VDD2, VDDQ):               <ul style="list-style-type: none"> <li>- VDD1: 1.70V~1.95V;1.8V typical</li> <li>- VDD2: 1.06V~1.17V;1.1V typical</li> <li>- VDDQ: 1.06V~1.17V;1.1V typical (For LPDDR4)</li> <li>- VDDQ: 0.57V~0.65V;0.6V typical (For LPDDR4X)</li> </ul> </li> <li>• Data width: x16/x32</li> <li>• Clock rate: up to 2133 MHz</li> <li>• Data rate: up to 4267 Mbps</li> <li>• 8 internal banks for concurrent operation</li> <li>• 16n pre-fetch operation</li> <li>• Interface:               <ul style="list-style-type: none"> <li>- LVSTL_11 (For LPDDR4)</li> <li>- LVSTL06 (For LPDDR4X)</li> </ul> </li> <li>• Burst length: 16, 32, on-the-fly 16 or 32</li> <li>• Burst type: Sequential</li> <li>• Programmable Driver strength</li> <li>• Coded command input in double clock edges</li> <li>• Single data rate architecture on the CA bus</li> <li>• Double data rate architecture on the DQ pins</li> <li>• Differential clock input</li> <li>• Bidirectional differential data strobe</li> </ul> | <ul style="list-style-type: none"> <li>• Input clock stop and frequency change</li> <li>• On-die termination (ODT)</li> <li>• Write leveling support</li> <li>• Programmable Read and Write Latencies (RL/WL)</li> <li>• CA training support</li> <li>• DQ-DQS training</li> <li>• Refresh feature:               <ul style="list-style-type: none"> <li>- Auto Refresh (per bank / all bank)</li> <li>- Partial array self-refresh</li> <li>- Auto temperature compensated self-refresh</li> </ul> </li> <li>• Post Package Repair</li> <li>• Target Row Refresh Mode</li> <li>• Frequency-Set-Points for fast frequency switch</li> <li>• Support write mask and data bus inversion (DBI)</li> <li>• Support Single Ended CK and DQS</li> <li>• Support Low speed CA buffer</li> <li>• Support package:               <ul style="list-style-type: none"> <li>VFBGA 100 Ball (10x7.5mm<sup>2</sup> with thickness of 1.0 mm)</li> <li>TFBGA 200 Ball (10x14.5mm<sup>2</sup> with thickness of 1.1 mm)</li> </ul> </li> <li>• Operating Temperature Range:               <ul style="list-style-type: none"> <li>-40°C ≤ TCASE ≤ 105°C</li> </ul> </li> </ul> |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|



### 3. ORDER INFORMATION

| Part Number  | VDD1/VDD2/VDDQ        | I/O Width | Type                 | Others                      |
|--------------|-----------------------|-----------|----------------------|-----------------------------|
| W66CP6RBHAFJ | 1.8V/1.1V/1.1 or 0.6V | 16        | VFBGA 100 ball (SDP) | LPDDR4/4X-3200, -40°C~105°C |
| W66CP6RBHAGJ | 1.8V/1.1V/1.1 or 0.6V | 16        | VFBGA 100 ball (SDP) | LPDDR4/4X-3733, -40°C~105°C |
| W66CP6RBHAHJ | 1.8V/1.1V/1.1 or 0.6V | 16        | VFBGA 100 ball (SDP) | LPDDR4/4X-4267, -40°C~105°C |
| W66CP6RBQAFJ | 1.8V/1.1V/1.1 or 0.6V | 16        | TFBGA 200 ball (SDP) | LPDDR4/4X-3200, -40°C~105°C |
| W66CP6RBQAGJ | 1.8V/1.1V/1.1 or 0.6V | 16        | TFBGA 200 ball (SDP) | LPDDR4/4X-3733, -40°C~105°C |
| W66CP6RBQAHJ | 1.8V/1.1V/1.1 or 0.6V | 16        | TFBGA 200 ball (SDP) | LPDDR4/4X-4267, -40°C~105°C |
| W66DP2RQQAFJ | 1.8V/1.1V/1.1 or 0.6V | 32        | TFBGA 200 ball (DDP) | LPDDR4/4X-3200, -40°C~105°C |
| W66DP2RQQAGJ | 1.8V/1.1V/1.1 or 0.6V | 32        | TFBGA 200 ball (DDP) | LPDDR4/4X-3733, -40°C~105°C |
| W66DP2RQQAHJ | 1.8V/1.1V/1.1 or 0.6V | 32        | TFBGA 200 ball (DDP) | LPDDR4/4X-4267, -40°C~105°C |



#### 4. BALL ASSIGNMENT

##### 4.1 Single-Die-Package (SDP) VFBGA 100 Ball Assignment

[Top View]

|   | 1    | 2      | 3      | 4    | 5    | 6 | 7 | 8    | 9    | 10     | 11      | 12   |
|---|------|--------|--------|------|------|---|---|------|------|--------|---------|------|
| A | DNU  | DNU    | VSS    | VDD2 | ZQ0  |   |   | NC   | VDD2 | VSS    | DNU     | DNU  |
| B | DNU  | DQ0    | VDDQ   | DQ7  | VDDQ |   |   | VDDQ | DQ15 | VDDQ   | DQ8     | DNU  |
| C | VSS  | DQ1    | DMI0   | DQ6  | VSS  |   |   | VSS  | DQ14 | DMI1   | DQ9     | VSS  |
| D | VDDQ | VSS    | DQS0_t | VSS  | VDDQ |   |   | VDDQ | VSS  | DQS1_t | VSS     | VDDQ |
| E | VSS  | DQ2    | DQS0_c | DQ5  | VSS  |   |   | VSS  | DQ13 | DQS1_c | DQ10    | VSS  |
| F | VDD1 | DQ3    | VDDQ   | DQ4  | VDD2 |   |   | VDD2 | DQ12 | VDDQ   | DQ11    | VDD1 |
| G | VSS  | ODT_CA | VSS    | VDD1 | VSS  |   |   | VSS  | VDD1 | VSS    | RESET_n | VSS  |
| H | VDD2 | CA0    | NC     | CS0  | VDD2 |   |   | VDD2 | CA2  | CA3    | CA4     | VDD2 |
| J | VSS  | CA1    | VSS    | CKE0 | NC   |   |   | CK_t | CK_c | VSS    | CA5     | VSS  |
| K | VDD2 | VSS    | VDD2   | VSS  | NC   |   |   | NC   | VSS  | VDD2   | VSS     | VDD2 |

VFBGA 100 Ball Assignments for SDP



## 4.2 Single-Die-Package (SDP) TFBGA 200 Ball Assignment

[Top View]

|    | 1    | 2        | 3        | 4      | 5    | 6 | 7 | 8      | 9      | 10       | 11      | 12   |
|----|------|----------|----------|--------|------|---|---|--------|--------|----------|---------|------|
| A  | DNU  | DNU      | VSS      | VDD2   | ZQ0  |   |   | NC     | VDD2   | VSS      | DNU     | DNU  |
| B  | DNU  | DQ0_A    | VDDQ     | DQ7_A  | VDDQ |   |   | VDDQ   | DQ15_A | VDDQ     | DQ8_A   | DNU  |
| C  | VSS  | DQ1_A    | DMI0_A   | DQ6_A  | VSS  |   |   | VSS    | DQ14_A | DMI1_A   | DQ9_A   | VSS  |
| D  | VDDQ | VSS      | DQS0_t_A | VSS    | VDDQ |   |   | VDDQ   | VSS    | DQS1_t_A | VSS     | VDDQ |
| E  | VSS  | DQ2_A    | DQS0_c_A | DQ5_A  | VSS  |   |   | VSS    | DQ13_A | DQS1_c_A | DQ10_A  | VSS  |
| F  | VDD1 | DQ3_A    | VDDQ     | DQ4_A  | VDD2 |   |   | VDD2   | DQ12_A | VDDQ     | DQ11_A  | VDD1 |
| G  | VSS  | ODT_CA_A | VSS      | VDD1   | VSS  |   |   | VSS    | VDD1   | VSS      | NC      | VSS  |
| H  | VDD2 | CA0_A    | NC       | CS0_A  | VDD2 |   |   | VDD2   | CA2_A  | CA3_A    | CA4_A   | VDD2 |
| J  | VSS  | CA1_A    | VSS      | CKE0_A | NC   |   |   | CK_t_A | CK_c_A | VSS      | CA5_A   | VSS  |
| K  | VDD2 | VSS      | VDD2     | VSS    | NC   |   |   | NC     | VSS    | VDD2     | VSS     | VDD2 |
| L  |      |          |          |        |      |   |   |        |        |          |         |      |
| M  |      |          |          |        |      |   |   |        |        |          |         |      |
| N  | VDD2 | VSS      | VDD2     | VSS    | NC   |   |   | NC     | VSS    | VDD2     | VSS     | VDD2 |
| P  | VSS  | NC       | VSS      | NC     | NC   |   |   | NC     | NC     | VSS      | NC      | VSS  |
| R  | VDD2 | NC       | NC       | NC     | VDD2 |   |   | VDD2   | NC     | NC       | NC      | VDD2 |
| T  | VSS  | NC       | VSS      | VDD1   | VSS  |   |   | VSS    | VDD1   | VSS      | RESET_n | VSS  |
| U  | VDD1 | NC       | VDDQ     | NC     | VDD2 |   |   | VDD2   | NC     | VDDQ     | NC      | VDD1 |
| V  | VSS  | NC       | NC       | NC     | VSS  |   |   | VSS    | NC     | NC       | NC      | VSS  |
| W  | VDDQ | VSS      | NC       | VSS    | VDDQ |   |   | VDDQ   | VSS    | NC       | VSS     | VDDQ |
| Y  | VSS  | NC       | NC       | NC     | VSS  |   |   | VSS    | NC     | NC       | NC      | VSS  |
| AA | DNU  | NC       | VDDQ     | NC     | VDDQ |   |   | VDDQ   | NC     | VDDQ     | NC      | DNU  |
| AB | DNU  | DNU      | VSS      | VDD2   | VSS  |   |   | VSS    | VDD2   | VSS      | DNU     | DNU  |

TFBGA 200 Ball Assignments for SDP



### 4.3 Dual-Die-Package (DDP) TFBGA 200 Ball Assignment

[Top View]

|    | 1    | 2        | 3        | 4      | 5    | 6 | 7 | 8      | 9      | 10       | 11      | 12   |
|----|------|----------|----------|--------|------|---|---|--------|--------|----------|---------|------|
| A  | DNU  | DNU      | VSS      | VDD2   | ZQ0  |   |   | NC     | VDD2   | VSS      | DNU     | DNU  |
| B  | DNU  | DQ0_A    | VDDQ     | DQ7_A  | VDDQ |   |   | VDDQ   | DQ15_A | VDDQ     | DQ8_A   | DNU  |
| C  | VSS  | DQ1_A    | DMI0_A   | DQ6_A  | VSS  |   |   | VSS    | DQ14_A | DMI1_A   | DQ9_A   | VSS  |
| D  | VDDQ | VSS      | DQS0_t_A | VSS    | VDDQ |   |   | VDDQ   | VSS    | DQS1_t_A | VSS     | VDDQ |
| E  | VSS  | DQ2_A    | DQS0_c_A | DQ5_A  | VSS  |   |   | VSS    | DQ13_A | DQS1_c_A | DQ10_A  | VSS  |
| F  | VDD1 | DQ3_A    | VDDQ     | DQ4_A  | VDD2 |   |   | VDD2   | DQ12_A | VDDQ     | DQ11_A  | VDD1 |
| G  | VSS  | ODT_CA_A | VSS      | VDD1   | VSS  |   |   | VSS    | VDD1   | VSS      | NC      | VSS  |
| H  | VDD2 | CA0_A    | NC       | CS0_A  | VDD2 |   |   | VDD2   | CA2_A  | CA3_A    | CA4_A   | VDD2 |
| J  | VSS  | CA1_A    | VSS      | CKE0_A | NC   |   |   | CK_t_A | CK_c_A | VSS      | CA5_A   | VSS  |
| K  | VDD2 | VSS      | VDD2     | VSS    | NC   |   |   | NC     | VSS    | VDD2     | VSS     | VDD2 |
| L  |      |          |          |        |      |   |   |        |        |          |         |      |
| M  |      |          |          |        |      |   |   |        |        |          |         |      |
| N  | VDD2 | VSS      | VDD2     | VSS    | NC   |   |   | NC     | VSS    | VDD2     | VSS     | VDD2 |
| P  | VSS  | CA1_B    | VSS      | CKE0_B | NC   |   |   | CK_t_B | CK_c_B | VSS      | CA5_B   | VSS  |
| R  | VDD2 | CA0_B    | NC       | CS0_B  | VDD2 |   |   | VDD2   | CA2_B  | CA3_B    | CA4_B   | VDD2 |
| T  | VSS  | ODT_CA_B | VSS      | VDD1   | VSS  |   |   | VSS    | VDD1   | VSS      | RESET_n | VSS  |
| U  | VDD1 | DQ3_B    | VDDQ     | DQ4_B  | VDD2 |   |   | VDD2   | DQ12_B | VDDQ     | DQ11_B  | VDD1 |
| V  | VSS  | DQ2_B    | DQS0_c_B | DQ5_B  | VSS  |   |   | VSS    | DQ13_B | DQS1_c_B | DQ10_B  | VSS  |
| W  | VDDQ | VSS      | DQS0_t_B | VSS    | VDDQ |   |   | VDDQ   | VSS    | DQS1_t_B | VSS     | VDDQ |
| Y  | VSS  | DQ1_B    | DMI0_B   | DQ6_B  | VSS  |   |   | VSS    | DQ14_B | DMI1_B   | DQ9_B   | VSS  |
| AA | DNU  | DQ0_B    | VDDQ     | DQ7_B  | VDDQ |   |   | VDDQ   | DQ15_B | VDDQ     | DQ8_B   | DNU  |
| AB | DNU  | DNU      | VSS      | VDD2   | VSS  |   |   | VSS    | VDD2   | VSS      | DNU     | DNU  |

TFBGA 200 Ball Assignment for DDP





## 5. BALL/PAD/PIN CONFIGURATION

### 5.1 Ball/Pad/Pin Description

| Name                                                            | Type      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----------------------------------------------------------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CK_t_A, CK_c_A,<br>CK_t_B, CK_c_B                               | Input     | <b>Clock:</b> CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.                                                                                                                                                                                                                            |
| CKE_A, CKE_B                                                    | Input     | <b>Clock Enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.                                                                                                                                                                                                                                                  |
| CS_A, CS_B                                                      | Input     | <b>Chip Select:</b> CS is part of the command code. Each channel (A & B) has its own CS signal.                                                                                                                                                                                                                                                                                                                                                                                                                               |
| CA[5:0]_A,<br>CA[5:0]_B                                         | Input     | <b>Command/Address Inputs:</b> CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A & B) has its own CA signals.                                                                                                                                                                                                                                                                                                                                                           |
| ODT_CA_A,<br>ODT_CA_B                                           | Input     | <b>LPDDR4 CA CA ODT Control:</b> The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.<br><b>LPDDR4X CA ODT Control:</b> The ODT_CA pin is ignored by LPDDR4X devices. ODT-CS/CA/CK function is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either VDD2 or VSS.                                                                                                                                                                    |
| DQ[15:0]_A,<br>DQ[15:0]_B                                       | I/O       | <b>Data Inputs/Output:</b> Bi-directional data bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| DQS[1:0]_t_A,<br>DQS[1:0]_c_A,<br>DQS[1:0]_t_B,<br>DQS[1:0]_c_B | I/O       | <b>Data Strobe:</b> DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.                                                                                                       |
| DMI[1:0]_A,<br>DMI[1:0]_B                                       | I/O       | <b>Data Mask Inversion:</b> DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting. |
| RESET_n                                                         | Input     | <b>RESET:</b> When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.                                                                                                                                                                                                                                                                                                                                                                                                         |
| VDDQ, VDD1,<br>VDD2                                             | Supply    | <b>Power Supplies:</b> Isolated on the die for improved noise immunity.                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| VSS, VSSQ                                                       | Supply    | <b>Ground Reference:</b> Power supply ground reference.                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| ZQ0                                                             | Reference | <b>Calibration Reference:</b> Used to calibrate the output drive strength and the termination resistance. The ZQ0 pin shall be connected to VDDQ through a $240\Omega \pm 1\%$ resistor.                                                                                                                                                                                                                                                                                                                                      |
| DNU                                                             | --        | <b>Do Not Use</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| NC                                                              | --        | <b>No connect:</b> Not internally connected.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

#### Notes:

- For this package device ball, pad and pin are same meaning. Meanwhile, the VSSQ mentioned in this datasheet are connected to VSS inside package
- "\_A" and "\_B" indicate DRAM channel.



## 5.2 Addressing Table

|                                      |                  | 256M x 16                            | 256M x 32                             |
|--------------------------------------|------------------|--------------------------------------|---------------------------------------|
| Die per package                      |                  | 1                                    | 2                                     |
| Memory Density (per package)         |                  | 4 Gb                                 | 8 Gb                                  |
| Memory Density (per die)             |                  | 4 Gb                                 | 4 Gb                                  |
| Memory Density (per channel)         |                  | 4 Gb                                 | 4 Gb                                  |
| Configuration                        |                  | 32 Mb x 16 DQs x 8 banks x 1 channel | 32 Mb x 16 DQs x 8 banks x 2 channels |
| Number of Channels (per die)         |                  | 1                                    | 1                                     |
| Number of Banks (per channel)        |                  | 8                                    | 8                                     |
| Array Pre-Fetch (bits, per channel)  |                  | 256                                  | 256                                   |
| Number of Rows (per channel)         |                  | 32768                                | 32768                                 |
| Number of Columns (fetch boundaries) |                  | 64                                   | 64                                    |
| Page Size (Bytes)                    |                  | 2048                                 | 2048                                  |
| Bank Address                         |                  | BA0 – BA2                            | BA0 – BA2                             |
| x16                                  | Row Addresses    | R0 – R14                             | R0 – R14                              |
|                                      | Column Addresses | C0 – C9                              | C0 – C9                               |
| Burst Starting Address Boundary      |                  | 64 bits                              | 64 bits                               |

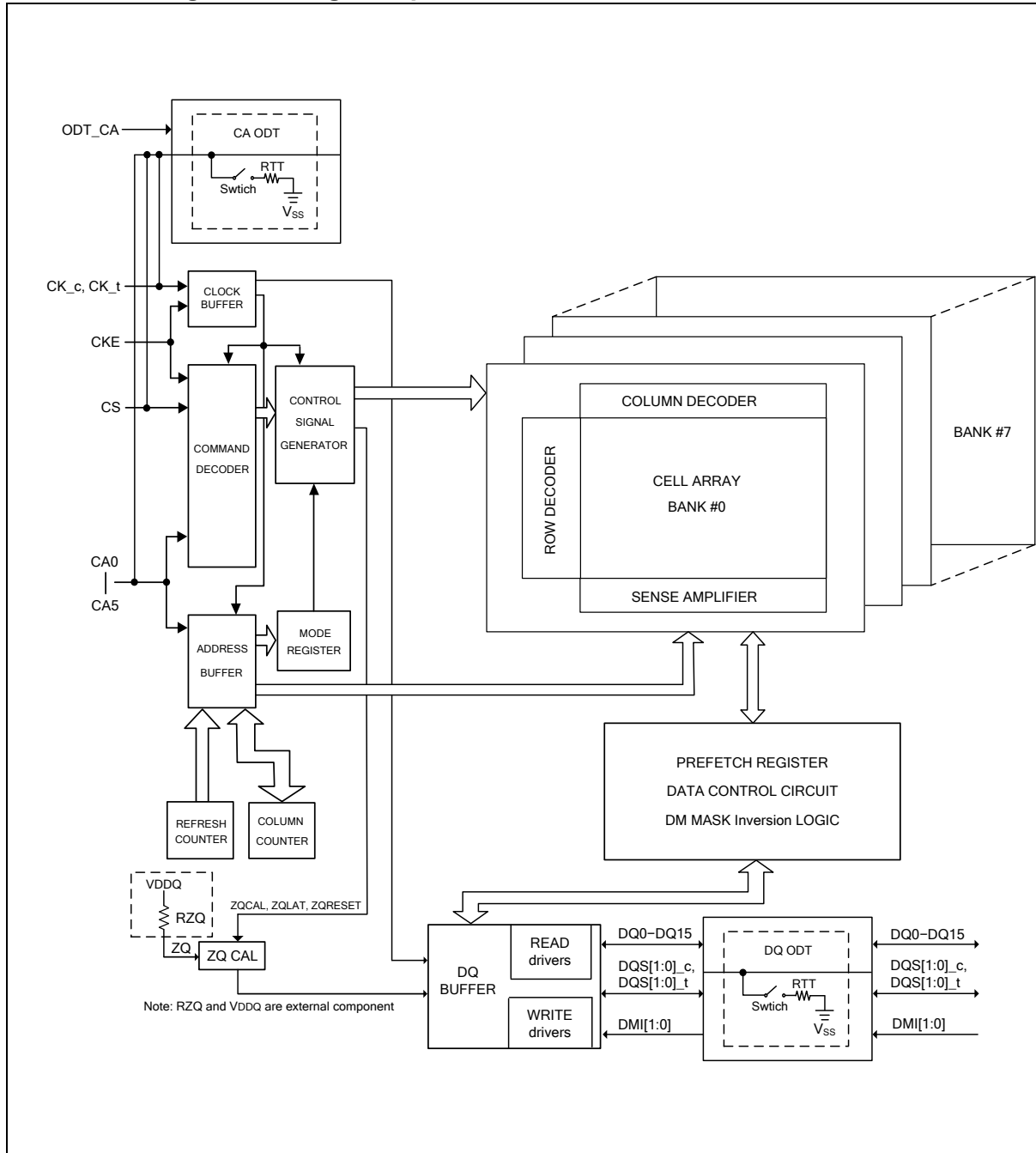
### Note:

1. The lower two column addresses (C0 - C1) are assumed to be "zero" and are not transmitted on the CA bus.



## 6. BLOCK DIAGRAM

### 6.1 Block diagram of single chip

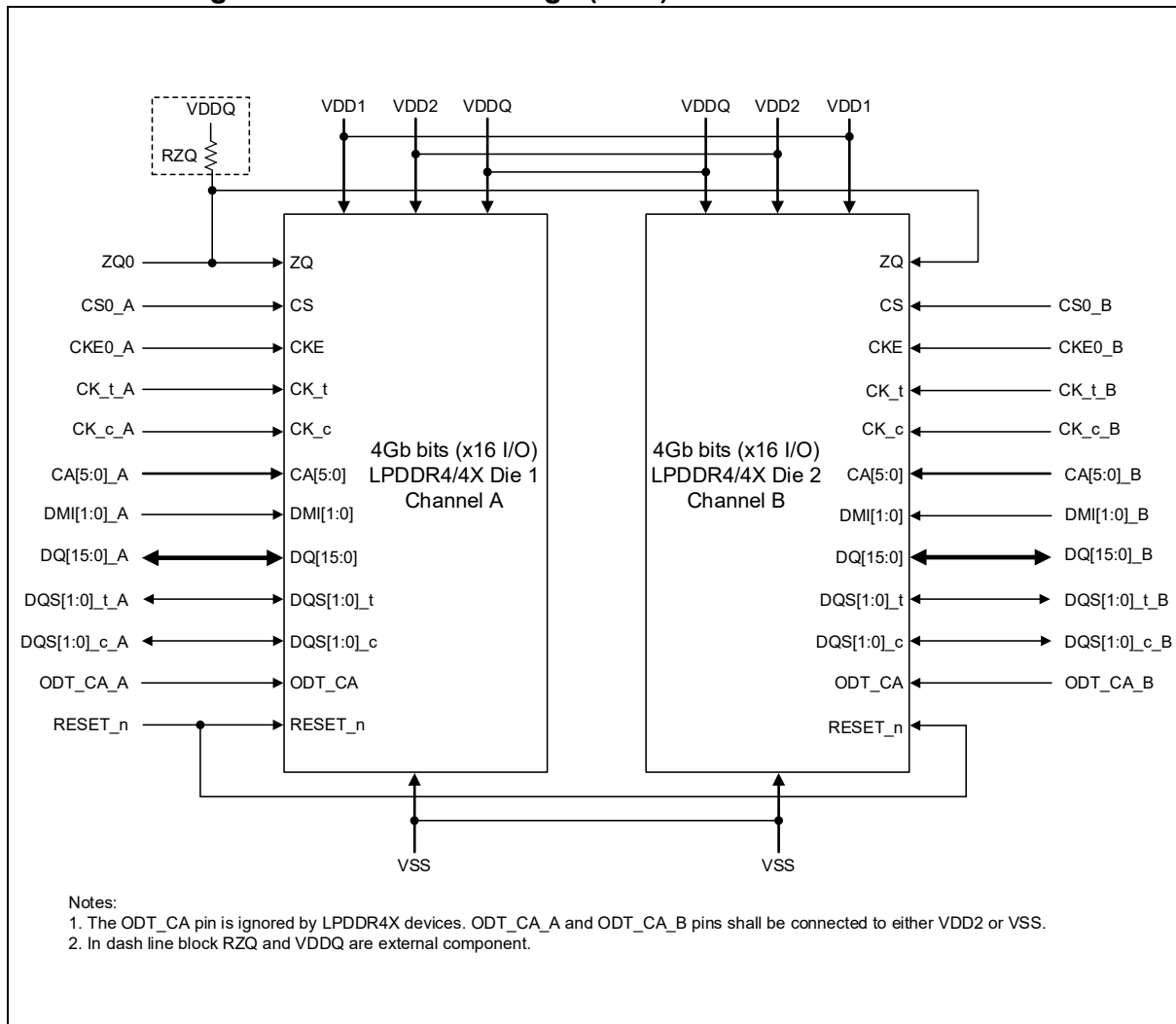


#### Notes:

1. In LPDDR4 mode ODT\_CA pin connected ODT\_CA.
2. In LPDDR4X mode ODT\_CA pin shall be connected to either VDD2 or VSS.



## 6.2 Block diagram of Dual-Die-Package (DDP)





## 7. FUNCTIONAL DESCRIPTION

For The LPDDR4/LPDDR4X SDRAM, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

This device also uses double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a  $16n$  prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR4/LPDDR4X SDRAM effectively consists of a single  $16n$ -bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding  $n$ -bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to The LPDDR4/LPDDR4X SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Prior to normal operation, The LPDDR4/LPDDR4X SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

### 7.1 Simplified LPDDR4/LPDDR4X State Diagram

LPDDR4/LPDDR4X SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram; they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see chapter 7.4 “**Command Definitions and Timing Diagrams**”.



### 7.1.1 Simplified Bus Interface State Diagram

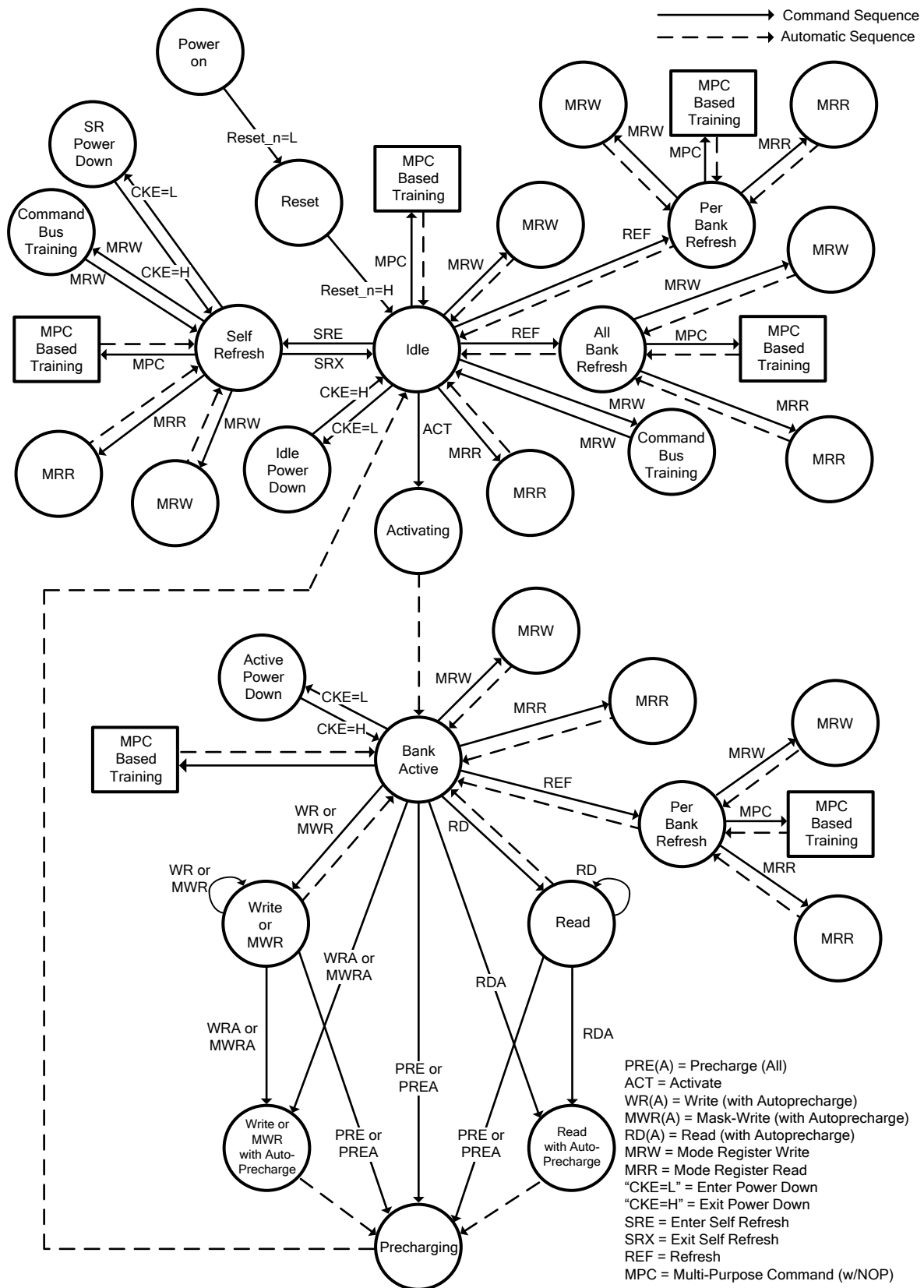
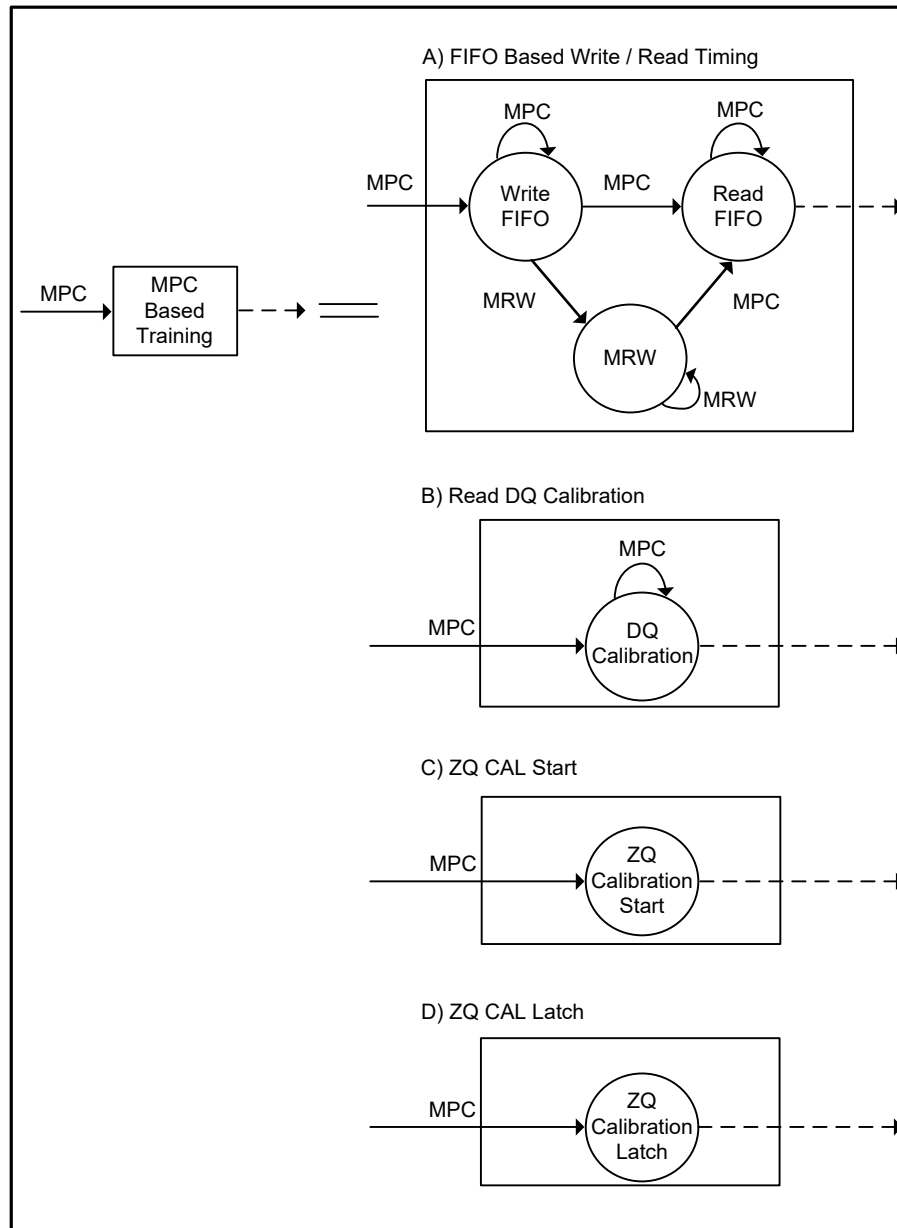


Figure 1 - Simplified Bus Interface State Diagram-1



**Figure 2 - Simplified Bus Interface State Diagram-2**

**Notes:**

1. From the Self Refresh state the device can enter Power-Down, MRR, MRW, or MPC states. See the section on Self Refresh for more information.
2. In Idle state, all banks are precharged.
3. In the case of a MRW command to enter a training mode, the state machine will not automatically return to the Idle state at the conclusion of training. See section 7.4.24 for more information.
4. In the case of a MPC command to enter a training mode, the state machine may not automatically return to the Idle state at the conclusion of training. See section 7.4.35 for more information.
5. This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (Ex. MRW from either Idle or Active states) will return to the state from when they were initiated (Ex. MRW from Idle will return to Idle).
7. The RESET\_n pin can be asserted from any state, and will cause the SDRAM to go to the Reset State. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET\_n.



## 7.2 Power-up, Initialization, and Power-Off Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as the table below.

**Table 1 - MRS defaults settings – LPDDR4**

| Item             | MRS          | Default Setting | Description                     |
|------------------|--------------|-----------------|---------------------------------|
| FSP-OP/WR        | MR13 OP[7:6] | 00B             | FSP-OP/WR[0] are enabled        |
| WLS              | MR2 OP[6]    | 0B              | Write Latency Set A is selected |
| WL               | MR2 OP[5:3]  | 000B            | WL = 4                          |
| RL               | MR2 OP[2:0]  | 000B            | RL = 6, nRTP=8                  |
| nWR              | MR1 OP[6:4]  | 000B            | nWR = 6                         |
| DBI-WR/RD        | MR3 OP[7:6]  | 00B             | Write & Read DBI are disabled   |
| CA ODT           | MR11 OP[6:4] | 000B            | CA ODT is disabled              |
| DQ ODT           | MR11 OP[2:0] | 000B            | DQ ODT is disabled              |
| VREF(CA) Setting | MR12 OP[6]   | 1B              | VREF(CA) Range[1] enabled       |
| VREF(CA) Value   | MR12 OP[5:0] | 001101B         | Range1 : 27.2% of VDD2          |
| VREF(DQ) Setting | MR14 OP[6]   | 1B              | VREF(DQ) Range[1] enabled       |
| VREF(DQ) Value   | MR14 OP[5:0] | 001101B         | Range1 : 27.2% of VDDQ          |

### 7.2.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4/LPDDR4X SDRAM. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after  $T_a$ ), RESET\_n is recommended to be LOW ( $\leq 0.2 \times VDD2$ ) and all other inputs must be between  $V_{ILmin}$  and  $V_{IHmax}$ . The device outputs remain at High-Z while RESET\_n is held LOW. Power supply voltage ramp requirements are provided in Table 2. VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

**Table 2 - Voltage Ramp Conditions**

| After         | Applicable Conditions                  |
|---------------|----------------------------------------|
| Ta is reached | VDD1 must be greater than VDD2         |
|               | VDD2 must be greater than VDDQ - 200mV |

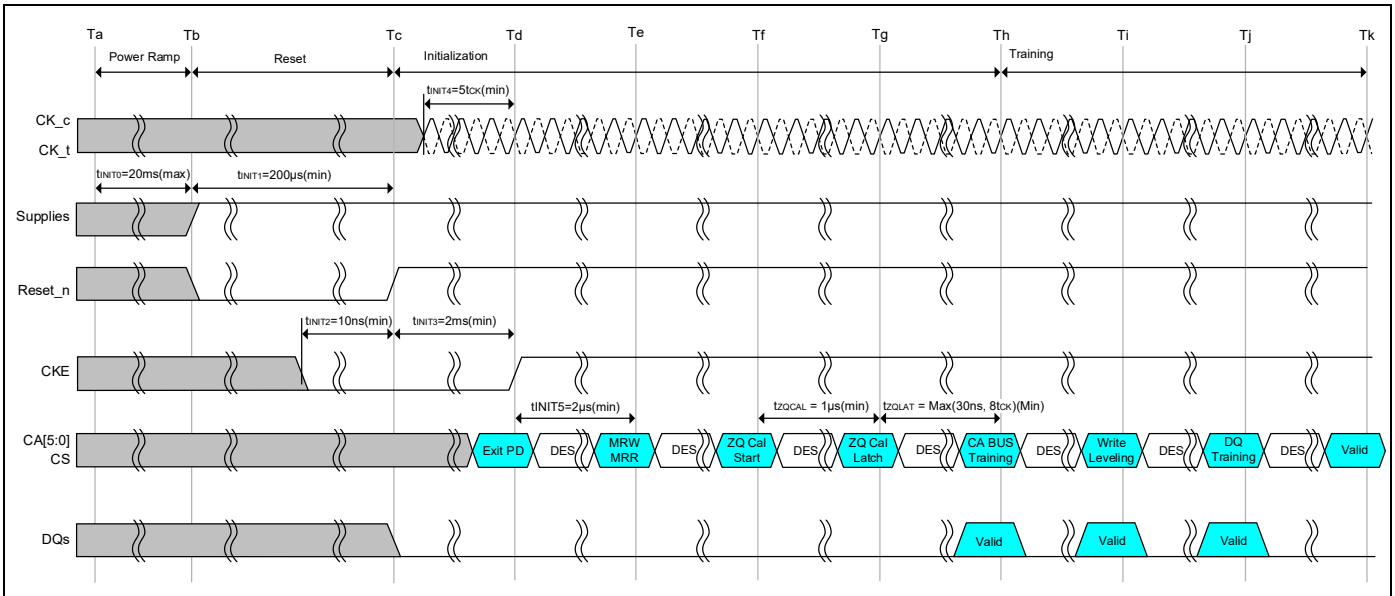
**Notes:**

1.  $T_a$  is the point when any power supply first reaches 300 mV.
2. Noted voltage ramp conditions in Table 2 apply between  $T_a$  and power-off (controlled or uncontrolled).
3.  $T_b$  is the point at which all supply and reference voltages are within their defined ranges.
4. Power ramp duration  $t_{INIT0}$  ( $T_b - T_a$ ) must not exceed 20 mS.
5. The voltage difference between of VSS and VSSQ pin must not exceed 100 mV.
2. Following the completion of the voltage ramp ( $T_b$ ), RESET\_n must be maintained LOW. DQ, DMI, DQS\_t and DQS\_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. CKE, CK\_t, CK\_c, CS\_n and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.
3. Beginning at  $T_b$ , RESET\_n must remain LOW for at least  $t_{INIT1}$  ( $T_c$ ), after which RESET\_n can be deasserted to HIGH ( $T_c$ ). At least 10ns before RESET\_n de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".
4. After RESET\_n is de-asserted ( $T_c$ ), wait at least  $t_{INIT3}$  before activating CKE. Clock (CK\_t, CK\_c) is required to be started and stabilized for  $t_{INIT4}$  before CKE goes active ( $T_d$ ). CS is required to be maintained LOW when controller activates CKE.
5. After setting CKE high, wait minimum of  $t_{INIT5}$  to issue any MRR or MRW commands ( $T_e$ ). For both MRR and MRW commands, the clock frequency must be within the range defined for  $t_{CKb}$ . Some AC parameters (for example,  $t_{DQSCK}$ ) could have relaxed timings (such as  $t_{DQSCKb}$ ) before the system is appropriately configured.





6. After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory (Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4/LPDDR4X SDRAMs share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4/LPDDR4X SDRAM. ZQ calibration sequence is completed after tZQCAL(Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.
  7. After tZQLAT is satisfied (Th) the command bus (internal VREF (CA), CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR4/LPDDR4X SDRAM will power-up with receivers configured for low-speed operations, and VREF (CA) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.
- NOTE:** The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See section 7.4.28 for information on how to enter/exit the training mode.
8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high (Ti). See section 7.4.30, Mode Register Write-WR Leveling Mode, for detailed description of write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS\_t/c timing to the point where the LPDDR4/LPDDR4X SDRAM recognizes the start of write DQ data burst with desired write latency.
  9. After write leveling, the DQ Bus (internal VREF (DQ), DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust VREF (DQ) (Tj). The LPDDR4/LPDDR4X SDRAM will power-up with receivers configured for low-speed operations and VREF (DQ) set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See DQ Bus Training section for detailed DQ Bus Training sequence.
  10. At Tk the LPDDR4/LPDDR4X SDRAM is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.



**Note:**

1. Training is optional and may be done at the system architect's discretion. The training sequence after ZQ\_CAL Latch (Th, Sequence 7~9) in Figure 3 is simplified recommendation and actual training sequence may vary depending on systems.

**Figure 3 - Power Ramp and Initialization Sequence**



Table 3 - Initialization Timing Parameters

| Parameter | Value           |          | Unit | Comment                                                   |
|-----------|-----------------|----------|------|-----------------------------------------------------------|
|           | Min             | Max      |      |                                                           |
| tINIT0    | -               | 20       | mS   | Maximum voltage-ramp time                                 |
| tINIT1    | 200             | -        | μS   | Minimum RESET_n LOW time after completion of voltage ramp |
| tINIT2    | 10              | -        | nS   | Minimum CKE low time before RESET_n high                  |
| tINIT3    | 2               | -        | mS   | Minimum CKE low time after RESET_n high                   |
| tINIT4    | 5               | -        | tCK  | Minimum stable clock before first CKE high                |
| tINIT5    | 2               | -        | μS   | Minimum idle time before first MRW/MRR command            |
| tZQCAL    | 1               | -        | μS   | ZQ calibration time                                       |
| tZQLAT    | Max(30nS, 8tCK) | -        | nS   | ZQCAL latch quiet time                                    |
| tCKb      | Note*1,2        | Note*1,2 | nS   | Clock cycle time during boot                              |

**Notes:**

1. Min tCKb guaranteed by DRAM test is 18nS.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent.

**7.2.2 Reset Initialization with Stable Power**

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET\_n below  $0.2 \times VDD2$  anytime when reset is needed. RESET\_n needs to be maintained for minimum tPW\_RESET. CKE must be pulled LOW at least 10 nS before de-asserting RESET\_n.
2. Repeat steps 4 to 10 in section 7.2.1 Voltage Ramp and Device Initialization.

Table 4 - Reset Timing Parameter

| Symbol    | Value |     | Unit | Comment                                                             |
|-----------|-------|-----|------|---------------------------------------------------------------------|
|           | min   | max |      |                                                                     |
| tPW_RESET | 100   |     | nS   | Minimum RESET_n low Time for Reset Initialization with stable power |

**7.2.3 Power-off Sequence**

The following procedure is required to power off the device.

While powering off, CKE must be held LOW ( $\leq 0.2 \times VDD2$ ) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. DQ, DMI, DQS\_t and DQS\_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. RESET\_n, CK\_t, CK\_c, CS and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.

Table 5 - Power Supply Conditions

| Between   | Applicable Conditions                   |
|-----------|-----------------------------------------|
| Tx and Tz | VDD1 must be greater than VDD2          |
|           | VDD2 must be greater than VDDQ - 200 mV |

The voltage difference between any of VSS, VSSQ pins must not exceed 100 mV.



#### 7.2.4 Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5V/ $\mu$ S between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

**Table 6 - Timing Parameters Power-Off**

| Symbol | Value |     | Unit | Comment                     |
|--------|-------|-----|------|-----------------------------|
|        | min   | max |      |                             |
| tPOFF  | -     | 2   | S    | Maximum Power-Off Ramp Time |



### 7.3 Mode Register Definition

The section 7.3.1 to 7.3.35 shows the Mode Registers for LPDDR4/LPDDR4X SDRAM. Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

**Table 7 - Mode Register Assignment in LPDDR4/LPDDR4X SDRAM**

| MR#   | OP[7]                                                   | OP[6]          | OP[5]               | OP[4]   | OP[3]              | OP[2]             | OP[1]             | OP[0]        |
|-------|---------------------------------------------------------|----------------|---------------------|---------|--------------------|-------------------|-------------------|--------------|
| 0     | CATR                                                    | RFU            | Single Ended Mode   | RZQI    |                    | RFU               | Latency Mode      | Refresh Mode |
| 1     | RPST                                                    | nWR (for AP)   |                     |         | RD-PRE             | WR-PRE            | BL                |              |
| 2     | WR Lev                                                  | WLS            | WL                  |         |                    | RL                |                   |              |
| 3     | DBI-WR                                                  | DBI-RD         | PDDS                |         |                    | PPRP              | WR PST            | PU-CAL       |
| 4     | TUF                                                     | Thermal Offset |                     | PPRE    | SR Abort           | Refresh Rate      |                   |              |
| 5     | LPDDR4/LPDDR4X Manufacturer ID                          |                |                     |         |                    |                   |                   |              |
| 6     | Revision ID-1                                           |                |                     |         |                    |                   |                   |              |
| 7     | Revision ID-2                                           |                |                     |         |                    |                   |                   |              |
| 8     | IO Width                                                |                | Density             |         |                    |                   | Type              |              |
| 9     | Vendor Specific Test Register                           |                |                     |         |                    |                   |                   |              |
| 10    | RFU                                                     |                |                     |         |                    |                   |                   | ZQ-Reset     |
| 11    | Reserved                                                | CA ODT         |                     |         | Reserved           | DQ ODT            |                   |              |
| 12    | RFU                                                     | VR-CA          | VREF(CA)            |         |                    |                   |                   |              |
| 13    | FSP-OP                                                  | FSP-WR         | DMD                 | RRO     | VRCG               | VRO               | RPT               | CBT          |
| 14    | RFU                                                     | VR(dq)         | VREF(DQ)            |         |                    |                   |                   |              |
| 15    | Lower-Byte Invert Register for Calibration              |                |                     |         |                    |                   |                   |              |
| 16    | PASR Bank Mask                                          |                |                     |         |                    |                   |                   |              |
| 17    | PASR Segment Mask                                       |                |                     |         |                    |                   |                   |              |
| 18    | DQS Oscillator Count - LSB                              |                |                     |         |                    |                   |                   |              |
| 19    | DQS Oscillator Count - MSB                              |                |                     |         |                    |                   |                   |              |
| 20    | Upper-Byte Invert Register for DQ Calibration           |                |                     |         |                    |                   |                   |              |
| 21    | RFU                                                     |                | Low Speed CA Buffer | RFU     |                    |                   |                   |              |
| 22    | RFU                                                     |                | ODTD-CA             | ODTE-CS | ODTE-CK            | SOC ODT           |                   |              |
| 23    | DQS interval timer run time setting                     |                |                     |         |                    |                   |                   |              |
| 24    | TRR Mode                                                | TRR Mode BAn   |                     |         | Unlimited MAC      | MAC Value         |                   |              |
| 25    | PPR Resource                                            |                |                     |         |                    |                   |                   |              |
| 26~29 | RFU                                                     |                |                     |         |                    |                   |                   |              |
| 30    | Reserved for testing – SDRAM will ignore                |                |                     |         |                    |                   |                   |              |
| 31    | RFU                                                     |                |                     |         |                    |                   |                   |              |
| 32    | DQ Calibration Pattern “A” (default = 5A <sub>H</sub> ) |                |                     |         |                    |                   |                   |              |
| 33~38 | RFU                                                     |                |                     |         |                    |                   |                   |              |
| 39    | Reserved for testing – SDRAM will ignore                |                |                     |         |                    |                   |                   |              |
| 40    | DQ Calibration Pattern “B” (default = 3C <sub>H</sub> ) |                |                     |         |                    |                   |                   |              |
| 41~50 | RFU                                                     |                |                     |         |                    |                   |                   |              |
| 51    | RFU                                                     |                |                     |         | Single Ended Clock | Single Ended WDQS | Single Ended RDQS | RFU          |

**Note:** For LPDDR4X mode specific requirements of MR0, MR3, MR12, MR14 and MR22, refer to section 10.1.1 to 10.1.5.

Publication Release Date: Dec. 30, 2024

Revision: A01-001



### 7.3.1 MR0 Register Information (MA[5:0] = 00H)

| OP[7] | OP[6] | OP[5]             | OP[4] | OP[3] | OP[2] | OP[1]        | OP[0]        |
|-------|-------|-------------------|-------|-------|-------|--------------|--------------|
| CATR  | RFU   | Single Ended Mode | RZQI  |       | RFU   | Latency Mode | Refresh Mode |

| Function                             | Type      | Operand | Data                                                                                                                                                                                                                                                                                                                  | Notes      |
|--------------------------------------|-----------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| Refresh Mode                         | Read-only | OP[0]   | <b>0<sub>b</sub></b> : Both legacy and modified refresh mode supported (default)<br><b>1<sub>b</sub></b> : Only modified refresh mode supported                                                                                                                                                                       |            |
| Latency Mode                         |           | OP[1]   | <b>0<sub>b</sub></b> : Device supports normal latency<br><b>1<sub>b</sub></b> : Reserved                                                                                                                                                                                                                              | 5          |
| RZQI<br>(Built-in Self-Test for RZQ) |           | OP[4:3] | <b>00<sub>b</sub></b> : RZQ Self-Test not support.<br><b>01<sub>b</sub></b> : ZQ-pin may connect to VSSQ or float<br><b>10<sub>b</sub></b> : ZQ-pin may short to VDDQ<br><b>11<sub>b</sub></b> : ZQ-pin Self-Test completed, no error condition detected (ZQ-pin may not connect to VSSQ or float, nor short to VDDQ) | 1, 2, 3, 4 |
| Single Ended Mode                    |           | OP[5]   | <b>1<sub>b</sub></b> : Supports for Single Ended Mode                                                                                                                                                                                                                                                                 | 6          |
| CATR<br>(CA Terminating Rank)        |           | OP[7]   | <b>0<sub>b</sub></b> : CA for this rank is not terminated<br><b>1<sub>b</sub></b> : CA for this rank is terminated                                                                                                                                                                                                    | 7          |

#### Notes:

- RZQI MR value, if supported, will be valid after the following sequence:
  - Completion of MPC ZQCAL Start command to either channel.
  - Completion of MPC ZQCAL Latch command to either channel then tZQLAT is satisfied.  
RZQI value will be lost after Reset.
- If the ZQ-pin is connected to VSSQ to set default calibration, OP[4:3] shall be set to 01<sub>b</sub>. If the ZQ-pin is not connected to VSSQ, either OP[4:3] = 01<sub>b</sub> or OP[4:3] = 10<sub>b</sub> might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
- In the case of possible assembly error, the LPDDR4/LPDDR4X SDRAM will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.
- If ZQ Self-Test returns OP[4:3] = 11<sub>b</sub>, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240Ω ± 1%).
- Byte mode is not supported.
- OP[5] set to 1<sub>b</sub> support for Single Ended Mode, Single Ended Write DQS, Read DQS and CK can be enabled in MR51.
- CATR can either indicate the connection status of the ODTCA pad for the die or whether CA for the rank is terminated.



### 7.3.2 MR1 Register Information (MA[5:0] = 01<sub>H</sub>)

| OP[7] | OP[6]        | OP[5] | OP[4] | OP[3]  | OP[2]  | OP[1] | OP[0] |
|-------|--------------|-------|-------|--------|--------|-------|-------|
| RPST  | nWR (for AP) |       |       | RD-PRE | WR-PRE | BL    |       |

| Function                                            | Type       | Operand | Data                                                                                                                                                                                                                                                                                                          | Notes   |
|-----------------------------------------------------|------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| BL<br>(Burst Length)                                | Write only | OP[1:0] | <b>00<sub>b</sub></b> : BL=16 Sequential (default)<br><b>01<sub>b</sub></b> : BL=32 Sequential<br><b>10<sub>b</sub></b> : BL=16 or 32 Sequential (on-the-fly)<br>All Others: Reserved                                                                                                                         | 1       |
| WR-PRE<br>(WR Pre-ambble Length)                    |            | OP[2]   | <b>0<sub>b</sub></b> : Reserved<br><b>1<sub>b</sub></b> : WR Pre-ambble = 2*tCK                                                                                                                                                                                                                               | 5, 6    |
| RD-PRE<br>(RD Pre-ambble Type)                      |            | OP[3]   | <b>0<sub>b</sub></b> : RD Pre-ambble = Static (default)<br><b>1<sub>b</sub></b> : RD Pre-ambble = Toggle                                                                                                                                                                                                      | 3, 5, 6 |
| nWR<br>(Write-Recovery for Auto-Precharge commands) |            | OP[6:4] | <b>000<sub>b</sub></b> : nWR = 6 (default)<br><b>001<sub>b</sub></b> : nWR = 10<br><b>010<sub>b</sub></b> : nWR = 16<br><b>011<sub>b</sub></b> : nWR = 20<br><b>100<sub>b</sub></b> : nWR = 24<br><b>101<sub>b</sub></b> : nWR = 30<br><b>110<sub>b</sub></b> : nWR = 34<br><b>111<sub>b</sub></b> : nWR = 40 | 2, 5, 6 |
| RPST<br>(RD Post-Ambble Length)                     |            | OP[7]   | <b>0<sub>b</sub></b> : RD Post-ambble = 0.5*tCK (default)<br><b>1<sub>b</sub></b> : RD Post-ambble = 1.5*tCK                                                                                                                                                                                                  | 4, 5, 6 |

#### Notes:

- Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the "BL" bit in the command operands. See the Command Truth Table.
- The programmed value of nWR is the number of clock cycles the LPDDR4/LPDDR4X SDRAM uses to determine the starting point of an internal Precharge operation after a Write burst with AP (auto-precharge) enabled. See section 7.4.12 Read and Write Latencies.
- For Read operations this bit must be set to select between a "toggling" pre-ambble and a "Non-toggling" Pre-ambble. See section 7.4.4 Read Preamble and Postamble, for a drawing of each type of pre-ambble.
- OP[7] provides an alternative READ post-ambble with an additional rising and falling edge of DQS<sub>t</sub>. This alternative post-ambble cycle is provided for the benefit of certain memory controllers.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be read from with an MRR command to this address.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.



Table 8 - Burst Sequence for READ

| Burst Length | Burst Type | C4 | C3 | C2 | C1 | C0 | Burst Cycle Number and Burst Address Sequence |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|--------------|------------|----|----|----|----|----|-----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|              |            |    |    |    |    |    | 1                                             | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| 16           | SEQ        | V  | 0  | 0  | 0  | 0  | 0                                             | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|              |            | V  | 0  | 1  | 0  | 0  | 4                                             | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|              |            | V  | 1  | 0  | 0  | 0  | 8                                             | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|              |            | V  | 1  | 1  | 0  | 0  | C                                             | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 32           | SEQ        | 0  | 0  | 0  | 0  | 0  | 0                                             | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
|              |            | 0  | 0  | 1  | 0  | 0  | 4                                             | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 |
|              |            | 0  | 1  | 0  | 0  | 0  | 8                                             | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|              |            | 0  | 1  | 1  | 0  | 0  | C                                             | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B |
|              |            | 1  | 0  | 0  | 0  | 0  | 10                                            | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  |
|              |            | 1  | 0  | 1  | 0  | 0  | 14                                            | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  |
|              |            | 1  | 1  | 0  | 0  | 0  | 18                                            | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 8  | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  |
|              |            | 1  | 1  | 1  | 0  | 0  | 1C                                            | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  |

**Notes:**

- 1.C0-C1 are assumed to be '0', and are not transmitted on the command bus.
- 2.The starting burst address is on 64-bit (4n) boundaries.

Table 9 - Burst Sequence for Write

| Burst Length | Burst Type | C4 | C3 | C2 | C1 | C0 | Burst Cycle Number and Burst Address Sequence |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|--------------|------------|----|----|----|----|----|-----------------------------------------------|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|              |            |    |    |    |    |    | 1                                             | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| 16           | SEQ        | V  | 0  | 0  | 0  | 0  | 0                                             | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9  | A  | B  | C  | D  | E  | F  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 32           | SEQ        | 0  | 0  | 0  | 0  | 0  | 0                                             | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |

**Notes:**

- 1.C0-C1 are assumed to be '0', and are not transmitted on the command bus.
- 2.The starting address is on 256-bit (16n) boundaries for Burst length 16.
- 3.The starting address is on 512-bit (32n) boundaries for Burst length 32.
- 4.C2-C3 shall be set to '0' for all Write operations.



### 7.3.3 MR2 Register Information (MA[5:0] = 02<sub>H</sub>)

| OP[7]  | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------|-------|-------|-------|-------|-------|-------|-------|
| WR Lev | WLS   | WL    |       |       | RL    |       |       |

| Function                   | Type       | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Notes   |
|----------------------------|------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| RL<br>(Read Latency)       | Write-only | OP[2:0] | <b>RL &amp; nRTP for DBI-RD Disabled (MR3 OP[6]= 0<sub>b</sub>)</b><br><b>000<sub>b</sub></b> : RL=6, nRTP = 8 (default)<br><b>001<sub>b</sub></b> : RL=10, nRTP = 8<br><b>010<sub>b</sub></b> : RL=14, nRTP = 8<br><b>011<sub>b</sub></b> : RL=20, nRTP = 8<br><b>100<sub>b</sub></b> : RL=24, nRTP = 10<br><b>101<sub>b</sub></b> : RL=28, nRTP = 12<br><b>110<sub>b</sub></b> : RL=32, nRTP = 14<br><b>111<sub>b</sub></b> : RL=36, nRTP = 16<br><b>RL &amp; nRTP for DBI-RD Enabled (MR3 OP[6]= 1<sub>b</sub>)</b><br><b>000<sub>b</sub></b> : RL=6, nRTP = 8<br><b>001<sub>b</sub></b> : RL=12, nRTP = 8<br><b>010<sub>b</sub></b> : RL=16, nRTP = 8<br><b>011<sub>b</sub></b> : RL=22, nRTP = 8<br><b>100<sub>b</sub></b> : RL=28, nRTP = 10<br><b>101<sub>b</sub></b> : RL=32, nRTP = 12<br><b>110<sub>b</sub></b> : RL=36, nRTP = 14<br><b>111<sub>b</sub></b> : RL=40, nRTP = 16 | 1, 3, 4 |
| WL<br>(Write Latency)      |            | OP[5:3] | <b>WL Set "A" (MR2 OP[6]= 0<sub>b</sub>)</b><br><b>000<sub>b</sub></b> : WL=4 (default)<br><b>001<sub>b</sub></b> : WL=6<br><b>010<sub>b</sub></b> : WL=8<br><b>011<sub>b</sub></b> : WL=10<br><b>100<sub>b</sub></b> : WL=12<br><b>101<sub>b</sub></b> : WL=14<br><b>110<sub>b</sub></b> : WL=16<br><b>111<sub>b</sub></b> : WL=18<br><b>WL Set "B" (MR2 OP[6]= 1<sub>b</sub>)</b><br><b>000<sub>b</sub></b> : WL=4<br><b>001<sub>b</sub></b> : WL=8<br><b>010<sub>b</sub></b> : WL=12<br><b>011<sub>b</sub></b> : WL=18<br><b>100<sub>b</sub></b> : WL=22<br><b>101<sub>b</sub></b> : WL=26<br><b>110<sub>b</sub></b> : WL=30<br><b>111<sub>b</sub></b> : WL=34                                                                                                                                                                                                                         | 1, 3, 4 |
| WLS<br>(Write Latency Set) |            | OP[6]   | <b>0<sub>b</sub></b> : WL Set "A" (default)<br><b>1<sub>b</sub></b> : WL Set "B"                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 1, 3, 4 |
| WR LEV<br>(Write Leveling) |            | OP[7]   | <b>0<sub>b</sub></b> : Disabled (default)<br><b>1<sub>b</sub></b> : Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 2       |

#### Notes:

- See section 7.4.12 Read and Write Latencies for detail.
- After a MRW to set the Write Leveling Enable bit (OP[7]= 1<sub>b</sub>), the LPDDR4/LPDDR4X SDRAM device remains in the MRW state until another MRW command clears the bit (OP[7]= 0<sub>b</sub>). No other commands are allowed until the Write Leveling Enable bit is cleared.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.





### 7.3.4 MR3 Register Information (MA[5:0] = 03<sub>H</sub>)

| OP[7]  | OP[6]  | OP[5] | OP[4] | OP[3] | OP[2] | OP[1]  | OP[0]  |
|--------|--------|-------|-------|-------|-------|--------|--------|
| DBI-WR | DBI-RD | PDDS  |       |       | PPRP  | WR PST | PU-CAL |

| Function                              | Type       | Operand | Data                                                                                                                                                                                                                                                                                    | Notes   |
|---------------------------------------|------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| PU-Cal<br>(Pull-up Calibration Point) | Write only | OP[0]   | <b>0<sub>b</sub></b> : VDDQ/2.5<br><b>1<sub>b</sub></b> : VDDQ/3 (default)                                                                                                                                                                                                              | 1, 4    |
| WR PST<br>(WR Post-Amble Length)      |            | OP[1]   | <b>0<sub>b</sub></b> : WR Post-amble = 0.5*tCK (default)<br><b>1<sub>b</sub></b> : WR Post-amble = 1.5*tCK                                                                                                                                                                              | 2, 3, 5 |
| Post Package Repair Protection        |            | OP[2]   | <b>0<sub>b</sub></b> : PPR protection disabled (default)<br><b>1<sub>b</sub></b> : PPR protection enabled                                                                                                                                                                               | 6       |
| PDDS<br>(Pull-Down Drive strength)    |            | OP[5:3] | <b>000<sub>b</sub></b> : RFU<br><b>001<sub>b</sub></b> : RZQ/1<br><b>010<sub>b</sub></b> : RZQ/2<br><b>011<sub>b</sub></b> : RZQ/3<br><b>100<sub>b</sub></b> : RZQ/4<br><b>101<sub>b</sub></b> : RZQ/5<br><b>110<sub>b</sub></b> : RZQ/6 (default)<br><b>111<sub>b</sub></b> : Reserved | 1, 2, 3 |
| DBI-RD<br>(DBI-Read Enable)           |            | OP[6]   | <b>0<sub>b</sub></b> : Disabled (default)<br><b>1<sub>b</sub></b> : Enabled                                                                                                                                                                                                             | 2, 3    |
| DBI-WR<br>(DBI-Write Enable)          |            | OP[7]   | <b>0<sub>b</sub></b> : Disabled (default)<br><b>1<sub>b</sub></b> : Enabled                                                                                                                                                                                                             | 2, 3    |

#### Notes:

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.
5. 1.5\*tCK apply > 1.6GHz clock.
6. If MR3 OP[2] is set to 1<sub>b</sub> then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0<sub>b</sub> by a power on reset. MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].



### 7.3.5 MR4 Register Information (MA[5:0] = 04<sub>H</sub>)

| OP[7] | OP[6]          | OP[5] | OP[4] | OP[3]    | OP[2]        | OP[1] | OP[0] |
|-------|----------------|-------|-------|----------|--------------|-------|-------|
| TUF   | Thermal Offset |       | PPRE  | SR Abort | Refresh Rate |       |       |

| Function                                 | Type       | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                          | Notes            |
|------------------------------------------|------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Refresh Rate                             | Read-only  | OP[2:0] | <b>000<sub>b</sub></b> : SDRAM Low temperature operating limit exceeded<br><b>001<sub>b</sub></b> : 4x refresh<br><b>010<sub>b</sub></b> : 2x refresh<br><b>011<sub>b</sub></b> : 1x refresh (default)<br><b>100<sub>b</sub></b> : 0.5x refresh<br><b>101<sub>b</sub></b> : 0.25x refresh, no de-rating<br><b>110<sub>b</sub></b> : 0.25x refresh, with de-rating<br><b>111<sub>b</sub></b> : SDRAM High temperature operating limit exceeded | 1, 2, 3, 6, 7, 8 |
| SR Abort<br>(Self Refresh Abort)         | Write-only | OP[3]   | <b>0<sub>b</sub></b> : Disable (default)<br><b>1<sub>b</sub></b> : Reserved                                                                                                                                                                                                                                                                                                                                                                   | 8                |
| PPRE<br>(Post-package repair entry/exit) | Write-only | OP[4]   | <b>0<sub>b</sub></b> : Exit PPR mode (default)<br><b>1<sub>b</sub></b> : Enter PPR mode                                                                                                                                                                                                                                                                                                                                                       | 4, 8             |
| Thermal Offset                           | Write-only | OP[6:5] | <b>00<sub>b</sub></b> : No offset, 0~5°C gradient (default)<br><b>01<sub>b</sub></b> : 5°C offset, 5~10°C gradient<br><b>10<sub>b</sub></b> : 10°C offset, 10~15°C gradient<br><b>11<sub>b</sub></b> : Reserved                                                                                                                                                                                                                               |                  |
| TUF<br>(Temperature Update Flag)         | Read-only  | OP[7]   | <b>0<sub>b</sub></b> : No change in OP[2:0] since last MR4 read (default)<br><b>1<sub>b</sub></b> : Change in OP[2:0] since last MR4 read                                                                                                                                                                                                                                                                                                     | 5, 6, 7          |

#### Notes:

- The refresh rate for each MR4-OP[2:0] setting applies to tREFI, tREFI<sub>pb</sub>, and tREFW. OP[2:0]=011<sub>b</sub> corresponds to a device temperature of 85°C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1<sub>b</sub>, the device temperature is greater than 85°C.
- At higher temperatures (>85°C), AC timing derating may be required. If derating is required the LPDDR4/LPDDR4X SDRAM will set OP[2:0]=110<sub>b</sub>. See derating timing requirements in section 8.6.3, Table 121.
- The device may not operate properly when OP[2:0]=000<sub>b</sub> or 111<sub>b</sub>.
- Post-package repair can be entered or exited by writing to OP[4].
- When OP[7]=1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.
- OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence (Te).
- See section 7.4.37 "Temperature Sensor" for information on the recommended frequency of reading MR4.
- OP[6:3] bits that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register.

### 7.3.6 MR5 Register Information (MA[5:0] = 05<sub>H</sub>)

| OP[7]                          | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------------------------|-------|-------|-------|-------|-------|-------|-------|
| LPDDR4/LPDDR4X Manufacturer ID |       |       |       |       |       |       |       |

| Function                       | Type      | Operand | Data                             | Note |
|--------------------------------|-----------|---------|----------------------------------|------|
| LPDDR4/LPDDR4X Manufacturer ID | Read-only | OP[7:0] | 0000 1000 <sub>b</sub> : Winbond |      |



### 7.3.7 MR6 Register Information (MA[5:0] = 06<sub>H</sub>)

| OP[7]         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| Revision ID-1 |       |       |       |       |       |       |       |

| Function                     | Type      | Operand | Data                    | Note |
|------------------------------|-----------|---------|-------------------------|------|
| LPDDR4/LPDDR4X Revision ID-1 | Read-only | OP[7:0] | xxxx xxxxb <sub>b</sub> |      |

### 7.3.8 MR7 Register Information (MA[5:0] = 07<sub>H</sub>)

| OP[7]         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| Revision ID-2 |       |       |       |       |       |       |       |

| Function                     | Type      | Operand | Data                    | Note |
|------------------------------|-----------|---------|-------------------------|------|
| LPDDR4/LPDDR4X Revision ID-2 | Read-only | OP[7:0] | xxxx xxxxb <sub>b</sub> |      |

### 7.3.9 MR8 Register Information (MA[5:0] = 08<sub>H</sub>)

| OP[7]     | OP[6] | OP[5]   | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-----------|-------|---------|-------|-------|-------|-------|-------|
| I/O width |       | Density |       |       |       | Type  |       |

| Function  | Type      | Operand | Data                                                                                              | Note |
|-----------|-----------|---------|---------------------------------------------------------------------------------------------------|------|
| Type      | Read-only | OP[1:0] | 00 <sub>b</sub> : S16 SDRAM (16n pre-fetch)<br>All others: Reserved                               |      |
| Density   |           | OP[5:2] | 0010 <sub>b</sub> : 8Gb dual channel package / 4Gb single channel package<br>All others: Reserved |      |
| I/O width |           | OP[7:6] | 00 <sub>b</sub> : x16 (per channel)<br>All others: Reserved                                       |      |

### 7.3.10 MR9 Register Information (MA[5:0] = 09<sub>H</sub>)

| OP[7]                         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Vendor Specific Test Register |       |       |       |       |       |       |       |

**Note:** Only 00<sub>H</sub> should be written to this register.

### 7.3.11 MR10 Register Information (MA[5:0] = 0A<sub>H</sub>)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0]    |
|-------|-------|-------|-------|-------|-------|-------|----------|
| RFU   |       |       |       |       |       |       | ZQ-Reset |

| Function | Type       | Operand | Data                                                                     | Notes |
|----------|------------|---------|--------------------------------------------------------------------------|-------|
| ZQ-Reset | Write-only | OP[0]   | 0 <sub>b</sub> : Normal Operation (Default)<br>1 <sub>b</sub> : ZQ Reset | 1, 2  |

**Notes:**

- See section 7.4.38.1 Table 71 - ZQCal Timing Parameters for calibration latency and timing.
- If the ZQ-pin is connected to VDDQ through RZQ, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to VSS, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.



### 7.3.12 MR11 Register Information (MA[5:0] = 0B<sub>H</sub>)

| OP[7]    | OP[6]  | OP[5] | OP[4] | OP[3]    | OP[2]  | OP[1] | OP[0] |
|----------|--------|-------|-------|----------|--------|-------|-------|
| Reserved | CA ODT |       |       | Reserved | DQ ODT |       |       |

| Function                                       | Type       | Operand | Data                                                                                                                                                                                                                                                                                   | Notes   |
|------------------------------------------------|------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| DQ ODT<br>(DQ Bus Receiver On-Die-Termination) | Write-only | OP[2:0] | <b>000<sub>b</sub></b> : Disable (Default)<br><b>001<sub>b</sub></b> : RZQ/1<br><b>010<sub>b</sub></b> : RZQ/2<br><b>011<sub>b</sub></b> : RZQ/3<br><b>100<sub>b</sub></b> : RZQ/4<br><b>101<sub>b</sub></b> : RZQ/5<br><b>110<sub>b</sub></b> : RZQ/6<br><b>111<sub>b</sub></b> : RFU | 1, 2, 3 |
| CA ODT<br>(CA Bus Receiver On-Die-Termination) |            | OP[6:4] | <b>000<sub>b</sub></b> : Disable (Default)<br><b>001<sub>b</sub></b> : RZQ/1<br><b>010<sub>b</sub></b> : RZQ/2<br><b>011<sub>b</sub></b> : RZQ/3<br><b>100<sub>b</sub></b> : RZQ/4<br><b>101<sub>b</sub></b> : RZQ/5<br><b>110<sub>b</sub></b> : RZQ/6<br><b>111<sub>b</sub></b> : RFU | 1, 2, 3 |

#### Notes:

- All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

### 7.3.13 MR12 Register Information (MA[5:0] = 0C<sub>H</sub>)

| OP[7] | OP[6] | OP[5]    | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|-------|----------|-------|-------|-------|-------|-------|
| RFU   | VR-CA | VREF(CA) |       |       |       |       |       |

| Function                       | Type       | Operand | Data                                                                                                                    | Notes         |
|--------------------------------|------------|---------|-------------------------------------------------------------------------------------------------------------------------|---------------|
| VREF(CA)<br>(VREF(CA) Setting) | Read/Write | OP[5:0] | <b>000000<sub>b</sub></b> :<br>-- Thru --<br><b>110010<sub>b</sub></b> : See table below<br><b>All Others: Reserved</b> | 1, 2, 3, 5, 6 |
| VR-CA<br>(VREF(CA) Range)      |            | OP[6]   | <b>0<sub>b</sub></b> : VREF(CA) Range[0] enabled<br><b>1<sub>b</sub></b> : VREF(CA) Range[1] enabled (default)          | 1, 2, 4, 5, 6 |

#### Notes:

- This register controls the VREF(CA) levels. Refer to Table 10 - VREF Settings for Range[0] and Range[1] for actual voltage of VREF(CA).
- A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See section 7.4.23 on MRR Operation.
- A write to OP[5:0] sets the internal VREF(CA) level for FSP[0] when MR13 OP[6]=0<sub>b</sub>, or sets the internal VREF(CA) level for FSP[1] when MR13 OP[6]=1<sub>b</sub>. The time required for VREF(CA) to reach the set level depends on the step size from the current level to the new level. See section 7.4.26 on VREF(CA) training for more information.
- A write to OP[6] switches the LPDDR4 SDRAM between two internal VREF(CA) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(CA) register. The value, once set, will be retained until over written, or until the next power-on or RESET event.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.



Table 10 - VREF Settings for Range[0] and Range[1]

| Function               | Operand | Range[0] Values (% of VDD2) |                             | Range[1] Values (% of VDD2)              |                             | Notes   |
|------------------------|---------|-----------------------------|-----------------------------|------------------------------------------|-----------------------------|---------|
| VREF Settings for MR12 | OP[5:0] | 000000 <sub>b</sub> : 10.0% | 011010 <sub>b</sub> : 20.4% | 000000 <sub>b</sub> : 22.0%              | 011010 <sub>b</sub> : 32.4% | 1, 2, 3 |
|                        |         | 000001 <sub>b</sub> : 10.4% | 011011 <sub>b</sub> : 20.8% | 000001 <sub>b</sub> : 22.4%              | 011011 <sub>b</sub> : 32.8% |         |
|                        |         | 000010 <sub>b</sub> : 10.8% | 011100 <sub>b</sub> : 21.2% | 000010 <sub>b</sub> : 22.8%              | 011100 <sub>b</sub> : 33.2% |         |
|                        |         | 000011 <sub>b</sub> : 11.2% | 011101 <sub>b</sub> : 21.6% | 000011 <sub>b</sub> : 23.2%              | 011101 <sub>b</sub> : 33.6% |         |
|                        |         | 000100 <sub>b</sub> : 11.6% | 011110 <sub>b</sub> : 22.0% | 000100 <sub>b</sub> : 23.6%              | 011110 <sub>b</sub> : 34.0% |         |
|                        |         | 000101 <sub>b</sub> : 12.0% | 011111 <sub>b</sub> : 22.4% | 000101 <sub>b</sub> : 24.0%              | 011111 <sub>b</sub> : 34.4% |         |
|                        |         | 000110 <sub>b</sub> : 12.4% | 100000 <sub>b</sub> : 22.8% | 000110 <sub>b</sub> : 24.4%              | 100000 <sub>b</sub> : 34.8% |         |
|                        |         | 000111 <sub>b</sub> : 12.8% | 100001 <sub>b</sub> : 23.2% | 000111 <sub>b</sub> : 24.8%              | 100001 <sub>b</sub> : 35.2% |         |
|                        |         | 001000 <sub>b</sub> : 13.2% | 100010 <sub>b</sub> : 23.6% | 001000 <sub>b</sub> : 25.2%              | 100010 <sub>b</sub> : 35.6% |         |
|                        |         | 001001 <sub>b</sub> : 13.6% | 100011 <sub>b</sub> : 24.0% | 001001 <sub>b</sub> : 25.6%              | 100011 <sub>b</sub> : 36.0% |         |
|                        |         | 001010 <sub>b</sub> : 14.0% | 100100 <sub>b</sub> : 24.4% | 001010 <sub>b</sub> : 26.0%              | 100100 <sub>b</sub> : 36.4% |         |
|                        |         | 001011 <sub>b</sub> : 14.4% | 100101 <sub>b</sub> : 24.8% | 001011 <sub>b</sub> : 26.4%              | 100101 <sub>b</sub> : 36.8% |         |
|                        |         | 001100 <sub>b</sub> : 14.8% | 100110 <sub>b</sub> : 25.2% | 001100 <sub>b</sub> : 26.8%              | 100110 <sub>b</sub> : 37.2% |         |
|                        |         | 001101 <sub>b</sub> : 15.2% | 100111 <sub>b</sub> : 25.6% | 001101 <sub>b</sub> : 27.2%<br>(Default) | 100111 <sub>b</sub> : 37.6% |         |
|                        |         | 001110 <sub>b</sub> : 15.6% | 101000 <sub>b</sub> : 26.0% | 001110 <sub>b</sub> : 27.6%              | 101000 <sub>b</sub> : 38.0% |         |
|                        |         | 001111 <sub>b</sub> : 16.0% | 101001 <sub>b</sub> : 26.4% | 001111 <sub>b</sub> : 28.0%              | 101001 <sub>b</sub> : 38.4% |         |
|                        |         | 010000 <sub>b</sub> : 16.4% | 101010 <sub>b</sub> : 26.8% | 010000 <sub>b</sub> : 28.4%              | 101010 <sub>b</sub> : 38.8% |         |
|                        |         | 010001 <sub>b</sub> : 16.8% | 101011 <sub>b</sub> : 27.2% | 010001 <sub>b</sub> : 28.8%              | 101011 <sub>b</sub> : 39.2% |         |
|                        |         | 010010 <sub>b</sub> : 17.2% | 101100 <sub>b</sub> : 27.6% | 010010 <sub>b</sub> : 29.2%              | 101100 <sub>b</sub> : 39.6% |         |
|                        |         | 010011 <sub>b</sub> : 17.6% | 101101 <sub>b</sub> : 28.0% | 010011 <sub>b</sub> : 29.6%              | 101101 <sub>b</sub> : 40.0% |         |
|                        |         | 010100 <sub>b</sub> : 18.0% | 101110 <sub>b</sub> : 28.4% | 010100 <sub>b</sub> : 30.0%              | 101110 <sub>b</sub> : 40.4% |         |
|                        |         | 010101 <sub>b</sub> : 18.4% | 101111 <sub>b</sub> : 28.8% | 010101 <sub>b</sub> : 30.4%              | 101111 <sub>b</sub> : 40.8% |         |
|                        |         | 010110 <sub>b</sub> : 18.8% | 110000 <sub>b</sub> : 29.2% | 010110 <sub>b</sub> : 30.8%              | 110000 <sub>b</sub> : 41.2% |         |
|                        |         | 010111 <sub>b</sub> : 19.2% | 110001 <sub>b</sub> : 29.6% | 010111 <sub>b</sub> : 31.2%              | 110001 <sub>b</sub> : 41.6% |         |
|                        |         | 011000 <sub>b</sub> : 19.6% | 110010 <sub>b</sub> : 30.0% | 011000 <sub>b</sub> : 31.6%              | 110010 <sub>b</sub> : 42.0% |         |
|                        |         | 011001 <sub>b</sub> : 20.0% | All Others: Reserved        | 011001 <sub>b</sub> : 32.0%              | All Others: Reserved        |         |

**Notes:**

1. These values may be used for MR12 OP[5:0] to set the VREF(CA) levels in the LPDDR4 mode.
2. The range may be selected in the MR12 register by setting OP[6] appropriately.
3. The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high frequency setting which may use different terminations values.



### 7.3.14 MR13 Register Information (MA[5:0] = 0D<sub>H</sub>)

| OP[7]  | OP[6]  | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------|--------|-------|-------|-------|-------|-------|-------|
| FSP-OP | FSP-WR | DMD   | RRO   | VRCG  | VRO   | RPT   | CBT   |

| Function                                       | Type       | Operand | Data                                                                                                               | Notes |
|------------------------------------------------|------------|---------|--------------------------------------------------------------------------------------------------------------------|-------|
| CBT<br>(Command Bus Training)                  | Write-only | OP[0]   | 0 <sub>b</sub> : Normal Operation (default)<br>1 <sub>b</sub> : Command Bus Training Mode Enabled                  | 1     |
| RPT<br>(Read Preamble Training Mode)           |            | OP[1]   | 0 <sub>b</sub> : Disable (default)<br>1 <sub>b</sub> : Enable                                                      |       |
| VRO<br>(VREF Output)                           |            | OP[2]   | 0 <sub>b</sub> : Normal Operation (default)<br>1 <sub>b</sub> : Output the VREF(CA) and VREF(DQ) values on DQ bits | 2     |
| VRCG<br>(VREF Current Generator)               |            | OP[3]   | 0 <sub>b</sub> : Normal Operation (default)<br>1 <sub>b</sub> : VREF Fast Response (high current) mode             | 3     |
| RRO<br>Refresh rate option                     |            | OP[4]   | 0 <sub>b</sub> : Disable codes 001 and 010 in MR4 OP[2:0]<br>1 <sub>b</sub> : Enable all codes in MR4 OP[2:0]      | 4, 5  |
| DMD<br>(Data Mask Disable)                     |            | OP[5]   | 0 <sub>b</sub> : Data Mask Operation Enabled (default)<br>1 <sub>b</sub> : Data Mask Operation Disabled            | 6     |
| FSP-WR<br>(Frequency Set Point Write/Read)     |            | OP[6]   | 0 <sub>b</sub> : Frequency-Set-Point[0] (default)<br>1 <sub>b</sub> : Frequency-Set-Point [1]                      | 7     |
| FSP-OP<br>(Frequency Set Point Operation Mode) |            | OP[7]   | 0 <sub>b</sub> : Frequency-Set-Point[0] (default)<br>1 <sub>b</sub> : Frequency-Set-Point [1]                      | 8     |

#### Notes:

1. A write to set OP[0]=1 causes the LPDDR4/LPDDR4X SDRAM to enter the Command Bus Training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See section 7.4.28 on Command Bus Training for more information.
2. When set, the LPDDR4/LPDDR4X SDRAM will output the VREF(CA) and VREF(DQ) voltages on DQ pins. Only the “active” frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal VREF levels. When the function of VRO turn on, output the VREF(DQ) value onto DQ6 and VREF(CA) value onto DQ7.
3. When OP[3]=1, the VREF circuit uses a high-current mode to improve VREF settling time.
4. MR13 OP[4] RRO bit is valid only when MR0 OP[0] = 1. For LPDDR4/LPDDR4X SDRAMs with MR0 OP[0] = 0, MR4 OP[2:0] bits are not dependent on MR13 OP[4].
5. When OP[4] = 0, only 001<sub>b</sub> and 010<sub>b</sub> in MR4 OP[2:0] are disabled. LPDDR4/LPDDR4X SDRAMs must report 011<sub>b</sub> instead of 001<sub>b</sub> or 010<sub>b</sub> in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6. When enabled (OP[5]=0<sub>b</sub>) data masking is enabled for the device. When disabled (OP[5]=1<sub>b</sub>), masked write command is illegal. See section 7.4.16 Data Mask (DM) and Data Bus Inversion (DBI<sub>dc</sub>) Function.
7. FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as VREF(CA) Setting, VREF(CA) Range, VREF(DQ) Setting, VREF(DQ) Range. For more information, refer to section 7.4.29 Frequency Set Point.
8. FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as VREF(CA) Setting, VREF(CA) Range, VREF(DQ) Setting, VREF(DQ) Range. For more information, refer to section 7.4.29 Frequency Set Point.



### 7.3.15 MR14 Register Information (MA[5:0] = 0E<sub>H</sub>)

| OP[7] | OP[6]  | OP[5]    | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|--------|----------|-------|-------|-------|-------|-------|
| RFU   | VR(dq) | VREF(DQ) |       |       |       |       |       |

| Function                       | Type       | Operand | Data                                                                                                                  | Notes         |
|--------------------------------|------------|---------|-----------------------------------------------------------------------------------------------------------------------|---------------|
| VREF(DQ)<br>(VREF(DQ) Setting) | Read/Write | OP[5:0] | <b>000000<sub>b</sub>:</b><br>-- Thru --<br><b>110010<sub>b</sub>: See table below</b><br><b>All Others: Reserved</b> | 1, 2, 3, 5, 6 |
| VR(dq)<br>(VREF(DQ) Range)     |            | OP[6]   | <b>0<sub>b</sub>:</b> VREF(DQ) Range[0] enabled<br><b>1<sub>b</sub>:</b> VREF(DQ) Range[1] enabled (default)          | 1, 2, 4, 5, 6 |

#### Notes:

1. This register controls the VREF(DQ) levels for Frequency-Set-Point[1:0]. Values from either VR(dq)[0] or VR(dq)[1] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See section 7.4.23 on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(DQ) level for FSP[0] when MR13 OP[6]=0<sub>b</sub>, or sets FSP[1] when MR13 OP[6]=1<sub>b</sub>. The time required for VREF(DQ) to reach the set level depends on the step size from the current level to the new level. See section 7.4.27 on VREF(DQ) training for more information.
4. A write to OP[6] switches the LPDDR4 SDRAM between two internal VREF(DQ) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(DQ) register. The value, once set, will be retained until over written, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.



Table 11 - VREF Settings for Range[0] and Range[1]

| Function               | Operand | Range[0] Values (% of VDDQ) |                             | Range[1] Values (% of VDDQ)              |                             | Notes   |
|------------------------|---------|-----------------------------|-----------------------------|------------------------------------------|-----------------------------|---------|
| VREF Settings for MR14 | OP[5:0] | 000000 <sub>b</sub> : 10.0% | 011010 <sub>b</sub> : 20.4% | 000000 <sub>b</sub> : 22.0%              | 011010 <sub>b</sub> : 32.4% | 1, 2, 3 |
|                        |         | 000001 <sub>b</sub> : 10.4% | 011011 <sub>b</sub> : 20.8% | 000001 <sub>b</sub> : 22.4%              | 011011 <sub>b</sub> : 32.8% |         |
|                        |         | 000010 <sub>b</sub> : 10.8% | 011100 <sub>b</sub> : 21.2% | 000010 <sub>b</sub> : 22.8%              | 011100 <sub>b</sub> : 33.2% |         |
|                        |         | 000011 <sub>b</sub> : 11.2% | 011101 <sub>b</sub> : 21.6% | 000011 <sub>b</sub> : 23.2%              | 011101 <sub>b</sub> : 33.6% |         |
|                        |         | 000100 <sub>b</sub> : 11.6% | 011110 <sub>b</sub> : 22.0% | 000100 <sub>b</sub> : 23.6%              | 011110 <sub>b</sub> : 34.0% |         |
|                        |         | 000101 <sub>b</sub> : 12.0% | 011111 <sub>b</sub> : 22.4% | 000101 <sub>b</sub> : 24.0%              | 011111 <sub>b</sub> : 34.4% |         |
|                        |         | 000110 <sub>b</sub> : 12.4% | 100000 <sub>b</sub> : 22.8% | 000110 <sub>b</sub> : 24.4%              | 100000 <sub>b</sub> : 34.8% |         |
|                        |         | 000111 <sub>b</sub> : 12.8% | 100001 <sub>b</sub> : 23.2% | 000111 <sub>b</sub> : 24.8%              | 100001 <sub>b</sub> : 35.2% |         |
|                        |         | 001000 <sub>b</sub> : 13.2% | 100010 <sub>b</sub> : 23.6% | 001000 <sub>b</sub> : 25.2%              | 100010 <sub>b</sub> : 35.6% |         |
|                        |         | 001001 <sub>b</sub> : 13.6% | 100011 <sub>b</sub> : 24.0% | 001001 <sub>b</sub> : 25.6%              | 100011 <sub>b</sub> : 36.0% |         |
|                        |         | 001010 <sub>b</sub> : 14.0% | 100100 <sub>b</sub> : 24.4% | 001010 <sub>b</sub> : 26.0%              | 100100 <sub>b</sub> : 36.4% |         |
|                        |         | 001011 <sub>b</sub> : 14.4% | 100101 <sub>b</sub> : 24.8% | 001011 <sub>b</sub> : 26.4%              | 100101 <sub>b</sub> : 36.8% |         |
|                        |         | 001100 <sub>b</sub> : 14.8% | 100110 <sub>b</sub> : 25.2% | 001100 <sub>b</sub> : 26.8%              | 100110 <sub>b</sub> : 37.2% |         |
|                        |         | 001101 <sub>b</sub> : 15.2% | 100111 <sub>b</sub> : 25.6% | 001101 <sub>b</sub> : 27.2%<br>(Default) | 100111 <sub>b</sub> : 37.6% |         |
|                        |         | 001110 <sub>b</sub> : 15.6% | 101000 <sub>b</sub> : 26.0% | 001110 <sub>b</sub> : 27.6%              | 101000 <sub>b</sub> : 38.0% |         |
|                        |         | 001111 <sub>b</sub> : 16.0% | 101001 <sub>b</sub> : 26.4% | 001111 <sub>b</sub> : 28.0%              | 101001 <sub>b</sub> : 38.4% |         |
|                        |         | 010000 <sub>b</sub> : 16.4% | 101010 <sub>b</sub> : 26.8% | 010000 <sub>b</sub> : 28.4%              | 101010 <sub>b</sub> : 38.8% |         |
|                        |         | 010001 <sub>b</sub> : 16.8% | 101011 <sub>b</sub> : 27.2% | 010001 <sub>b</sub> : 28.8%              | 101011 <sub>b</sub> : 39.2% |         |
|                        |         | 010010 <sub>b</sub> : 17.2% | 101100 <sub>b</sub> : 27.6% | 010010 <sub>b</sub> : 29.2%              | 101100 <sub>b</sub> : 39.6% |         |
|                        |         | 010011 <sub>b</sub> : 17.6% | 101101 <sub>b</sub> : 28.0% | 010011 <sub>b</sub> : 29.6%              | 101101 <sub>b</sub> : 40.0% |         |
|                        |         | 010100 <sub>b</sub> : 18.0% | 101110 <sub>b</sub> : 28.4% | 010100 <sub>b</sub> : 30.0%              | 101110 <sub>b</sub> : 40.4% |         |
|                        |         | 010101 <sub>b</sub> : 18.4% | 101111 <sub>b</sub> : 28.8% | 010101 <sub>b</sub> : 30.4%              | 101111 <sub>b</sub> : 40.8% |         |
|                        |         | 010110 <sub>b</sub> : 18.8% | 110000 <sub>b</sub> : 29.2% | 010110 <sub>b</sub> : 30.8%              | 110000 <sub>b</sub> : 41.2% |         |
|                        |         | 010111 <sub>b</sub> : 19.2% | 110001 <sub>b</sub> : 29.6% | 010111 <sub>b</sub> : 31.2%              | 110001 <sub>b</sub> : 41.6% |         |
|                        |         | 011000 <sub>b</sub> : 19.6% | 110010 <sub>b</sub> : 30.0% | 011000 <sub>b</sub> : 31.6%              | 110010 <sub>b</sub> : 42.0% |         |
|                        |         | 011001 <sub>b</sub> : 20.0% | All Others: Reserved        | 011001 <sub>b</sub> : 32.0%              | All Others: Reserved        |         |

**Notes:**

1. These values may be used for MR14 OP[5:0] to set the VREF(DQ) levels in the LPDDR4 mode.
2. The range may be selected in the MR14 register by setting OP[6] appropriately.
3. The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high frequency setting which may use different terminations values.





### 7.3.16 MR15 Register Information (MA[5:0] = 0FH)

| OP[7]                                         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-----------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Lower-Byte Invert Register for DQ Calibration |       |       |       |       |       |       |       |

| Function                             | Type       | Operand | Data                                                                                                                                                                                                                                                                                             | Notes   |
|--------------------------------------|------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| Lower-Byte Invert for DQ Calibration | Write-only | OP[7:0] | <p>The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane:</p> <p><b>0b:</b> Do not invert</p> <p><b>1b:</b> Invert the DQ Calibration patterns in MR32 and MR40</p> <p>Default value for OP[7:0]=55H</p> | 1, 2, 3 |

#### Notes:

1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101<sub>b</sub>, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.
2. DMI[0] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

**Table 12 - MR15 Invert Register Pin Mapping**

| PIN  | DQ[7] | DQ [6] | DQ [5] | DQ [4] | DMI0      | DQ [3] | DQ [2] | DQ [1] | DQ [0] |
|------|-------|--------|--------|--------|-----------|--------|--------|--------|--------|
| MR15 | OP[7] | OP[6]  | OP[5]  | OP[4]  | No-Invert | OP[3]  | OP[2]  | OP[1]  | OP[0]  |



### 7.3.17 MR16 Register Information (MA[5:0] = 10<sub>H</sub>)

| OP[7]          | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| PASR Bank Mask |       |       |       |       |       |       |       |

| Function       | Type       | Operand | Data                                                                                                                    | Notes |
|----------------|------------|---------|-------------------------------------------------------------------------------------------------------------------------|-------|
| Bank[7:0] Mask | Write-only | OP[7:0] | <b>0<sub>b</sub></b> : Bank Refresh enabled (default): Unmasked<br><b>1<sub>b</sub></b> : Bank Refresh disabled: Masked | 1     |

| OP[n] | Bank Mask | 8-Bank SDRAM |
|-------|-----------|--------------|
| 0     | XXXXXXX1  | Bank 0       |
| 1     | XXXXXX1X  | Bank 1       |
| 2     | XXXXX1XX  | Bank 2       |
| 3     | XXXX1XXX  | Bank 3       |
| 4     | XXX1XXXX  | Bank 4       |
| 5     | XX1XXXXX  | Bank 5       |
| 6     | X1XXXXXX  | Bank 6       |
| 7     | 1XXXXXXX  | Bank 7       |

**Notes:**

- When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.
- PASR bank-masking is on a per-channel basis. The two channels on the die may have different bank masking in dual channel devices.

### 7.3.18 MR17 Register Information (MA[5:0] = 11<sub>H</sub>)

| OP[7]             | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------------|-------|-------|-------|-------|-------|-------|-------|
| PASR Segment Mask |       |       |       |       |       |       |       |

| Function          | Type       | Operand | Data                                                                                                        | Notes |
|-------------------|------------|---------|-------------------------------------------------------------------------------------------------------------|-------|
| PASR Segment Mask | Write-only | OP[7:0] | <b>0<sub>b</sub></b> : Segment Refresh enabled (default)<br><b>1<sub>b</sub></b> : Segment Refresh disabled |       |

| Segment | OP[n] | Segment Mask | Per Channel      |
|---------|-------|--------------|------------------|
|         |       |              | R[14:12]         |
| 0       | 0     | XXXXXXX1     | 000 <sub>b</sub> |
| 1       | 1     | XXXXXX1X     | 001 <sub>b</sub> |
| 2       | 2     | XXXXX1XX     | 010 <sub>b</sub> |
| 3       | 3     | XXXX1XXX     | 011 <sub>b</sub> |
| 4       | 4     | XXX1XXXX     | 100 <sub>b</sub> |
| 5       | 5     | XX1XXXXX     | 101 <sub>b</sub> |
| 6       | 6     | X1XXXXXX     | 110 <sub>b</sub> |
| 7       | 7     | 1XXXXXXX     | 111 <sub>b</sub> |

**Notes:**

- This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.
- PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking in dual channel devices.



### 7.3.19 MR18 Register Information (MA[5:0] = 12<sub>H</sub>)

| OP[7]                      | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| DQS Oscillator Count - LSB |       |       |       |       |       |       |       |

| Function                                       | Type      | Operand | Data                                | Notes   |
|------------------------------------------------|-----------|---------|-------------------------------------|---------|
| DQS Oscillator<br>(WR Training DQS Oscillator) | Read-only | OP[7:0] | 0-255 LSB DRAM DQS Oscillator Count | 1, 2, 3 |

**Notes:**

- MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
- Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
- A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

### 7.3.20 MR19 Register Information (MA[5:0] = 13<sub>H</sub>)

| OP[7]                      | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| DQS Oscillator Count - MSB |       |       |       |       |       |       |       |

| Function                                       | Type      | Operand | Data                                | Notes   |
|------------------------------------------------|-----------|---------|-------------------------------------|---------|
| DQS Oscillator<br>(WR Training DQS Oscillator) | Read-only | OP[7:0] | 0-255 MSB DRAM DQS Oscillator Count | 1, 2, 3 |

**Notes:**

- MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
- Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
- A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

### 7.3.21 MR20 Register Information (MA[5:0] = 14<sub>H</sub>)

| OP[7]                                         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-----------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Upper-Byte Invert Register for DQ Calibration |       |       |       |       |       |       |       |

| Function                                | Type       | Operand | Data                                                                                                                                                                                                                                                                                                                 | Notes |
|-----------------------------------------|------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Upper-Byte Invert<br>for DQ Calibration | Write-only | OP[7:0] | The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane:<br><b>0<sub>b</sub></b> : Do not invert<br><b>1<sub>b</sub></b> : Invert the DQ Calibration patterns in MR32 and MR40<br>Default value for OP[7:0] = 55 <sub>H</sub> | 1, 2  |

**Notes:**

- This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR20 OP[7:0]=00010101<sub>b</sub>, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.
- DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.
- No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

**Table 13 - MR20 Invert Register Pin Mapping**

| PIN  | DQ[15] | DQ [14] | DQ [13] | DQ [12] | DMI1      | DQ [11] | DQ [10] | DQ [9] | DQ [8] |
|------|--------|---------|---------|---------|-----------|---------|---------|--------|--------|
| MR20 | OP[7]  | OP[6]   | OP[5]   | OP[4]   | No-Invert | OP[3]   | OP[2]   | OP[1]  | OP[0]  |



### 7.3.22 MR21 Register Information (MA[5:0] = 15H)

| OP[7] | OP[6] | OP[5]               | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|-------|---------------------|-------|-------|-------|-------|-------|
| RFU   |       | Low Speed CA Buffer |       | RFU   |       |       |       |

| Function            | Type       | Operand | Data                                                                                                    | Notes         |
|---------------------|------------|---------|---------------------------------------------------------------------------------------------------------|---------------|
| Low Speed CA buffer | Write-only | OP[5]   | <b>0<sub>b</sub></b> : Normal CA Buffer (Default)<br><b>1<sub>b</sub></b> : Low Speed CA Buffer Enabled | 1, 2, 3, 4, 5 |

#### Notes:

- Low speed CA buffer feature can enable lower power. The maximum clock speed for this mode is not above 800 MHz.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
- After completing all other MRW commands to set the values besides MR21 OP[5] setting, MR21 OP[5] can be enabled to "high". Low Power CA Buffer cannot be enabled prior to full device initialization (completion of step 9 in power up sequence).
- Low speed CA buffer is allowed to be enabled only when CA ODT is disabled.

### 7.3.23 MR22 Register Information (MA[5:0] = 16H)

| OP[7] | OP[6] | OP[5]   | OP[4]   | OP[3]   | OP[2]   | OP[1] | OP[0] |
|-------|-------|---------|---------|---------|---------|-------|-------|
| RFU   |       | ODTD-CA | ODTE-CS | ODTE-CK | SOC ODT |       |       |

| Function                                              | Type       | Operand | Data                                                                                                                                                                                                                                                                                   | Notes         |
|-------------------------------------------------------|------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| SoC ODT<br>(Controller ODT Value for VOH calibration) | Write-only | OP[2:0] | <b>000<sub>b</sub></b> : Disable (Default)<br><b>001<sub>b</sub></b> : RZQ/1<br><b>010<sub>b</sub></b> : RZQ/2<br><b>011<sub>b</sub></b> : RZQ/3<br><b>100<sub>b</sub></b> : RZQ/4<br><b>101<sub>b</sub></b> : RZQ/5<br><b>110<sub>b</sub></b> : RZQ/6<br><b>111<sub>b</sub></b> : RFU | 1, 2, 3       |
| ODTE-CK<br>(CK ODT enabled for nonterminating rank)   |            | OP[3]   | <b>0<sub>b</sub></b> : ODT-CK Over-ride Disabled (default)<br><b>1<sub>b</sub></b> : ODT-CK Over-ride Enabled                                                                                                                                                                          | 2, 3, 4, 6, 8 |
| ODTE-CS<br>(CS ODT enable for nonterminating rank)    |            | OP[4]   | <b>0<sub>b</sub></b> : ODT-CS Over-ride Disabled (default)<br><b>1<sub>b</sub></b> : ODT-CS Over-ride Enabled                                                                                                                                                                          | 2, 3, 5, 6, 8 |
| ODTD-CA<br>(CA ODT termination disable)               |            | OP[5]   | <b>0<sub>b</sub></b> : ODT-CA Obey ODT_CA bond pad (default)<br><b>1<sub>b</sub></b> : ODT-CA Disabled                                                                                                                                                                                 | 2, 3, 6, 7, 8 |

#### Notes:

- All values are "typical".
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
- When OP[3]=1, then the CK signals will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT\_CA bond pad. This overrides the ODT\_CA bond pad for configurations where CA is shared by two or more DRAMs but CK is not, allowing CK to terminate on all DRAMs.
- When OP[4]=1, then the CS signal will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT\_CA bond pad. This overrides the ODT\_CA bond pad for configurations where CA is shared by two or more DRAMs but CS is not, allowing CS to terminate on all DRAMs.
- For system configurations where the CK, CS, and CA signals are shared between packages, the package design should provide for the ODT\_CA ball to be bonded on the system board outside of the memory package. This provides the necessary control of the ODT function for all die with shared Command Bus signals.
- When OP[5]=0, CA[5:0] will terminate when the ODT\_CA bond pad is HIGH and MR11-OP[6:4] is VALID, and disables termination when ODT\_CA is LOW or MR11-OP[6:4] is disabled. When OP[5]=1, termination for CA[5:0] is disabled, regardless of the state of the ODT\_CA bond pad or MR11-OP[6:4].
- To ensure proper operation in a multi-rank configuration, when CA, CK or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or ODT\_CA pad setting, the rank providing ODT will continue to terminate the command bus in all DRAM states including Active Self Refresh, Self Refresh Power-down, Active Power-down and Precharge Power-down.



### 7.3.24 MR23 Register Information (MA[5:0] = 17H)

| OP[7]                               | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| DQS interval timer run time setting |       |       |       |       |       |       |       |

| Function                    | Type       | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Notes |
|-----------------------------|------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| DQS interval timer run time | Write-only | OP[7:0] | <b>00000000<sub>b</sub></b> : DQS interval timer stop via MPC Command (default)<br><b>00000001<sub>b</sub></b> : DQS timer stops automatically at 16th clocks after timer start<br><b>00000010<sub>b</sub></b> : DQS timer stops automatically at 32nd clocks after timer start<br><b>00000011<sub>b</sub></b> : DQS timer stops automatically at 48th clocks after timer start<br><b>00000100<sub>b</sub></b> : DQS timer stops automatically at 64th clocks after timer start<br>----- Thru -----<br><b>00111111<sub>b</sub></b> : DQS timer stops automatically at (63x16)th clocks after timer start<br><b>01XXXXXX<sub>b</sub></b> : DQS timer stops automatically at 2048th clocks after timer start<br><b>10XXXXXX<sub>b</sub></b> : DQS timer stops automatically at 4096th clocks after timer start<br><b>11XXXXXX<sub>b</sub></b> : DQS timer stops automatically at 8192nd clocks after timer start | 1, 2  |

#### Notes:

1. MPC command with OP[6:0]=1001101<sub>b</sub> (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR23 OP[7:0] = 00000000<sub>b</sub>.
2. MPC command with OP[6:0]=1001101<sub>b</sub> (Stop DQS Interval Oscillator) is illegal with non-zero values in MR23OP[7:0].

### 7.3.25 MR24 Register Information (MA[5:0] = 18H)

| OP[7]    | OP[6]        | OP[5] | OP[4] | OP[3]         | OP[2]     | OP[1] | OP[0] |
|----------|--------------|-------|-------|---------------|-----------|-------|-------|
| TRR Mode | TRR Mode BAn |       |       | Unlimited MAC | MAC Value |       |       |

| Function      | Type       | Operand | Data                                                                                                                                                                                                                                                                                                                                         | Notes |
|---------------|------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| MAC Value     | Read-only  | OP[2:0] | <b>000<sub>b</sub></b> : Unknown when bit OP[3]=0 (Note 1)<br>Unlimited when bit OP[3]=1 (Note 2)<br><b>001<sub>b</sub></b> : 700K<br><b>010<sub>b</sub></b> : 600K<br><b>011<sub>b</sub></b> : 500K<br><b>100<sub>b</sub></b> : 400K<br><b>101<sub>b</sub></b> : 300K<br><b>110<sub>b</sub></b> : 200K<br><b>111<sub>b</sub></b> : Reserved |       |
| Unlimited MAC | Read-only  | OP[3]   | <b>0<sub>b</sub></b> : OP[2:0] define MAC value<br><b>1<sub>b</sub></b> : Unlimited MAC value (Note 2, Note 3)                                                                                                                                                                                                                               |       |
| TRR Mode BAn  | Write-only | OP[6:4] | <b>000<sub>b</sub></b> : Bank 0<br><b>001<sub>b</sub></b> : Bank 1<br><b>010<sub>b</sub></b> : Bank 2<br><b>011<sub>b</sub></b> : Bank 3<br><b>100<sub>b</sub></b> : Bank 4<br><b>101<sub>b</sub></b> : Bank 5<br><b>110<sub>b</sub></b> : Bank 6<br><b>111<sub>b</sub></b> : Bank 7                                                         |       |
| TRR Mode      | Write-only | OP[7]   | <b>0<sub>b</sub></b> : Disabled (default)<br><b>1<sub>b</sub></b> : Enabled                                                                                                                                                                                                                                                                  |       |

#### Notes:

1. Unknown means that the device is not tested for tMAC and pass/fail value is unknown.
2. There is no restriction to number of activates.
3. MR24 OP[2:0] is set to zero.



### 7.3.26 MR25 Register Information (MA[5:0] = 19H)

Mode Register 25 contains one bit of readout per bank indicating that at least one resource is available for Post Package Repair programming.

| OP[7]  | OP[6]  | OP[5]  | OP[4]  | OP[3]  | OP[2]  | OP[1]  | OP[0]  |
|--------|--------|--------|--------|--------|--------|--------|--------|
| Bank 7 | Bank 6 | Bank 5 | Bank 4 | Bank 3 | Bank 2 | Bank 1 | Bank 0 |

| Function     | Type      | Operand | Data                                                                             | Note |
|--------------|-----------|---------|----------------------------------------------------------------------------------|------|
| PPR Resource | Read-only | OP[7:0] | <b>0b:</b> PPR Resource is not available<br><b>1b:</b> PPR Resource is available |      |

### 7.3.27 MR26~29 Registers (Reserved) (MA[5:0] = 1AH-1DH)

### 7.3.28 MR30 Register Information (MA[5:0] = 1EH)

| OP[7]        | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| Valid 0 or 1 |       |       |       |       |       |       |       |

| Function          | Type       | Operand | Data       | Note |
|-------------------|------------|---------|------------|------|
| SDRAM will ignore | Write-only | OP[7:0] | Don't care | 1    |

**Note:**

1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

### 7.3.29 MR31 Register (Reserved) (MA[5:0] = 1FH)

### 7.3.30 MR32 Register Information (MA[5:0] = 20H)

| OP[7]                                      | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| DQ Calibration Pattern "A" (default = 5AH) |       |       |       |       |       |       |       |

| Function                                  | Type       | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                    | Note |
|-------------------------------------------|------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| Return DQ Calibration Pattern MR32 + MR40 | Write-only | OP[7:0] | <b>Xb:</b> An MPC command with OP[6:0]= 1000011 <sub>b</sub> causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern "5AH" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information) |      |

### 7.3.31 MR33~38 Registers (Reserved) (MA[5:0] = 21H-26H)



### 7.3.32 MR39 Register Information (MA[5:0] = 27H)

| OP[7]        | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| Valid 0 or 1 |       |       |       |       |       |       |       |

| Function          | Type       | Operand | Data       | Note |
|-------------------|------------|---------|------------|------|
| SDRAM will ignore | Write-only | OP[7:0] | Don't care | 1    |

**Note:**

1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

### 7.3.33 MR40 Register Information (MA[5:0] = 28H)

| OP[7]                                      | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| DQ Calibration Pattern "B" (default = 3CH) |       |       |       |       |       |       |       |

| Function                                  | Type       | Operand | Data                                                                                                                                                                        | Notes   |
|-------------------------------------------|------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| Return DQ Calibration Pattern MR32 + MR40 | Write-only | OP[7:0] | <b>X<sub>b</sub></b> : A default pattern "3CH" is loaded at power up or RESET, or the pattern may be overwritten with a MRW to this register. See MR32 for more information | 1, 2, 3 |

**Notes:**

1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H, then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111<sub>b</sub>.
2. MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6].
4. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

### 7.3.34 MR41~50 Registers (Reserved) (MA[5:0] = 29H-32H)

### 7.3.35 MR51 Register Information (MA[5:0] = 33H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3]              | OP[2]             | OP[1]             | OP[0] |
|-------|-------|-------|-------|--------------------|-------------------|-------------------|-------|
| RFU   |       |       |       | Single Ended Clock | Single Ended WDQS | Single Ended RDQS | RFU   |

| Function           | Type       | Operand | Data                                                                                                                                                      | Note       |
|--------------------|------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| Single Ended RDQS  | Write-only | OP[1]   | <b>0<sub>b</sub></b> : Differential Read DQS (default)<br><b>1<sub>b</sub></b> : Single Ended Read DQS                                                    | 1, 2, 3, 4 |
| Single Ended WDQS  |            | OP[2]   | <b>0<sub>b</sub></b> : Differential Write DQS (default)<br><b>1<sub>b</sub></b> : Single Ended Write DQS                                                  | 1, 2, 3, 5 |
| Single Ended Clock |            | OP[3]   | <b>0<sub>b</sub></b> : Differential Clock (default), CK <sub>t</sub> / CK <sub>c</sub><br><b>1<sub>b</sub></b> : Single Ended Clock, only CK <sub>t</sub> | 1, 2, 3, 6 |

**Notes:**

1. Device support for Single Ended mode features (MR51 OP[3:1]) is indicated in MR0 OP[5].
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. When Single Ended RDQS mode is enabled (MR51 OP[1] = 1<sub>b</sub>), DRAM drives Read DQSB low or Hi-Z.
5. When Single Ended WDQS mode is enabled (MR51 OP[2] = 1<sub>b</sub>), Write DQSB is required to be at a valid logic level. A valid Write DQSB signal will meet this requirement.
6. When Single Ended Clock mode is enabled (MR51 OP[3] = 1<sub>b</sub>), CK<sub>c</sub> is required to be at a valid logic level. A valid CK<sub>c</sub> signal will meet this requirement.

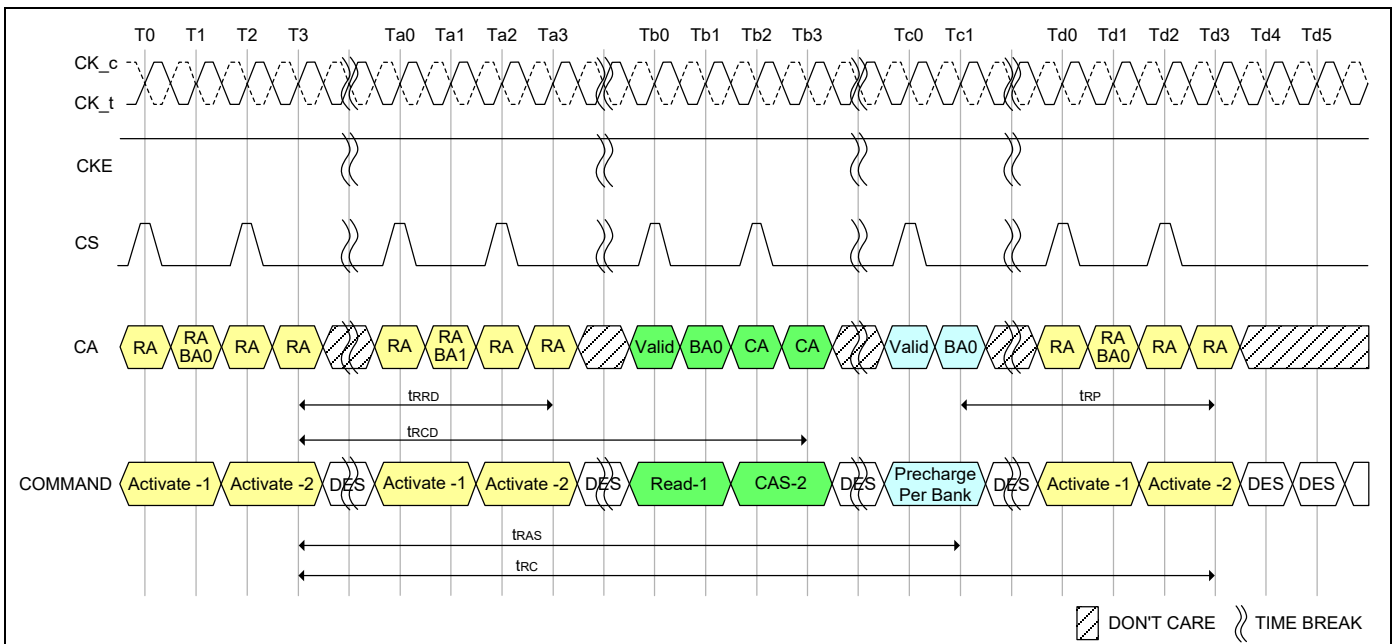




## 7.4 Command Definitions and Timing Diagrams

### 7.4.1 Activate Command

The Activate command, Figure 4, is composed of two consecutive commands, Activate-1 command and Activate-2. Activate-1 command is issued by holding CS HIGH, CA0 HIGH and CA1 LOW at the first rising edge of the clock and Activate-2 command issued by holding CS HIGH, CA0 HIGH and CA1 HIGH at the first rising edge of the clock. The bank addresses BA0, BA1 and BA2 are used to select desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. After a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as  $t_{RAS}$  and  $t_{RP}$  respectively. The minimum time interval between Activate commands to the same bank is determined by the RAS cycle time of the device ( $t_{RC}$ ). The minimum time interval between Activate commands to different banks is  $t_{RRD}$ .



**Note:**

1. A PRECHARGE command uses  $t_{RPab}$  timing for all bank PRECHARGE and  $t_{RPpb}$  timing for single-bank PRECHARGE. In this figure,  $t_{RP}$  is used to denote either all bank PRECHARGE or a single-bank PRECHARGE.

**Figure 4 - Activate Command**

#### 7.4.1.1 8-Bank Device Operation

Certain restrictions on operation of the 8-bank LPDDR4/LPDDR4X SDRAMs must be observed. There are two rules: One rule restricts the number of sequential Activate commands that can be issued; the other provides more time for RAS precharge for a Precharge All command. The rules are as follows:

**8-bank device Sequential Bank Activation Restriction:**

No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling  $t_{FAW}$  window (Figure 5). The number of clocks in a  $t_{FAW}$  period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting clocks is done by dividing  $t_{FAW}$  [ns] by  $t_{CK}$  [nS], and rounding up to the next integer value. As an example of the rolling window, if  $RU(t_{FAW}/t_{CK})$  is 10 clocks, and an Activate command is issued in clock  $n$ , no more than three further Activate commands can be issued at or between clock  $n + 1$  and  $n + 9$ . REFpb also counts as bank activation for purposes of  $t_{FAW}$ . If the clock frequency is changed during the  $t_{FAW}$  period, the rolling  $t_{FAW}$  window may be calculated in clock cycles by adding up the time spent in each clock period. The  $t_{FAW}$  requirement is met when the previous  $n$  clock cycles exceeds the  $t_{FAW}$  time.

**The 8-bank device Precharge-All Allowance:**

$t_{RP}$  for a Precharge All command must equal  $t_{RPab}$ , which is greater than  $t_{RPpb}$ .



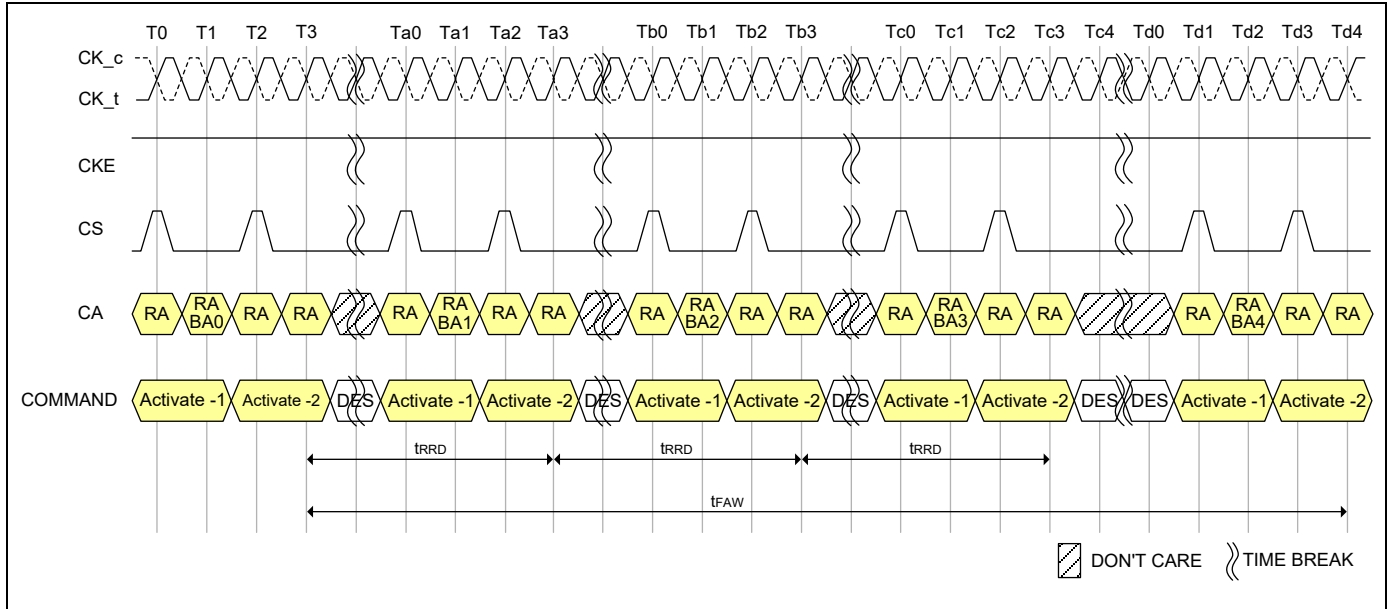


Figure 5 - tFAW Timing

## 7.4.2 Core Timing

Table 14 present the Core AC timing.

Table 14 - Core AC Timing

| Parameter                                       | Symbol | Min/Max | Data Rate                                                                        |      |      |      |      |      |      |                  | Unit     | Note |
|-------------------------------------------------|--------|---------|----------------------------------------------------------------------------------|------|------|------|------|------|------|------------------|----------|------|
| Core Parameters                                 |        |         | 533                                                                              | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4267             |          |      |
| ACTIVATE-to-ACTIVATE command period (same bank) | tRC    | MIN     | tRAS + tRPab (with all bank precharge)<br>tRAS + tRPpb (with per bank precharge) |      |      |      |      |      |      |                  | nS       |      |
| Minimum Self Refresh Time (Entry to Exit)       | tSR    | MIN     | max(15nS, 3nCK)                                                                  |      |      |      |      |      |      |                  | nS       |      |
| Self Refresh exit to next valid command delay   | tXSR   | MIN     | max(tRFCab + 7.5nS, 2nCK)                                                        |      |      |      |      |      |      |                  | nS       |      |
| Exit Power-Down to next valid command delay     | tXP    | MIN     | max(7.5nS, 5nCK)                                                                 |      |      |      |      |      |      |                  | nS       |      |
| CAS-to-CAS delay                                | tCCD   | MIN     | 8                                                                                |      |      |      |      |      |      |                  | tCK(avg) | 3    |
| Internal READ to PRECHARGE command delay        | tRTP   | MIN     | max(7.5nS, 8nCK)                                                                 |      |      |      |      |      |      |                  | nS       |      |
| RAS-to-CAS delay                                | tRCD   | MIN     | max(18nS, 4nCK)                                                                  |      |      |      |      |      |      |                  | nS       |      |
| Row precharge time (single bank)                | tRPpb  | MIN     | max(18nS, 4nCK)                                                                  |      |      |      |      |      |      |                  | nS       |      |
| Row precharge time (all banks)                  | tRPab  | MIN     | max(21nS, 4nCK)                                                                  |      |      |      |      |      |      |                  | nS       |      |
| Row active time                                 | tRAS   | MIN     | max(42nS, 3nCK)                                                                  |      |      |      |      |      |      |                  | nS       |      |
|                                                 |        | MAX     | min(9 * tREFI * Refresh Rate, 70.2μS)                                            |      |      |      |      |      |      |                  | μS       | 4    |
| WRITE recovery time                             | tWR    | MIN     | max(18nS, 6nCK)                                                                  |      |      |      |      |      |      |                  | nS       |      |
| WRITE-to-READ delay                             | tWTR   | MIN     | max(10nS, 8nCK)                                                                  |      |      |      |      |      |      |                  | nS       |      |
| Active bank-A to active bank-B                  | tRRD   | MIN     | max(10nS, 4nCK)                                                                  |      |      |      |      |      |      | max(7.5nS, 4nCK) | nS       | 2, 5 |
| Precharge to Precharge Delay                    | tPPD   | MIN     | 4                                                                                |      |      |      |      |      |      |                  | tCK(avg) | 1    |
| Four-bank ACTIVATE window                       | tFAW   | MIN     | 40                                                                               |      |      |      |      |      |      | 30               | nS       | 2    |

### Notes:

1. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
2. Devices supporting 4267 Mbps specification shall support these timings at lower data rates.
3. The value is based on BL16. For BL32 need additional 8 tCK(avg) delay.
4. Refresh Rate is specified by MR4, OP[2:0].
5. For LPDDR4X mode specific requirement, refer to section 10.11 "Core Timing - LPDDR4X".

Publication Release Date: Dec. 30, 2024

Revision: A01-001



### 7.4.3 Read and Write Access Operations

After a bank has been activated, a read or write command can be executed. This is accomplished by asserting CKE asynchronously, with CS and CA[5:0] set to the proper state (See Table 87, Command Truth Table) at a rising edge of CK.

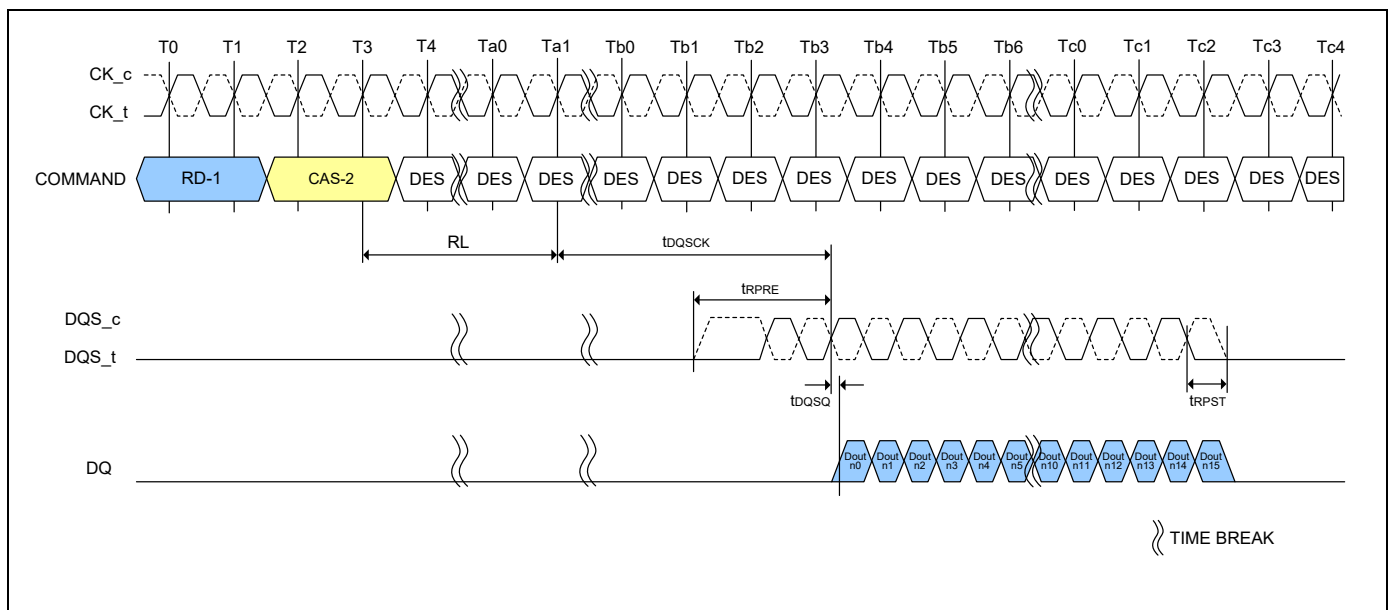
The LPDDR4/LPDDR4X SDRAM provides a fast column access operation. A single Read or Write command will initiate a burst read or write operation, where data is transferred to/from the DRAM on successive clock cycles. Burst interrupts are not allowed, but the optimal burst length may be set on the fly (See Table 87, Command Truth Table).

### 7.4.4 Read Preamble and Postamble

The DQS strobe for the LPDDR4/LPDDR4X SDRAM (Figure 6 and 7) requires a pre-amble prior to the first latching edge (the rising edge of DQS\_t with DATA "valid"), and it requires a post-amble after the last latching edge. The pre-amble and post-amble lengths are set via mode register writes (MRW).

For READ operations the pre-amble is  $2 \cdot t_{CK}$ , but the pre-amble is static (no-toggle) or toggling, selectable via mode register.

LPDDR4/LPDDR4X will have a DQS Read post-amble of  $0.5 \cdot t_{CK}$  (or extended to  $1.5 \cdot t_{CK}$ ). Standard DQS post-amble will be  $0.5 \cdot t_{CK}$  driven by the DRAM for Reads. A mode register setting instructs the DRAM to drive an additional (extended) one cycle DQS Read post-amble. The drawings below show examples of DQS Read post-amble for both standard ( $t_{RPST}$ ) and extended ( $t_{RPSTe}$ ) post-amble operation.

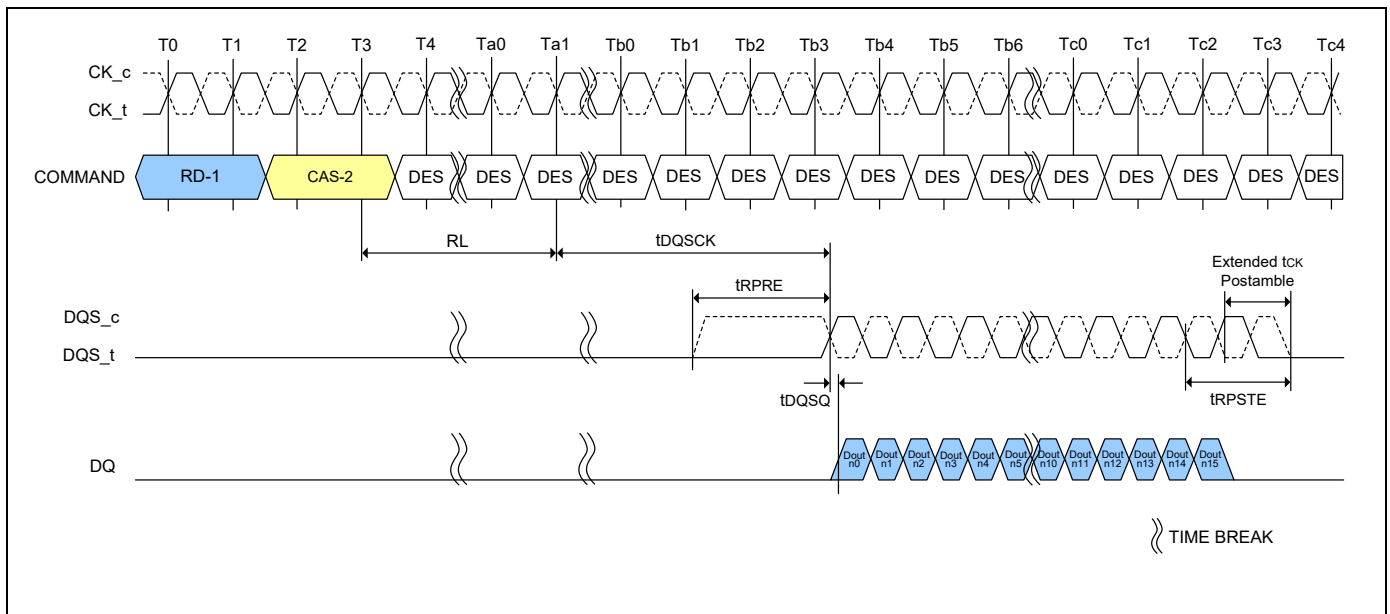


#### Notes:

1. BL = 16, Preamble = Toggling, Postamble =  $0.5nCK$ .
2. DQS and DQ terminated VSSQ.
3. DQS\_t/DQS\_c is "don't care" prior to the start of  $t_{RPRE}$ .

No transition of DQS is implied, as DQS\_t/DQS\_c can be HIGH, LOW, or HI-Z prior to  $t_{RPRE}$ .

**Figure 6 - DQS Read Preamble and Postamble: Toggling Preamble and  $0.5nCK$  Postamble**

**Notes:**

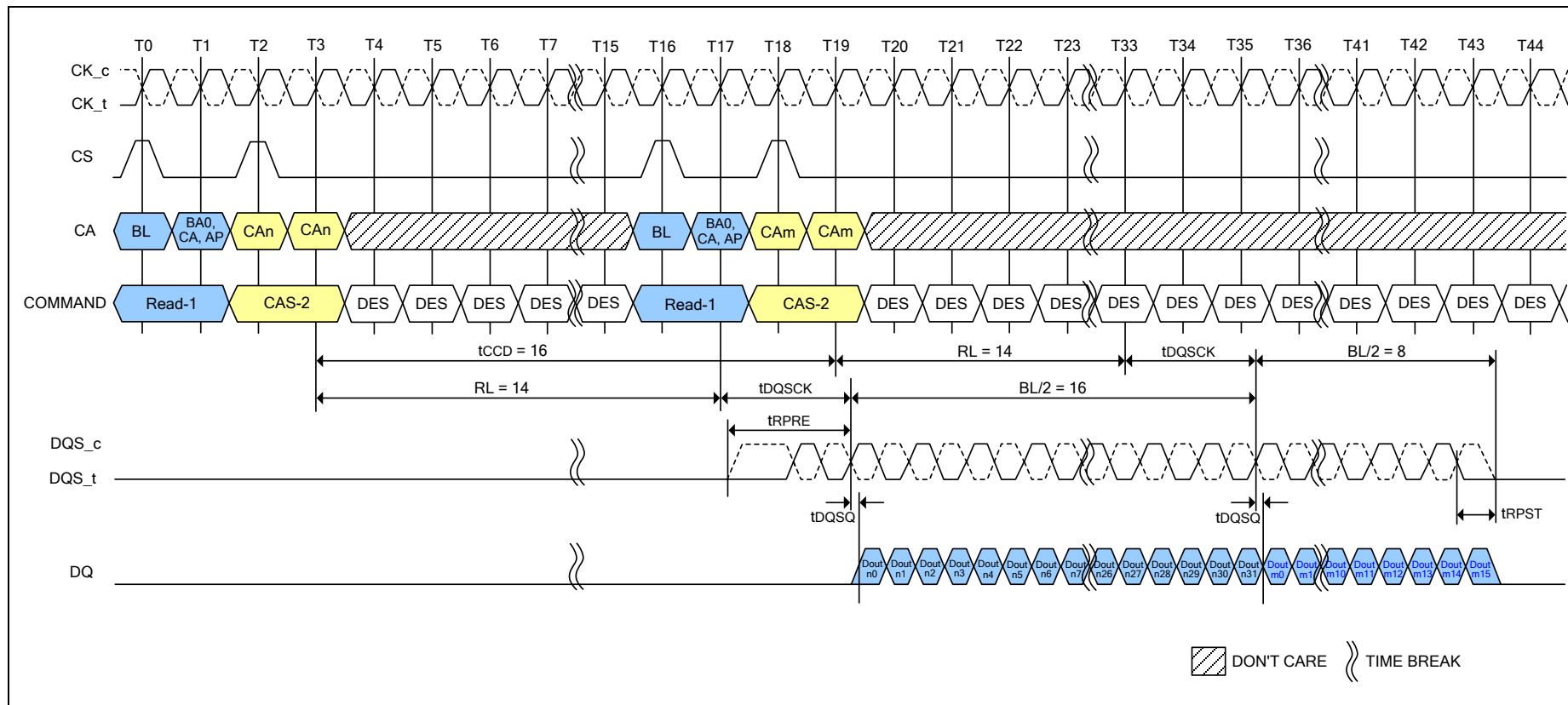
1. BL = 16, Preamble = Static, Postamble = 1.5nCK (Extended).
2. DQS and DQ terminated VSSQ.
3. DQS\_t/DQS\_c is "don't care" prior to the start of trPRE.

No transition of DQS is implied, as DQS\_t/DQS\_c can be HIGH, LOW, or HI-Z prior to trPRE.

**Figure 7 - DQS Read Preamble and Postamble: Static Preamble and 1.5nCK Postamble**

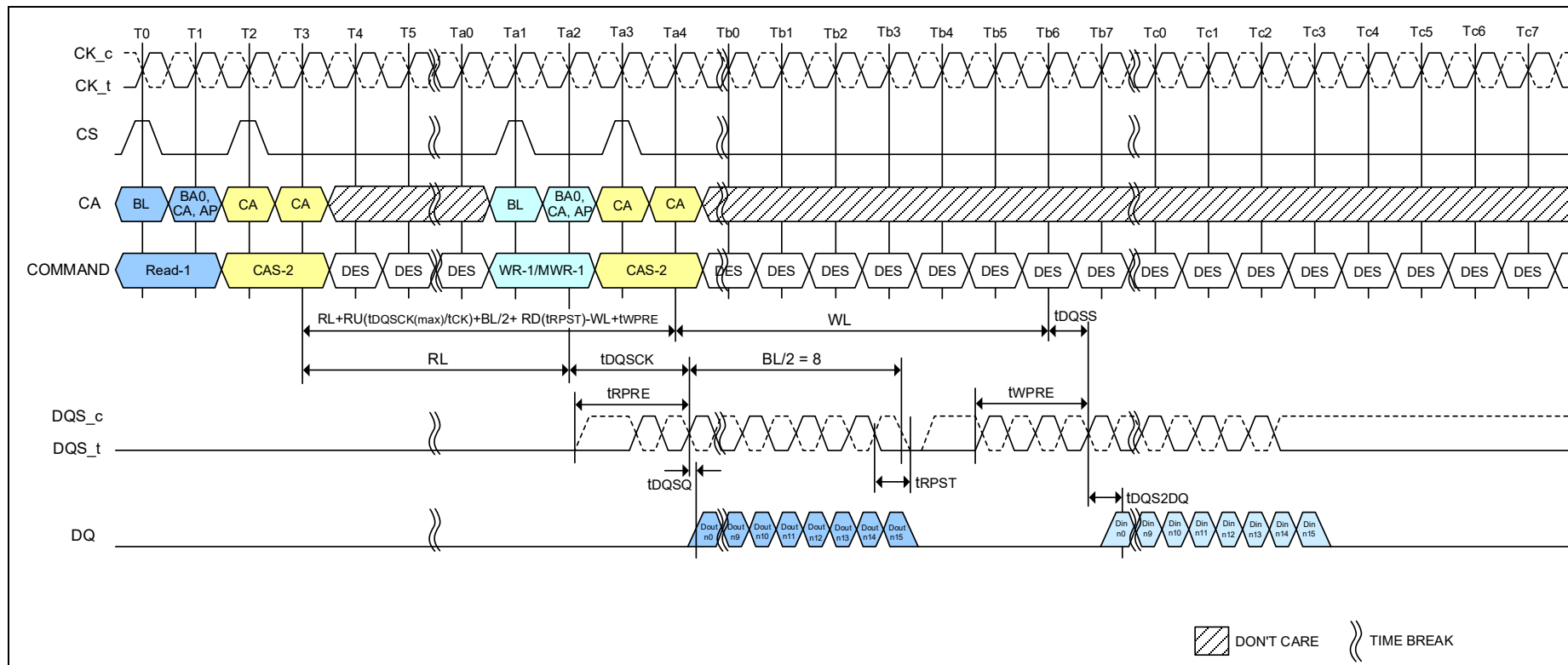
### 7.4.5 Burst Read Operation

A burst Read command (Figure 8, 9 and 10) is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Table 87, Command Truth Table. The command address bus inputs determine the starting column address for the burst. The two low-order address bits are not transmitted on the CA bus and are implied to be "0", so that the starting burst address is always a multiple of four (ex. 0x0, 0x4, 0x8, 0xC). The read latency (RL) is defined from the last rising edge of the clock that completes a read command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available  $RL * tCK + tDQSCK + tDQSQ$  after the rising edge of Clock that completes a read command. The data strobe output is driven trPRE before the first valid rising strobe edge. The first data-bit of the burst is synchronized with the first valid (i.e., post-preamble) rising edge of the data strobe. Each subsequent data out appears on each DQ pin, edge-aligned with the data strobe. At the end of a burst the DQS signals are driven for another half cycle post-amble, or for a 1.5-cycle post-amble if the programmable post-amble bit is set in the mode register. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the cross-point of DQS\_t and DQS\_c.

**Notes:**

1. BL = 32 for column n, BL = 16 for column m, RL = 14, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

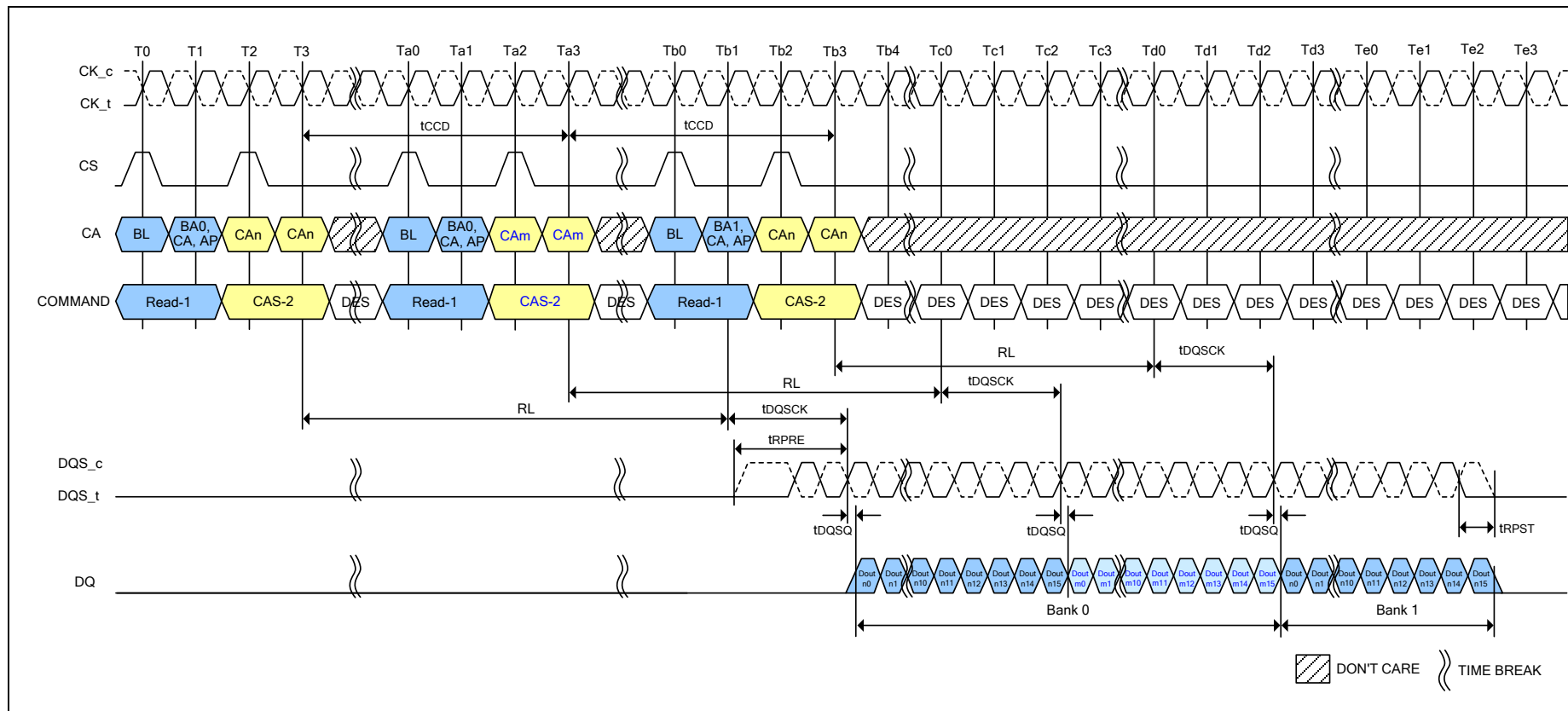
**Figure 8 - Burst Read Timing**

**Notes:**

1. BL=16, Read Preamble = Toggle, Read Postamble = 0.5nCK, Write Preamble = 2nCK, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Dout n = data-out from column n and Din n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 9 - Burst Read followed by Burst Write or Burst Mask Write**

The minimum time from a Burst Read command to a Write or MASK WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE or MASK WRITE latency is  $RL + RU(tDQSK(max)/tCK) + BL/2 + RD(tRPST) - WL + tWPST$ .

**Notes:**

1. BL = 16, tCCD = 8, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

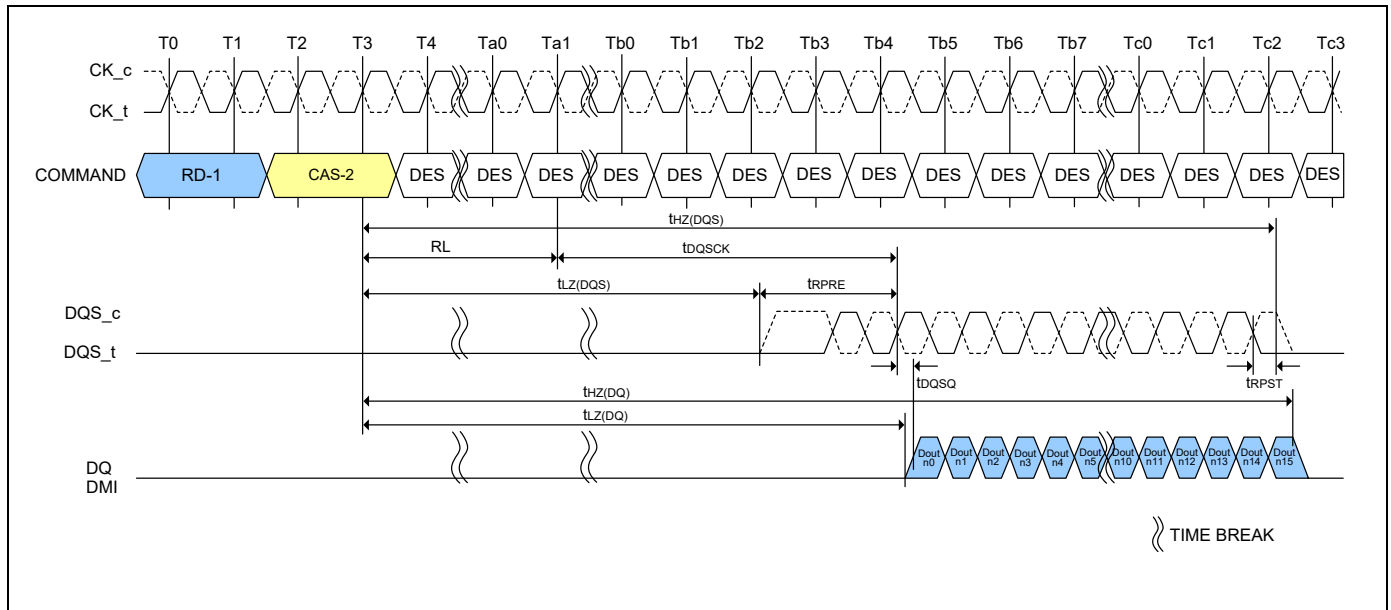
**Figure 10 - Seamless Burst Read**

The seamless Burst READ operation is supported by placing a READ command at every tCCD(Min) interval for BL16 (or every 2 x tCCD(Min) for BL32). The seamless Burst READ can access any open bank.



### 7.4.6 Read Timing

The read timing is shown in the figure below.



#### Notes:

1. BL = 16, Preamble = Toggling, Postamble = 0.5nCK.
2. DQS, DQ and DMI terminated VSSQ.
3. Output driver does not turn on before an end point of tLZ(DQS) and tLZ(DQ).
4. Output driver does not turn off before an end point of tHZ(DQS) and tHZ(DQ).

**Figure 11 - Read Timing**

### 7.4.7 tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ).

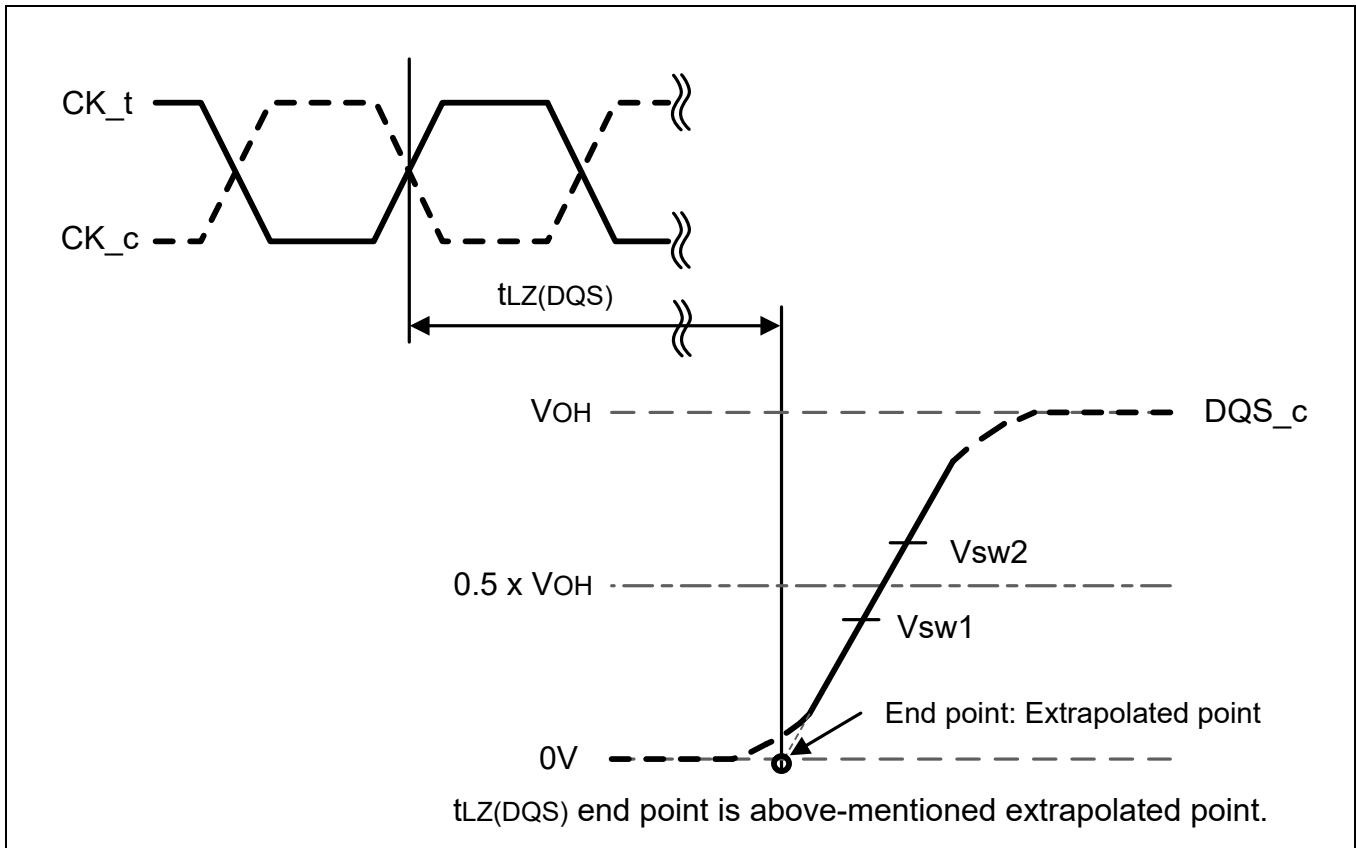
This section shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single ended.



#### 7.4.7.1 tLZ(DQS) and tHZ(DQS) Calculation for ATE (Automatic Test Equipment) – LPDDR4

The calculation method is shown in Figure 12 and Figure 13, and Table 15.

CK\_t - CK\_c crossing at 2nd CAS-2 of Read Command



#### Notes:

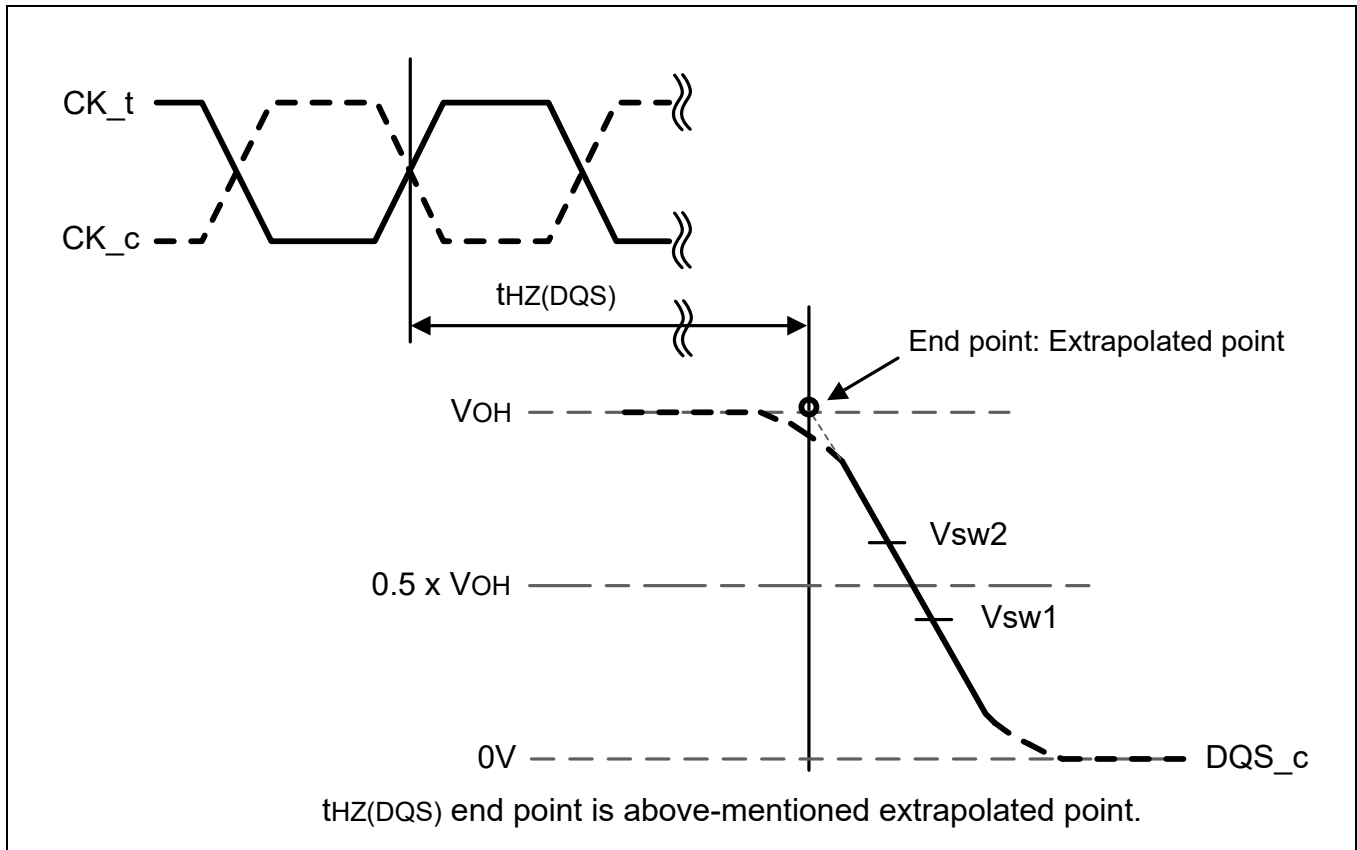
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3.
2. Termination condition for DQS\_t and DQS\_c = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.  
Use the actual VOH value for tHZ and tLZ measurements.

**Figure 12 - tLZ(DQS) method for calculating transitions and end point**





CK<sub>t</sub> - CK<sub>c</sub> crossing at 2nd CAS-2 of Read Command



**Notes:**

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3.
2. Termination condition for DQS<sub>t</sub> and DQS<sub>c</sub> = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.  
Use the actual VOH value for tHZ and tLZ measurements.

**Figure 13 - tHZ(DQS) method for calculating transitions and end point**

**Table 15 - Reference Voltage for tLZ(DQS), tHZ(DQS) Timing Measurements**

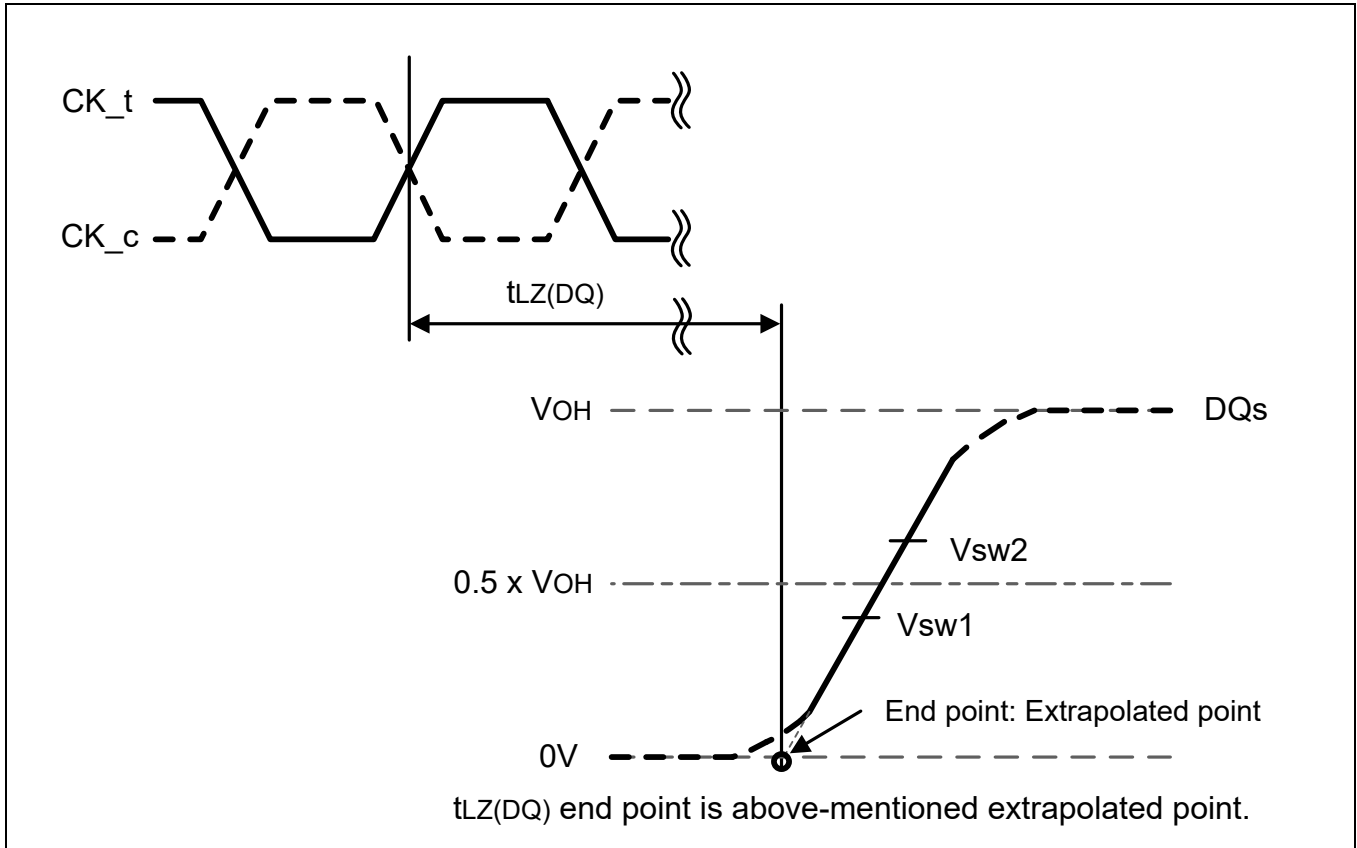
| Measured Parameter                                                          | Measured Parameter Symbol | Vsw1[V]   | Vsw2[V]   | Note |
|-----------------------------------------------------------------------------|---------------------------|-----------|-----------|------|
| DQS <sub>c</sub> low-impedance time from CK <sub>t</sub> , CK <sub>c</sub>  | tLZ(DQS)                  | 0.4 x VOH | 0.6 x VOH |      |
| DQS <sub>c</sub> high impedance time from CK <sub>t</sub> , CK <sub>c</sub> | tHZ(DQS)                  | 0.4 x VOH | 0.6 x VOH |      |



#### 7.4.7.2 tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment) – LPDDR4

The calculation method is shown in Figure 14 and Figure 15, and Table 16.

CK\_t - CK\_c crossing at 2nd CAS-2 of Read Command



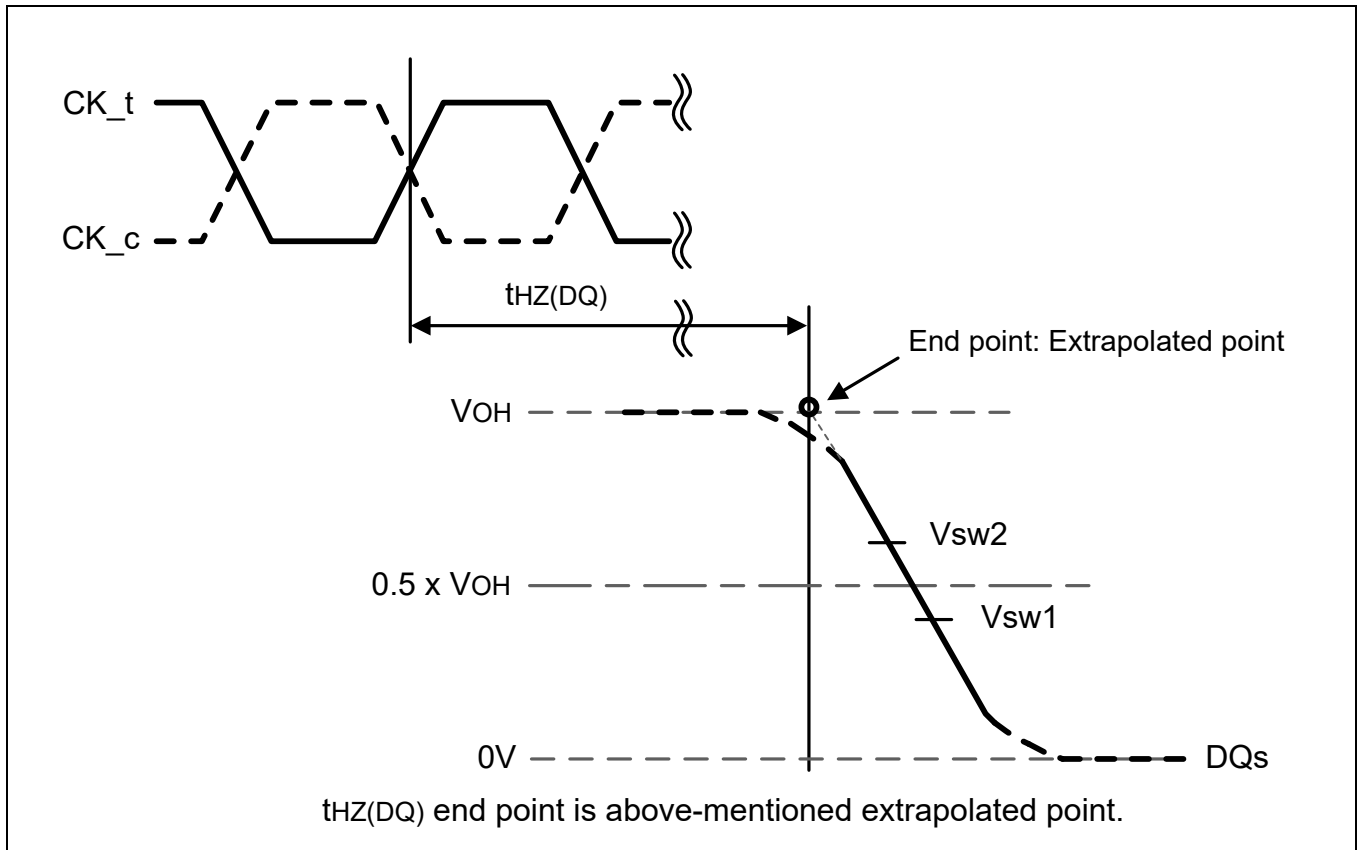
#### Notes:

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3.
2. Termination condition for DQ and DMI = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.  
Use the actual VOH value for tHZ and tLZ measurements.

**Figure 14 - tLZ(DQ) method for calculating transitions and end point**



CK<sub>t</sub> - CK<sub>c</sub> crossing at 2nd CAS-2 of Read Command



**Notes:**

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3.
2. Termination condition for DQ and DMI = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.  
Use the actual VOH value for tHZ and tLZ measurements.

**Figure 15 - tHZ(DQ) method for calculating transitions and end point**

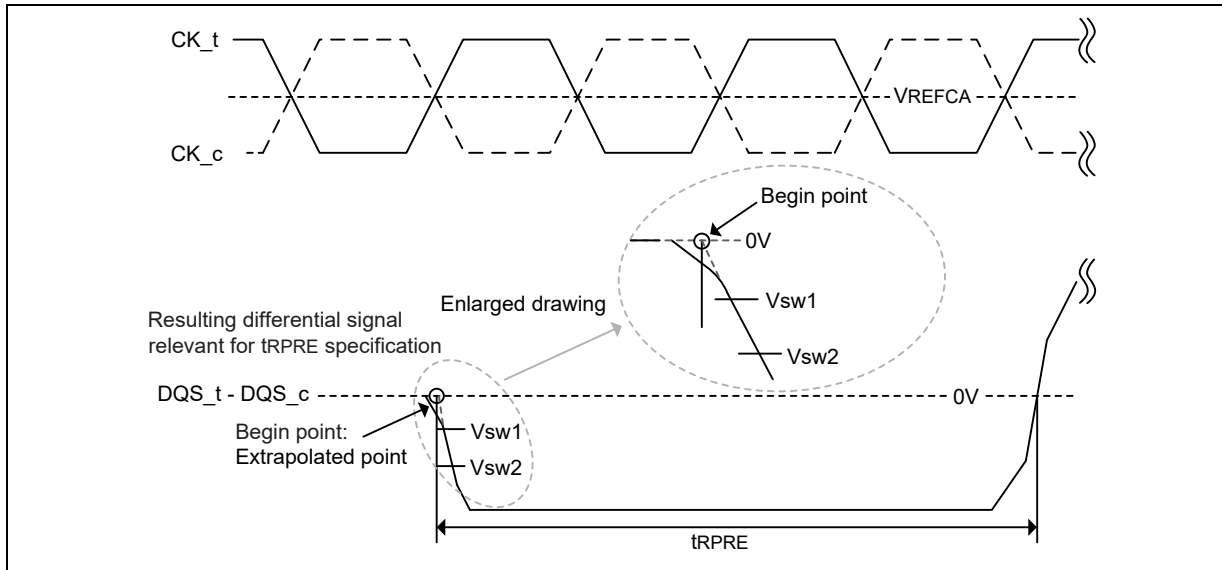
**Table 16 - Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements**

| Measured Parameter                                            | Measured Parameter Symbol | Vsw1[V]   | Vsw2[V]   | Note |
|---------------------------------------------------------------|---------------------------|-----------|-----------|------|
| DQ low-impedance time from CK <sub>t</sub> , CK <sub>c</sub>  | tLZ(DQ)                   | 0.4 x VOH | 0.6 x VOH |      |
| DQ high impedance time from CK <sub>t</sub> , CK <sub>c</sub> | tHZ(DQ)                   | 0.4 x VOH | 0.6 x VOH |      |



### 7.4.7.3 tRPRE Calculation for ATE (Automatic Test Equipment) – LPDDR4

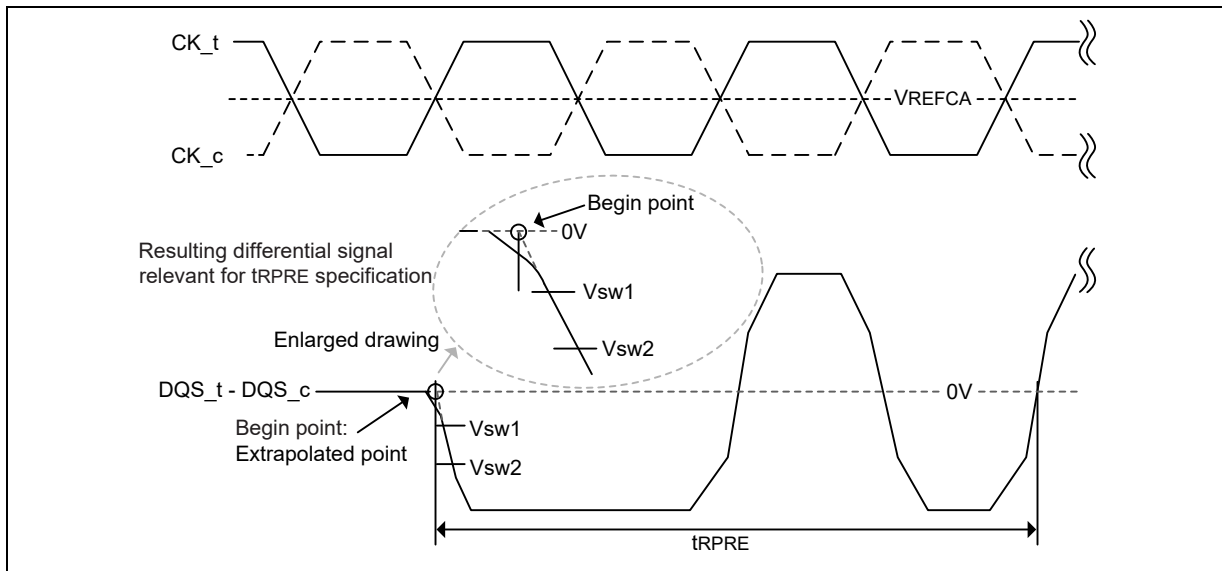
The method for calculating differential pulse widths for tRPRE is shown in Figure 16 and Figure 17, and Table 17.



**Notes:**

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3.
2. Termination condition for DQS\_t, DQS\_c, DQ and DMI = 50ohm to VSSQ.
3. Preamble = Static.

**Figure 16 - Method for calculating tRPRE transitions and endpoints**



**Notes:**

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3.
2. Termination condition for DQS\_t, DQS\_c, DQ and DMI = 50ohm to VSSQ.
3. Preamble = Toggle.

**Figure 17 - Method for calculating tRPRE transitions and endpoints**

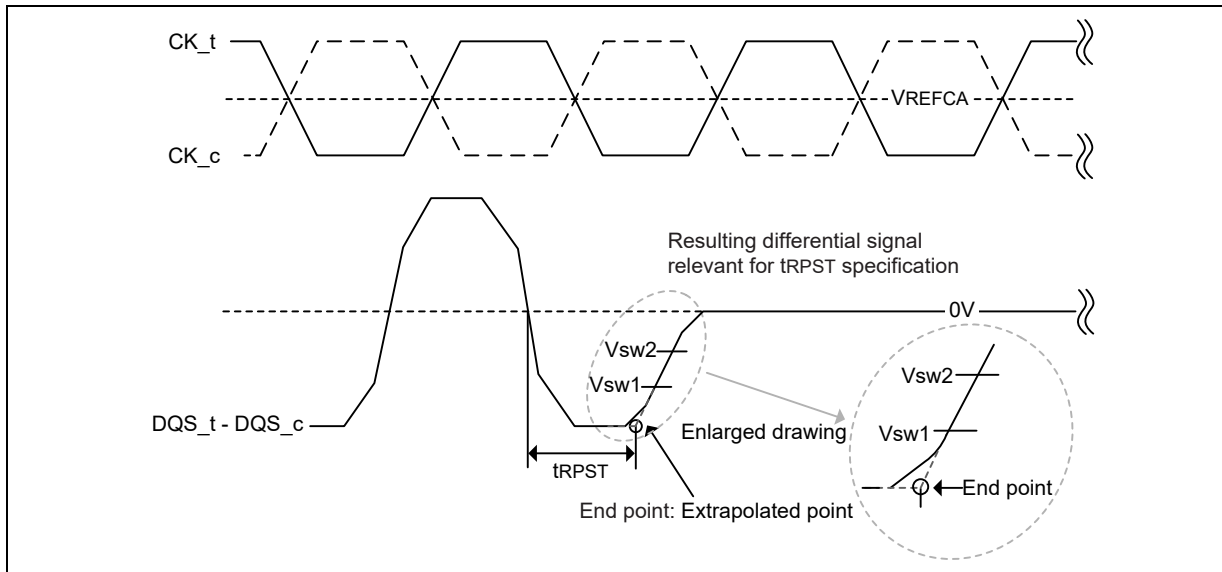
**Table 17 - Reference Voltage for tRPRE Timing Measurements**

| Measured Parameter                      | Measured Parameter Symbol | Vsw1[V]      | Vsw2[V]      | Note |
|-----------------------------------------|---------------------------|--------------|--------------|------|
| DQS_t, DQS_c differential Read Preamble | tRPRE                     | -(0.3 x VOH) | -(0.7 x VOH) |      |



#### 7.4.7.4 tRPST Calculation for ATE (Automatic Test Equipment) – LPDDR4

The method for calculating differential pulse widths for tRPST is shown in Figure 18, and Table 18 and Table 19.



##### Notes:

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3.
2. Termination condition for DQS\_t, DQS\_c, DQ and DMI = 50ohm to VSSQ.
3. Read Postamble: 0.5tCK.
4. The method for calculating differential pulse widths for 1.5 tCK Postamble is same as 0.5 tCK Postamble.

**Figure 18 - Method for calculating tRPST transitions and endpoints**

**Table 18 - Reference Voltage for tRPST Timing Measurements**

| Measured Parameter                       | Measured Parameter Symbol | Vsw1[V]      | Vsw2[V]      | Note |
|------------------------------------------|---------------------------|--------------|--------------|------|
| DQS_t, DQS_c differential Read Postamble | tRPST                     | -(0.7 x VOH) | -(0.3 x VOH) |      |

**Table 19 - Read AC Timing**

| Parameter                                 | Symbol   | Min/Max | Data Rate                                                            |      |      |      |      |      |      |      | Unit     |
|-------------------------------------------|----------|---------|----------------------------------------------------------------------|------|------|------|------|------|------|------|----------|
| Read Timing                               |          |         | 533                                                                  | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4267 |          |
| READ preamble                             | tRPRE    | Min     | 1.8                                                                  |      |      |      |      |      |      |      | tCK(avg) |
| 0.5 tCK READ postamble                    | tRPST    | Min     | 0.4                                                                  |      |      |      |      |      |      |      | tCK(avg) |
| 1.5 tCK READ postamble                    | tRPST    | Min     | 1.4                                                                  |      |      |      |      |      |      |      | tCK(avg) |
| DQ low-impedance time from CK_t, CK_c     | tLZ(DQ)  | Min     | (RL x tCK) + tDQSCK(Min) - 200pS                                     |      |      |      |      |      |      |      | pS       |
| DQ high impedance time from CK_t, CK_c    | tHZ(DQ)  | Max     | (RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK) - 100pS         |      |      |      |      |      |      |      | pS       |
| DQS_c low-impedance time from CK_t, CK_c  | tLZ(DQS) | Min     | (RL x tCK) + tDQSCK(Min) - (tRPRE(Max) x tCK) - 200pS                |      |      |      |      |      |      |      | pS       |
| DQS_c high impedance time from CK_t, CK_c | tHZ(DQS) | Max     | (RL x tCK) + tDQSCK(Max) + (BL/2 x tCK) + (tRPST(Max) x tCK) - 100pS |      |      |      |      |      |      |      | pS       |
| DQS-DQ skew                               | tDQSQ    | Max     | 0.18                                                                 |      |      |      |      |      |      |      | UI       |



#### 7.4.8 tDQSCK Timing Table

The timing parameters are provided in Table 20.

**Table 20 - tDQSCK Timing Table**

| Parameter                                                     | Symbol      | Min | Max | Unit  | Notes |
|---------------------------------------------------------------|-------------|-----|-----|-------|-------|
| DQS Output Access Time from CK_t/CK_c                         | tDQSCK      | 1.5 | 3.5 | nS    | 1     |
| DQS Output Access Time from CK_t/CK_c - Temperature Variation | tDQSCK_temp | -   | 4   | pS/°C | 2     |
| DQS Output Access Time from CK_t/CK_c - Voltage Variation     | tDQSCK_volt | -   | 7   | pS/mV | 3     |

**Notes:**

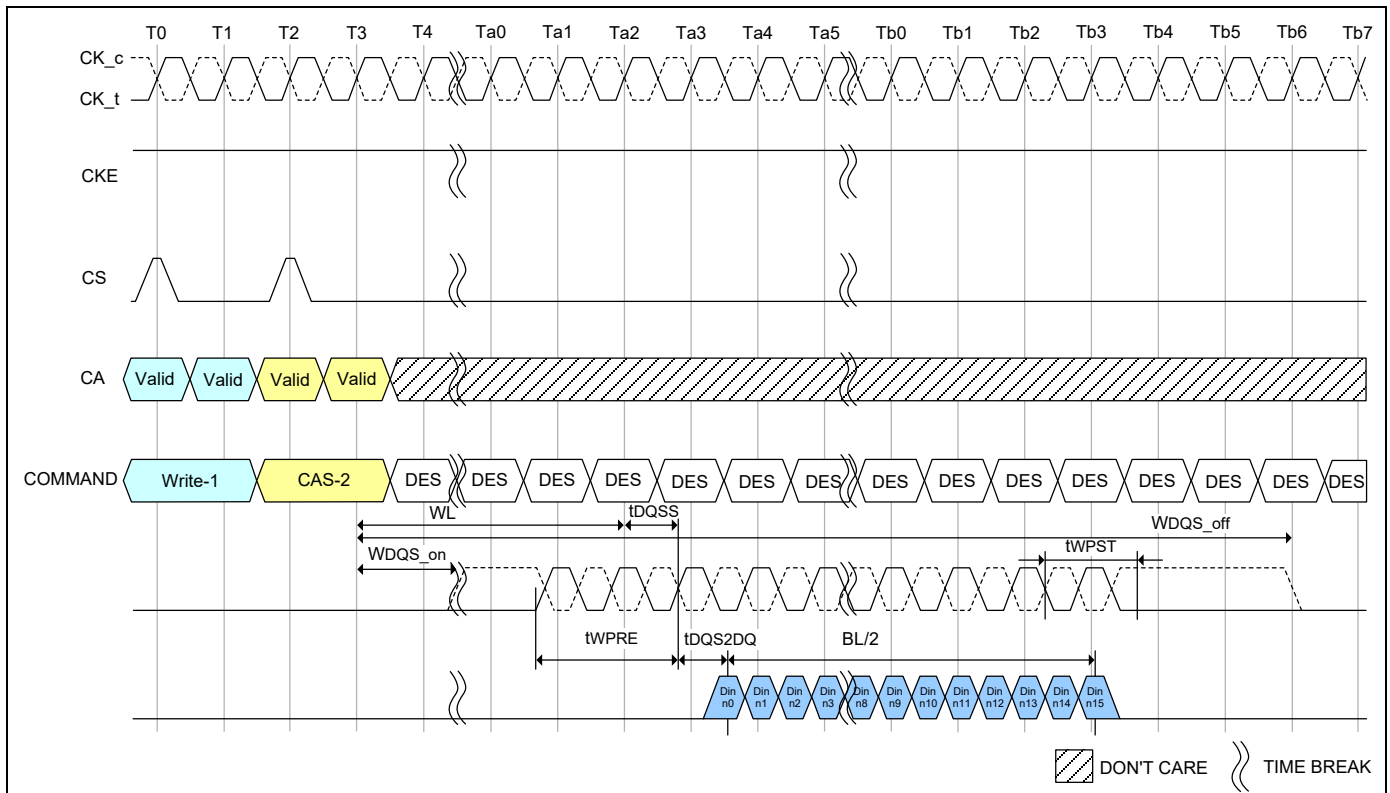
1. Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply with to the component Min-Max DC Operating conditions.
2. tDQSCK\_temp max delay variation as a function of temperature.
3. tDQSCK\_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSCK\_volt should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions.

The voltage variation is defined as the

$$\text{Max}[\text{abs}\{\text{tDQSCKmin@V1} - \text{tDQSCKmax@V2}\}, \text{abs}\{\text{tDQSCKmax@V1} - \text{tDQSCKmin@V2}\}] / \text{abs}\{V1 - V2\}.$$

For tester measurement VDDQ = VDD2 is assumed.

Downloaded from [Arrow.com](https://arrow.com).

**Notes:**

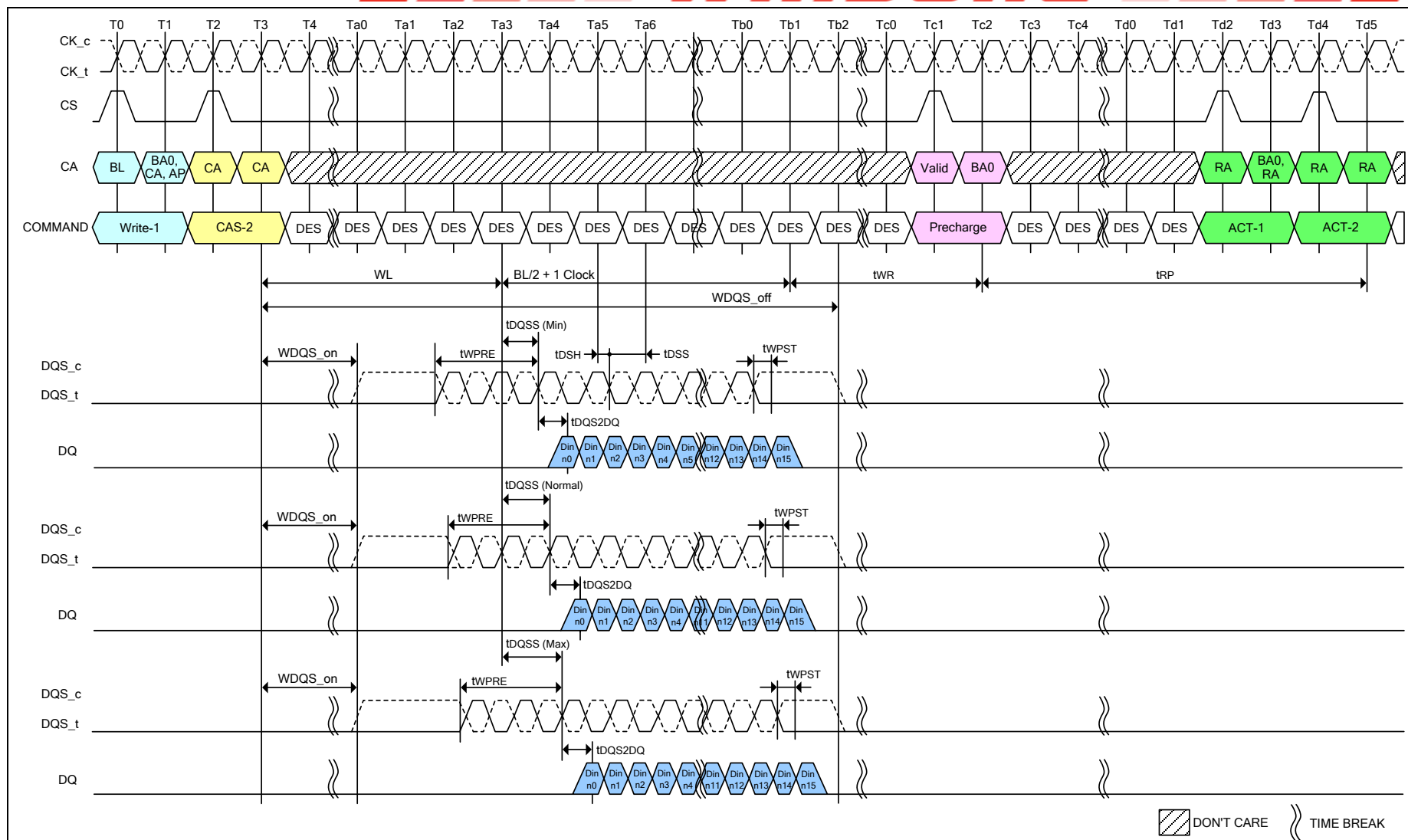
1. BL = 16, Postamble = 1.5nCK.
2. DQS and DQ terminated VSSQ.
3. DQS<sub>t</sub>/DQS<sub>c</sub> is "don't care" prior to the start of tWPRE.  
No transition of DQS is implied, as DQS<sub>t</sub>/DQS<sub>c</sub> can be HIGH, LOW, or HI-Z prior to tWPRE.

**Figure 20 - DQS Write Preamble and Postamble: 1.5nCK Postamble****7.4.10 Burst Write Operation**

A burst WRITE command (Figure 21 and Figure 22) is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table (Table 87). Column addresses C[3:2] should be driven LOW for Burst WRITE commands, and column addresses C[1:0] are not transmitted on the CA bus (and are assumed to be zero), so that the starting column burst address is always aligned with a 32B boundary. The write latency (WL) is defined from the last rising edge of the clock that completes a write command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which tDQSS is measured. The first valid "latching" edge of DQS must be driven WL \* tCK + tDQSS after the rising edge of Clock that completes a write command.

The LPDDR4/LPDDR4X SDRAM uses an un-matched DQS-DQ path for lower power, so the DQS-strobe must arrive at the SDRAM ball prior to the DQ signal by the amount of tDQS2DQ. The DQS-strobe output is driven tWPRE before the first valid rising strobe edge. The tWPRE pre-amble is required to be 2 x tCK. The DQS strobe must be trained to arrive at the DQ pin center-aligned with the DQ-data. The DQ-data must be held for tDIVW (data input valid window) and the DQS must be periodically trained to stay centered in the tDIVW window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the SDRAM on successive edges of DQS until the 16 or 32 bit data burst is complete. The DQS-strobe must remain active (toggling) for tWPST (WRITE post-amble) after the completion of the burst WRITE. After a burst WRITE operation, tWR must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the cross point of DQS<sub>t</sub> and DQS<sub>c</sub>.



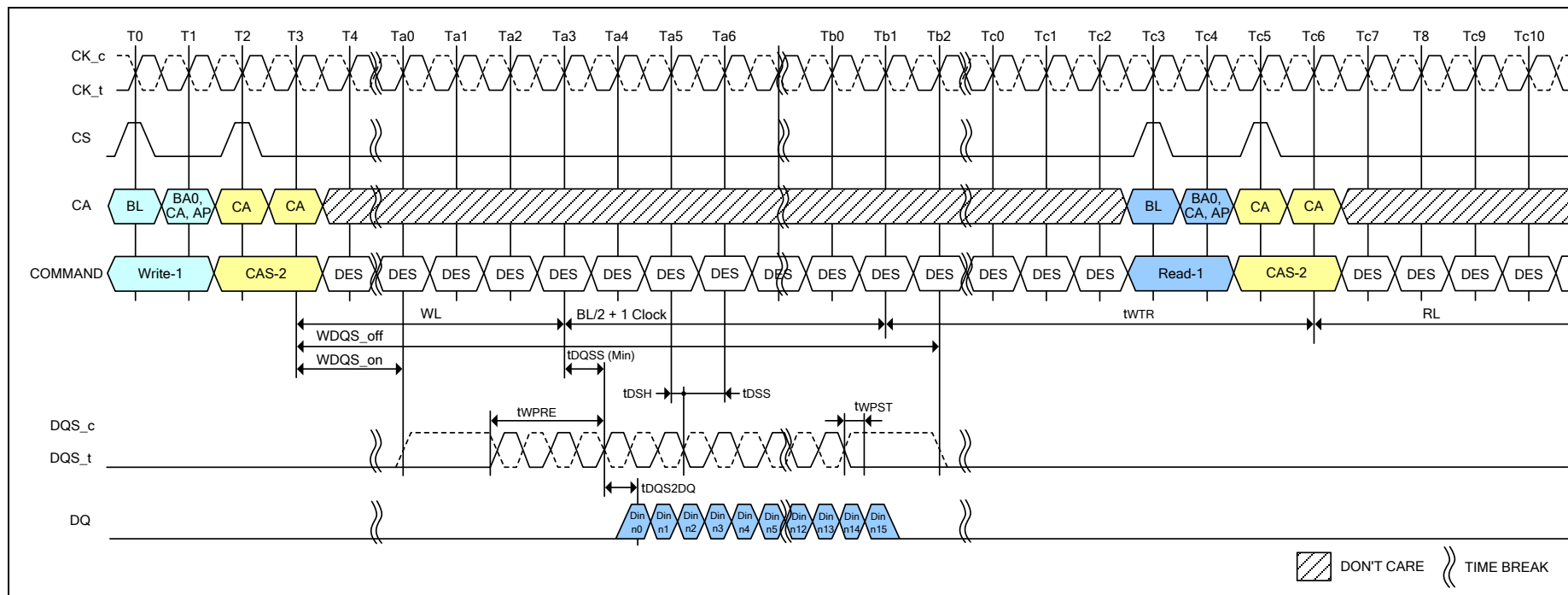
**Notes:**

1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Din n = data-in to column n.
3. The minimum number of clock cycles from the burst write command to the precharge command for same bank is  $[WL + 1 + BL/2 + RU(tWR/tCK)]$ .
4. tWR starts at the rising edge of CK after the last latching edge of DQS.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 21 - Burst Write Operation**

Publication Release Date: Dec. 30, 2024

Revision: A01-001

**Notes:**

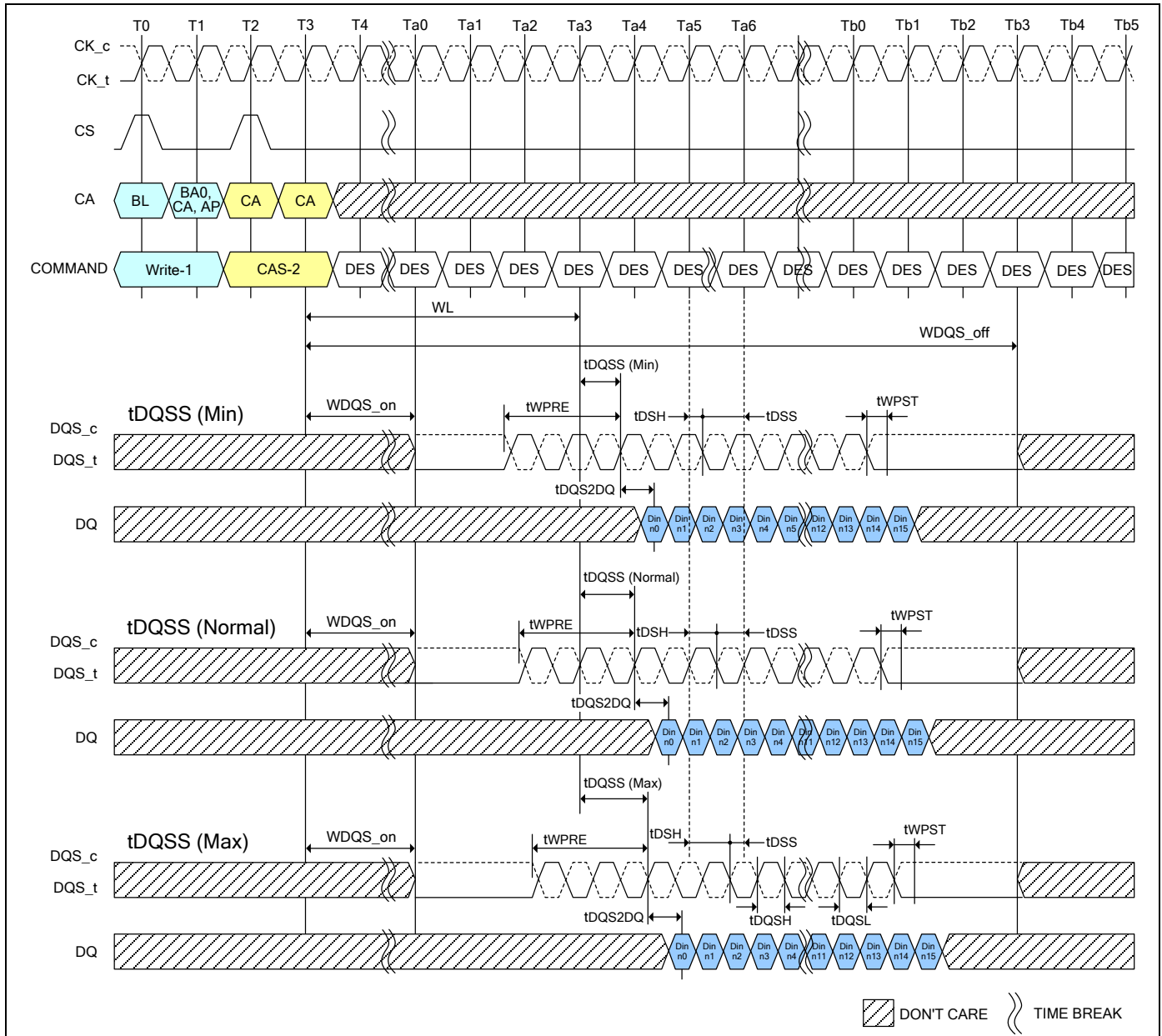
1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Din n = data-in to column n.
3. The minimum number of clock cycles from the burst write command to the burst read command for any bank is  $[WL + 1 + BL/2 + RU(tWTR/tCK)]$ .
4. tWTR starts at the rising edge of CK after the last latching edge of DQS.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 22 - Burst Write Followed by Burst Read**



### 7.4.11 Write Timing

The write timing is shown in Figure 23.



#### Notes:

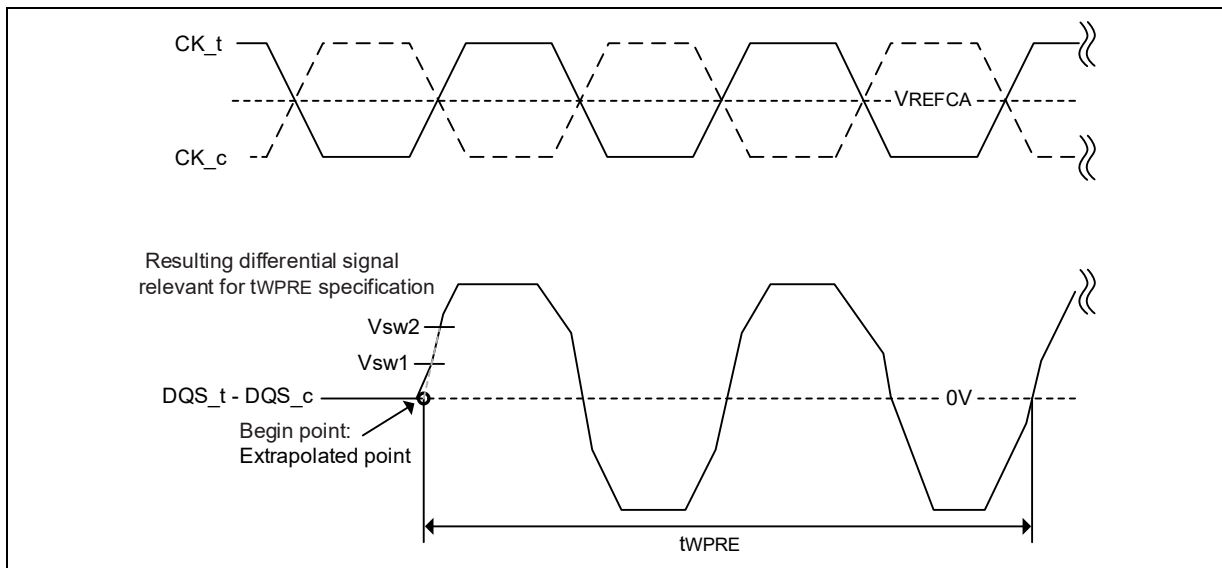
1. BL=16, Write Postamble = 0.5nCK.
2. Din n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 23 - Write Timing



#### 7.4.11.1 tWPRE Calculation for ATE (Automatic Test Equipment)

The method for calculating differential pulse widths for tWPRE is shown in Figure 24 and Table 21.



**Note:**

1. Termination condition for DQS\_t, DQS\_c, DQ and DMI = 50ohm to VSSQ.

**Figure 24 - Method for calculating tWPRE transitions and endpoints**

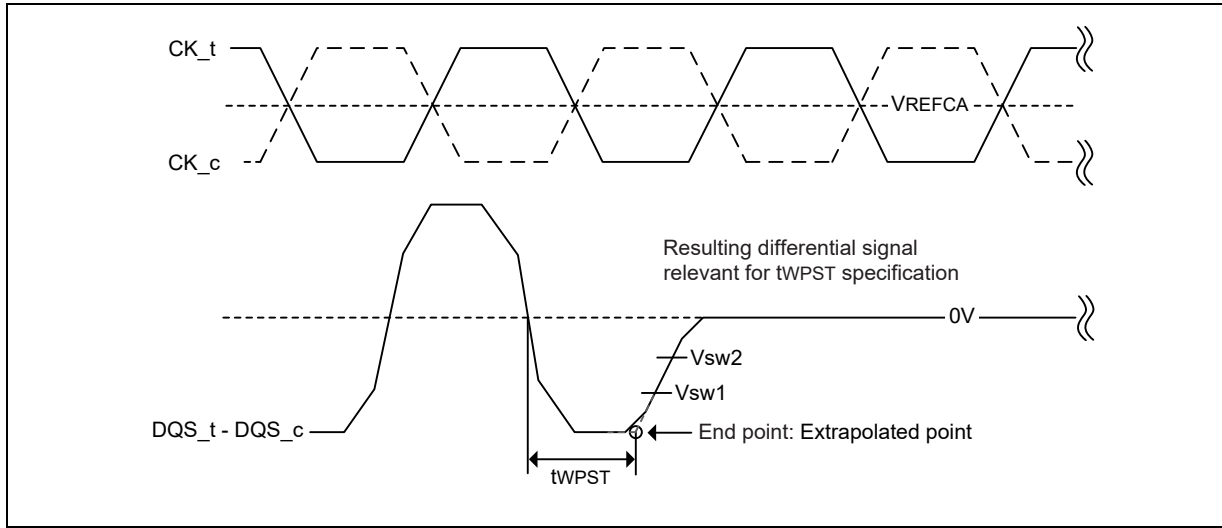
**Table 21 - Reference Voltage for tWPRE Timing Measurements**

| Measured Parameter                       | Measured Parameter Symbol | Vsw1[V]       | Vsw2[V]       | Note |
|------------------------------------------|---------------------------|---------------|---------------|------|
| DQS_t, DQS_c differential WRITE Preamble | tWPRE                     | VIHL_AC x 0.3 | VIHL_AC x 0.7 |      |



#### 7.4.11.2 tWPST Calculation for ATE (Automatic Test Equipment)

The method for calculating differential pulse widths for tWPST is shown in Figure 25 and Table 22 and Table 23.



**Note:**

1. Termination condition for DQS\_t, DQS\_c, DQ and DMI = 50ohm to VSSQ.
2. Write Postamble: 0.5tCK.
3. The method for calculating differential pulse widths for 1.5 tCK Postamble is same as 0.5 tCK Postamble.

**Figure 25 - Method for calculating tWPST transitions and endpoints**

**Table 22 - Reference Voltage for tWPST Timing Measurements**

| Measured Parameter                        | Measured Parameter Symbol | Vsw1[V]           | Vsw2[V]           | Note |
|-------------------------------------------|---------------------------|-------------------|-------------------|------|
| DQS_t, DQS_c differential WRITE Postamble | tWPST                     | - (VIHL_AC x 0.7) | - (VIHL_AC x 0.3) |      |

**Table 23 - Write AC Timing**

| Parameter                          | Symbol | Min/Max | Data Rate |      |      |      |      |      |      |      | Unit     | Note |
|------------------------------------|--------|---------|-----------|------|------|------|------|------|------|------|----------|------|
| Write Timing                       |        |         | 533       | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4267 |          |      |
| Write command to 1st DQS latching  | tDQSS  | Min     | 0.75      |      |      |      |      |      |      |      | tCK(avg) |      |
|                                    |        | Max     | 1.25      |      |      |      |      |      |      |      |          |      |
| DQS input high-level width         | tDQSH  | Min     | 0.4       |      |      |      |      |      |      |      | tCK(avg) |      |
| DQS input low-level width          | tDQSL  | Min     | 0.4       |      |      |      |      |      |      |      | tCK(avg) |      |
| .DQS falling edge to CK setup time | tDSS   | Min     | 0.2       |      |      |      |      |      |      |      | tCK(avg) |      |
| DQS falling edge hold time from CK | tDSH   | Min     | 0.2       |      |      |      |      |      |      |      | tCK(avg) |      |
| Write preamble                     | tWPRE  | Min     | 1.8       |      |      |      |      |      |      |      | tCK(avg) |      |
| 0.5 tCK Write postamble            | tWPST  | Min     | 0.4       |      |      |      |      |      |      |      | tCK(avg) | 1    |
| 1.5 tCK Write postamble            | tWPST  | Min     | 1.4       |      |      |      |      |      |      |      | tCK(avg) | 1    |

**Note:**

1. The length of Write Postamble depends on MR3 OP[1] setting.



#### 7.4.12 Read and Write Latencies

The latencies are provided in Table 24.

**Table 24 - Read and Write Latencies**

| Read Latency |        | Write Latency |       | nWR | nRTP | Lower Clock Frequency Limit (>) | Upper Clock Frequency Limit (≤) | Notes            |
|--------------|--------|---------------|-------|-----|------|---------------------------------|---------------------------------|------------------|
| No DBI       | w/ DBI | Set A         | Set B |     |      |                                 |                                 |                  |
| 6            | 6      | 4             | 4     | 6   | 8    | 10                              | 266                             | 1, 2, 3, 4, 5, 6 |
| 10           | 12     | 6             | 8     | 10  | 8    | 266                             | 533                             |                  |
| 14           | 16     | 8             | 12    | 16  | 8    | 533                             | 800                             |                  |
| 20           | 22     | 10            | 18    | 20  | 8    | 800                             | 1066                            |                  |
| 24           | 28     | 12            | 22    | 24  | 10   | 1066                            | 1333                            |                  |
| 28           | 32     | 14            | 26    | 30  | 12   | 1333                            | 1600                            |                  |
| 32           | 36     | 16            | 30    | 34  | 14   | 1600                            | 1866                            |                  |
| 36           | 40     | 18            | 34    | 40  | 16   | 1866                            | 2133                            |                  |
| nCK          | nCK    | nCK           | nCK   | nCK | nCK  | MHz                             | MHz                             |                  |

#### Notes:

1. The LPDDR4/LPDDR4X SDRAM device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
2. DBI for Read operations is enabled in MR3 OP[6]. When MR3 OP[6]=0, then the "No DBI" column should be used for Read Latency. When MR3 OP[6]=1, then the "w/DBI" column should be used for Read Latency.
3. Write Latency Set "A" and Set "B" is determined by MR2 OP[6]. When MR2 OP[6]=0, then Write Latency Set "A" should be used. When MR2 OP[6]=1, then Write Latency Set "B" should be used.
4. The programmed value of nWR is the number of clock cycles the LPDDR4/LPDDR4X SDRAM device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (Auto Precharge). It is determined by RU(tWR/tCK).
5. The programmed value of nRTP is the number of clock cycles the LPDDR4/LPDDR4X SDRAM device uses to determine the starting point of an internal Precharge operation after a Read burst with AP (Auto Precharge). It is determined by RU(tRTP/tCK).
6. nRTP shown in this table is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a precharge.

#### 7.4.13 Write and Masked Write operation DQS controls (WDQS Control)

LPDDR4/LPDDR4X SDRAMs support write and masked write operations with the following DQS controls. Before and after Write and Masked Write operations are issued, DQS\_t/DQS\_c is required to have a sufficient voltage gap to make sure the write buffers operating normally without any risk of metastability.

The LPDDR4/LPDDR4X SDRAM is supported by either of two WDQS control modes (Sections 7.4.13.1 and 7.4.13.2).

Mode 1: Read Based Control

Mode 2: WDQS\_on / WDQS\_off definition based control

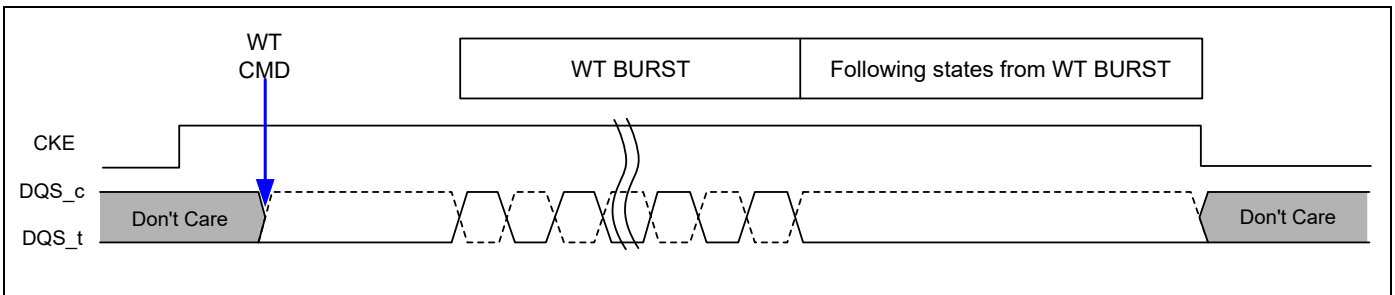
Regardless of ODT enable/disable, WDQS related timing described here does not allow any change of existing command timing constraints for all read/write operations. In case of any conflict or ambiguity on the command timing constraints caused by the specifications here, the specifications defined in section 7.4.35, Table 69 (or sections 7.4.13.1 and 7.4.13.2) should have higher priority than WDQS control requirements.



#### 7.4.13.1 WDQS Control Mode 1 - Read Based Control

The LPDDR4/LPDDR4X SDRAM needs to be guaranteed the differential WDQS, but the differential WDQS can be controlled as described below. WDQS control requirements here can be ignored while differential read DQS is operated or while DQS hands over from Read to Write and vice versa.

1. At the time a write / masked write command is issued, SoC makes the transition from driving DQS\_c high to driving differential DQS\_t/DQS\_c, followed by normal differential burst on DQS pins.
2. At the end of postamble of write /masked write burst, SoC resumes driving DQS\_c high through the subsequent states except for DQS toggling and DQS turn-around time of WT-RD and RD-WT as long as CKE is high.
3. When CKE is low, the state of DQS\_t and DQS\_c is allowed to be "Don't Care".



#### 7.4.13.2 WDQS Control Mode 2 - WDQS\_on/off

After write / masked write command is issued, DQS\_t and DQS\_c required to be differential from WDQS\_on, and DQS\_t and DQS\_c can be "Don't Care" status from WDQS\_off of write / masked write command. When ODT is enabled, WDQS\_on and WDQS\_off timing is located in the middle of the operations. When host disables ODT, WDQS\_on and WDQS\_off constraints conflict with tRTW. The timing does not conflict when ODT is enabled because WDQS\_on and WDQS\_off timing is covered in section 7.4.41, ODTLon and ODTLoff. However, regardless of ODT on/off, WDQS\_on/off timing below does not change any command timing constraints for all read and write operations. In order to prevent the conflict, WDQS\_on/off requirement can be ignored when WDQS\_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD). In addition, the period during DQS toggling caused by Read and Write can be counted as WDQS\_on/off.

See Tables 25, 26 and 27, and Figures 26, 27 and 28.

#### Parameters

- WDQS\_on: the max delay from write / masked write command to differential DQS\_t and DQS\_c.
- WDQS\_off: the min delay for DQS\_t and DQS\_c differential input after the last write / masked write command.
- WDQS\_Exception: the period where WDQS\_on and WDQS\_off timing is overlapped with read operation or with DQS turn-around (RD-WT, WT-RD).
  - WDQS\_Exception @ ODT disable =  $\max(WL - WDQS\_on + tDQSTA - tWPRE - n \cdot tCK, 0 \cdot tCK)$   
 where RD to WT command gap =  $tRTW(\min)@ODT\ disable + n \cdot tCK$
  - WDQS\_Exception @ ODT enable = tDQSTA



Table 25 - WDQS\_on / WDQS\_off Definition

| WL    |       | nWR | nRTP | WDQS_on (max) |       | WDQS_off (min) |       | Lower Clock Frequency Limit (>) | Upper Clock Frequency Limit (≤) |
|-------|-------|-----|------|---------------|-------|----------------|-------|---------------------------------|---------------------------------|
| Set A | Set B |     |      | Set A         | Set B | Set A          | Set B |                                 |                                 |
| 4     | 4     | 6   | 8    | 0             | 0     | 15             | 15    | 10                              | 266                             |
| 6     | 8     | 10  | 8    | 0             | 0     | 18             | 20    | 266                             | 533                             |
| 8     | 12    | 16  | 8    | 0             | 6     | 21             | 25    | 533                             | 800                             |
| 10    | 18    | 20  | 8    | 4             | 12    | 24             | 32    | 800                             | 1066                            |
| 12    | 22    | 24  | 10   | 4             | 14    | 27             | 37    | 1066                            | 1333                            |
| 14    | 26    | 30  | 12   | 6             | 18    | 30             | 42    | 1333                            | 1600                            |
| 16    | 30    | 34  | 14   | 6             | 20    | 33             | 47    | 1600                            | 1866                            |
| 18    | 34    | 40  | 16   | 8             | 24    | 36             | 52    | 1866                            | 2133                            |
| nCK   | nCK   | nCK | nCK  | nCK           | nCK   | nCK            | nCK   | MHz                             | MHz                             |

**Notes:**

1. WDQS\_on/off requirement can be ignored when WDQS\_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD).
2. The period during which DQS is toggling because of a Read or Write can be counted as part of the WDQS\_on/off requirement.

Table 26 - WDQS\_on / WDQS\_off Allowable Variation Range

|          | Min   | Max  | Unit     |
|----------|-------|------|----------|
| WDQS_On  | -0.25 | 0.25 | tCK(avg) |
| WDQS_Off | -0.25 | 0.25 | tCK(avg) |

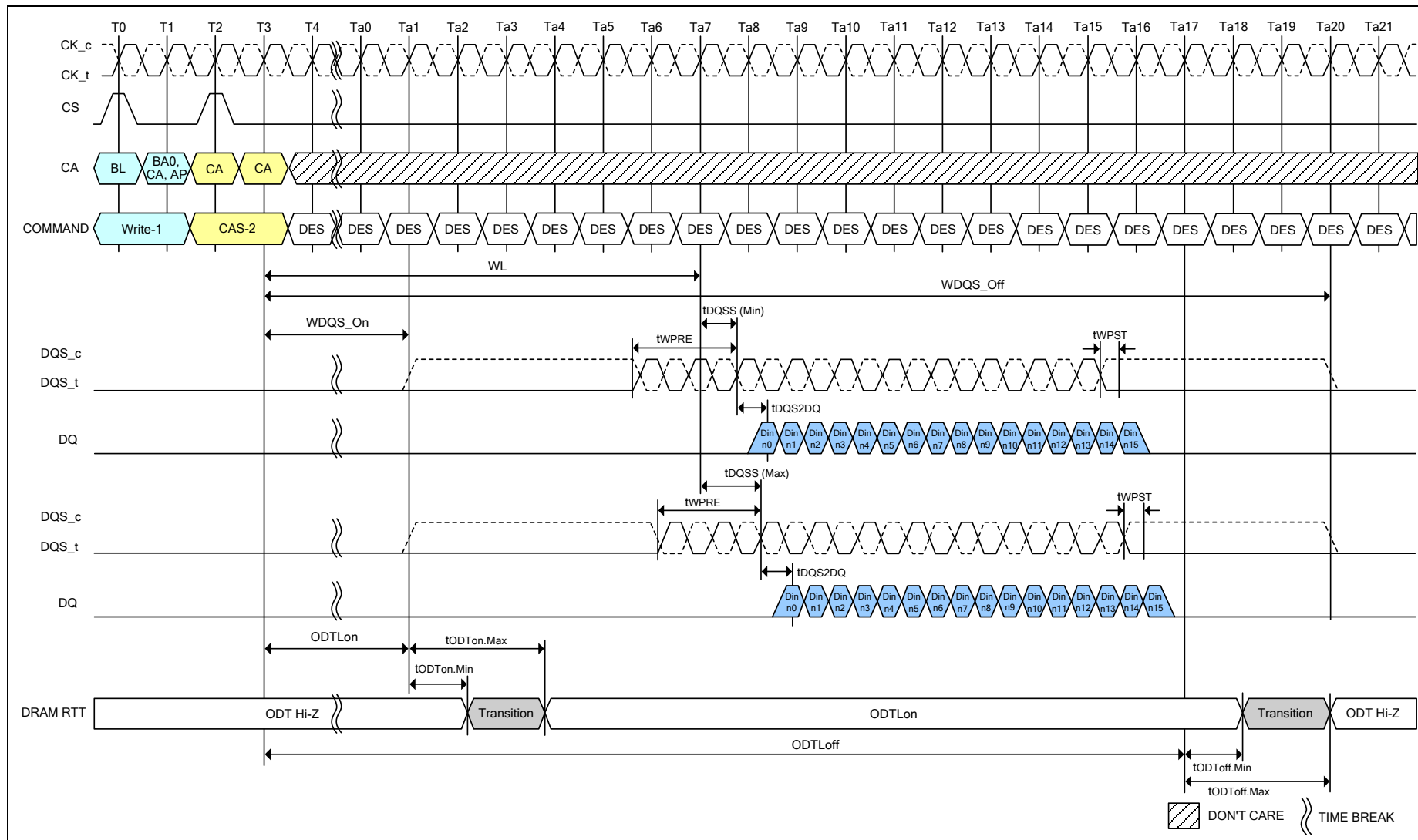
Table 27 - DQS turn around parameter

| Parameter | Description                                         | Value | Unit | Note |
|-----------|-----------------------------------------------------|-------|------|------|
| tDQSTA    | Turn-around time RDQS to WDQS for WDQS control case | -     | -    | 1    |

**Note:**

1. tDQSTA is only applied to WDQS\_exception case when WDQS Control. Except for WDQS Control, tDQSTA can be ignored. The tDQSTA is to be characterized at system level.



**Notes:**

1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Din n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. DRAM RTT is only applied when ODT is enabled (MR11 OP[2:0] is not 000<sub>b</sub>).

**Figure 26 - Burst Write Operation**

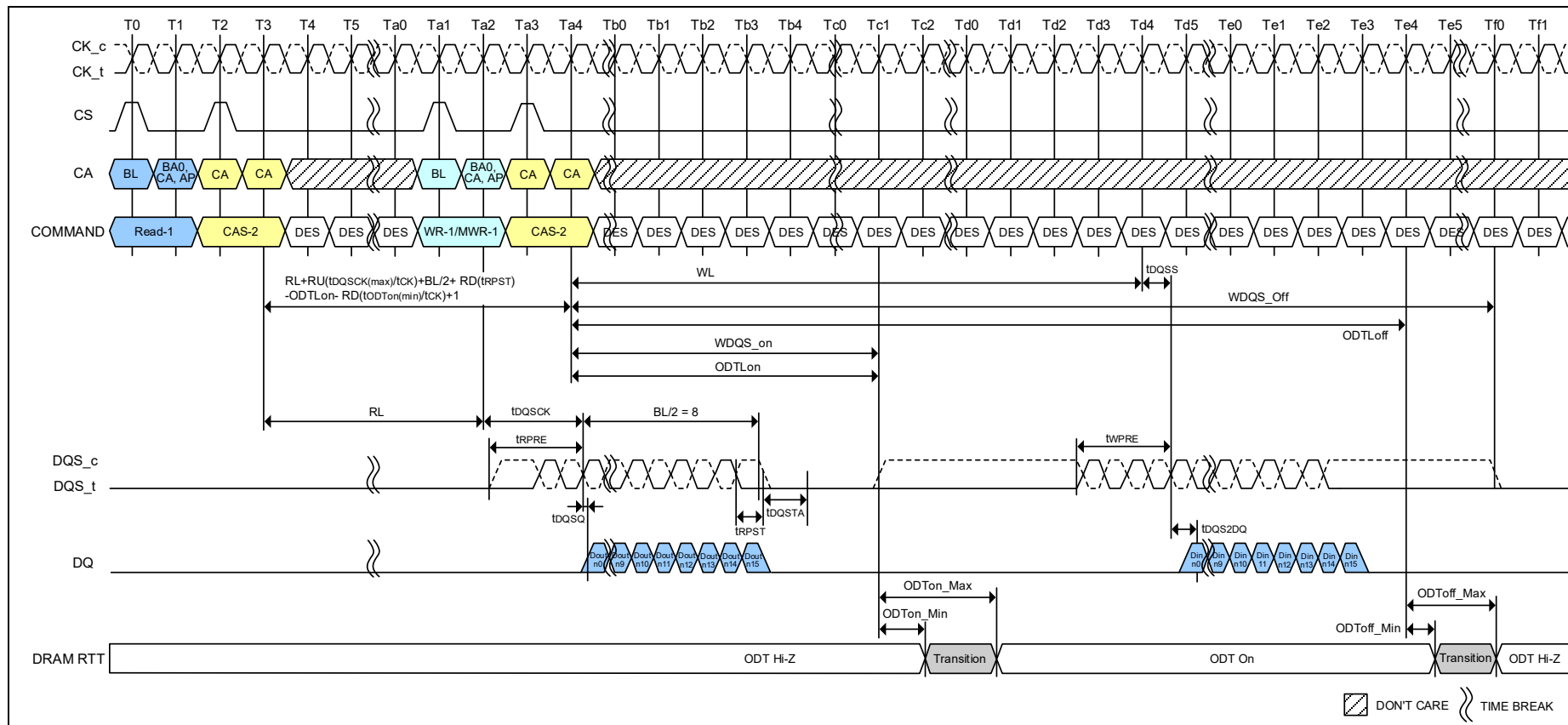
Publication Release Date: Dec. 30, 2024

Revision: A01-001



1. BL=16, Read Preamble = Toggle, Read Postamble = 0.5nCK, Write Preamble = 2nCK, Write Postamble = 0.5nCK.
2. Dout n = data-out from column n and Din n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. WDQS\_on and WDQS\_off requirement can be ignored where WDQS\_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD).

**Figure 27 - Burst Read followed by Burst Write or Burst Mask Write (ODT Disable)**



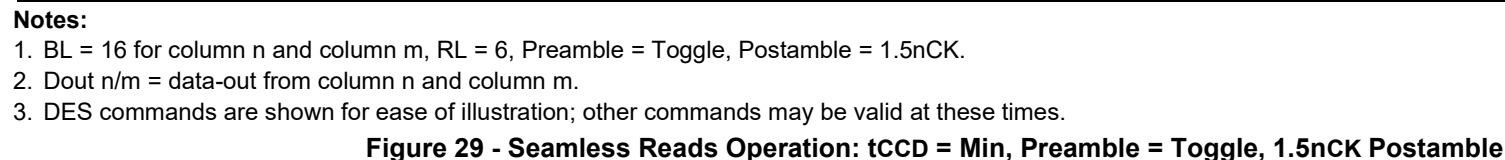
#### Notes:

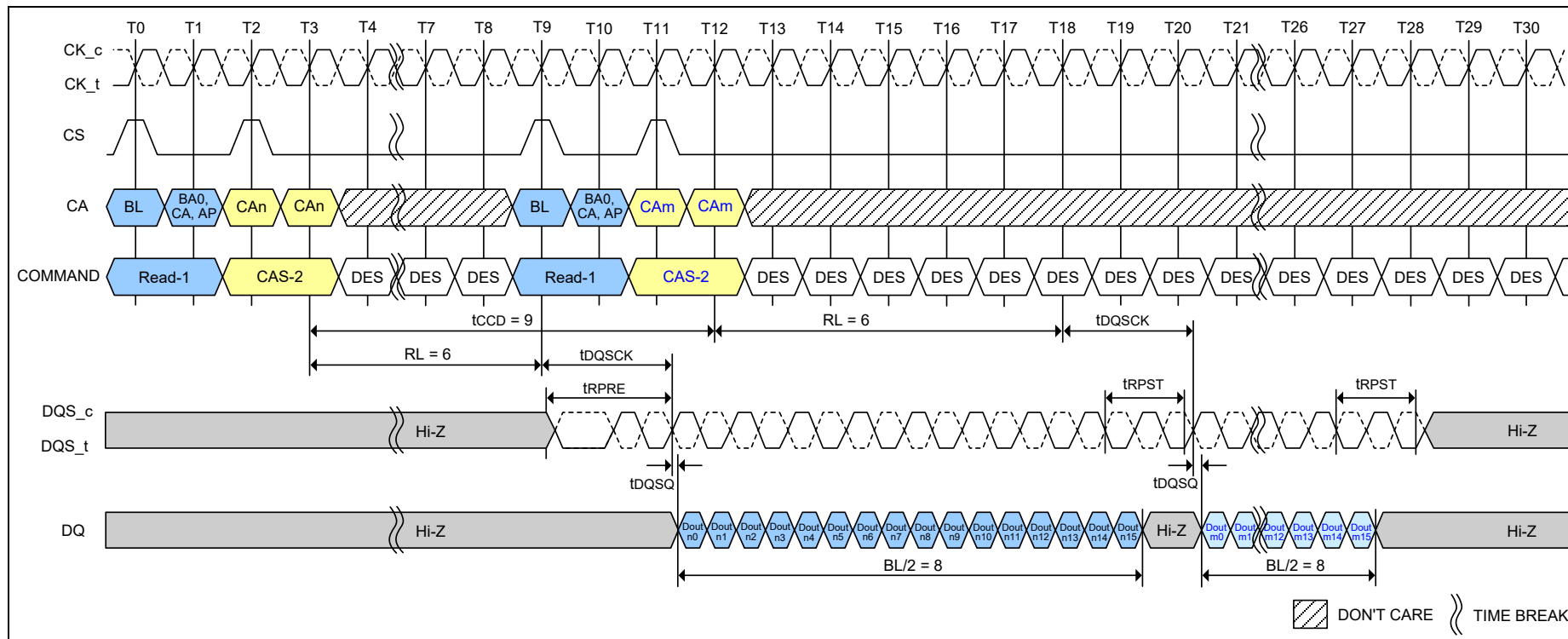
1. BL=16, Read Preamble = Toggle, Read Postamble = 0.5nCK, Write Preamble = 2nCK, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Dout n = data-out from column n and Din n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. WDQS\_on and WDQS\_off requirement can be ignored where WDQS\_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD).

**Figure 28 - Burst Read followed by Burst Write or Burst Mask Write (ODT Enable)**

Timing diagrams in this material describe Postamble and Preamble merging behavior in Read to Read or Write to Write operations with tCCD+n.

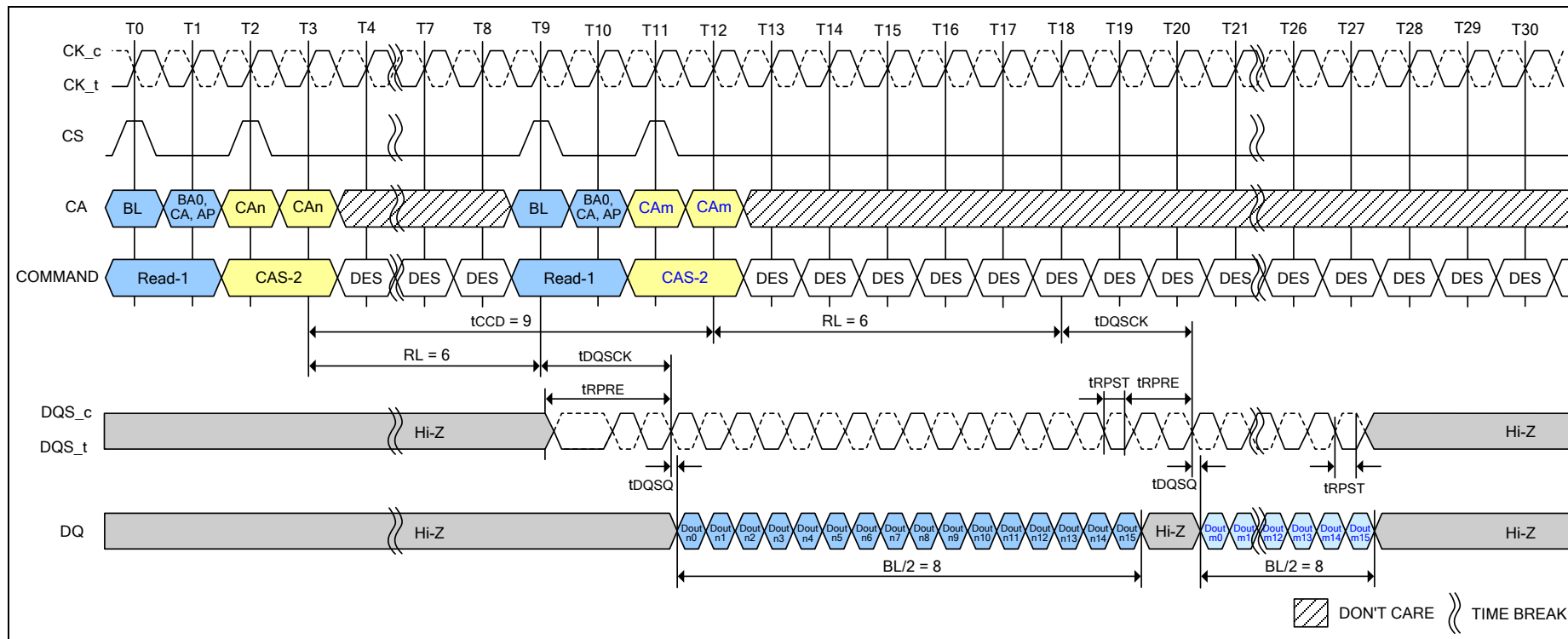
Read to read operation is shown in Figure 29 through Figure 41.



**Notes:**

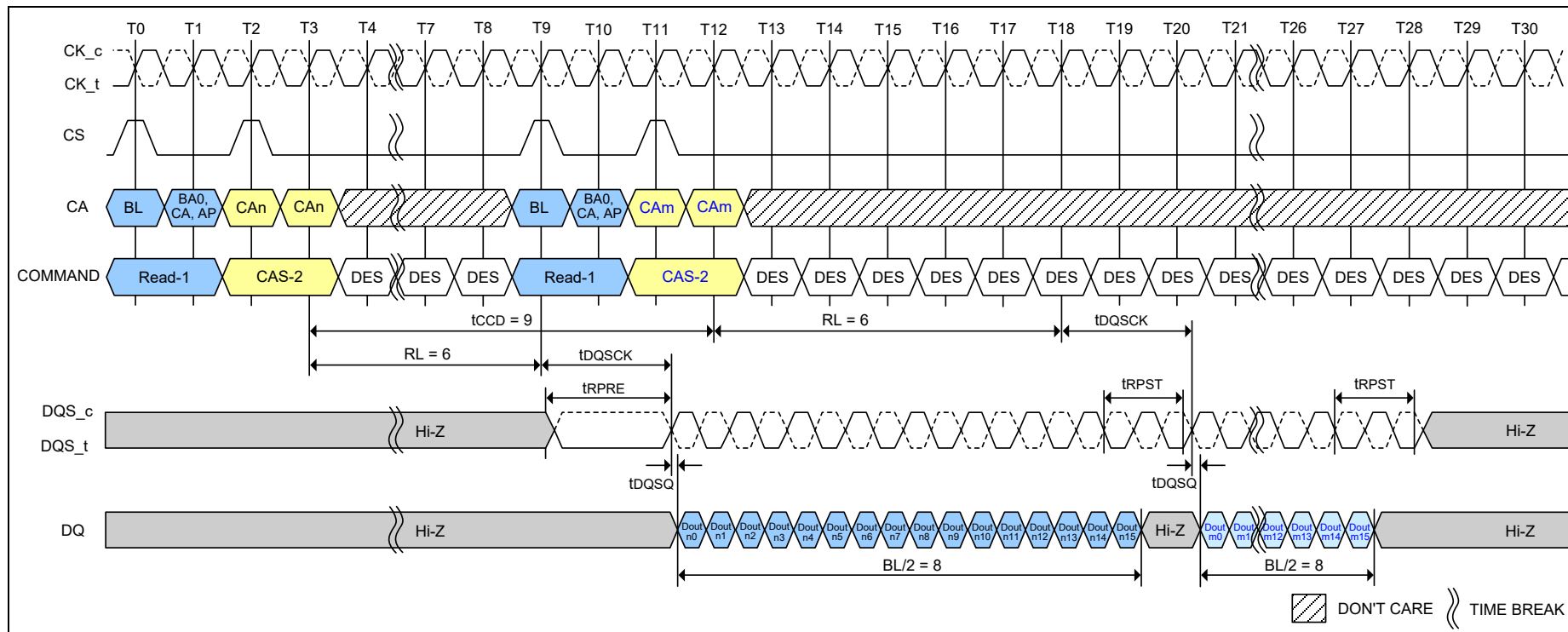
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 1.5nCK.
2. DQout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 30 - Consecutive Reads Operation:  $t_{CCD} = \text{Min} + 1$ , Preamble = Toggle, 1.5nCK Postamble**

**Notes:**

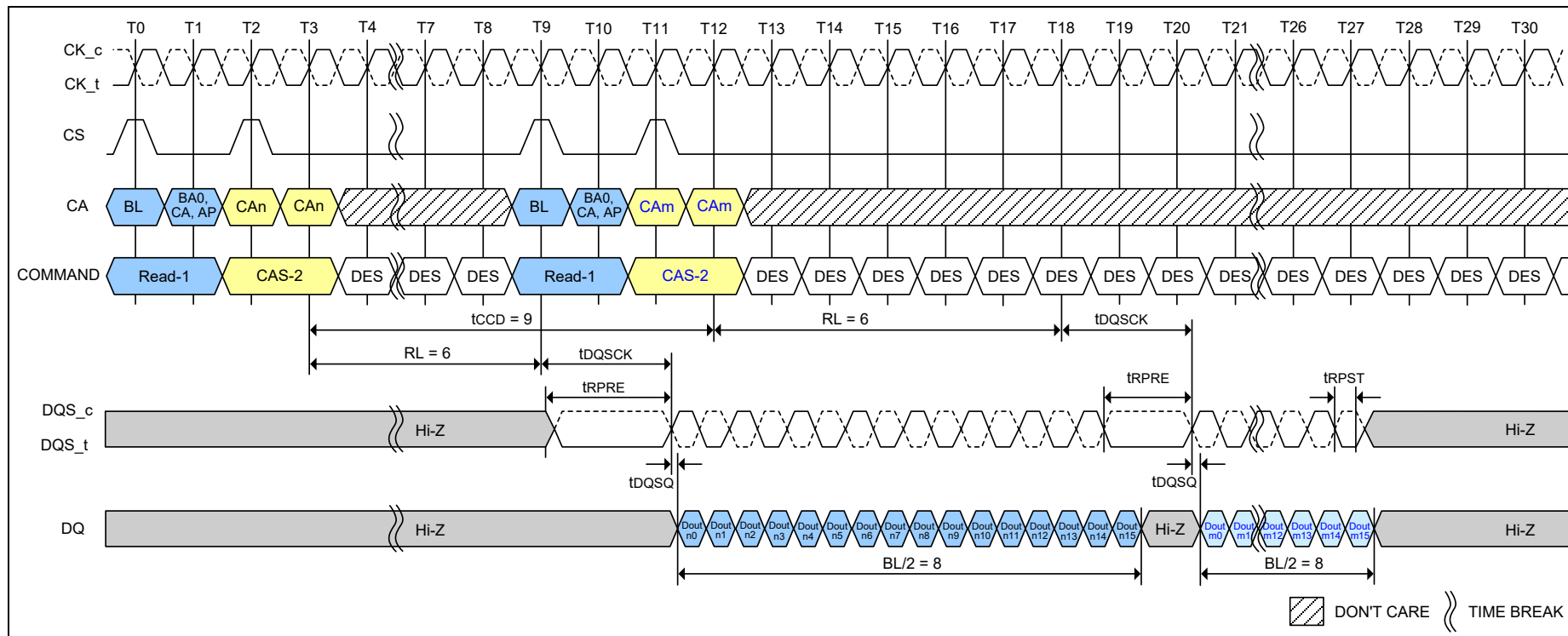
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 0.5nCK.
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 31 - Consecutive Reads Operation: tCCD = Min +1, Preamble = Toggle, 0.5nCK Postamble**

**Notes:**

1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 1.5nCK.
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

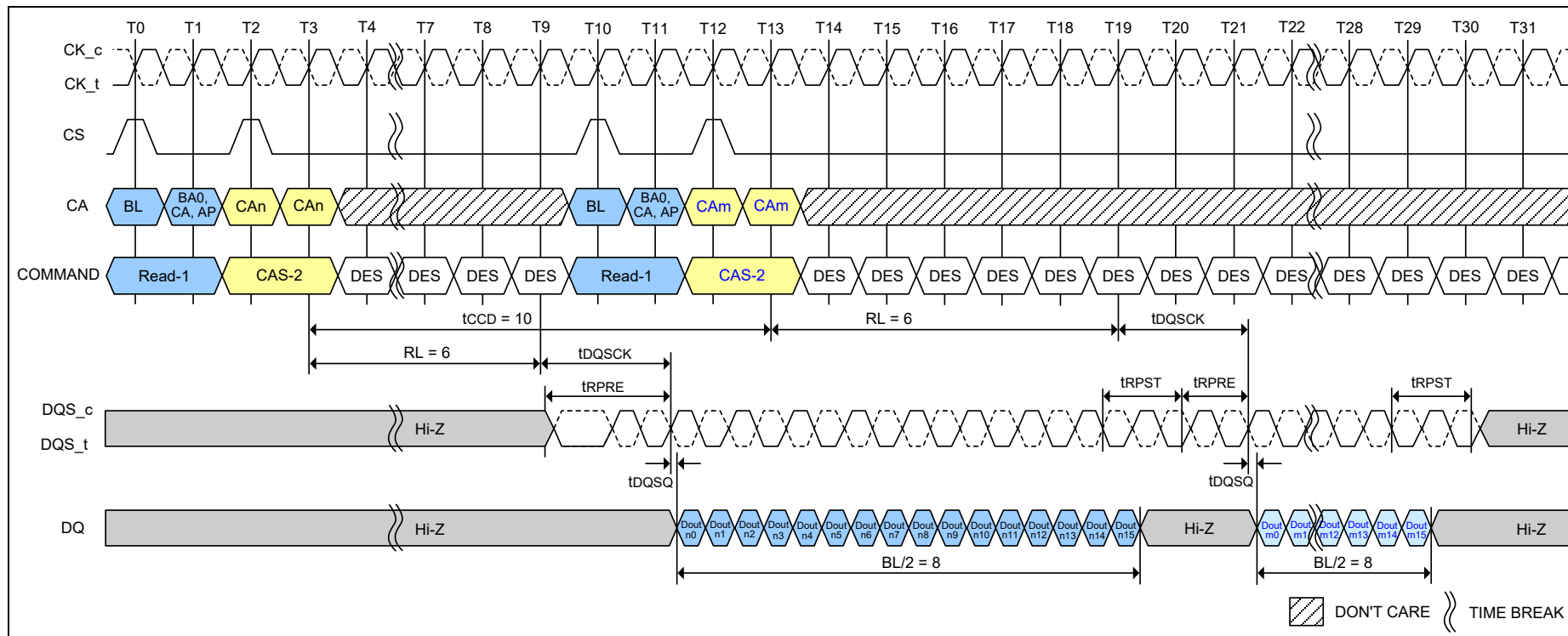
**Figure 32 - Consecutive Reads Operation:  $t_{CCD} = \text{Min} + 1$ , Preamble = Static, 1.5nCK Postamble**

**Notes:**

1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble =  $0.5nCK$ .
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

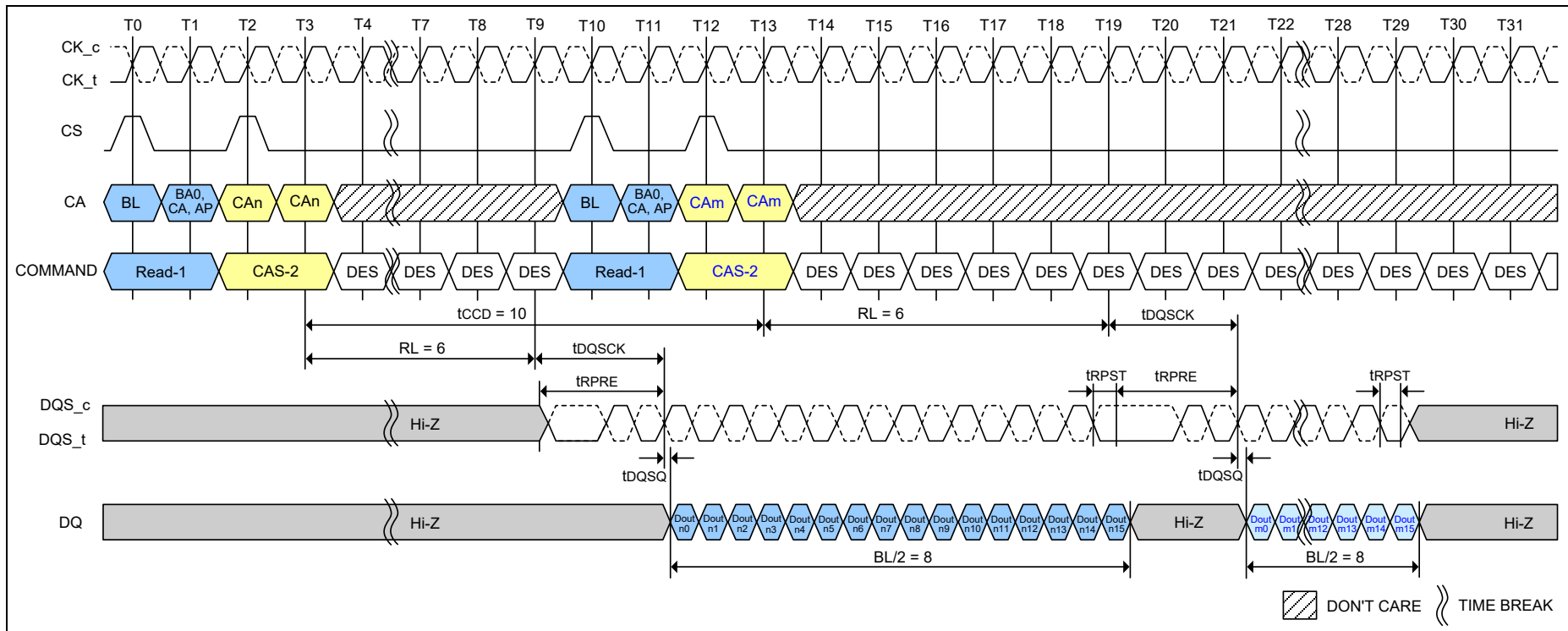
**Figure 33 - Consecutive Reads Operation:  $t_{CCD} = \text{Min} + 1$ , Preamble = Static,  $0.5nCK$  Postamble**



**Notes:**

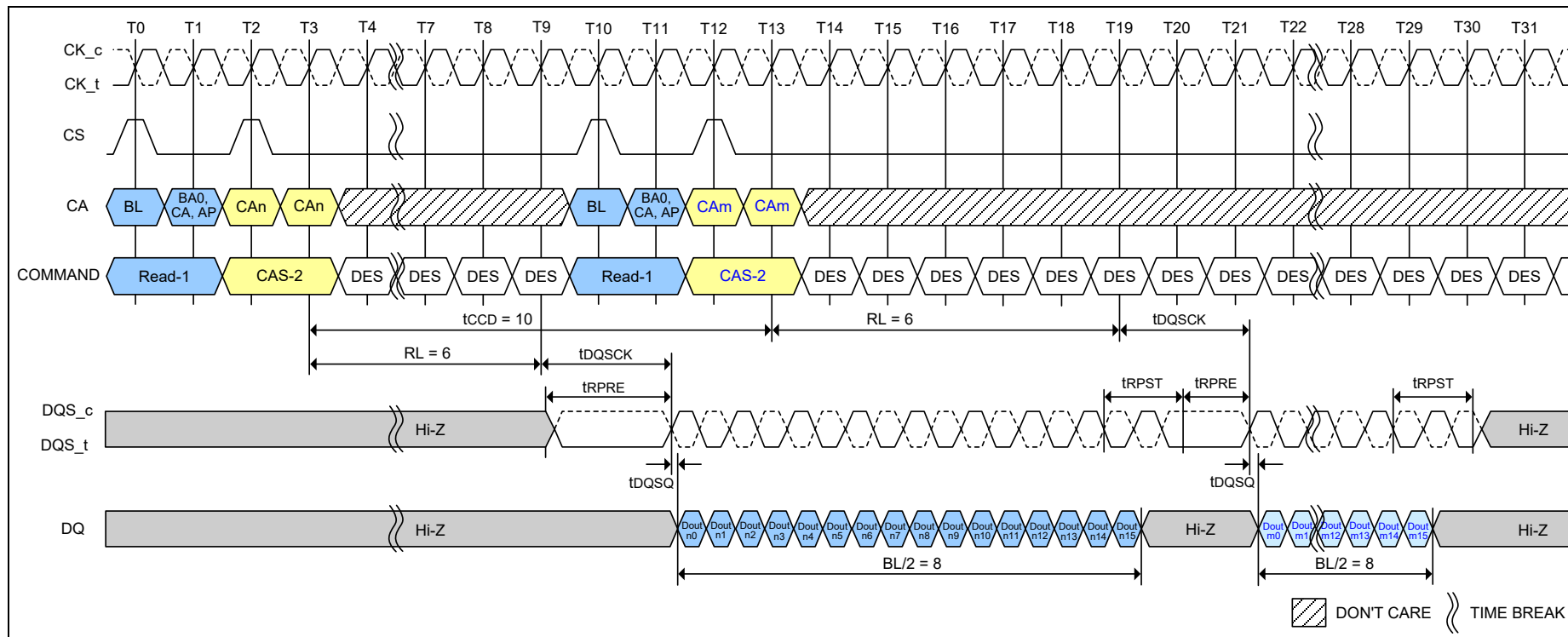
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 1.5nCK.
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 34 - Consecutive Reads Operation:  $t_{CCD} = \text{Min} + 2$ , Preamble = Toggle, 1.5nCK Postamble**

**Notes:**

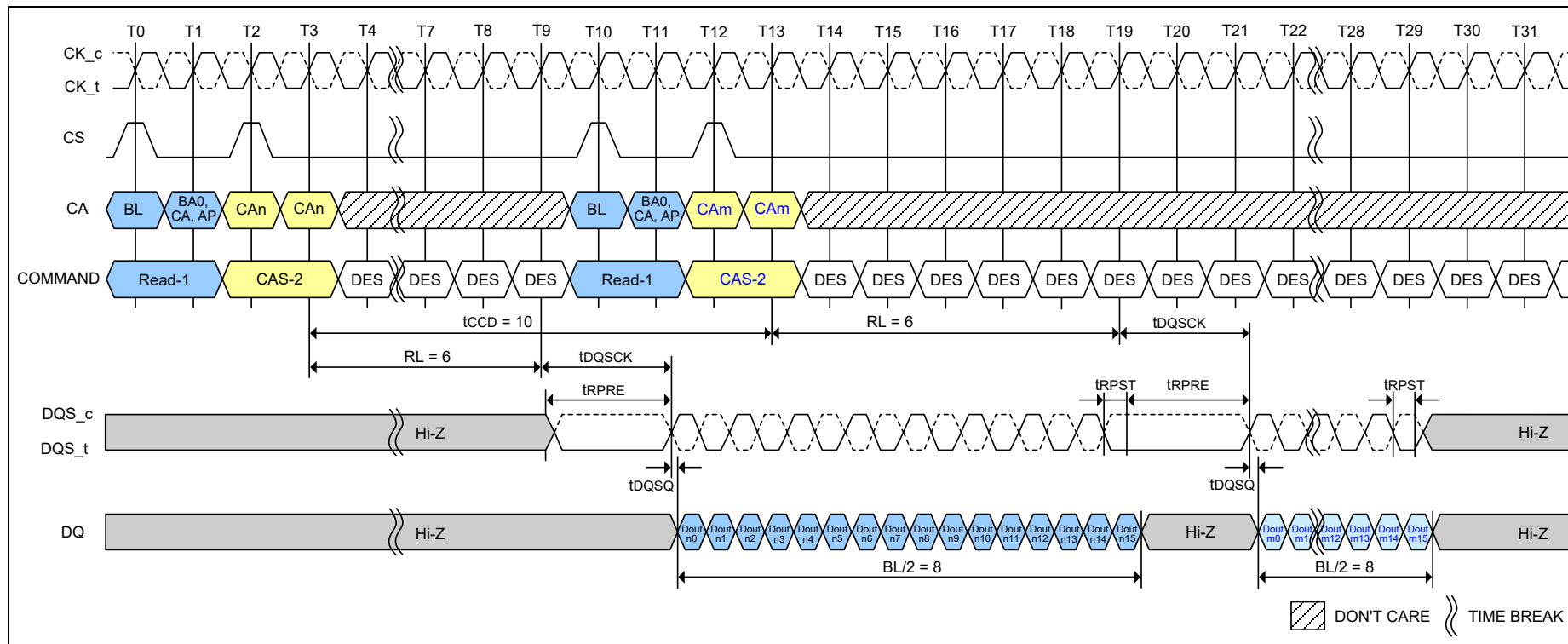
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 0.5nCK.
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 35 - Consecutive Reads Operation: tCCD = Min +2, Preamble = Toggle, 0.5nCK Postamble**

**Notes:**

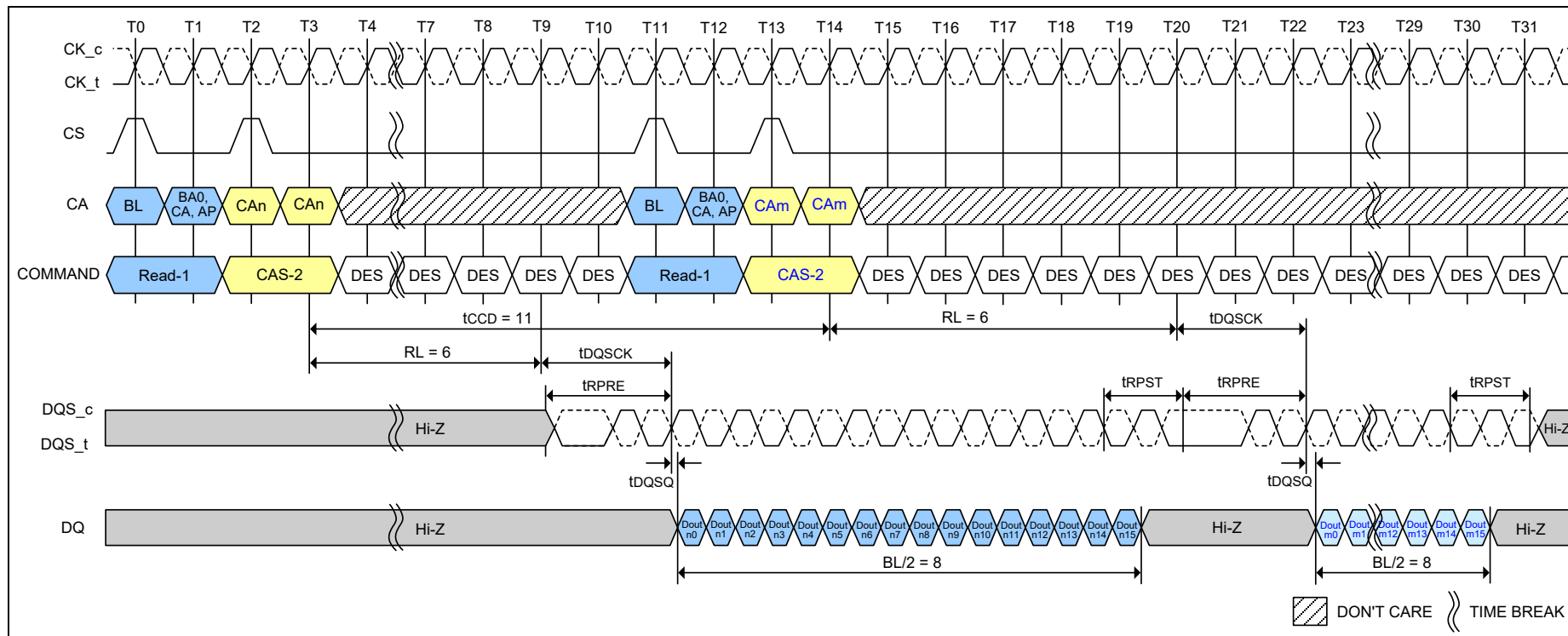
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 1.5nCK.
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 36 - Consecutive Reads Operation:  $t_{CCD} = \text{Min} + 2$ , Preamble = Static, 1.5nCK Postamble**

**Notes:**

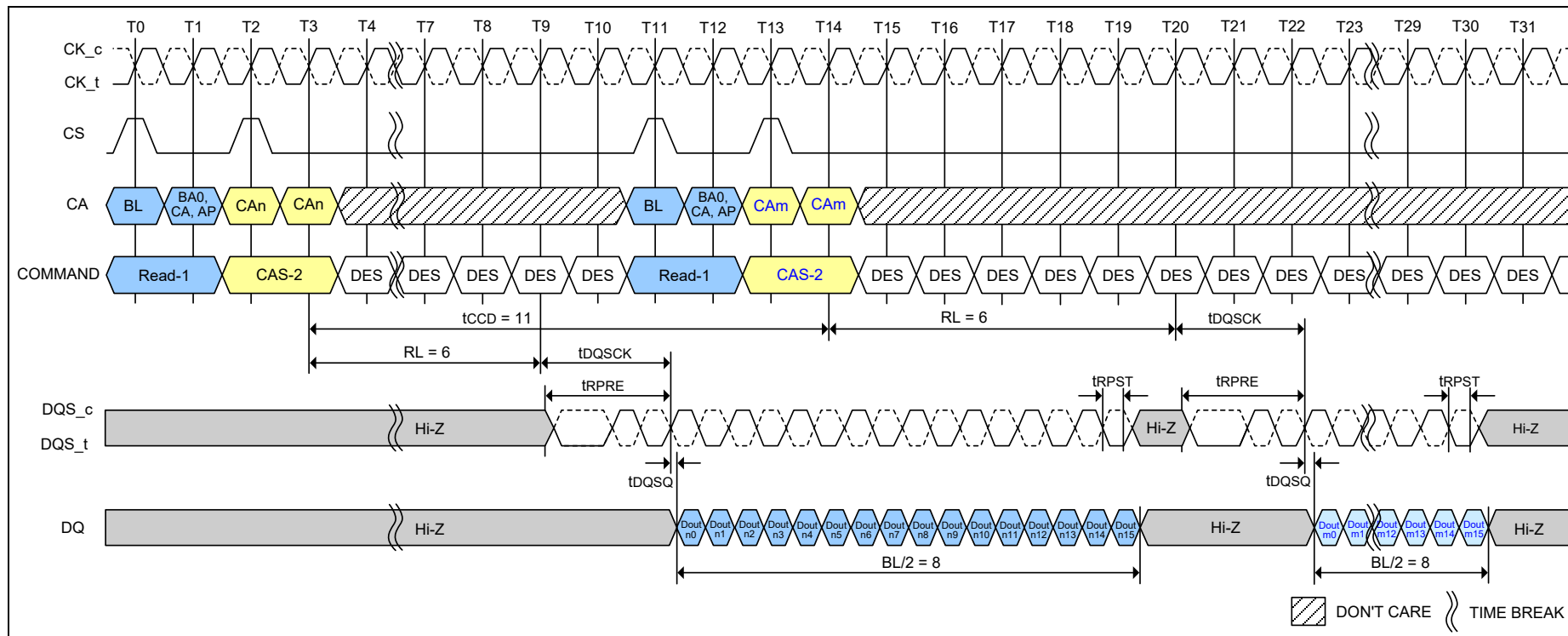
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 0.5nCK.
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 37 - Consecutive Reads Operation:  $t_{CCD} = \text{Min} + 2$ , Preamble = Static, 0.5nCK Postamble**

**Notes:**

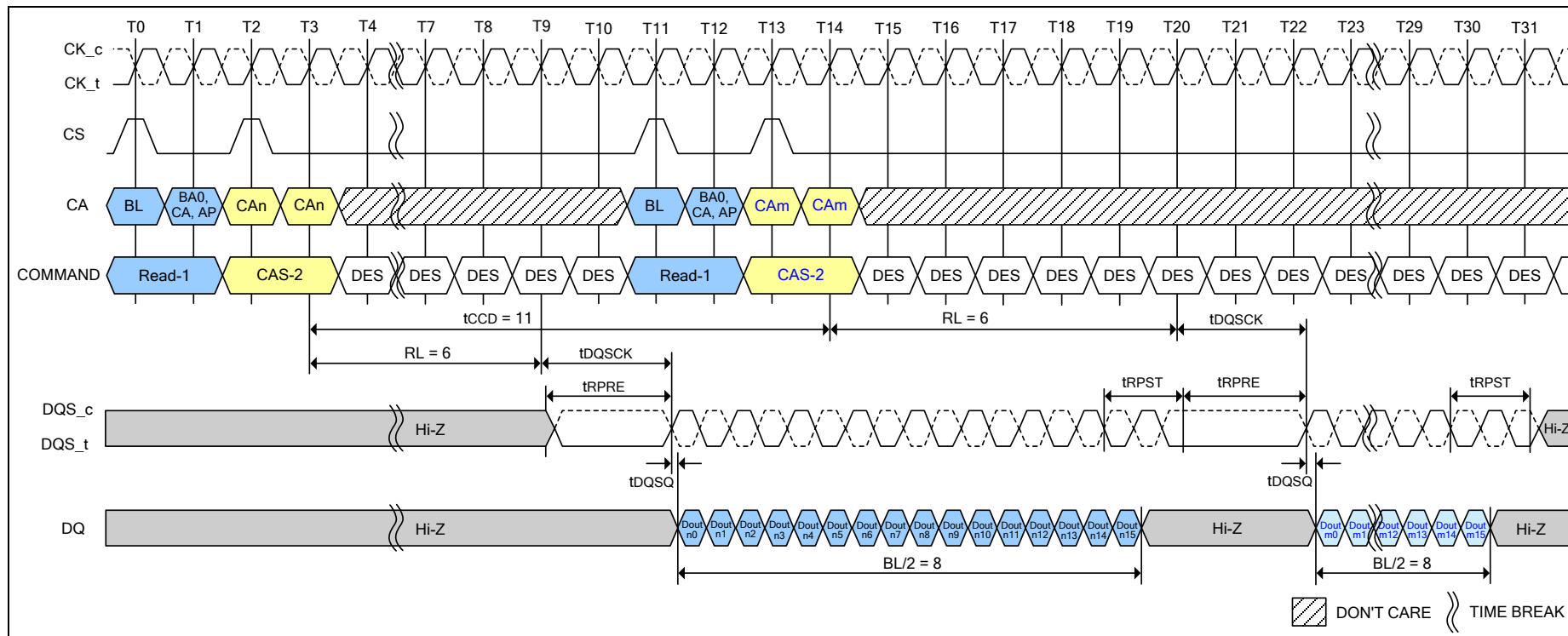
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 1.5nCK.
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 38 - Consecutive Reads Operation:  $t_{CCD} = \text{Min} + 3$ , Preamble = Toggle, 1.5nCK Postamble**

**Notes:**

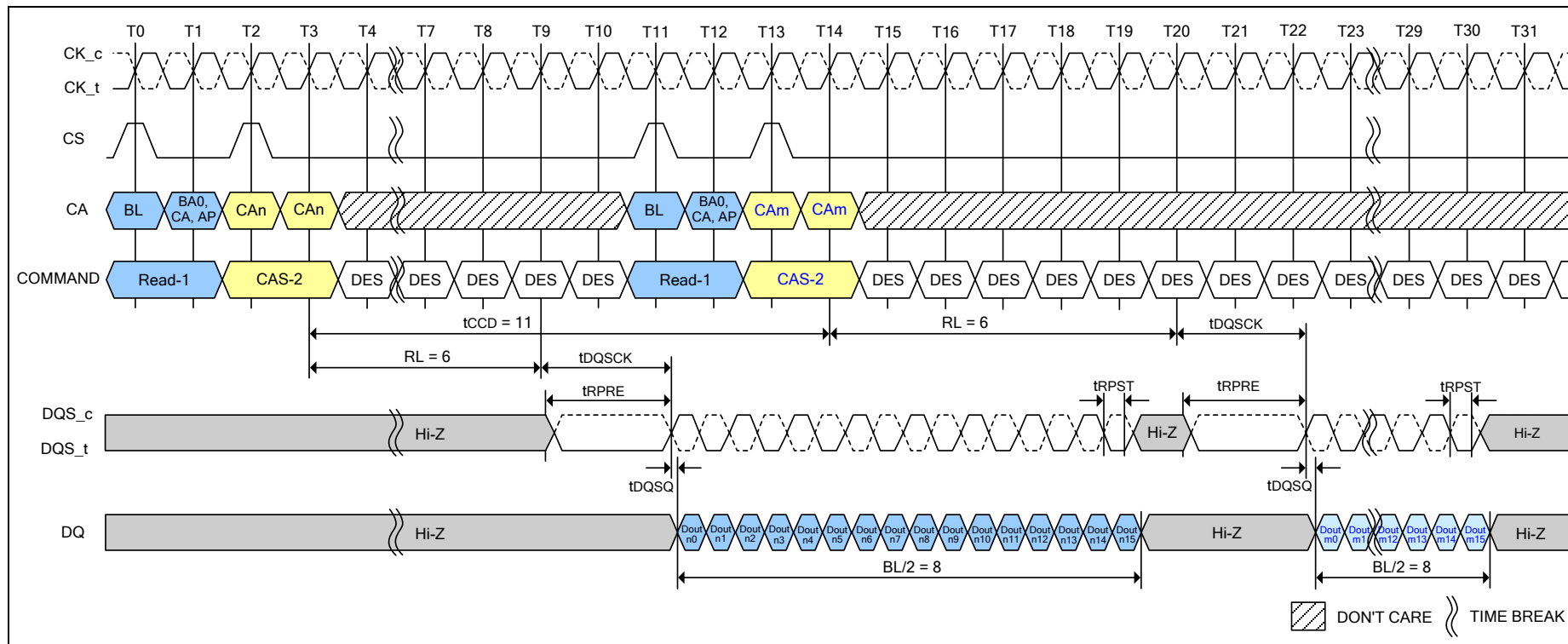
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 0.5nCK.
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 39 - Consecutive Reads Operation:  $t_{CCD} = \text{Min} + 3$ , Preamble = Toggle, 0.5nCK Postamble**

**Notes:**

1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 1.5nCK.
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 40 - Consecutive Reads Operation:  $t_{CCD} = \text{Min} + 3$ , Preamble = Static, 1.5nCK Postamble**

**Notes:**

1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 0.5nCK.
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

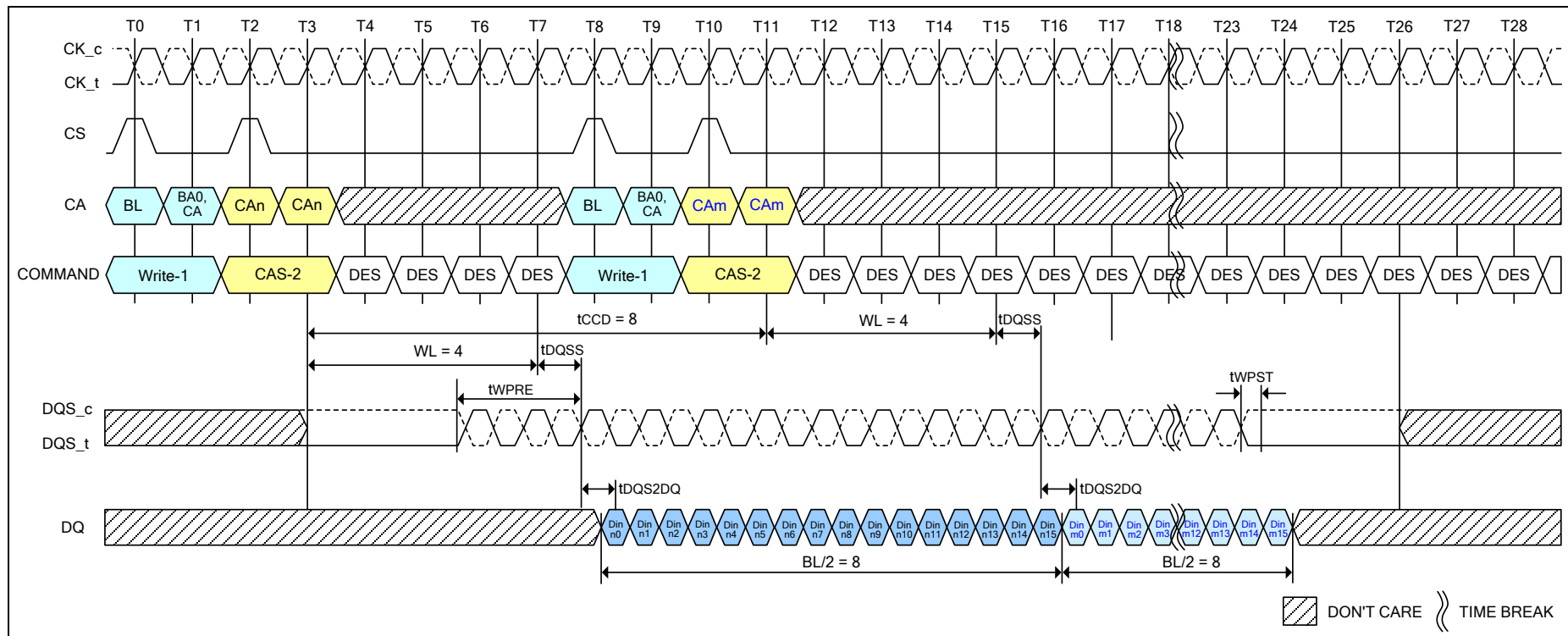
**Figure 41 - Consecutive Reads Operation: tCCD = Min +3, Preamble = Static, 0.5nCK Postamble**





#### 7.4.14.2 Write to Write Operation

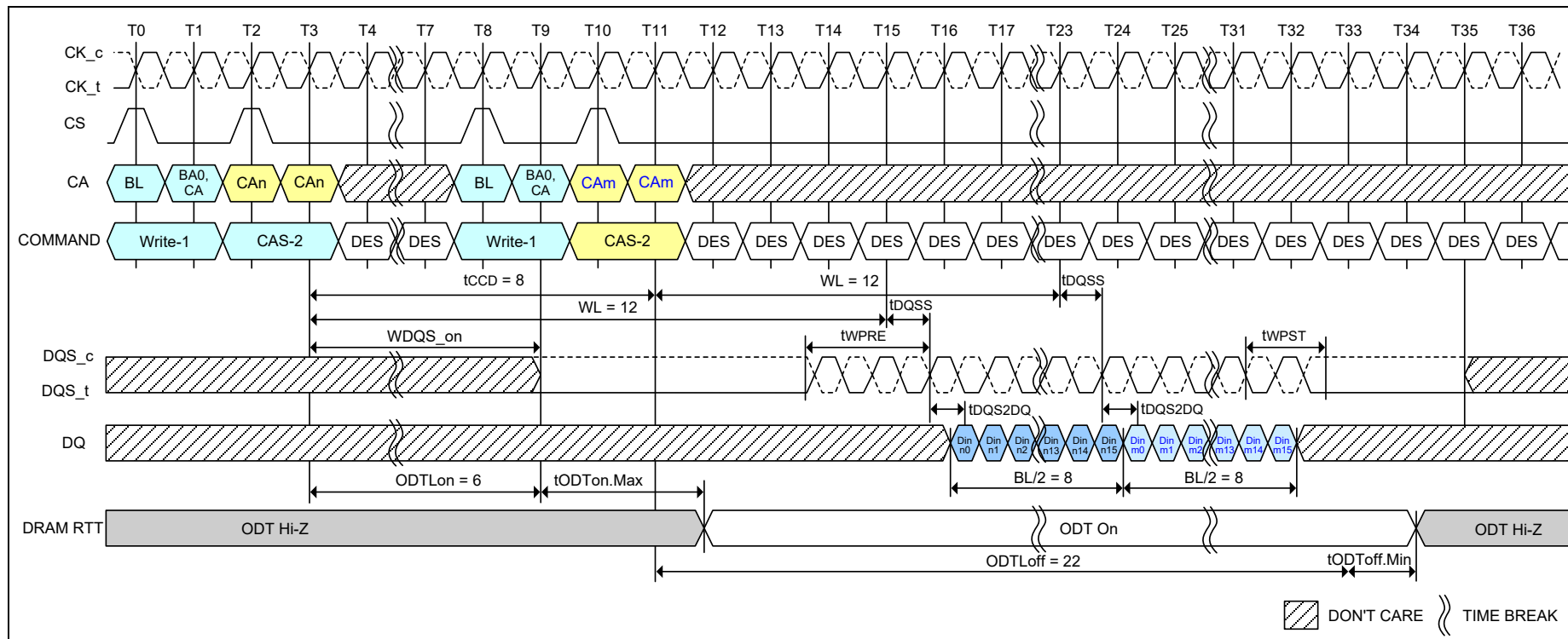
Write to write operation is shown in Figure 42 through Figure 51.



#### Notes:

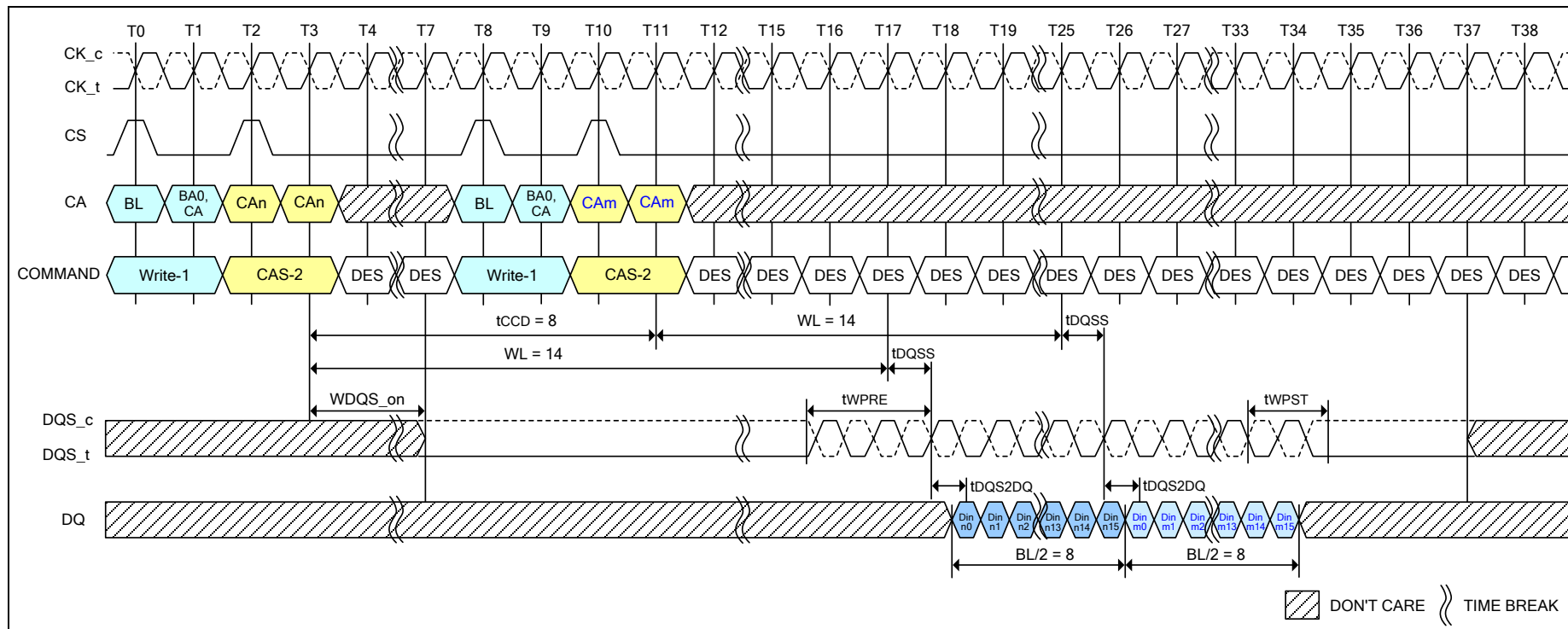
1. BL=16, Write Postamble = 0.5nCK.
2. Din n/m = data-in to column n and column m.
3. The minimum number of clock cycles from the burst write command to the burst write command for any bank is BL/2.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 42 - Seamless Writes Operation: tCCD = Min, 0.5nCK Postamble**

**Notes:**

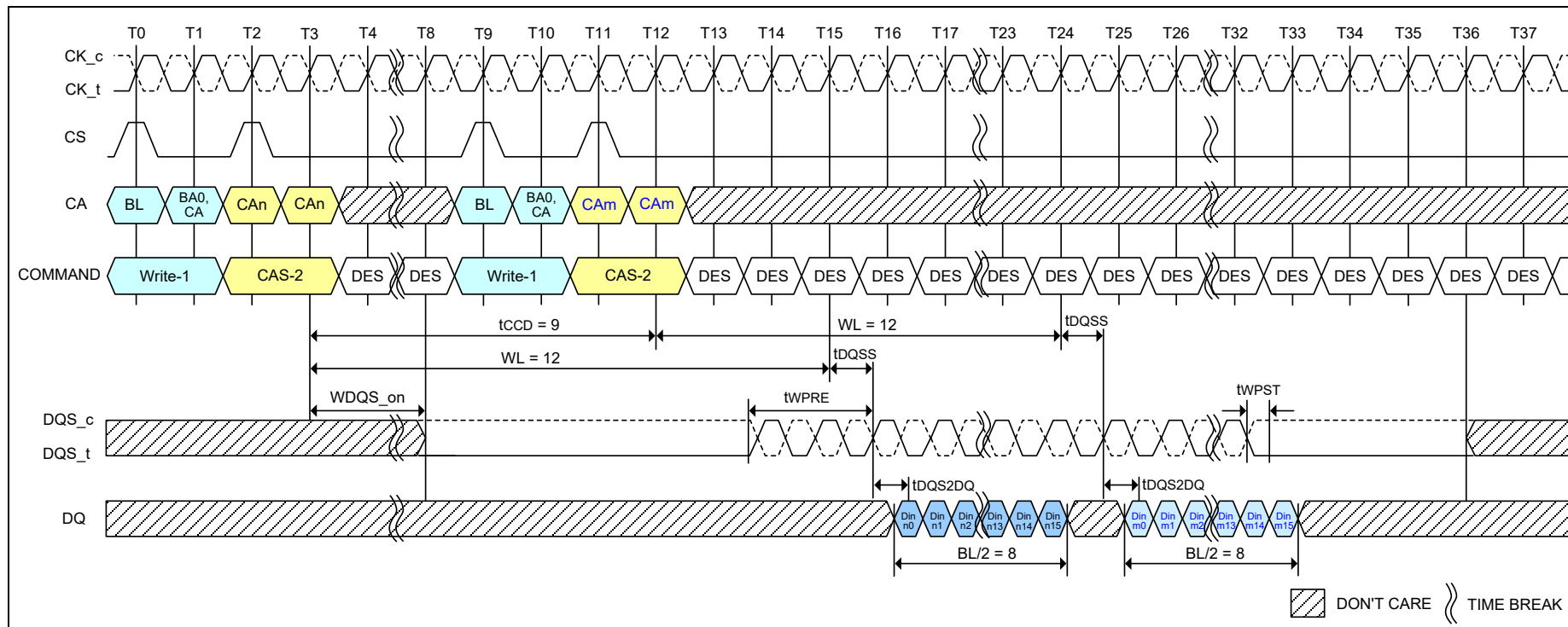
1. Clock Frequency = 800MHz,  $t_{CK(AVG)} = 1.25nS$ .
2. BL=16, Write Postamble = 1.5nCK.
3. Din n/m = data-in to column n and column m.
4. The minimum number of clock cycles from the burst write command to the burst write command for any bank is BL/2.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 43 - Seamless Writes Operation:  $t_{CCD} = \text{Min}$ , 1.5nCK Postamble, 533MHz < Clock Freq.  $\leq$  800MHz, ODT Worst Timing Case**

**Notes:**

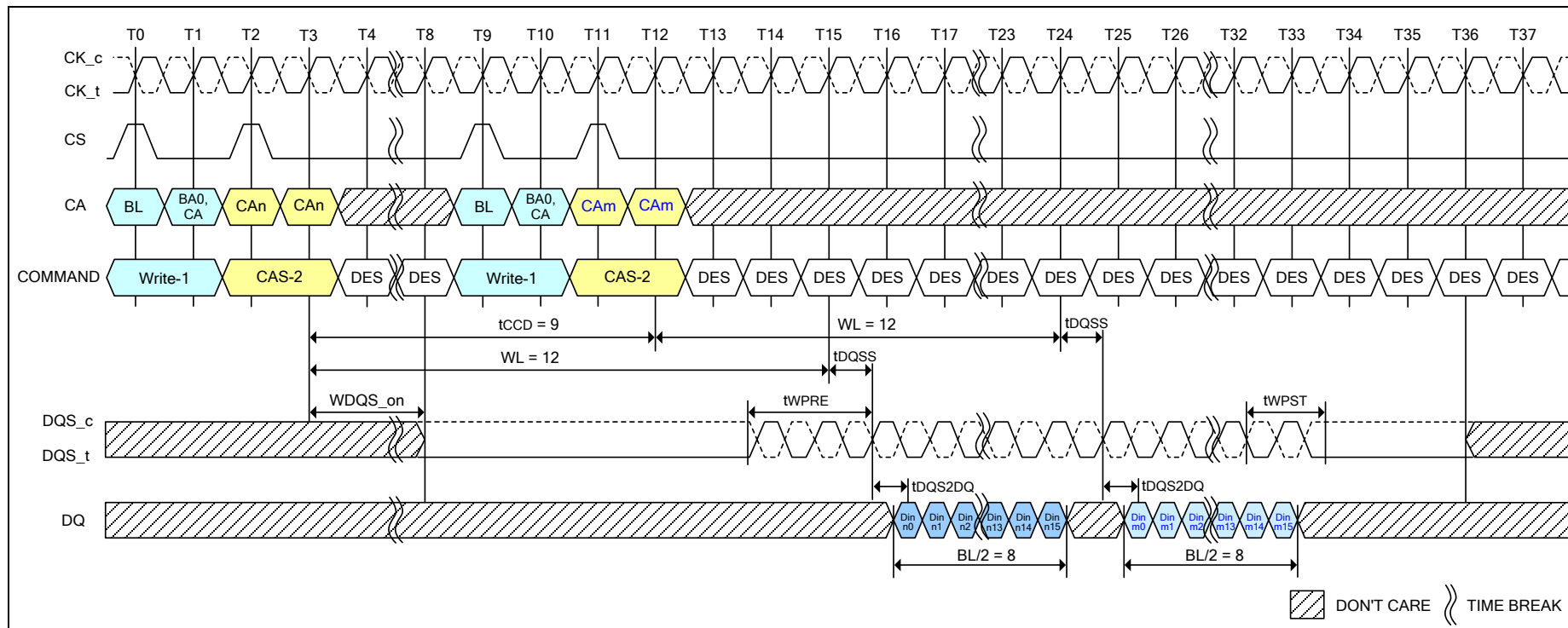
1. BL=16, Write Postamble = 1.5nCK.
2. Din n/m = data-in to column n and column m.
3. The minimum number of clock cycles from the burst write command to the burst write command for any bank is BL/2.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 44 - Seamless Writes Operation: tCCD = Min, 1.5nCK Postamble**

**Notes:**

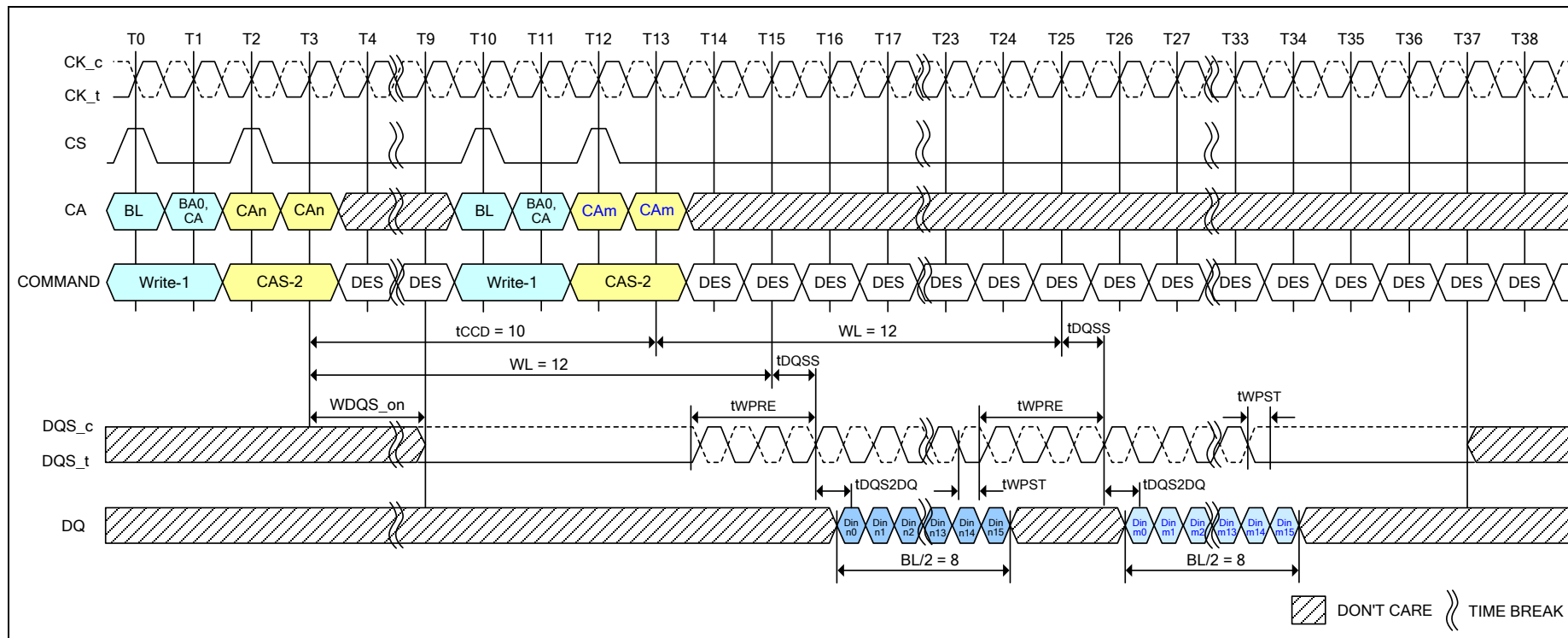
1. BL=16, Write Postamble = 0.5nCK.
2. Din n/m = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 45 - Consecutive Writes Operation:  $t_{CCD} = \text{Min} + 1$ , 0.5nCK Postamble**

**Notes:**

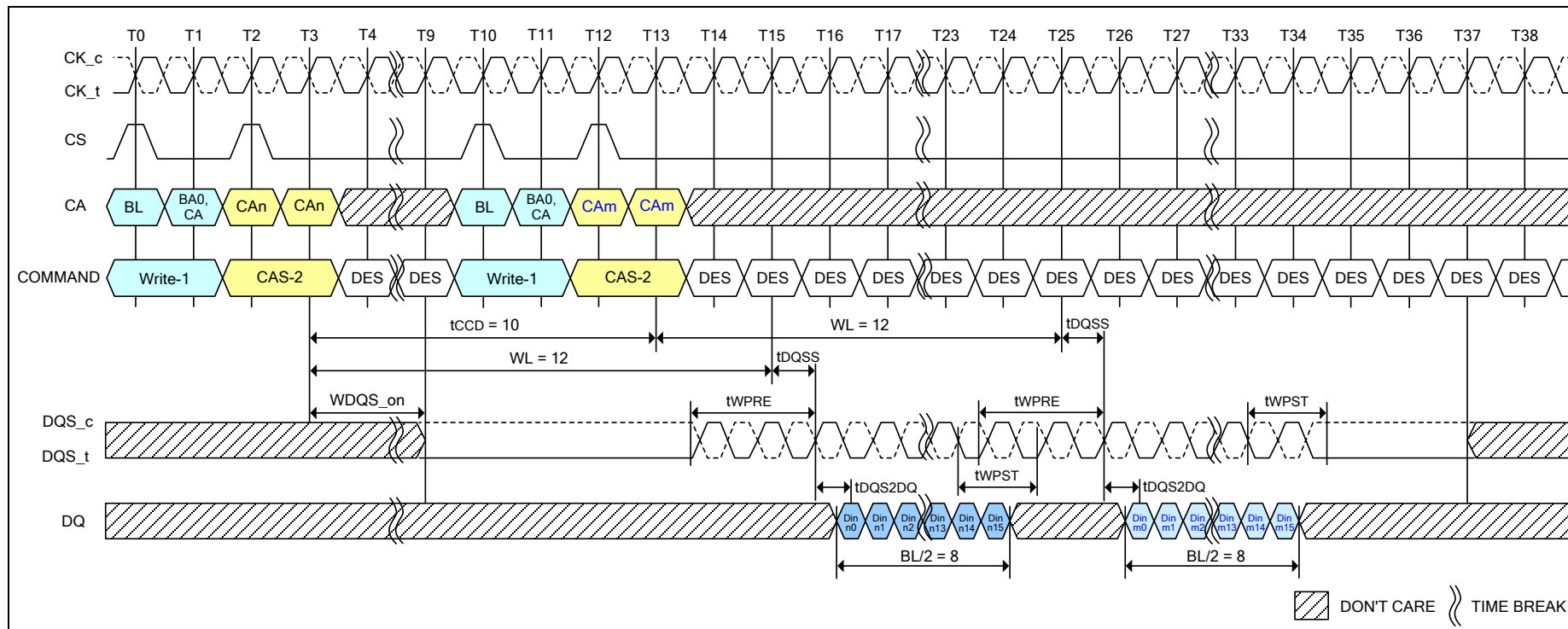
1. BL=16, Write Postamble = 1.5nCK.
2. Din n/m = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 46 - Consecutive Writes Operation:  $t_{CCD} = \text{Min} + 1$ , 1.5nCK Postamble**

**Notes:**

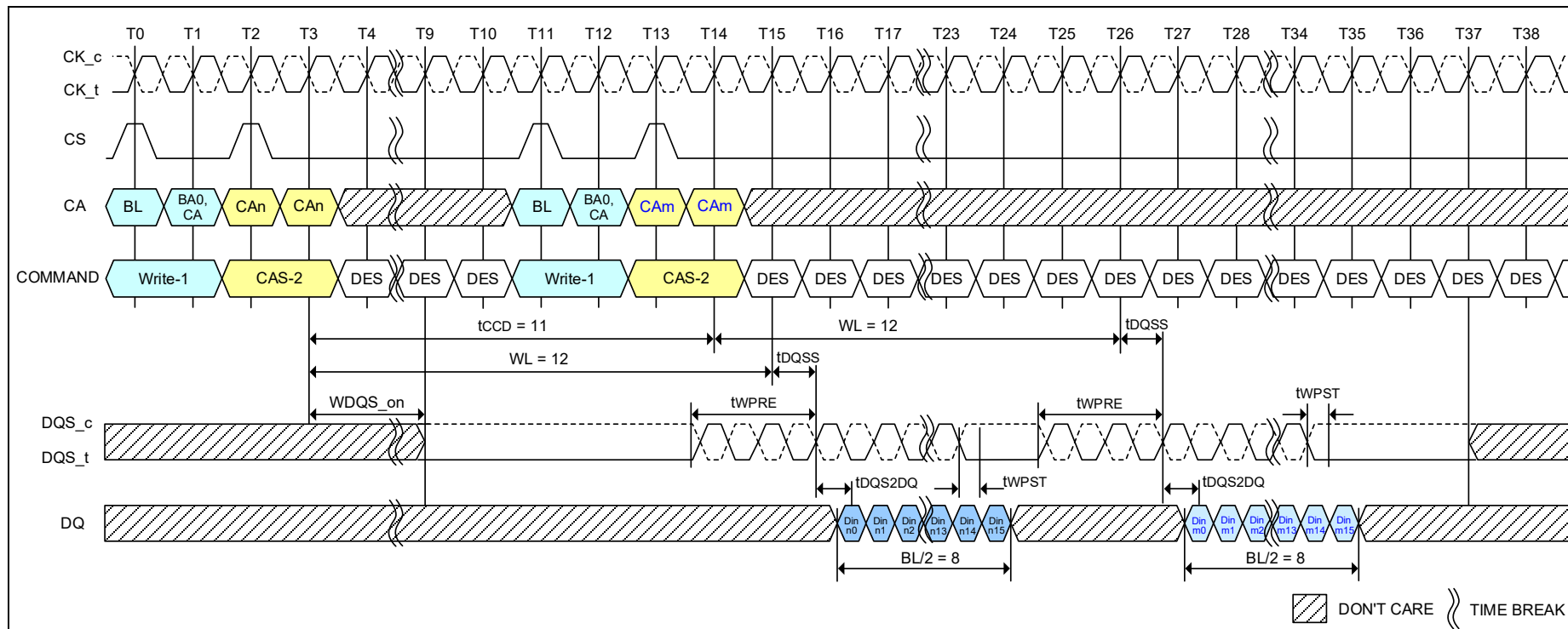
1. BL=16, Write Postamble = 0.5nCK.
2.  $Din_{n/m}$  = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 47 - Consecutive Writes Operation:  $t_{CCD} = Min + 2, 0.5nCK$  Postamble**

**Notes:**

1. BL=16, Write Postamble = 1.5nCK.
2. Din n/m = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

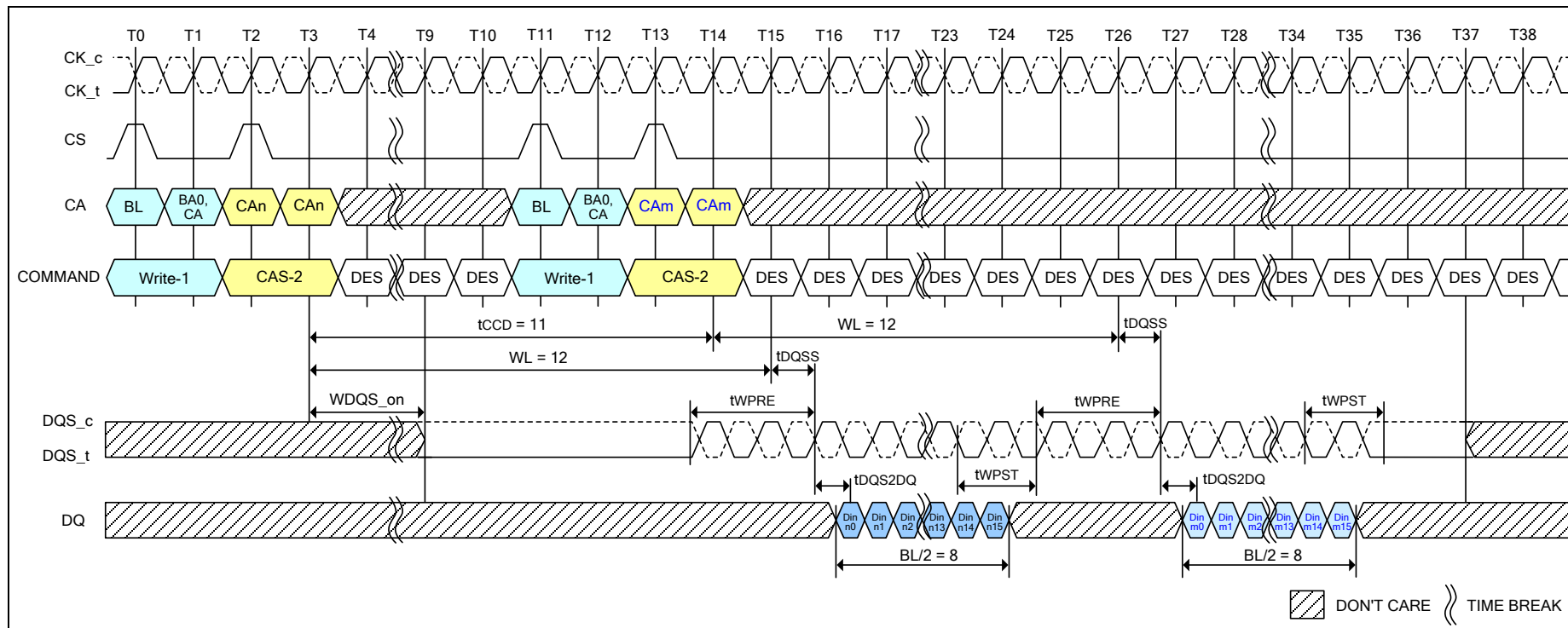
**Figure 48 - Consecutive Writes Operation:  $t_{CCD} = \text{Min} + 2, 1.5n\text{CK}$  Postamble**

**Notes:**

1. BL=16, Write Postamble = 0.5nCK.
2. Din n/m = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

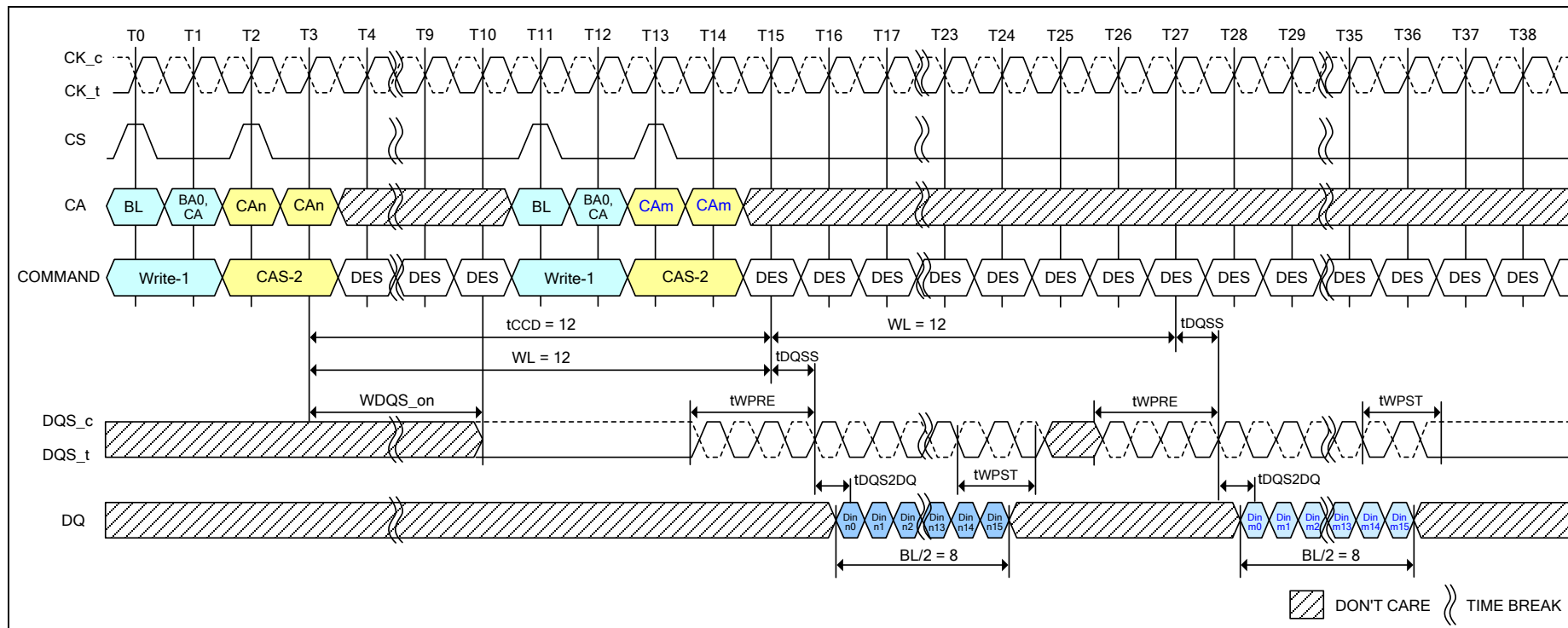
**Figure 49 - Consecutive Writes Operation:  $t_{CCD} = \text{Min} + 3, 0.5n\text{CK}$  Postamble**



**Notes:**

1. BL=16, Write Postamble = 1.5nCK.
2.  $Din_{n/m}$  = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 50 - Consecutive Writes Operation:  $t_{CCD} = Min + 3$ , 1.5nCK Postamble**

**Notes:**

1. BL=16, Write Postamble = 1.5nCK.
2. Din n/m = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

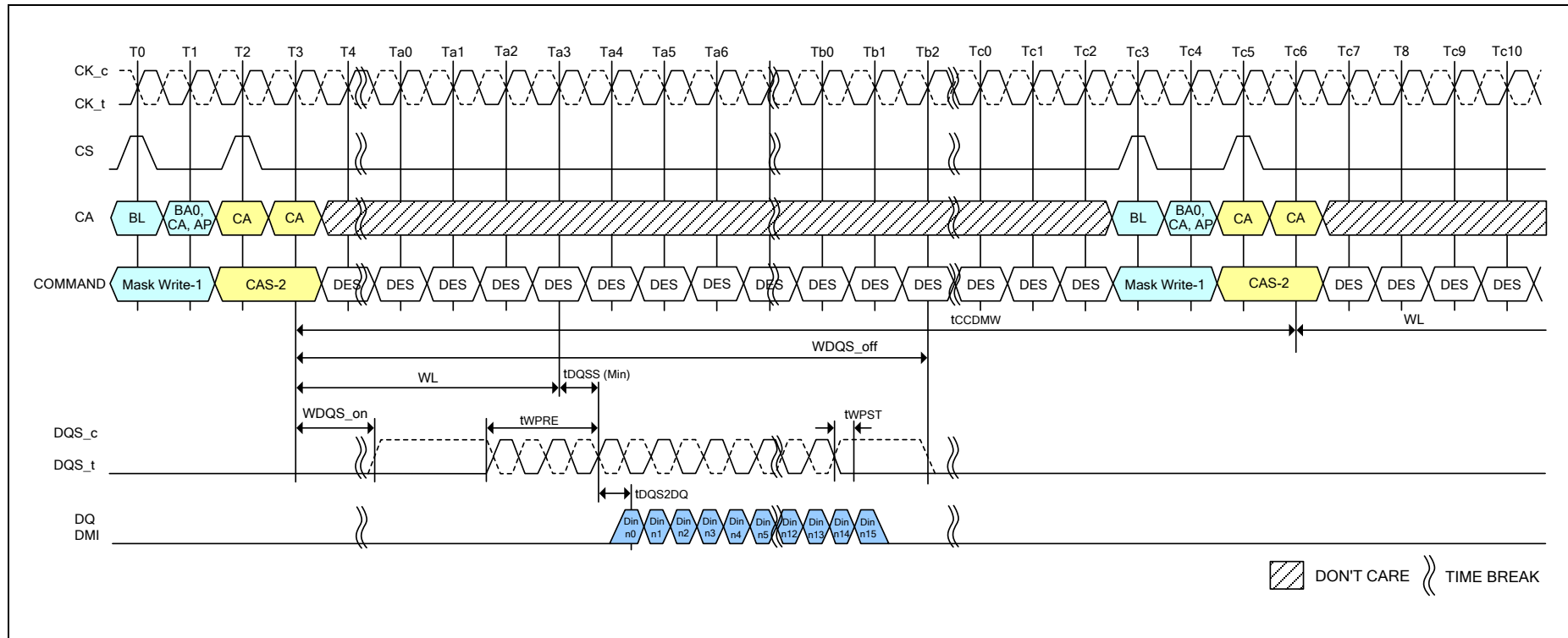
**Figure 51 - Consecutive Writes Operation:  $t_{CCD} = Min + 4$ , 1.5nCK Postamble**



#### 7.4.15 Masked Write Operation

The LPDDR4/LPDDR4X SDRAM requires that Write operations which include a byte mask anywhere in the burst sequence must use the Masked Write command (Figures 52 and 53). This allows the DRAM to implement efficient data protection schemes based on larger data blocks. The Masked Write-1 command is used to begin the operation, followed by a CAS-2 command.

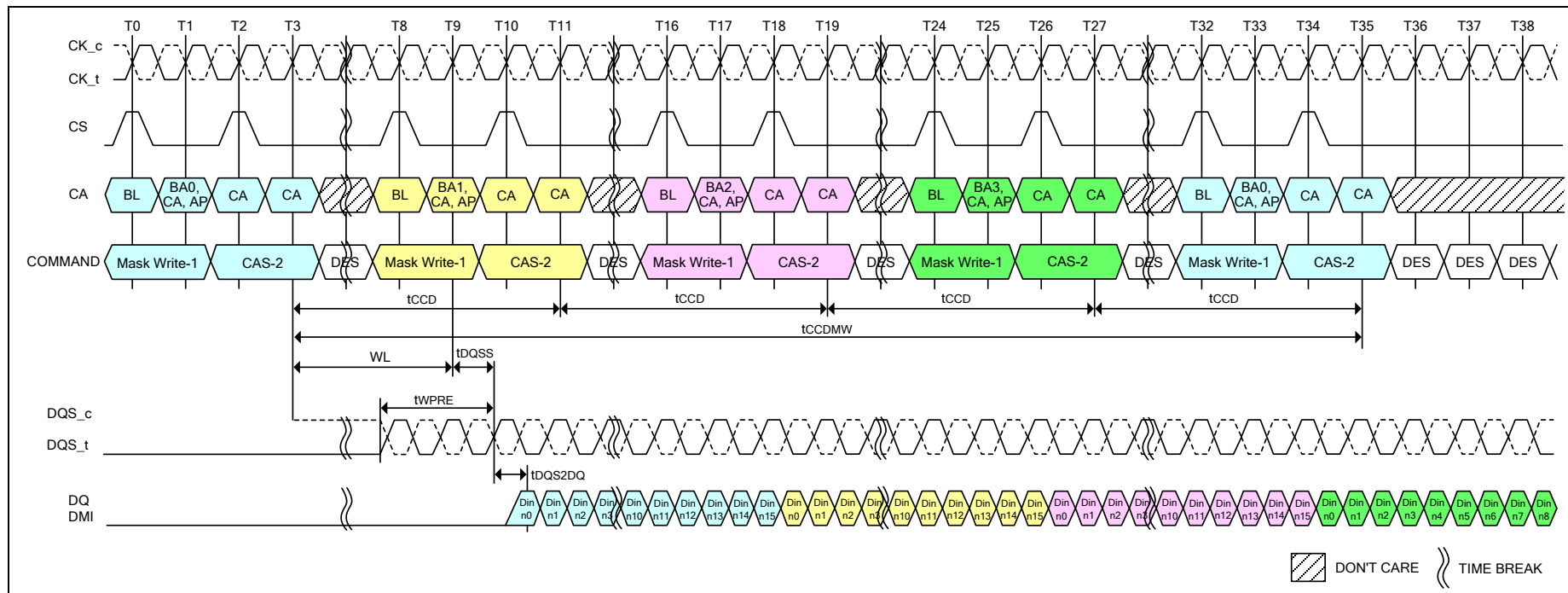
A Masked Write command to the same bank cannot be issued until  $t_{CCDMW}$  later, to allow the LPDDR4/LPDDR4X SDRAM to finish the internal Read-Modify-Write. One Data Mask-Invert (DMI) pin is provided per byte lane, and the Data Mask-Invert timings match data bit (DQ) timing. See the section on “Data Mask Invert” for more information on the use of the DMI signal.



#### Notes:

1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Din n = data-in to column n.
3. Mask-Write supports only BL16 operations. For BL32 configuration, the system needs to insert only 16 bit wide data for masked write operation.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 52 - Masked Write Command - Same Bank**

**Notes:**

1. BL=16, DQ/DQS/DQI: VSSQ termination.
2. Din n = data-in to column n.
3. Mask-Write supports only BL16 operations. For BL32 configuration, the system needs to insert only 16 bit wide data for masked write operation.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 53 - Masked Write Command - Different Bank**



#### 7.4.15.1 Masked Write Timing constraints for BL16

The timing constraints are provided in Table 28 through Table 31.

**Table 28 - Timing constraints for same bank: DQ ODT is Disabled**

| Next CMD<br>Current CMD | Active                        | Read (BL=16 or 32)         | Write (BL=16 or 32)                                 | Masked Write                                        | Precharge                    |
|-------------------------|-------------------------------|----------------------------|-----------------------------------------------------|-----------------------------------------------------|------------------------------|
| Active                  | illegal                       | RU(tRCD/tCK)               | RU(tRCD/tCK)                                        | RU(tRCD/tCK)                                        | RU(tRAS/tCK)                 |
| Read with<br>BL = 16    | illegal                       | 8* <sup>1</sup>            | RL+RU(tDQSCK(max)/tCK) +<br>BL/2-WL+tWPRE+RD(tRPST) | RL+RU(tDQSCK(max)/tCK) +<br>BL/2-WL+tWPRE+RD(tRPST) | BL/2+max{(8,RU(tRTP/tCK))-8} |
| Read with<br>BL = 32    | illegal                       | 16* <sup>2</sup>           | RL+RU(tDQSCK(max)/tCK) +<br>BL/2-WL+tWPRE+RD(tRPST) | RL+RU(tDQSCK(max)/tCK) +<br>BL/2-WL+tWPRE+RD(tRPST) | BL/2+max{(8,RU(tRTP/tCK))-8} |
| Write with<br>BL = 16   | illegal                       | WL+1+BL/2<br>+RU(tWTR/tCK) | 8* <sup>1</sup>                                     | tCCDMW* <sup>3</sup>                                | WL+ 1 + BL/2+RU(tWR/tCK)     |
| Write with<br>BL = 32   | illegal                       | WL+1+BL/2<br>+RU(tWTR/tCK) | 16* <sup>2</sup>                                    | tCCDMW +8* <sup>4</sup>                             | WL+ 1 + BL/2+RU(tWR/tCK)     |
| Masked Write            | illegal                       | WL+1+BL/2<br>+RU(tWTR/tCK) | tCCD                                                | tCCDMW* <sup>3</sup>                                | WL+ 1 + BL/2+RU(tWR/tCK)     |
| Precharge               | RU(tRP/tCK),<br>RU(tRPab/tCK) | illegal                    | illegal                                             | illegal                                             | 4                            |

**Notes:**

1. In the case of BL = 16, tCCD is 8\*tCK.
2. In the case of BL = 32, tCCD is 16\*tCK.
3. tCCDMW = 32\*tCK (4\*tCCD at BL=16)
4. Write with BL=32 operation has 8\*tCK longer than BL =16.
5. tRPST values depend on MR1-OP[7] respectively.

**Table 29 - Timing constraints for same bank: DQ ODT is Enabled**

| Next CMD<br>Current CMD | Active  | Read<br>(BL=16 or 32) | Write (BL=16 or 32)                                                       | Masked Write                                                              | Precharge                    |
|-------------------------|---------|-----------------------|---------------------------------------------------------------------------|---------------------------------------------------------------------------|------------------------------|
| Read with<br>BL = 16    | illegal | 8* <sup>1</sup>       | RL+RU(tDQSCK(max)/<br>tCK)+BL/2+RD(tRPST)-<br>ODTLon-RD(tODTon,min/tCK)+1 | RL+RU(tDQSCK(max)/<br>tCK)+BL/2+RD(tRPST)-<br>ODTLon-RD(tODTon,min/tCK)+1 | BL/2+max{(8,RU(tRTP/tCK))-8} |
| Read with<br>BL = 32    | illegal | 16* <sup>2</sup>      | RL+RU(tDQSCK(max)/<br>tCK)+BL/2+RD(tRPST)-<br>ODTLon-RD(tODTon,min/tCK)+1 | RL+RU(tDQSCK(max)/<br>tCK)+BL/2+RD(tRPST)-<br>ODTLon-RD(tODTon,min/tCK)+1 | BL/2+max{(8,RU(tRTP/tCK))-8} |

**Notes:**

1. In the case of BL = 16, tCCD is 8\*tCK.
2. In the case of BL = 32, tCCD is 16\*tCK.
3. The rest of the timing is same as DQ ODT is Disable case.
4. tRPST values depend on MR1-OP[7] respectively.



Table 30 - Timing constraints for Different bank: DQ ODT is Disabled

| Next CMD<br>Current CMD | Active       | Read (BL=16 or 32)         | Write (BL=16 or 32)                                 | Masked Write                                        | Precharge |
|-------------------------|--------------|----------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------|
| Active                  | RU(tRRD/tCK) | 4                          | 4                                                   | 4                                                   | 2         |
| Read with<br>BL = 16    | 4            | 8* <sup>1</sup>            | RL+RU(tDQSCK(max)/tCK) +<br>BL/2-WL+tWPRE+RD(tRPST) | RL+RU(tDQSCK(max)/tCK) +<br>BL/2-WL+tWPRE+RD(tRPST) | 2         |
| Read with<br>BL = 32    | 4            | 16* <sup>2</sup>           | RL+RU(tDQSCK(max)/tCK) +<br>BL/2-WL+tWPRE+RD(tRPST) | RL+RU(tDQSCK(max)/tCK) +<br>BL/2-WL+tWPRE+RD(tRPST) | 2         |
| Write with<br>BL = 16   | 4            | WL+1+BL/2<br>+RU(tWTR/tCK) | 8* <sup>1</sup>                                     | 8* <sup>1</sup>                                     | 2         |
| Write with<br>BL = 32   | 4            | WL+1+BL/2<br>+RU(tWTR/tCK) | 16* <sup>2</sup>                                    | 16* <sup>2</sup>                                    | 2         |
| Masked Write            | 4            | WL+1+BL/2<br>+RU(tWTR/tCK) | 8* <sup>1</sup>                                     | 8* <sup>1</sup>                                     | 2         |
| Precharge               | 4            | 4                          | 4                                                   | 4                                                   | 4         |

**Notes:**

1. In the case of BL = 16, tCCD is 8\*tCK.
2. In the case of BL = 32, tCCD is 16\*tCK.
3. tRPST values depend on MR1-OP[7] respectively.

Table 31 - Timing constraints for Different bank: DQ ODT is Enabled

| Next CMD<br>Current CMD | Active | Read<br>(BL=16 or 32) | Write (BL=16 or 32)                                                       | Masked Write                                                              | Precharge |
|-------------------------|--------|-----------------------|---------------------------------------------------------------------------|---------------------------------------------------------------------------|-----------|
| Read with<br>BL = 16    | 4      | 8* <sup>1</sup>       | RL+RU(tDQSCK(max)/<br>tCK)+BL/2+RD(tRPST)-<br>ODTLon-RD(tODTon,min/tCK)+1 | RL+RU(tDQSCK(max)/<br>tCK)+BL/2+RD(tRPST)-<br>ODTLon-RD(tODTon,min/tCK)+1 | 2         |
| Read with<br>BL = 32    | 4      | 16* <sup>2</sup>      | RL+RU(tDQSCK(max)/<br>tCK)+BL/2+RD(tRPST)-<br>ODTLon-RD(tODTon,min/tCK)+1 | RL+RU(tDQSCK(max)/<br>tCK)+BL/2+RD(tRPST)-<br>ODTLon-RD(tODTon,min/tCK)+1 | 2         |

**Notes:**

1. In the case of BL = 16, tCCD is 8\*tCK.
2. In the case of BL = 32, tCCD is 16\*tCK.
3. The rest of the timing is same as DQ ODT is Disable case.
4. tRPST values depend on MR1-OP[7] respectively.



#### 7.4.16 Data Mask (DM) and Data Bus Inversion (DBI) Function

LPDDR4/LPDDR4X SDRAM supports the function of Data Mask and Data Bus inversion. Details are shown below.

- LPDDR4/LPDDR4X SDRAM supports Data Mask (DM) function for Write operation.
- LPDDR4/LPDDR4X SDRAM supports Data Bus Inversion (DBI) function for Write and Read operation.
- LPDDR4/LPDDR4X supports DM and DBI function with a byte granularity.
- DBI function during Write or Masked Write can be enabled or disabled through MR3 OP[7].
- DBI function during Read can be enabled or disabled through MR3 OP[6].
- DM function during Masked Write can be enabled or disabled through MR13 OP[5].
- LPDDR4/LPDDR4X SDRAM has one Data Mask Inversion (DMI) signal pin per byte; total of 2 DMI signals per channel.
- DMI signal is a bi-directional DDR signal and is sampled along with the DQ signals for Read and Write or Masked Write operation.

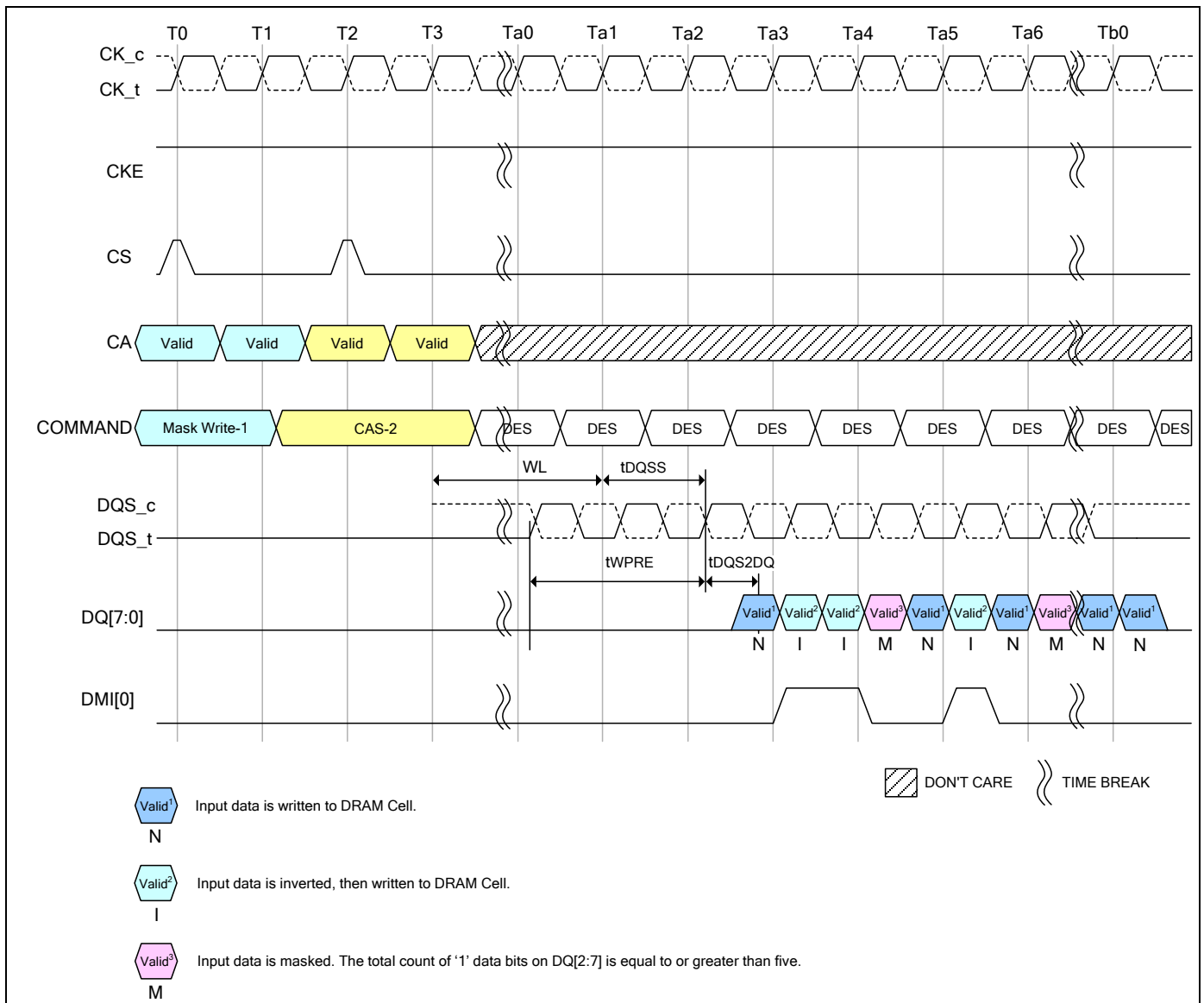
There are eight possible combinations for LPDDR4/LPDDR4X SDRAM with DM and DBI function. The table below describes the functional behavior for all combinations; timing is shown in Figure 54 and Figure 55.

**Table 32 - Function Behavior of DMI Signal during Write, Masked Write and Read Operation**

| DM Function | Write DBI Function | Read DBI Function | DMI Signal during Write Command | DMI Signal during Masked Write Command | DMI Signal During Read | DMI Signal during MPC WR FIFO | DMI Signal during MPC RD FIFO | DMI Signal during MPC DQ Read Training | DMI Signal During MRR |
|-------------|--------------------|-------------------|---------------------------------|----------------------------------------|------------------------|-------------------------------|-------------------------------|----------------------------------------|-----------------------|
| Disable     | Disable            | Disable           | Note 1                          | Note 1, 3                              | Note 2                 | Note 1                        | Note 2                        | Note 2                                 | Note 2                |
| Disable     | Enable             | Disable           | Note 4                          | Note 3                                 | Note 2                 | Note 9                        | Note 10                       | Note 11                                | Note 2                |
| Disable     | Disable            | Enable            | Note 1                          | Note 3                                 | Note 5                 | Note 9                        | Note 10                       | Note 11                                | Note 12               |
| Disable     | Enable             | Enable            | Note 4                          | Note 3                                 | Note 5                 | Note 9                        | Note 10                       | Note 11                                | Note 12               |
| Enable      | Disable            | Disable           | Note 6                          | Note 7                                 | Note 2                 | Note 9                        | Note 10                       | Note 11                                | Note 2                |
| Enable      | Enable             | Disable           | Note 4                          | Note 8                                 | Note 2                 | Note 9                        | Note 10                       | Note 11                                | Note 2                |
| Enable      | Disable            | Enable            | Note 6                          | Note 7                                 | Note 5                 | Note 9                        | Note 10                       | Note 11                                | Note 12               |
| Enable      | Enable             | Enable            | Note 4                          | Note 8                                 | Note 5                 | Note 9                        | Note 10                       | Note 11                                | Note 12               |

#### Notes:

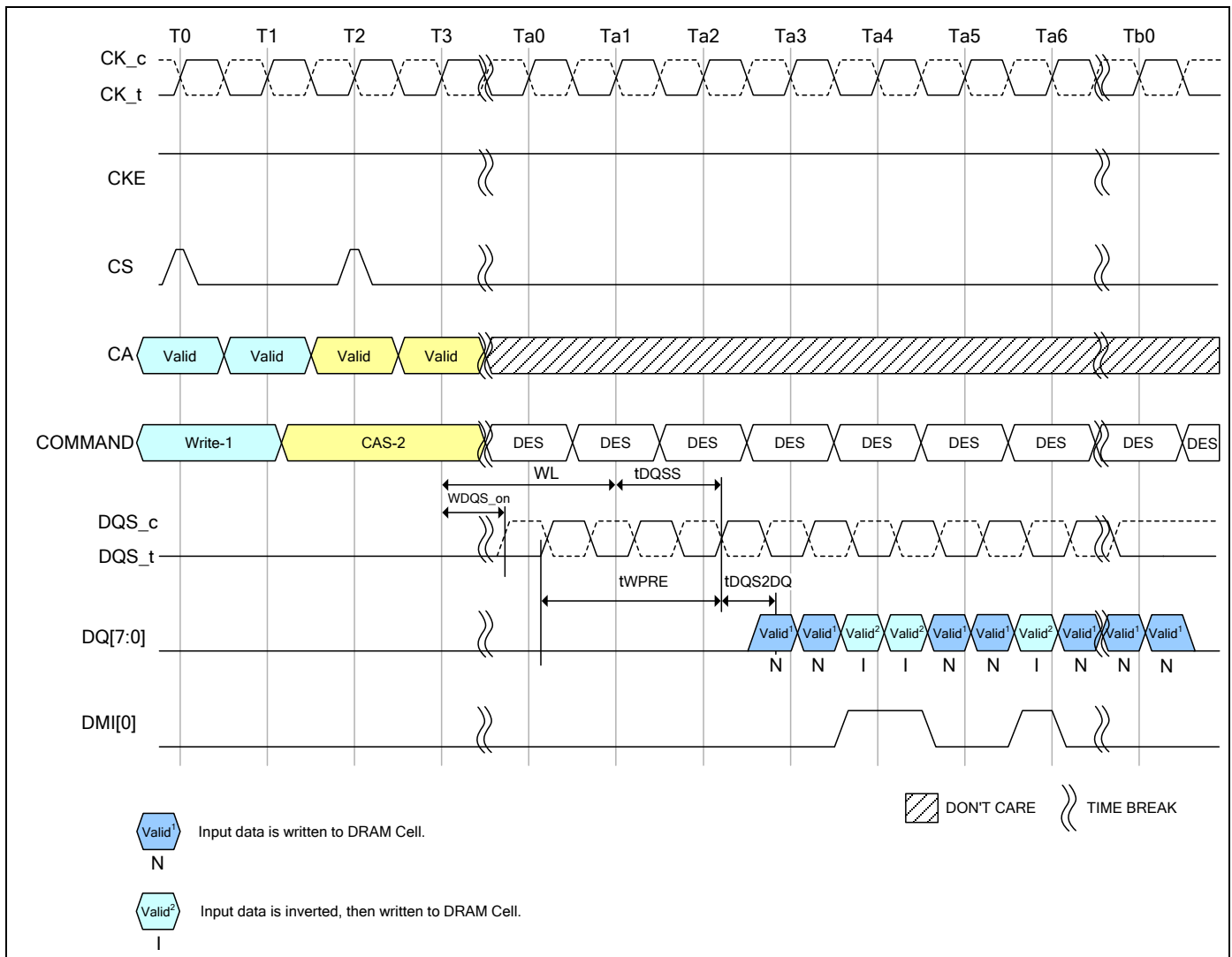
1. DMI input signal is don't care. DMI input receivers are turned OFF.
2. DMI output drivers are turned OFF.
3. Masked Write Command is not allowed and is considered an illegal command as DM function is disabled.
4. DMI signal is treated as DBI signal and it indicates whether DRAM needs to invert the Write data received on DQs within a byte. The LPDDR4/LPDDR4X SDRAM inverts Write data received on the DQ inputs in case DMI was sampled HIGH, or leaves the Write data non-inverted in case DMI was sampled LOW.
5. The LPDDR4/LPDDR4X SDRAM inverts Read data on its DQ outputs associated within a byte and drives DMI signal HIGH when the number of '1' data bits within a given byte lane is greater than four; otherwise the DRAM does not invert the read data and drives DMI signal LOW.
6. The LPDDR4/LPDDR4X SDRAM does not perform any mask operation when it receives Write command. During the Write burst associated with Write command, DMI signal must be driven LOW.
7. The LPDDR4/LPDDR4X SDRAM requires an explicit Masked Write command for all masked write operations. DMI signal is treated as DM signal and it indicates which bit time within the burst is to be masked. When DMI signal is HIGH, DRAM masks that bit time across all DQs associated within a byte. All DQ input signals within a byte are don't care (either HIGH or LOW) when DMI signal is HIGH. When DMI signal is LOW, the LPDDR4/LPDDR4X SDRAM does not perform mask operation and data received on DQ input is written to the array.
8. The LPDDR4/LPDDR4X SDRAM requires an explicit Masked Write command for all masked write operations. The LPDDR4/LPDDR4X SDRAM masks the Write data received on the DQ inputs if the total count of '1' data bits on DQ[2:7] or DQ[10:15] (for Lower Byte or Upper Byte respectively) is equal to or greater than five and DMI signal is LOW. Otherwise the LPDDR4/LPDDR4X SDRAM does not perform mask operation and treats it as a legal DBI pattern; DMI signal is treated as DBI signal and data received on DQ input is written to the array.
9. DMI signal is treated as a training pattern. The LPDDR4/LPDDR4X SDRAM does not perform any mask operation and does not invert Write data received on the DQ inputs.
10. DMI signal is treated as a training pattern. The LPDDR4/LPDDR4X SDRAM returns DMI pattern written in WR FIFO.
11. DMI signal is treated as a training pattern. For more details, see section 7.4.31, RD DQ Calibration.
12. DBI not apply during normal MRR. If read DBI is enable with MRS, DBI pin status should be low.



**Note:** 1. Data Mask (DM) is Enable: MR13 OP[5] = 0, Data Bus Inversion (DBI) Write is Enable: MR3 OP[7] = 1.

**Figure 54 - Masked Write Command w/ Write DBI Enabled; DM Enabled**





**Note:** 1. Data Mask (DM) is Disable: MR13 OP[5] = 1, Data Bus Inversion (DBI) Write is Enable: MR3 OP[7] = 1.

**Figure 55 - Write Command w/ Write DBI Enabled; DM Disabled**



#### 7.4.17 Precharge Operation

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS, and CA[5:0] in the proper state as defined by the Command Truth Table (Table 87). The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bit are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access tRPab after an all bank PRECHARGE command is issued, or tRPpb after a single-bank PRECHARGE command is issued.

To ensure that LPDDR4/LPDDR4X SDRAMs can meet the instantaneous current demands, the row-precharge time for an all bank PRECHARGE (tRPab) is longer than the per bank precharge time (tRPpb). See Table 33.

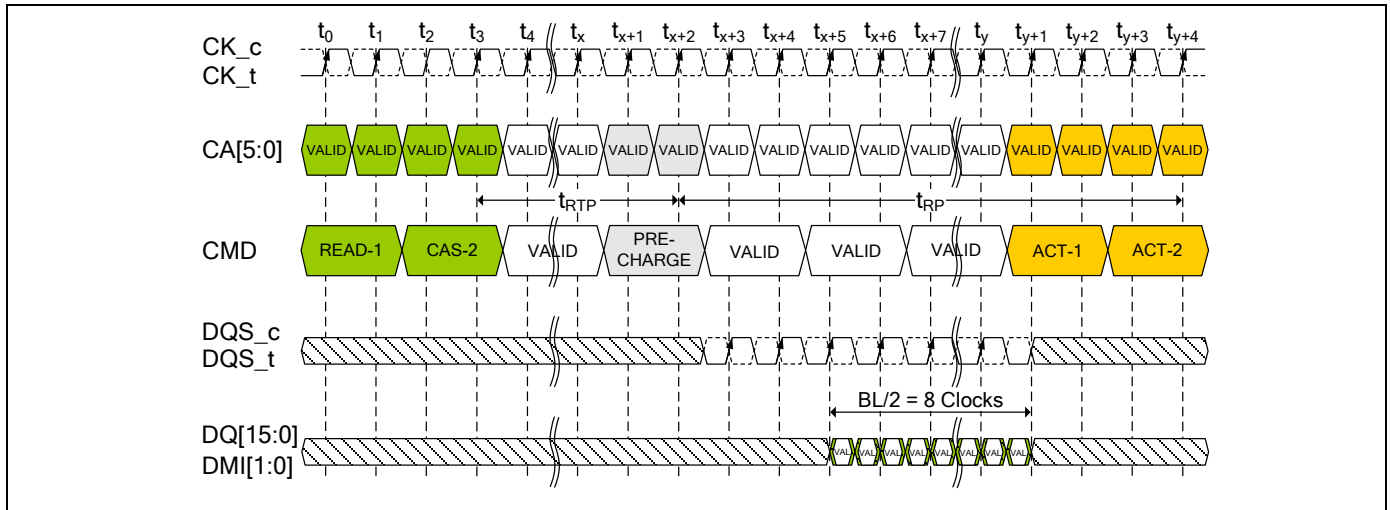
**Table 33 - Precharge Bank Selection**

| <b>AB</b><br><b>(CA[5], R1)</b> | <b>BA2</b><br><b>(CA[2], R2)</b> | <b>BA1</b><br><b>(CA[1], R2)</b> | <b>BA0</b><br><b>(CA[0], R2)</b> | <b>Precharged</b><br><b>Bank(s)</b> |
|---------------------------------|----------------------------------|----------------------------------|----------------------------------|-------------------------------------|
| 0                               | 0                                | 0                                | 0                                | Bank 0 only                         |
| 0                               | 0                                | 0                                | 1                                | Bank 1 only                         |
| 0                               | 0                                | 1                                | 0                                | Bank 2 only                         |
| 0                               | 0                                | 1                                | 1                                | Bank 3 only                         |
| 0                               | 1                                | 0                                | 0                                | Bank 4 only                         |
| 0                               | 1                                | 0                                | 1                                | Bank 5 only                         |
| 0                               | 1                                | 1                                | 0                                | Bank 6 only                         |
| 0                               | 1                                | 1                                | 1                                | Bank 7 only                         |
| 1                               | Valid                            | Valid                            | Valid                            | All Banks                           |

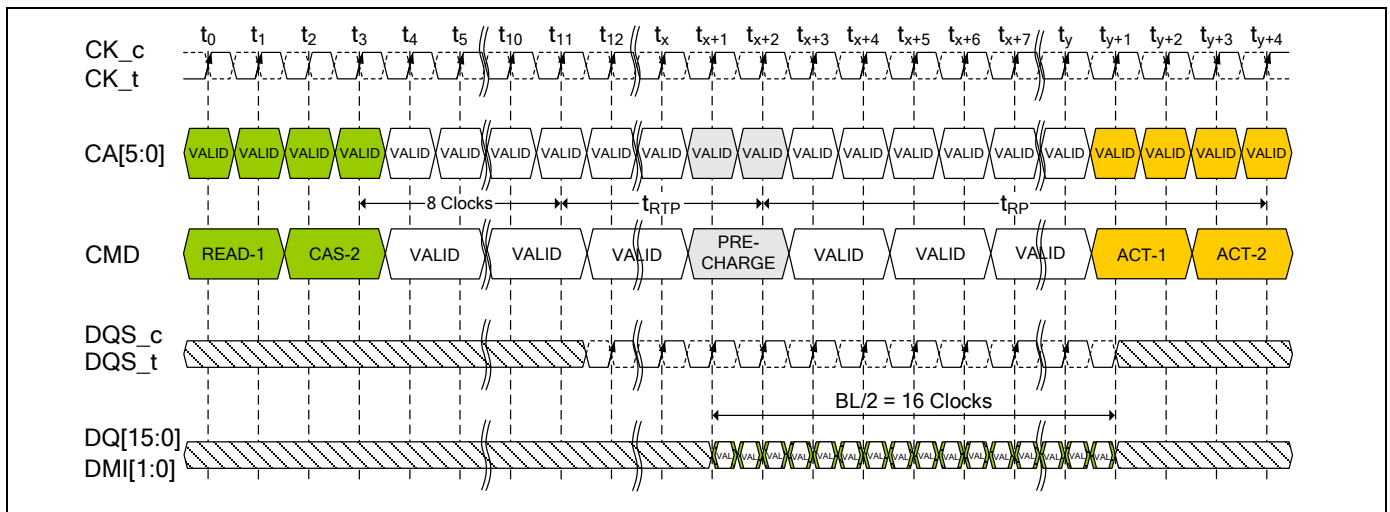


#### 7.4.17.1 Burst Read Operation Followed by Precharge

The PRECHARGE command (Figure 56 and Figure 57) can be issued as early as BL/2 clock cycles after a READ command, but PRECHARGE cannot be issued until after t<sub>RAS</sub> is satisfied. A new bank ACTIVATE command can be issued to the same bank after the row PRECHARGE time (t<sub>RP</sub>) has elapsed. The minimum READ-to-PRECHARGE time must also satisfy a minimum analog time from the 2nd rising clock edge of the CAS-2 command. t<sub>RTP</sub> begins BL/2 - 8 clock cycles after the READ command. For LPDDR4/LPDDR4X READ-to-PRECHARGE timings, see Table 34.



**Figure 56 - Burst READ followed by PRECHARGE**  
(Shown with BL16, 2tCK pre-ample)



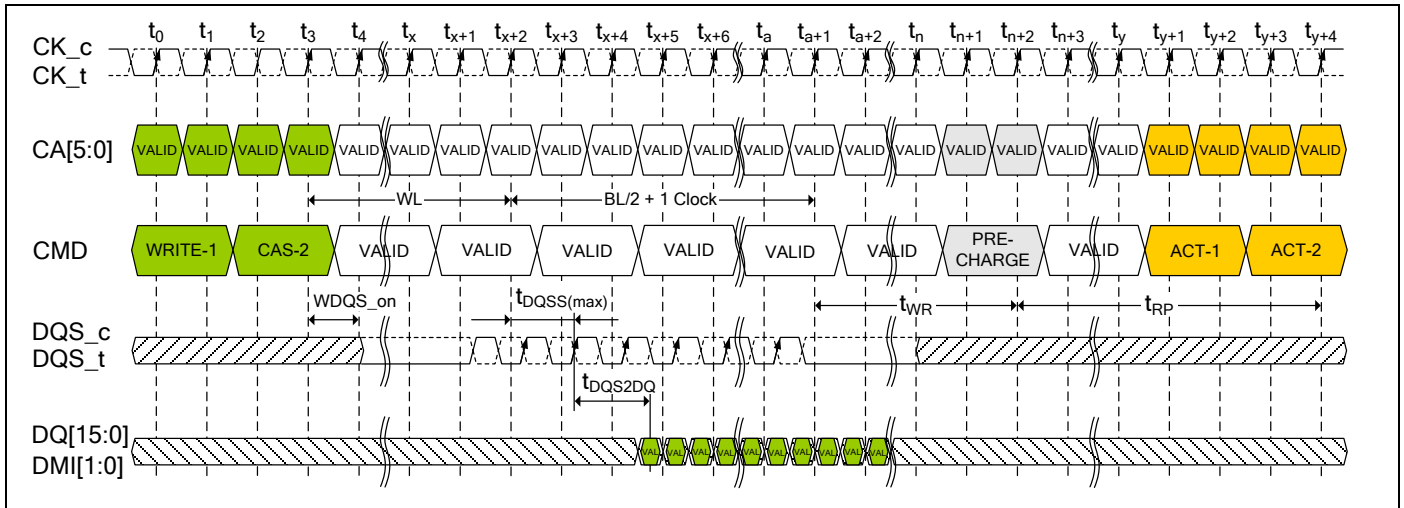
**Figure 57 - Burst READ followed by PRECHARGE**  
(Shown with BL32, 2tCK pre-ample)



#### 7.4.17.2 Burst Write Operation Followed by-Precharge

A Write Recovery time ( $t_{WR}$ ) (Figure 58) must be provided before a PRECHARGE command may be issued. This delay is referenced from the next rising edge of  $CK_t$  after the last latching DQS clock of the burst.

LPDDR4/LPDDR4X SDRAM devices write data to the memory array in prefetch multiples (prefetch=16). An internal WRITE operation can only begin after a prefetch group has been clocked, so  $t_{WR}$  starts at the prefetch boundaries. The minimum WRITE-to-PRECHARGE time for commands to the same bank is  $WL + BL/2 + 1 + RU(t_{WR}/t_{CK})$  clock cycles.



**Figure 58 - Burst WRITE Followed by PRECHARGE**  
(Shown with BL16, 2tCK pre-amble)

#### 7.4.17.3 Auto-Precharge Operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the Auto-Precharge function. When a READ, a WRITE or Masked Write command is issued to the device, the AP bit (CA5) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ, WRITE or Masked Write cycle.

If AP is LOW when the READ or WRITE command is issued, then the normal READ, WRITE or Masked Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ, WRITE or Masked Write command is issued, the Auto-Precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.



#### 7.4.17.4 Burst Read with Auto-Precharge

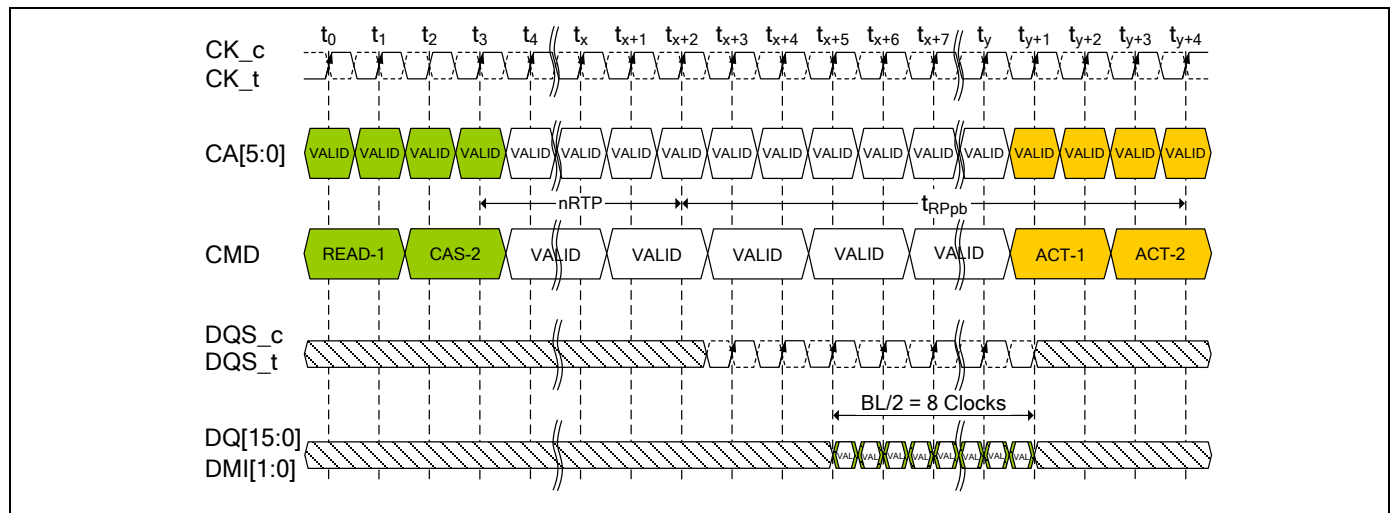
If AP is HIGH when a READ command is issued, the READ with Auto-Precharge function is engaged. An internal precharge procedure starts a following delay time after the READ command. And this delay time depends on BL setting. (See Figure 59 and Figure 60.)

BL = 16: nRTP

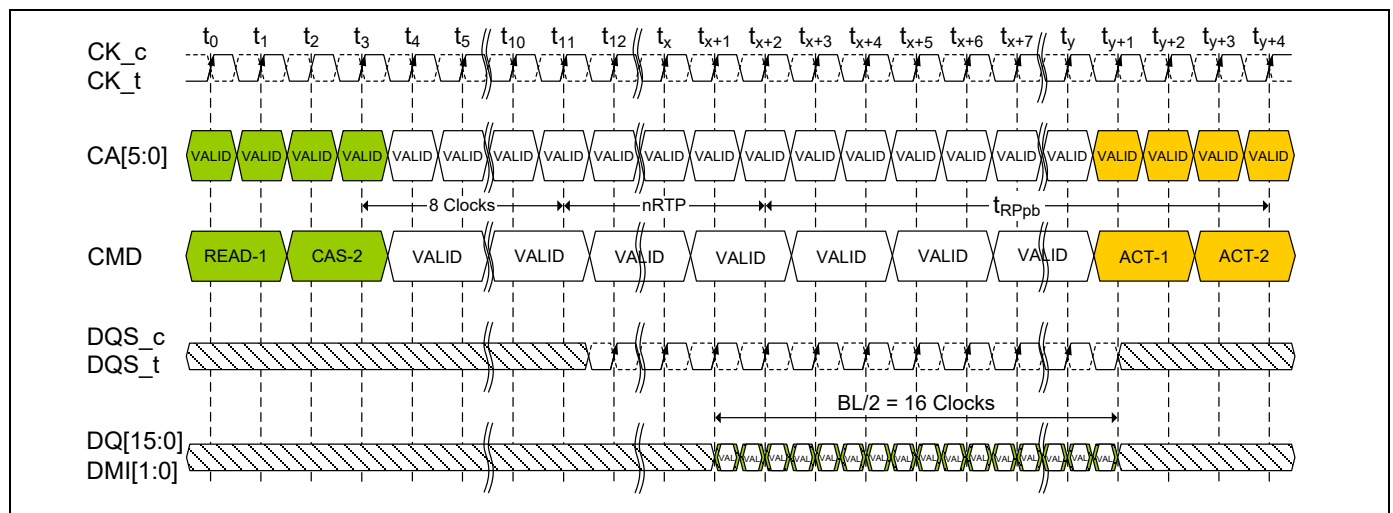
BL = 32: 8nCK + nRTP

For LPDDR4/LPDDR4X SDRAM Auto-Precharge calculations, see Table 34. Following an Auto-Precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are both satisfied:

- The RAS precharge time ( $t_{RP}$ ) has been satisfied from the clock at which the Auto-Precharge began, or
- The RAS cycle time ( $t_{RC}$ ) from the previous bank activation has been satisfied.



**Figure 59 - Burst READ with Auto-Precharge**  
(Shown with BL16, 2tCK pre-ambles)



**Figure 60 - Burst READ with Auto-Precharge**  
(Shown with BL32, 2tCK pre-ambles)





#### 7.4.18 Auto-Precharge Operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the Auto-Precharge function. When a READ, a WRITE or Masked Write command is issued to the device, the AP bit (CA5) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ, WRITE or Masked Write cycle.

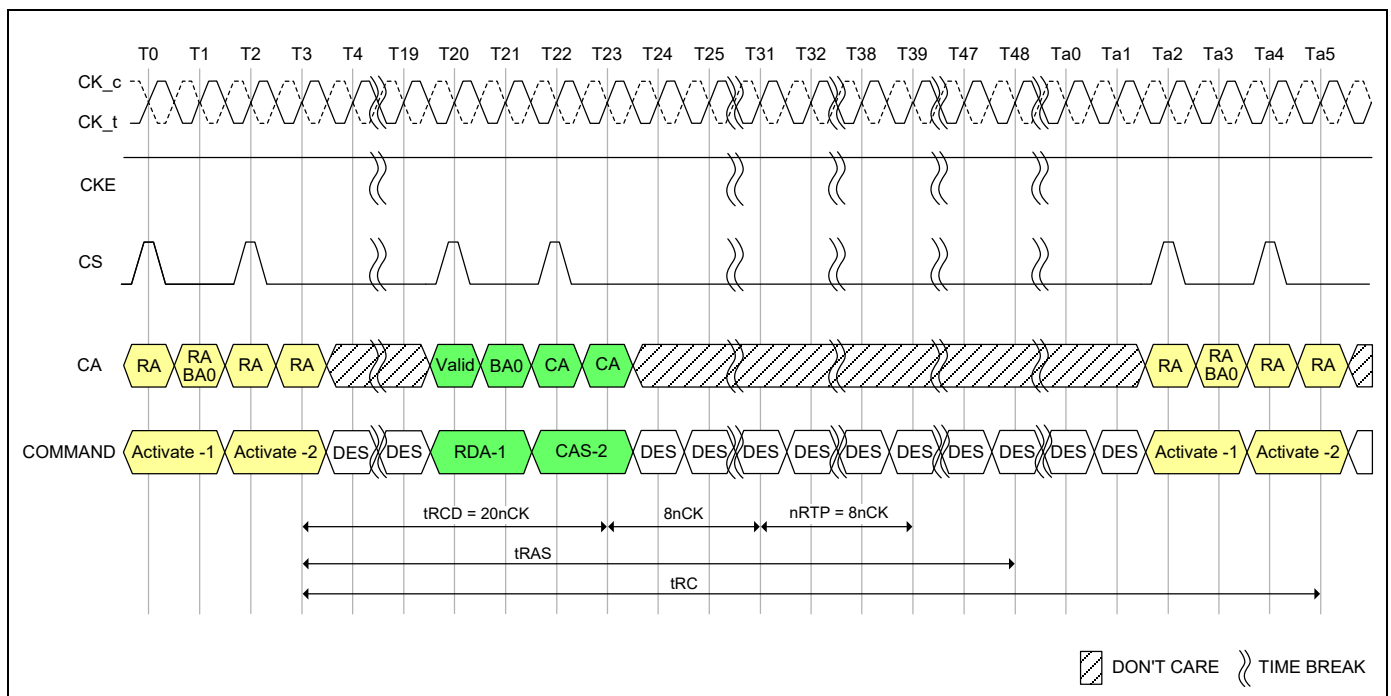
If AP is LOW when the READ or WRITE command is issued, then the normal READ, WRITE or Masked Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ, WRITE or Masked Write command is issued, the Auto-Precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

Read with Auto-Precharge or Write/Mask Write with Auto-Precharge commands may be issued after  $t_{RCD}$  has been satisfied. The LPDDR4/LPDDR4X SDRAM RAS Lockout feature will schedule the internal precharge to assure that  $t_{RAS}$  is satisfied.

$t_{RC}$  needs to be satisfied prior to issuing subsequent Activate commands to the same bank.

The figure below shows example of RAS lock function.



#### Notes:

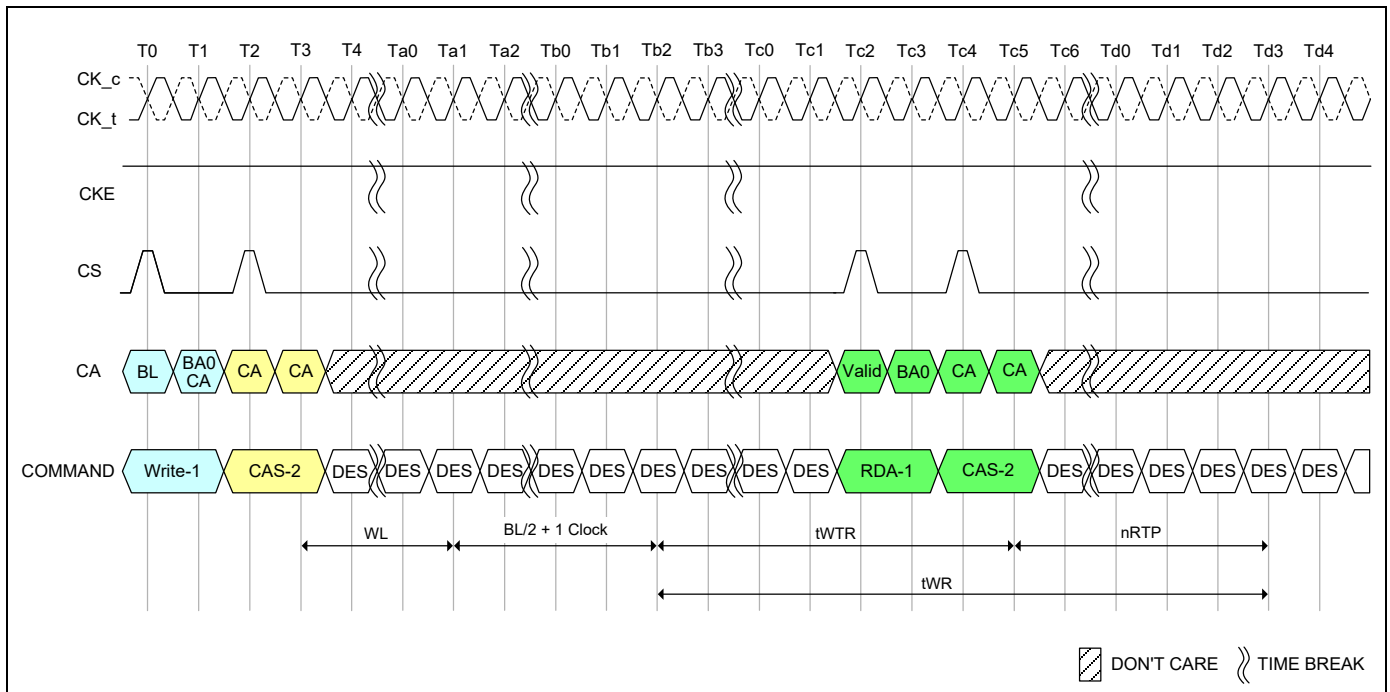
1.  $t_{CK(AVG)} = 0.938nS$ , Data Rate = 2133Mbps,  $t_{RCD(Min)} = \text{Max}(18nS, 4nCK)$ ,  $t_{RAS(Min)} = \text{Max}(42nS, 3nCK)$ ,  $nRTP = 8nCK$ ,  $BL = 32$ .
2.  $t_{RCD} = 20nCK$  comes from Roundup( $18nS/0.938nS$ ).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 62 - Command Input Timing with RAS lock**



### 7.4.18.1 Delay time from Write to Read with Auto-Precharge

In the case of write command followed by read with Auto-Precharge, controller must satisfy  $t_{WR}$  for the write command before initiating the DRAM internal Auto-Precharge. It means that  $(t_{WTR} + nRTP)$  should be equal or longer than  $(t_{WR})$  when BL setting is 16, as well as  $(t_{WTR} + nRTP + 8nCK)$  should be equal or longer than  $(t_{WR})$  when BL setting is 32. Refer to the following figure for details. Timing is shown in Table 34 and Table 35.



#### Notes:

1. Burst Length at Read = 16.
2. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 63 - Delay time from Write to Read with Auto-Precharge**





Table 34 - Timing between Commands (PRECHARGE and Auto-Precharge): DQ ODT is Disable

| From Command       | To Command                                  | Minimum Delay between "From Command" and "To Command" | Unit | Notes  |
|--------------------|---------------------------------------------|-------------------------------------------------------|------|--------|
| READ<br>BL=16      | PRECHARGE<br>(to same bank as Read)         | tRTP                                                  | tCK  | 1,6    |
|                    | PRECHARGE All                               | tRTP                                                  | tCK  | 1,6    |
| READ<br>BL=32      | PRECHARGE<br>(to same bank as Read)         | 8tCK + tRTP                                           | tCK  | 1,6    |
|                    | PRECHARGE All                               | 8tCK + tRTP                                           | tCK  | 1,6    |
| READ w/AP<br>BL=16 | PRECHARGE<br>(to same bank as READ w/AP)    | nRTP                                                  | tCK  | 1,10   |
|                    | PRECHARGE All                               | nRTP                                                  | tCK  | 1,10   |
|                    | Activate<br>(to same bank as READ w/AP)     | nRTP + tRPpb                                          | tCK  | 1,8,10 |
|                    | WRITE or WRITE w/AP<br>(same bank)          | Illegal                                               | -    |        |
|                    | MASK-WR or MASK-WR w/AP<br>(same bank)      | Illegal                                               | -    |        |
|                    | WRITE or WRITE w/AP<br>(different bank)     | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE        | tCK  | 3,4,5  |
|                    | MASK-WR or MASK-WR w/AP<br>(different bank) | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE        | tCK  | 3,4,5  |
|                    | READ or READ w/AP<br>(same bank)            | Illegal                                               | -    |        |
|                    | READ or READ w/AP<br>(different bank)       | BL/2                                                  | tCK  | 3      |
| READ w/AP<br>BL=32 | PRECHARGE<br>(to same bank as READ w/AP)    | 8tCK + nRTP                                           | tCK  | 1,10   |
|                    | PRECHARGE All                               | 8tCK + nRTP                                           | tCK  | 1,10   |
|                    | Activate<br>(to same bank as READ w/AP)     | 8tCK + nRTP + tRPpb                                   | tCK  | 1,8,10 |
|                    | WRITE or WRITE w/AP<br>(same bank)          | Illegal                                               | -    |        |
|                    | MASK-WR or MASK-WR w/AP<br>(same bank)      | Illegal                                               | -    |        |
|                    | WRITE or WRITE w/AP<br>(different bank)     | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE        | tCK  | 3,4,5  |
|                    | MASK-WR or MASK-WR w/AP<br>(different bank) | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE        | tCK  | 3,4,5  |
|                    | READ or READ w/AP<br>(same bank)            | Illegal                                               | -    |        |
|                    | READ or READ w/AP<br>(different bank)       | BL/2                                                  | tCK  | 3      |



Table 34 - Timing between Commands (PRECHARGE and Auto-Precharge): DQ ODT is Disable (cont'd)

| From Command             | To Command                                  | Minimum Delay between "From Command" and "To Command" | Unit | Notes  |
|--------------------------|---------------------------------------------|-------------------------------------------------------|------|--------|
| WRITE<br>BL=16 & 32      | PRECHARGE<br>(to same bank as WRITE)        | $WL + BL/2 + tWR + 1$                                 | tCK  | 1,7    |
|                          | PRECHARGE All                               | $WL + BL/2 + tWR + 1$                                 | tCK  | 1,7    |
| MASK-WR<br>BL=16         | PRECHARGE<br>(to same bank as MASK-WR)      | $WL + BL/2 + tWR + 1$                                 | tCK  | 1,7    |
|                          | PRECHARGE All                               | $WL + BL/2 + tWR + 1$                                 | tCK  | 1,7    |
| WRITE w/AP<br>BL=16 & 32 | PRECHARGE<br>(to same bank as WRITE w/AP)   | $WL + BL/2 + nWR + 1$                                 | tCK  | 1,11   |
|                          | PRECHARGE All                               | $WL + BL/2 + nWR + 1$                                 | tCK  | 1,11   |
|                          | ACTIVATE<br>(to same bank as WRITE w/AP)    | $WL + BL/2 + nWR + 1 + tRPpb$                         | tCK  | 1,8,11 |
|                          | WRITE or WRITE w/AP<br>(same bank)          | Illegal                                               | -    |        |
|                          | READ or READ w/AP<br>(same bank)            | Illegal                                               | -    |        |
|                          | WRITE or WRITE w/AP<br>(different bank)     | BL/2                                                  | tCK  | 3      |
|                          | MASK-WR or MASK-WR w/AP<br>(different bank) | BL/2                                                  | tCK  | 3      |
|                          | READ or READ w/AP<br>(different bank)       | $WL + BL/2 + tWTR + 1$                                | tCK  | 3,9    |
| MASK-WR w/AP<br>BL=16    | PRECHARGE<br>(to same bank as MASK-WR w/AP) | $WL + BL/2 + nWR + 1$                                 | tCK  | 1,11   |
|                          | PRECHARGE All                               | $WL + BL/2 + nWR + 1$                                 | tCK  | 1,11   |
|                          | ACTIVATE<br>(to same bank as MASK-WR w/AP)  | $WL + BL/2 + nWR + 1 + tRPpb$                         | tCK  | 1,8,11 |
|                          | WRITE or WRITE w/AP<br>(same bank)          | Illegal                                               | -    | 3      |
|                          | MASK-WR or MASK-WR w/AP<br>(same bank)      | Illegal                                               | -    | 3      |
|                          | WRITE or WRITE w/AP<br>(different bank)     | BL/2                                                  | tCK  | 3      |
|                          | MASK-WR or MASK-WR w/AP<br>(different bank) | BL/2                                                  | tCK  | 3      |
|                          | READ or READ w/AP<br>(same bank)            | Illegal                                               | -    | 3      |
|                          | READ or READ w/AP<br>(different bank)       | $WL + BL/2 + tWTR + 1$                                | tCK  | 3,9    |



Table 34 - Timing between Commands (PRECHARGE and Auto-Precharge): DQ ODT is Disable (cont'd)

| From Command     | To Command                               | Minimum Delay between "From Command" and "To Command" | Unit | Notes |
|------------------|------------------------------------------|-------------------------------------------------------|------|-------|
| PRECHARGE        | PRECHARGE<br>(to same bank as PRECHARGE) | 4                                                     | tCK  | 1     |
|                  | PRECHARGE All                            | 4                                                     | tCK  | 1     |
| PRECHARGE<br>All | PRECHARGE                                | 4                                                     | tCK  | 1     |
|                  | PRECHARGE All                            | 4                                                     | tCK  | 1     |

**Notes:**

- For a given bank, the precharge period should be counted from the latest precharge command, whether per bank or all bank, issued to that bank. The precharge period is satisfied tRP after that latest precharge command.
- Any command issued during the minimum delay time as specified in the table above is illegal.
- After READ w/AP, seamless read operations to different banks are supported. After WRITE w/AP or MASK-WR w/AP, seamless write operations to different banks are supported. READ, WRITE, and MASK-WR operations may not be truncated or interrupted.
- tRPST values depend on MR1-OP[7] respectively.
- tWPRE values depend on MR1-OP[2] respectively.
- Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tRTP(in nS) by tCK(in nS) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tRTP[nS] / tCK[nS]).
- Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tWR(in nS) by tCK(in nS) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tWR[nS] / tCK[nS]).
- Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tRPpb(in nS) by tCK(in nS) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tRPpb[nS] / tCK[nS]).
- Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tWTR(in nS) by tCK(in nS) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tWTR[nS] / tCK[nS]).
- For Read w/AP the value is nRTP which is defined in Mode Register 2.
- For Write w/AP the value is nWR which is defined in Mode Register 1.

Table 35 - Timing between Commands (read w/ AP and write command): DQ ODT is Enabled

| From Command       | To Command                                  | Minimum Delay between "From Command" and "To Command"                            | Unit | Notes |
|--------------------|---------------------------------------------|----------------------------------------------------------------------------------|------|-------|
| READ w/AP<br>BL=16 | WRITE or WRITE w/AP<br>(different bank)     | $RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon, min/tCK) + 1$ | tCK  | 2, 3  |
|                    | MASK-WR or MASK-WR w/AP<br>(different bank) | $RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon, min/tCK) + 1$ | tCK  | 2, 3  |
| READ w/AP<br>BL=32 | WRITE or WRITE w/AP<br>(different bank)     | $RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon, min/tCK) + 1$ | tCK  | 2, 3  |
|                    | MASK-WR or MASK-WR w/AP<br>(different bank) | $RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon, min/tCK) + 1$ | tCK  | 2, 3  |

**Notes:**

- The rest of the timing about precharge and Auto-Precharge is same as DQ ODT is Disable case.
- After READ w/AP, seamless read operations to different banks are supported. READ, WRITE, and MASK-WR operations may not be truncated or interrupted.
- tRPST values depend on MR1-OP[7] respectively.



#### 7.4.19 Refresh command

The REFRESH command is initiated with CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH and CA4 LOW at the first rising edge of the clock. Per bank REFRESH is initiated with CA5 LOW at the first rising edge of the clock. All bank REFRESH is initiated with CA5 HIGH at the first rising edge of the clock.

A per bank REFRESH command (REFpb) is performed to the bank address as transferred on CA0, CA1 and CA2 at the second rising edge of the clock. Bank address BA0 is transferred on CA0, bank address BA1 is transferred on CA1 and bank address BA2 is transferred on CA2. A per bank REFRESH command (REFpb) to the eight banks can be issued in any order. e.g., REFpb commands are issued in the following order: 1-3-0-2-4-7-5-6. After the eight banks have been refreshed using the per bank REFRESH command the controller can send another set of per bank REFRESH commands in the same order or a different order. e.g., REFpb commands are issued in the following order that is different from the previous order: 7-1-3-5-0-4-2-6. One of the possible order can also be a sequential round robin: 0-1-2-3-4-5-6-7. It is illegal to send a per-bank REFRESH command to the same bank unless all eight banks have been refreshed using the per bank REFRESH command. The count of eight REFpb commands starts with the first REFpb command after a synchronization event.

The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon asserting RESET\_n or at every exit from Self Refresh. REFab command also synchronizes the counter between the controller and SDRAM to zero. The SDRAM device can be placed in Self Refresh or a REFab command can be issued at any time without cycling through all eight banks using per bank REFRESH command. After the bank count is synchronized to zero the controller can issue per bank REFRESH commands in any order as described in the previous paragraph.

A REFab command issued when the bank counter is not zero will reset the bank counter to zero and the DRAM will perform refreshes to all banks as indicated by the row counter. If another refresh command (REFab or REFpb) is issued after the REFab command, then it uses an incremented value of the row counter. The table below shows examples of both bank and refresh counter increment behavior.

**Table 36 - Bank and Refresh counter increment behavior**

| #  | Command             | BA2 | BA1 | BA0 | Refresh Bank # | Bank Counter # | Ref Counter # (Row Address #) |
|----|---------------------|-----|-----|-----|----------------|----------------|-------------------------------|
| 0  | Reset, SRX or REFab |     |     |     |                | To 0           | -                             |
| 1  | REFpb               | 0   | 0   | 0   | 0              | 0 to 1         | n                             |
| 2  | REFpb               | 0   | 0   | 1   | 1              | 1 to 2         |                               |
| 3  | REFpb               | 0   | 1   | 0   | 2              | 2 to 3         |                               |
| 4  | REFpb               | 0   | 1   | 1   | 3              | 3 to 4         |                               |
| 5  | REFpb               | 1   | 0   | 0   | 4              | 4 to 5         |                               |
| 6  | REFpb               | 1   | 0   | 1   | 5              | 5 to 6         |                               |
| 7  | REFpb               | 1   | 1   | 0   | 6              | 6 to 7         |                               |
| 8  | REFpb               | 1   | 1   | 1   | 7              | 7 to 0         |                               |
| 9  | REFpb               | 1   | 1   | 0   | 6              | 0 to 1         | n + 1                         |
| 10 | REFpb               | 1   | 1   | 1   | 7              | 1 to 2         |                               |
| 11 | REFpb               | 0   | 0   | 1   | 1              | 2 to 3         |                               |
| 12 | REFpb               | 0   | 1   | 1   | 3              | 3 to 4         |                               |
| 13 | REFpb               | 1   | 0   | 1   | 5              | 4 to 5         |                               |
| 14 | REFpb               | 0   | 1   | 0   | 2              | 5 to 6         |                               |
| 15 | REFpb               | 0   | 0   | 0   | 0              | 6 to 7         |                               |
| 16 | REFpb               | 1   | 0   | 0   | 4              | 7 to 0         |                               |
| 17 | REFpb               | 0   | 0   | 0   | 0              | 0 to 1         | n + 2                         |
| 18 | REFpb               | 0   | 0   | 1   | 1              | 1 to 2         |                               |
| 19 | REFpb               | 0   | 1   | 0   | 2              | 2 to 3         |                               |
| 20 | REFab               | V   | V   | V   | 0~7            | To 0           | n + 2                         |
| 21 | REFpb               | 1   | 1   | 0   | 6              | 0 to 1         | n + 3                         |
| 22 | REFpb               | 1   | 1   | 1   | 7              | 1 to 2         |                               |



A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per bank REFRESH command. (Reference Table 37 and Figure 64 through 66.)

The REFpb command must not be issued to the device until the following conditions are met:

- tRFCab has been satisfied after the prior REFab command.
- tRFCpb has been satisfied after the prior REFpb command to the same bank.
- tpbR2pbR has been satisfied after the prior REFpb command to different bank.
- tRP has been satisfied after the prior PRECHARGE command to that bank.
- tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command).

The target bank is inaccessible during per bank REFRESH cycle time (tRFCpb) or Per-bank Refresh to Per-bank Refresh different bank Time (tpbR2pbR), however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, these conditions must be met:

- tRFCpb must be satisfied before issuing a REFab command.
- tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank.
- tRRD must be satisfied before issuing an ACTIVATE command to a different bank.
- tRFCpb must be satisfied before issuing another REFpb command to the same bank.
- tpbR2pbR must be satisfied before issuing another REFpb command to a different bank.

An all bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-all command prior to issuing an all bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied following the prior REFab command.
- tRFCpb has been satisfied following the prior REFpb command.
- tRP has been satisfied following the prior PRECHARGE commands.

When an all bank refresh cycle has completed, all banks will be idle. After issuing REFab:

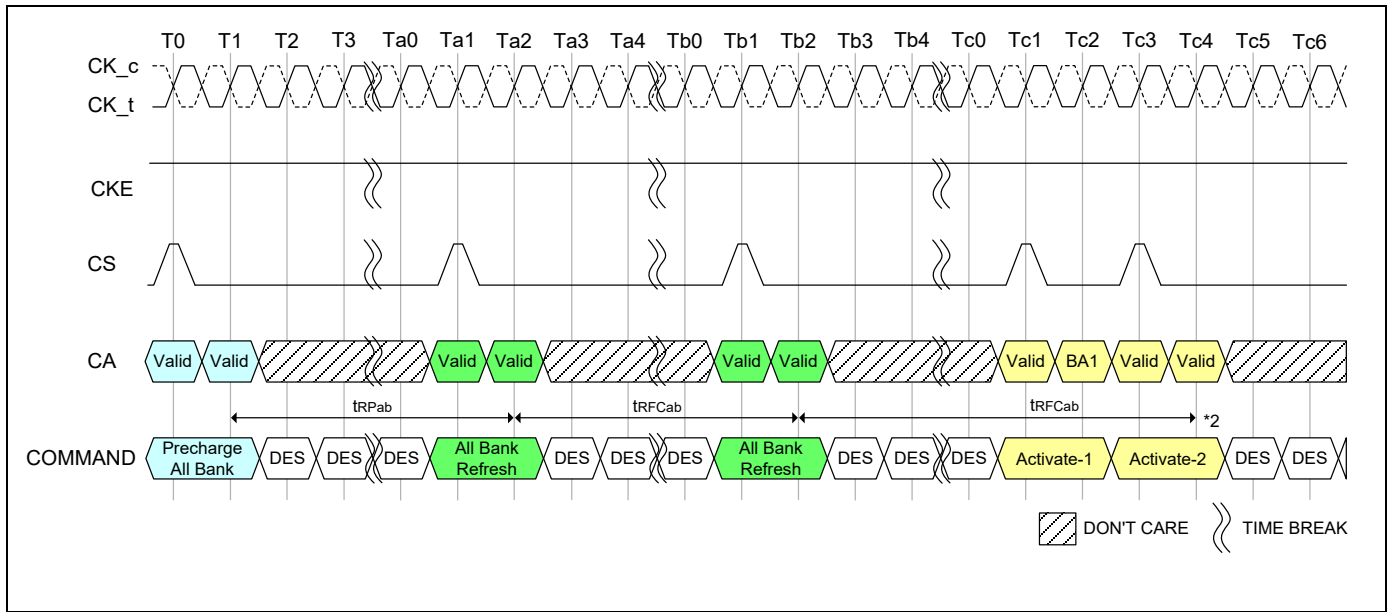
- tRFCab latency must be satisfied before issuing an ACTIVATE command.
- tRFCab latency must be satisfied before issuing a REFab or REFpb command.

**Table 37 - REFRESH Command Scheduling Separation requirements**

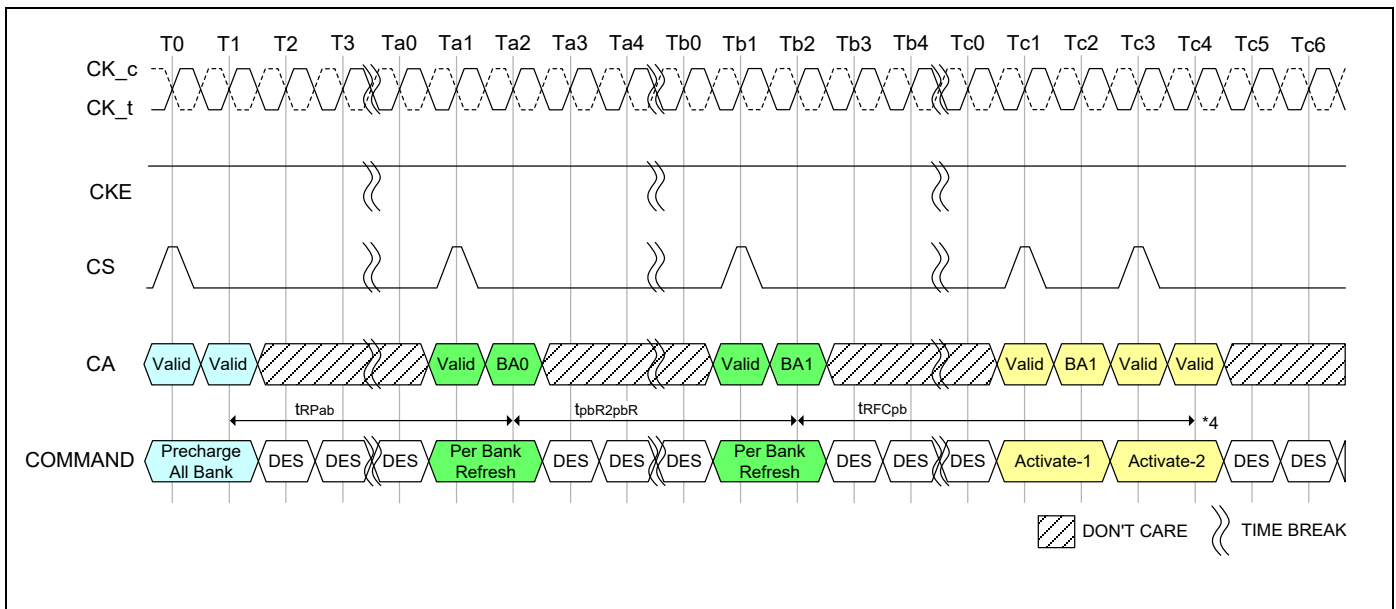
| Symbol   | Minimum Delay From | To                                                             | Notes |
|----------|--------------------|----------------------------------------------------------------|-------|
| tRFCab   | REFab              | REFab                                                          |       |
|          |                    | Activate command to any bank                                   |       |
|          |                    | REFpb                                                          |       |
| tRFCpb   | REFpb              | REFab                                                          |       |
|          |                    | Activate command to same bank as REFpb                         |       |
|          |                    | REFpb to the same bank                                         |       |
| tpbR2pbR | REFpb              | REFpb to a different bank                                      |       |
| tRRD     | REFpb              | Activate command to different bank than REFpb                  |       |
|          | Activate           | REFpb                                                          | 1     |
|          |                    | Activate command to different bank than prior Activate command |       |

**Note:**

1. A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state.

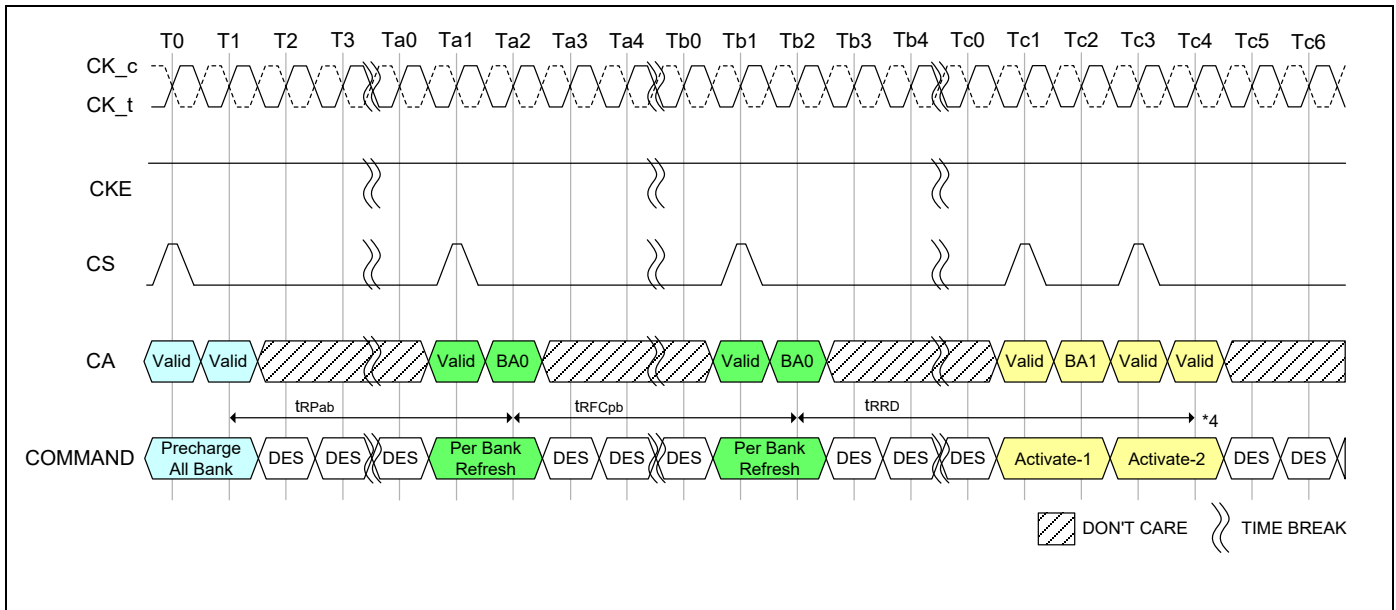
**Notes:**

1. DES commands are shown for ease of illustration; other commands may be valid at these times.
2. Activate Command is shown as an example. Other commands may be valid provided the timing specification is satisfied.

**Figure 64 - All Bank Refresh Operation****Notes:**

1. DES commands are shown for ease of illustration; other commands may be valid at these times.
2. In the beginning of this example, the REFpb bank is pointing to bank 0.
3. Operations to banks other than the bank being refreshed are supported during the tpbR2pbR period.
4. Activate Command is shown as an example. Other commands may be valid provided the timing specification is satisfied.

**Figure 65 - Per Bank Refresh to a different bank Operation**

**Notes:**

1. DES commands are shown for ease of illustration; other commands may be valid at these times.
2. In the beginning of this example, the REFpb bank is pointing to bank 0.
3. Operations to banks other than the bank being refreshed are supported during the trFCpb period.
4. Activate Command is shown as an example. Other commands may be valid provided the timing specification is satisfied.

**Figure 66 - Per Bank Refresh to the same bank Operation**

In general, a Refresh command needs to be issued to the LPDDR4/LPDDR4X SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR4/LPDDR4X SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed and maximum number of pulled-in or postponed REF command is dependent on refresh rate. It is described in the table below. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to  $9 \times \text{tREFI}$ . A maximum of 8 additional Refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to  $9 \times \text{tREFI}$ .





At any given time, a maximum of 16 REF commands can be issued within  $2 \times t_{REFI}$ . Self Refresh Mode may be entered with a maximum of eight Refresh commands being postponed. After exiting Self Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self Refresh) will never exceed eight. During Self Refresh Mode, the number of postponed or pulled-in REF commands does not change.

And for per bank refresh, a maximum 8 x 8 per bank refresh commands can be postponed or pulled in for scheduling efficiency. At any given time, a maximum of  $2 \times 8 \times 8$  per bank refresh commands can be issued within  $2 \times t_{REFI}$ . (Reference Table 38 and Table 39, and Figure 68.)

Table 38 - Legacy Refresh Command Timing Constraints

| MR4<br>OP[2:0]   | Refresh rate     | Max. No. of<br>pulled-in or<br>postponed REFab | Max. Interval<br>between two<br>REFab | Max. No. of REFab<br>within max( $2 \times t_{REFI}$<br>x refresh rate<br>multiplier, $16 \times t_{RFC}$ ) | Per bank Refresh |
|------------------|------------------|------------------------------------------------|---------------------------------------|-------------------------------------------------------------------------------------------------------------|------------------|
| 000 <sub>b</sub> | Low Temp. Limit  | N/A                                            | N/A                                   | N/A                                                                                                         | N/A              |
| 001 <sub>b</sub> | 4x $t_{REFI}$    | 8                                              | $9 \times 4 \times t_{REFI}$          | 16                                                                                                          | 1/8 of REFab     |
| 010 <sub>b</sub> | 2x $t_{REFI}$    | 8                                              | $9 \times 2 \times t_{REFI}$          | 16                                                                                                          | 1/8 of REFab     |
| 011 <sub>b</sub> | 1x $t_{REFI}$    | 8                                              | $9 \times t_{REFI}$                   | 16                                                                                                          | 1/8 of REFab     |
| 100 <sub>b</sub> | 0.5x $t_{REFI}$  | 8                                              | $9 \times 0.5 \times t_{REFI}$        | 16                                                                                                          | 1/8 of REFab     |
| 101 <sub>b</sub> | 0.25x $t_{REFI}$ | 8                                              | $9 \times 0.25 \times t_{REFI}$       | 16                                                                                                          | 1/8 of REFab     |
| 110 <sub>b</sub> | 0.25x $t_{REFI}$ | 8                                              | $9 \times 0.25 \times t_{REFI}$       | 16                                                                                                          | 1/8 of REFab     |
| 111 <sub>b</sub> | High Temp. Limit | N/A                                            | N/A                                   | N/A                                                                                                         | N/A              |

Table 39 - Modified REFRESH Command Timing Constraints

| MR4<br>OP[2:0]   | Refresh rate     | Max. No. of<br>pulled-in or<br>postponed REFab | Max. Interval<br>between two<br>REFab | Max. No. of REFab<br>within max( $2 \times t_{REFI}$<br>x refresh rate<br>multiplier, $16 \times t_{RFC}$ ) | Per bank Refresh |
|------------------|------------------|------------------------------------------------|---------------------------------------|-------------------------------------------------------------------------------------------------------------|------------------|
| 000 <sub>b</sub> | Low Temp. Limit  | N/A                                            | N/A                                   | N/A                                                                                                         | N/A              |
| 001 <sub>b</sub> | 4x $t_{REFI}$    | 2                                              | $3 \times 4 \times t_{REFI}$          | 4                                                                                                           | 1/8 of REFab     |
| 010 <sub>b</sub> | 2x $t_{REFI}$    | 4                                              | $5 \times 2 \times t_{REFI}$          | 8                                                                                                           | 1/8 of REFab     |
| 011 <sub>b</sub> | 1x $t_{REFI}$    | 8                                              | $9 \times t_{REFI}$                   | 16                                                                                                          | 1/8 of REFab     |
| 100 <sub>b</sub> | 0.5x $t_{REFI}$  | 8                                              | $9 \times 0.5 \times t_{REFI}$        | 16                                                                                                          | 1/8 of REFab     |
| 101 <sub>b</sub> | 0.25x $t_{REFI}$ | 8                                              | $9 \times 0.25 \times t_{REFI}$       | 16                                                                                                          | 1/8 of REFab     |
| 110 <sub>b</sub> | 0.25x $t_{REFI}$ | 8                                              | $9 \times 0.25 \times t_{REFI}$       | 16                                                                                                          | 1/8 of REFab     |
| 111 <sub>b</sub> | High Temp. Limit | N/A                                            | N/A                                   | N/A                                                                                                         | N/A              |

**Notes:**

- For any thermal transition phase where Refresh mode is transitioned to either 2x  $t_{REFI}$  or 4x  $t_{REFI}$ , DRAM will support the previous postponed refresh requirement provided the number of postponed refreshes is monotonically reduced to meet the new requirement. However, the pulled-in refresh commands in previous thermal phase are not applied in new thermal phase. Entering new thermal phase the controller must count the number of pulled-in refresh commands as zero, regardless of remaining pulled-in refresh commands in previous thermal phase.
- LPDDR4/LPDDR4X SDRAMs are refreshed properly if memory controller issues refresh commands with same or shorter refresh period than reported by MR4 OP[2:0]. If shorter refresh period is applied, the corresponding requirements from Table apply. For example, when MR4 OP[2:0]=001<sub>b</sub>, controller can be in any refresh rate from 4x  $t_{REFI}$  to 0.25x  $t_{REFI}$ . When MR4 OP[2:0]=010<sub>b</sub>, the only prohibited refresh rate is 4x  $t_{REFI}$ .



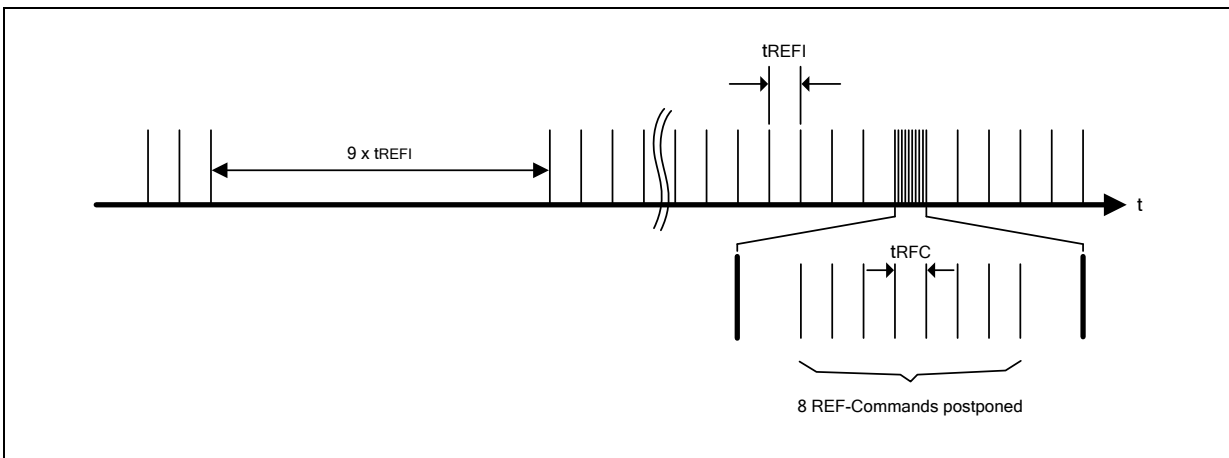


Figure 67 - Postponing Refresh Commands (Example)

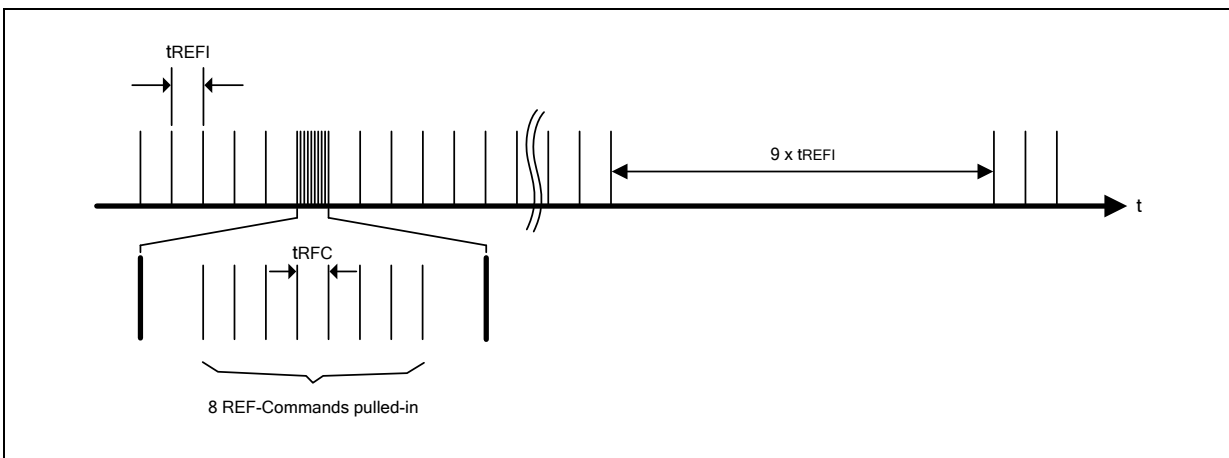
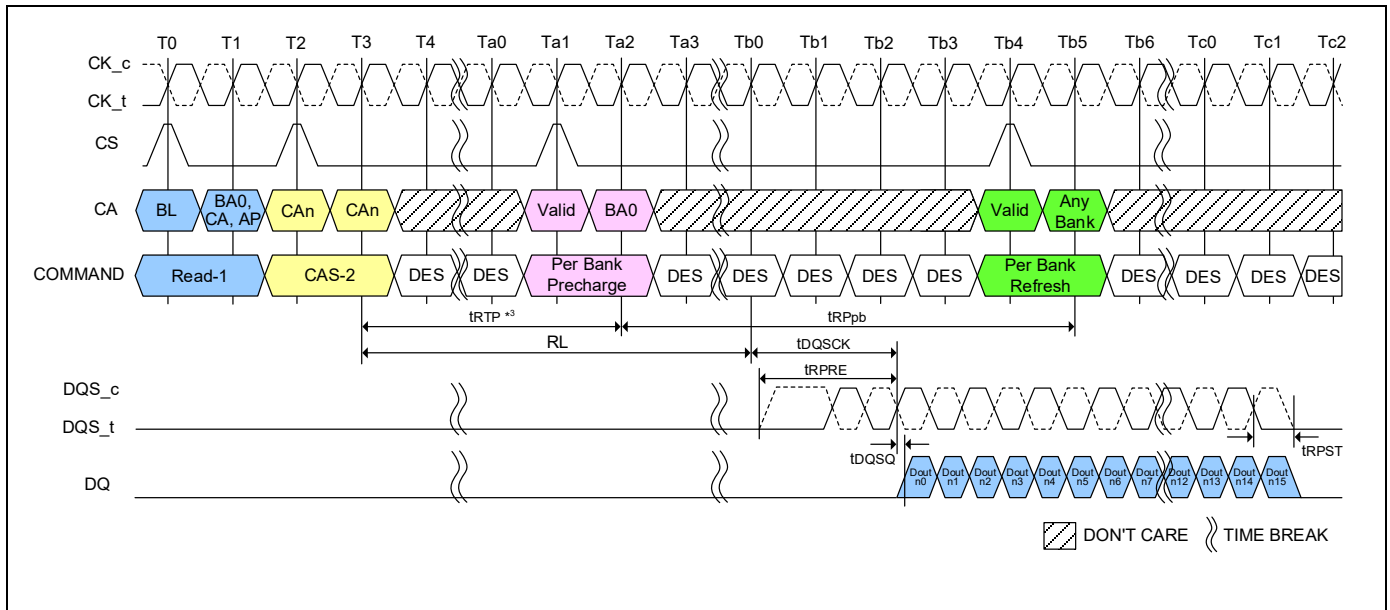


Figure 68 - Pulling-in Refresh Commands (Example)



#### 7.4.19.1 Burst Read operation followed by Per Bank Refresh

The Per Bank Refresh command can be issued after  $t_{RTP} + t_{RPpb}$  from Read command (Figure 69).

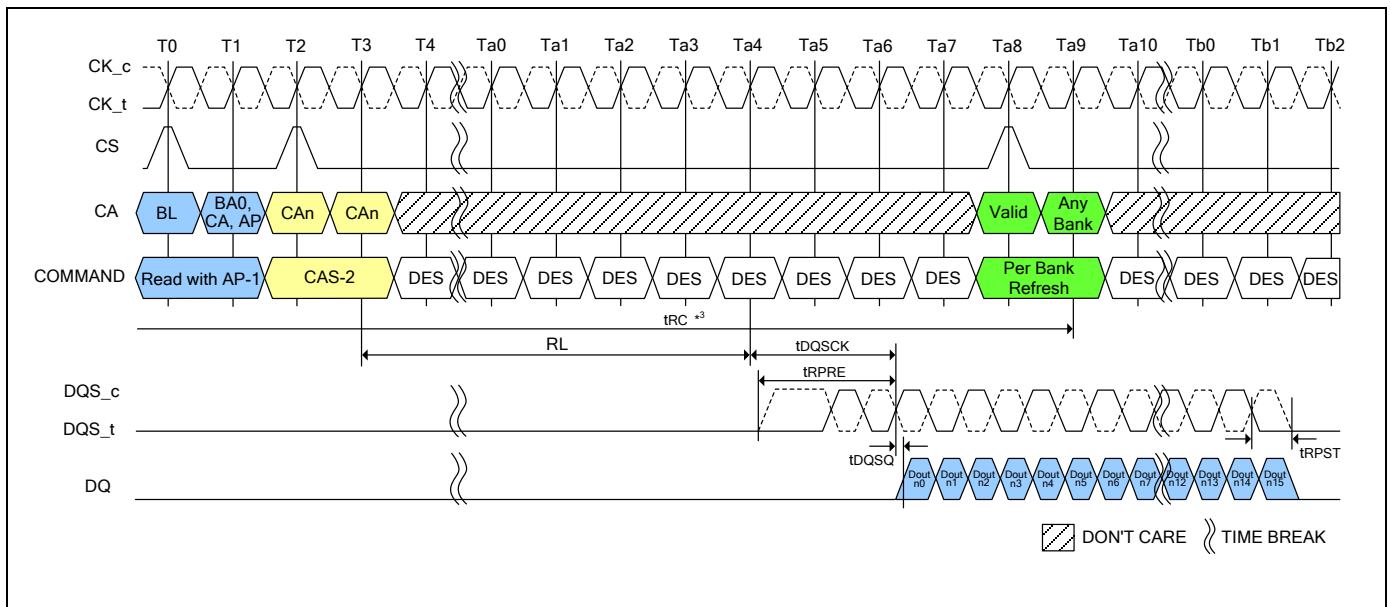


#### Notes:

1. BL = 16, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Dout n = data-out from column n.
3. In case of BL = 32, Delay time from Read to Per Bank Precharge is 8nCK +  $t_{RTP}$ .
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 69 - Burst Read operation followed by Per Bank Refresh**

The Per Bank Refresh command can be issued after  $t_{RC}$  from Read with Auto Precharge command (Figure 70).



#### Notes:

1. BL = 16, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Dout n = data-out from column n.
3.  $t_{RC}$  needs to be satisfied prior to issuing subsequent Per Bank Refresh command.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 70 - Burst Read with Auto-Precharge operation followed by Per Bank Refresh**



#### 7.4.20 Refresh Requirement

**Table 40 - Refresh Requirement Parameters per die for single Channel SDRAM devices**

| Refresh Requirements                                        |       | Symbol   | 4Gb   | Units |
|-------------------------------------------------------------|-------|----------|-------|-------|
| Density per Channel                                         |       |          | 4Gb   |       |
| Number of banks per channel                                 |       |          | 8     |       |
| Refresh Window (tREFW)<br>(1x Refresh)* <sup>2,3</sup>      |       | tREFW    | 32    | mS    |
| Required Number of REFRESH<br>Commands in a tREFW window    |       | R        | 8192  | -     |
| Average Refresh Interval<br>(1x Refresh)* <sup>2</sup>      | REFAB | tREFI    | 3.904 | μS    |
|                                                             | REFPB | tREFIpb  | 488   | nS    |
| Refresh Cycle Time (All Banks)                              |       | tRFCab   | 180   | nS    |
| Refresh Cycle Time (Per Bank)                               |       | tRFCpb   | 90    | nS    |
| Per-bank Refresh to Per-bank<br>Refresh different bank Time |       | tpbR2pbR | 90    | nS    |

**Note:**

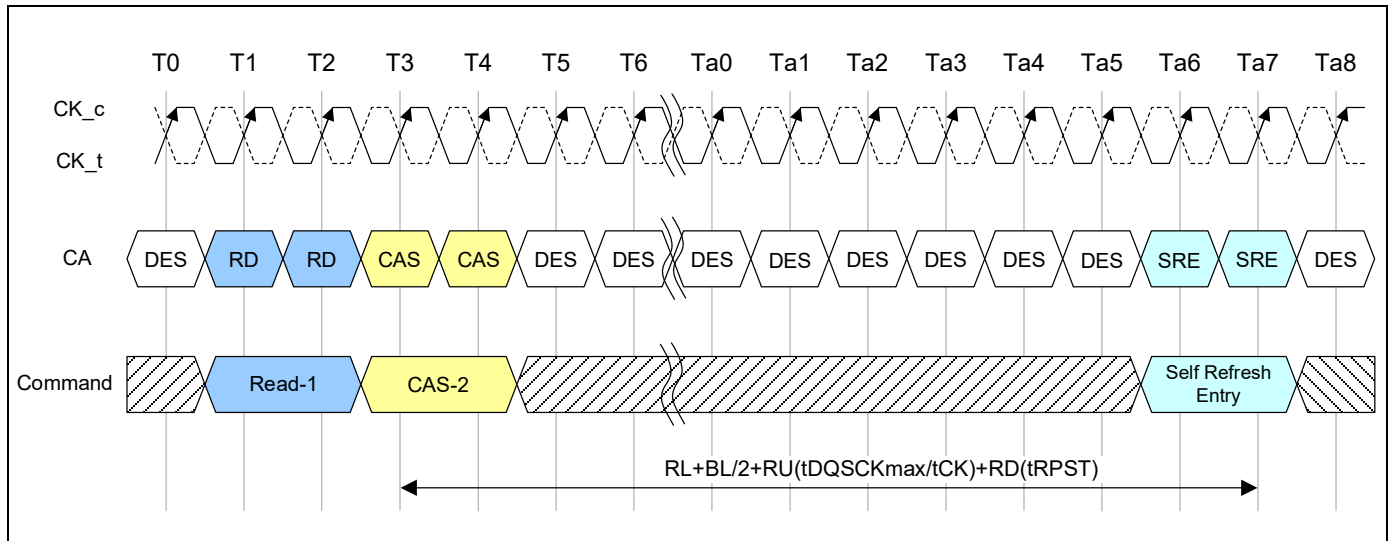
1. Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
2. 1x refresh rate (tREFW=32mS) is supported at all temperatures at or below 85°C TCASE. If MR4 OP[2:0] indicates a refresh rate of greater than 1x is supported, tREFW can be extended.
3. Refer to MR4 OP[2:0] for detailed Refresh Rate and its multipliers.



## 7.4.21 Self Refresh Operation

### 7.4.21.1 Self Refresh Entry and Exit

The Self Refresh command can be used to retain data in the LPDDR4/LPDDR4X SDRAM, the SDRAM retains data without external Refresh command. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh is entered by Self Refresh Entry Command defined by having CS High, CA0 Low, CA1 Low, CA2 Low; CA3 High; CA4 High, CA5 Valid (Valid that means it is Logic Level, High or Low) for the first rising edge and CS Low, CA0 Valid, CA1 Valid, CA2 Valid, CA3 Valid, CA4 Valid, CA5 Valid at the second rising edge of the clock. Self Refresh command is only allowed when read data burst is completed and SDRAM is idle state.



During Self Refresh mode, external clock input is needed and all input pin of SDRAM are activated. SDRAM can accept the following commands, MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2 except PASR Bank/Segment setting.

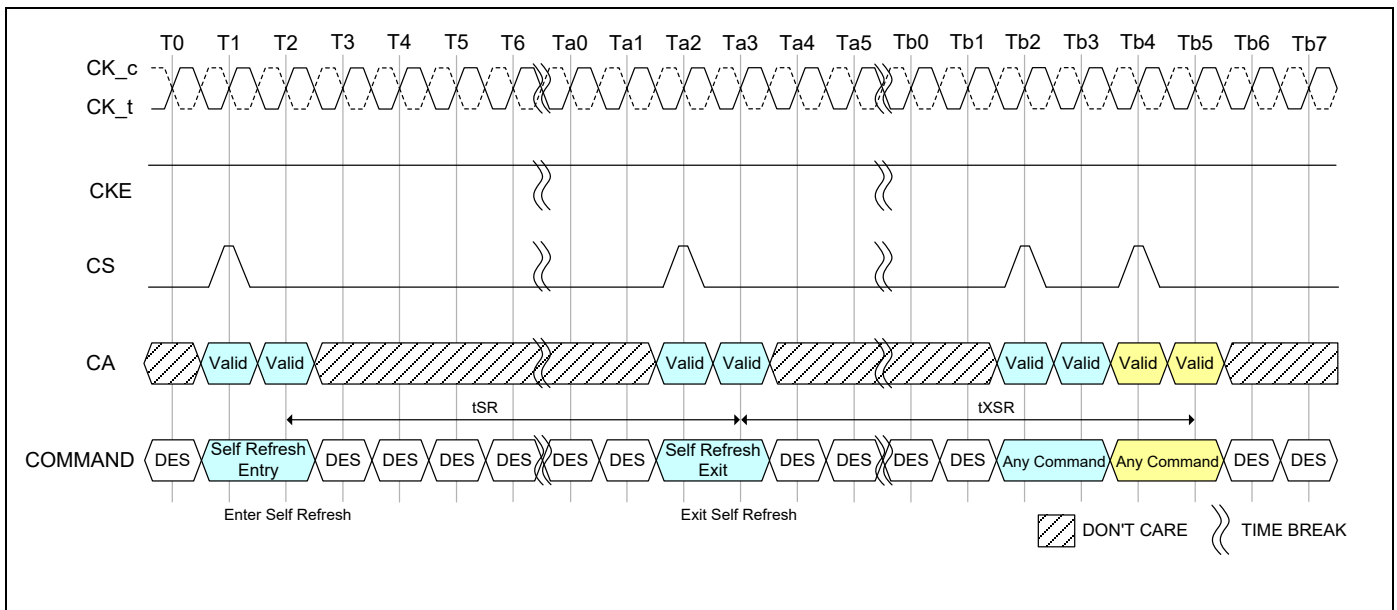
LPDDR4/LPDDR4X SDRAM can operate in Self Refresh in both the standard or elevated temperature ranges. SDRAM will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperature and higher at high temperatures.

For proper Self Refresh operation, power supply pins (VDD1, VDD2 and VDDQ) must be at valid levels. However, VDDQ may be turned off during Self Refresh with Power Down after tCKELCK (Max(5nS, 5nCK)) is satisfied (Refer to figure 72 about tCKELCK).

Prior to exiting Self Refresh with Power Down, VDDQ must be within specified limits. The minimum time that the SDRAM must remain in Self Refresh model is tSR min. Once Self Refresh Exit is registered, only MRR-1, CAS-2, DES, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting are allowed until tXSR is satisfied.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when Self Refresh Exit is registered. Upon exit from Self Refresh, it is required that at least one REFRESH command (8 per bank or 1 all bank) is issued before entry into a subsequent Self Refresh.

This REFRESH command is not included in the count of regular refresh commands required by the tREFI interval, and does not modify the postponed or pulled-in refresh counts; the REFRESH command does count toward the maximum refreshes permitted within 2 x tREFI.

**Notes:**

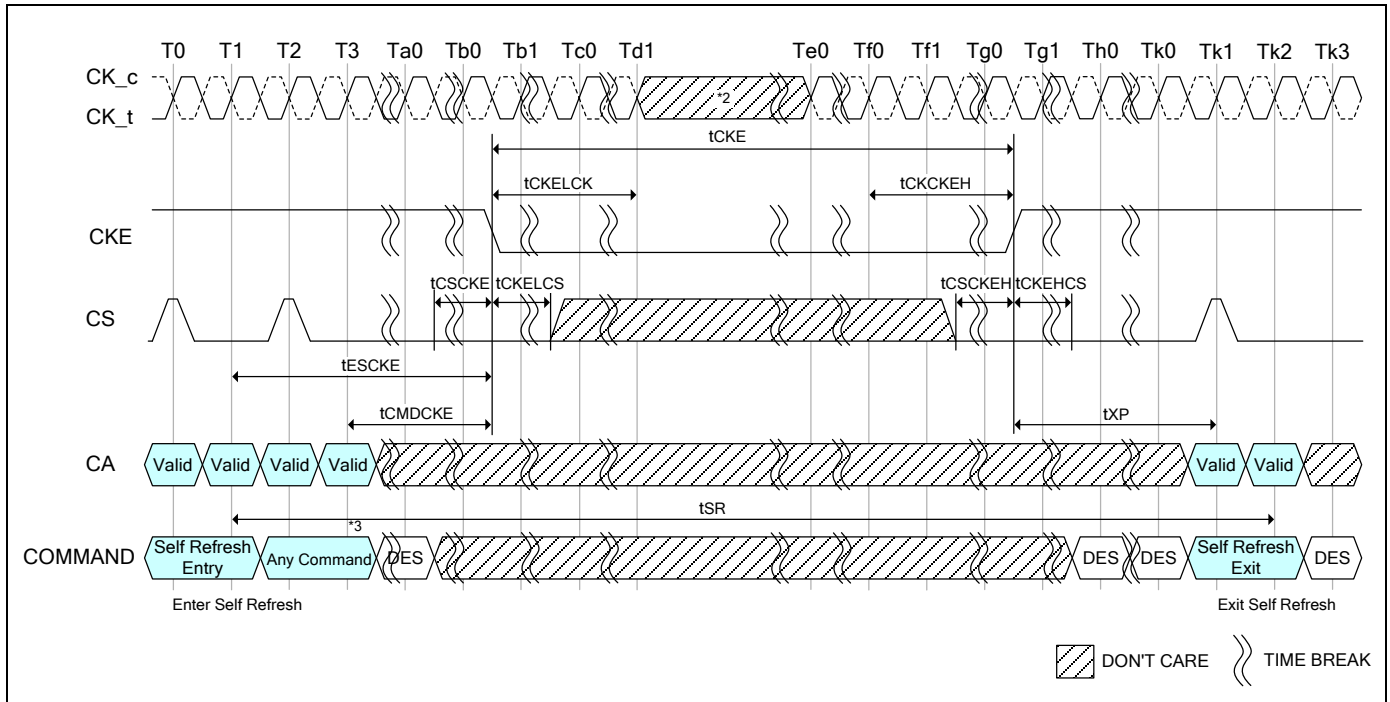
1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is allowed during Self Refresh.
2. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 71 - Self Refresh Entry/Exit Timing**



### 7.4.21.2 Power Down Entry and Exit during Self Refresh

Entering/Exiting Power Down Mode is allowed during Self Refresh mode in SDRAM. The related timing parameters between Self Refresh Entry/Exit and Power Down Entry/Exit are shown in Figure 72.



#### Notes:

1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is allowed during Self Refresh.
2. Input clock frequency can be changed or the input clock can be stopped or floated after  $t_{CKELCK}$  satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of  $t_{CKCKEH}$  of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
3. 2 Clock command for example.

**Figure 72 - Self Refresh Entry/Exit Timing with Power Down Entry/Exit**



### 7.4.21.3 Partial Array Self-Refresh (PASR)

#### PASR Bank Masking

The LPDDR4/LPDDR4X SDRAM has eight banks. Each bank of an LPDDR4/LPDDR4X SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits, accessible via MRW command, is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is described in the following section.

#### PASR Segment Masking

A segment masking scheme may be used in lieu of or in combination with the bank masking scheme in LPDDR4/LPDDR4X SDRAM which utilize eight segments per bank. For segment masking bit assignments, see Mode Register 17. For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, “masked”. Programming of segment mask bits is similar to the one of bank mask bits. Eight segments are used as listed in Mode Register 17. One mode register unit is used for the programming of segment mask bits up to 8 bits. One more mode register unit may be reserved for future use. Programming of bits in the reserved registers has no effect on the device operation.

**Example of Bank and Segment Masking use in LPDDR4/LPDDR4X SDRAM**

|                         | Segment Mask(MR17) | Bank 0 | Bank 1 | Bank 2 | Bank 3 | Bank 4 | Bank 5 | Bank 6 | Bank 7 |
|-------------------------|--------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| <b>Bank Mask (MR16)</b> |                    | 0      | 1      | 0      | 0      | 0      | 0      | 0      | 1      |
| <b>Segment 0</b>        | 0                  | -      | M      | -      | -      | -      | -      | -      | M      |
| <b>Segment 1</b>        | 0                  | -      | M      | -      | -      | -      | -      | -      | M      |
| <b>Segment 2</b>        | 1                  | M      | M      | M      | M      | M      | M      | M      | M      |
| <b>Segment 3</b>        | 0                  | -      | M      | -      | -      | -      | -      | -      | M      |
| <b>Segment 4</b>        | 0                  | -      | M      | -      | -      | -      | -      | -      | M      |
| <b>Segment 5</b>        | 0                  | -      | M      | -      | -      | -      | -      | -      | M      |
| <b>Segment 6</b>        | 0                  | -      | M      | -      | -      | -      | -      | -      | M      |
| <b>Segment 7</b>        | 1                  | M      | M      | M      | M      | M      | M      | M      | M      |

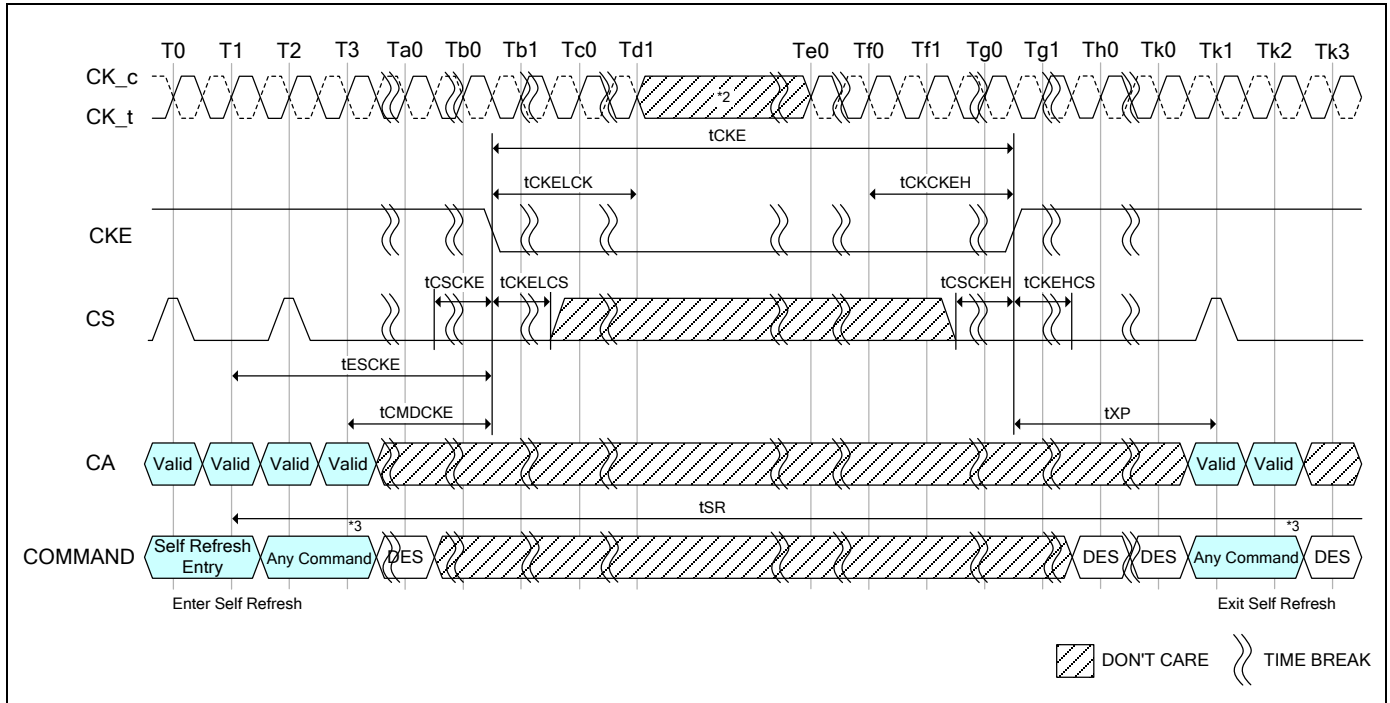
**Note:**

This table illustrates an example of an 8-bank LPDDR4/LPDDR4X SDRAM, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.



#### 7.4.21.4 Command input Timing after Power Down Exit

Command input timings after Power Down Exit during Self Refresh mode are shown in Figure 73.



#### Notes:

1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is allowed during Self Refresh.
2. Input clock frequency can be changed or the input clock can be stopped or floated after tCKELCK satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCKEH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
3. 2 Clock command for example.

**Figure 73 - Command input timings after Power Down Exit during Self Refresh**





## 7.4.21.5 Self Refresh Timing Table

Table 41 - Self Refresh Timing

| Parameter                               | Symbol | Min/Max | Data Rate                 | Unit | Note |
|-----------------------------------------|--------|---------|---------------------------|------|------|
| <b>Self Refresh Timing</b>              |        |         |                           |      |      |
| Delay from SRE command to CKE Input low | tESCKE | Min     | Max(1.75nS, 3tCK)         | nS   | 1    |
| Minimum Self Refresh Time               | tSR    | Min     | Max(15nS, 3tCK)           | nS   | 1    |
| Exit Self Refresh to Valid commands     | tXSR   | Min     | Max(tRFCab + 7.5nS, 2tCK) | nS   | 1, 2 |

**Notes:**

1. Delay time has to satisfy both analog time (nS) and clock count (tCK). It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 \* tCK) and 1.75nS has transpired. The case which 3tCK is applied to is shown in Figure 74.
2. MRR-1, CAS-2, DES, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting are only allowed during this period.

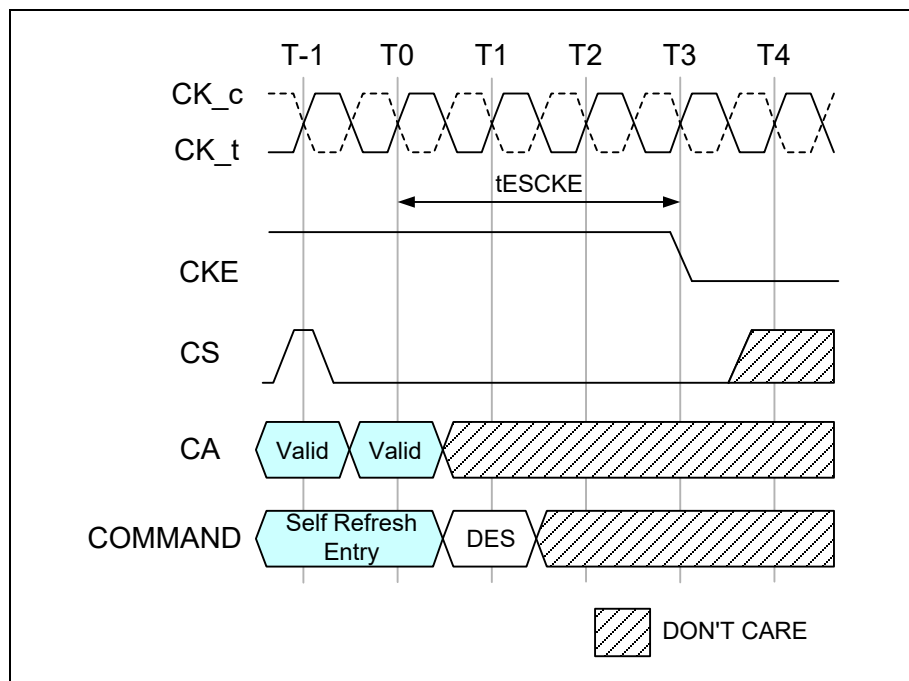
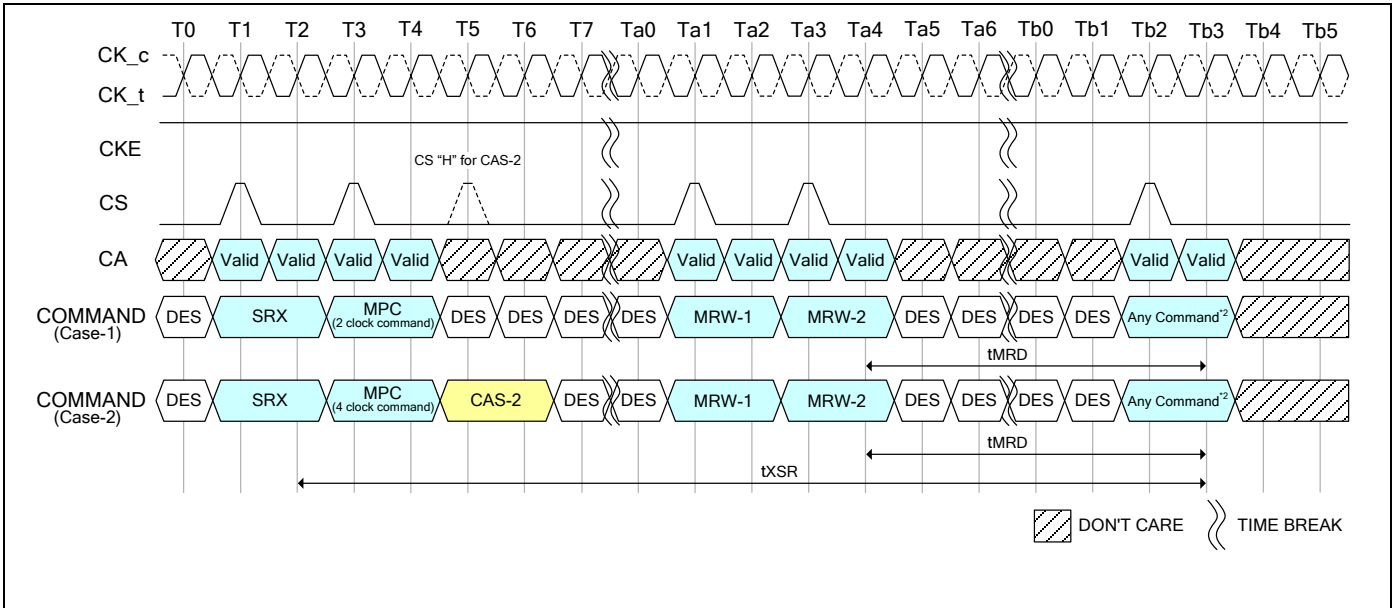


Figure 74 - tESCKE Timing



#### 7.4.22 MRR, MRW, MPC Command during t<sub>XS</sub>R, t<sub>RF</sub>C

Mode Register Read (MRR), Multi-Purpose (MPC) and Mode Register Write (MRW) command except PASR Bank/Segment setting can be issued during t<sub>XS</sub>R period (Figure 75).

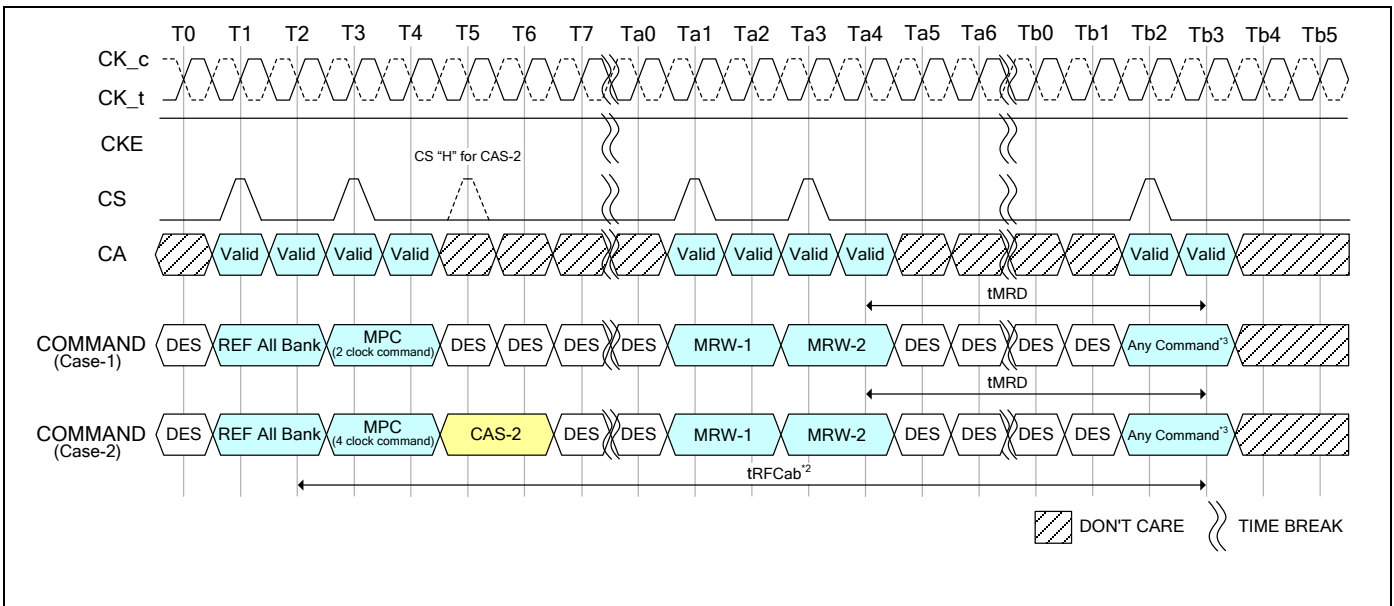


##### Notes:

1. MPC and MRW command are shown in figure at this time, any combination of MRR, MRW and MPC is allowed during t<sub>XS</sub>R period.
2. Any command also includes MRR, MRW and all MPC command.

**Figure 75 - MRR, MRW and MPC Commands Issuing Timing during t<sub>XS</sub>R**

Mode Register Read (MRR), Mode Register Write (MRW) and Multi-Purpose Command (MPC) can be issued during t<sub>RF</sub>C period (Figure 76).



##### Notes:

1. MPC and MRW command are shown in figure at this time, any combination of MRR, MRW and MPC is allowed during t<sub>RF</sub>Cab or t<sub>RF</sub>Cpb period.
2. Refresh cycle time depends on Refresh command. In case of REF per Bank command issued, Refresh cycle time will be t<sub>RF</sub>Cpb.
3. Any command also includes MRR, MRW and all MPC command.

**Figure 76 - MRR, MRW and MPC Commands Issuing Timing during t<sub>RF</sub>C**



### 7.4.23 Mode Register Read (MRR)

The Mode Register Read (MRR) command is used to read configuration and status data from the LPDDR4/LPDDR4X SDRAM registers. The MRR command is initiated with CS and CA[5:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[5:0]) allow the user to select one of 64 registers. The mode register contents are available on the first 4UI's data bits of DQ[7:0] after  $RL \times t_{CK} + t_{DQ_{SCK}} + t_{DQ_{SQ}}$  following the MRR command. Subsequent data bits contain valid but undefined content. DQS is toggled for the duration of the Mode Register READ burst. The MRR has a command burst length 16. Reference Table 42 and Figure 77.

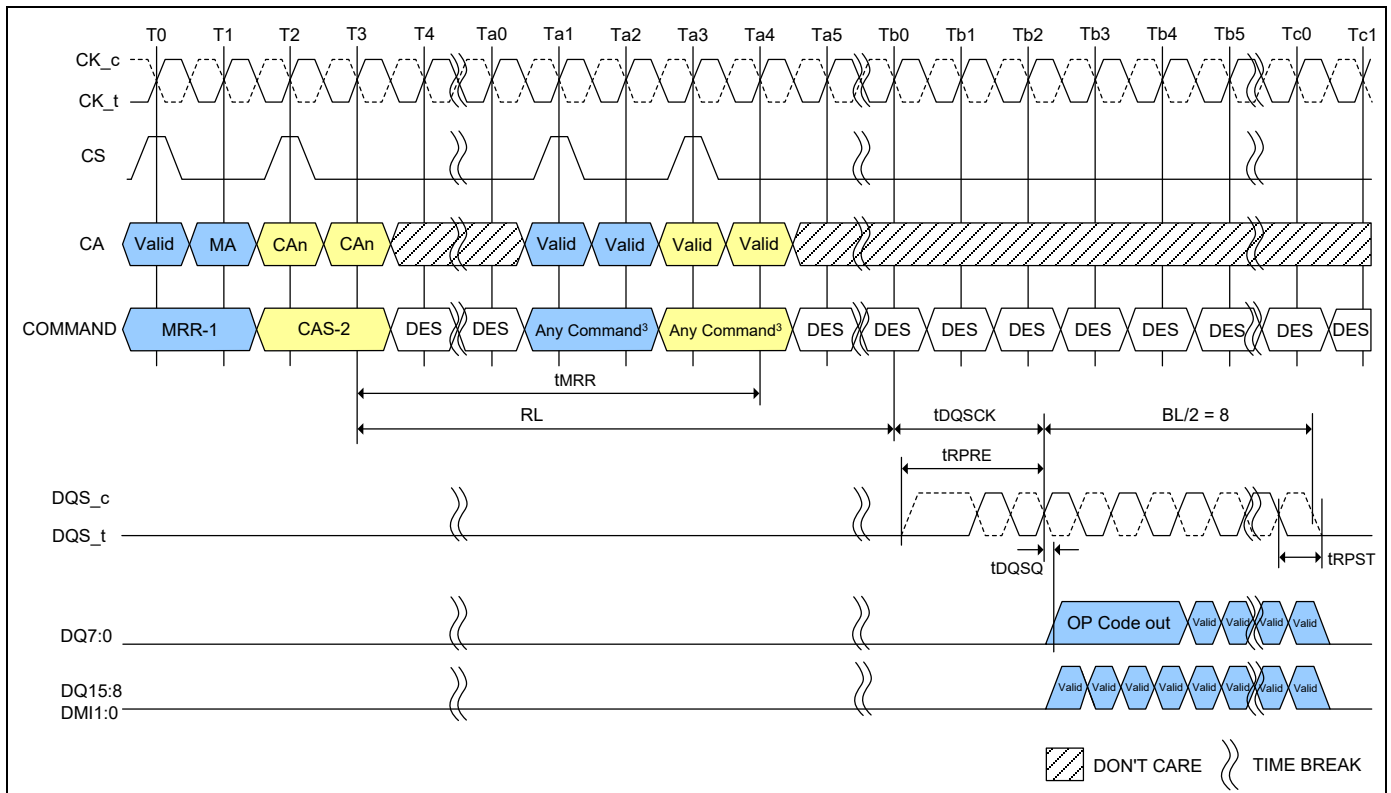
MRR operation must not be interrupted.

**Table 42 - DQ output mapping**

| UI     | 0   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|--------|-----|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| DQ0    | OP0 |   |   |   | V |   |   |   |   |   |    |    |    |    |    |    |
| DQ1    | OP1 |   |   |   | V |   |   |   |   |   |    |    |    |    |    |    |
| DQ2    | OP2 |   |   |   | V |   |   |   |   |   |    |    |    |    |    |    |
| DQ3    | OP3 |   |   |   | V |   |   |   |   |   |    |    |    |    |    |    |
| DQ4    | OP4 |   |   |   | V |   |   |   |   |   |    |    |    |    |    |    |
| DQ5    | OP5 |   |   |   | V |   |   |   |   |   |    |    |    |    |    |    |
| DQ6    | OP6 |   |   |   | V |   |   |   |   |   |    |    |    |    |    |    |
| DQ7    | OP7 |   |   |   | V |   |   |   |   |   |    |    |    |    |    |    |
| DQ8-15 | V   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |
| DMI0-1 | V   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |

**Notes:**

1. MRR data are extended to first 4 UI's for DRAM controller to sample data easily.
2. The read pre-amble and post-amble of MRR are same as normal read.

**Notes:**

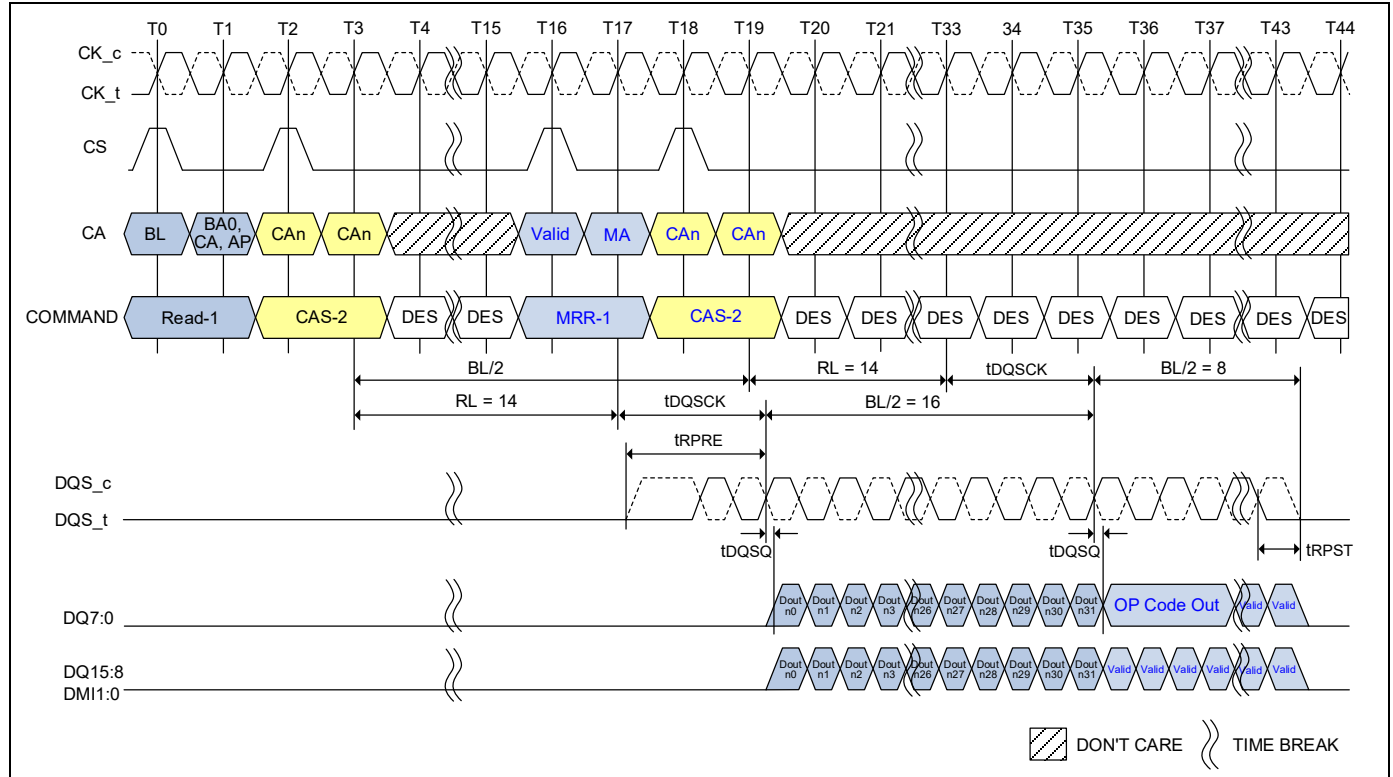
1. Only BL=16 is supported.
2. Only DES is allowed during tMRR period.
3. There are some exceptions about issuing commands after tMRR. Refer to MRR/MRW Timing Constraints Table for detail.
4. DBI is Disable mode.
5. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.
6. DQ/DQS: VSSQ termination.

**Figure 77 - Mode Register Read Operation**



#### 7.4.23.1 MRR after Read and Write command

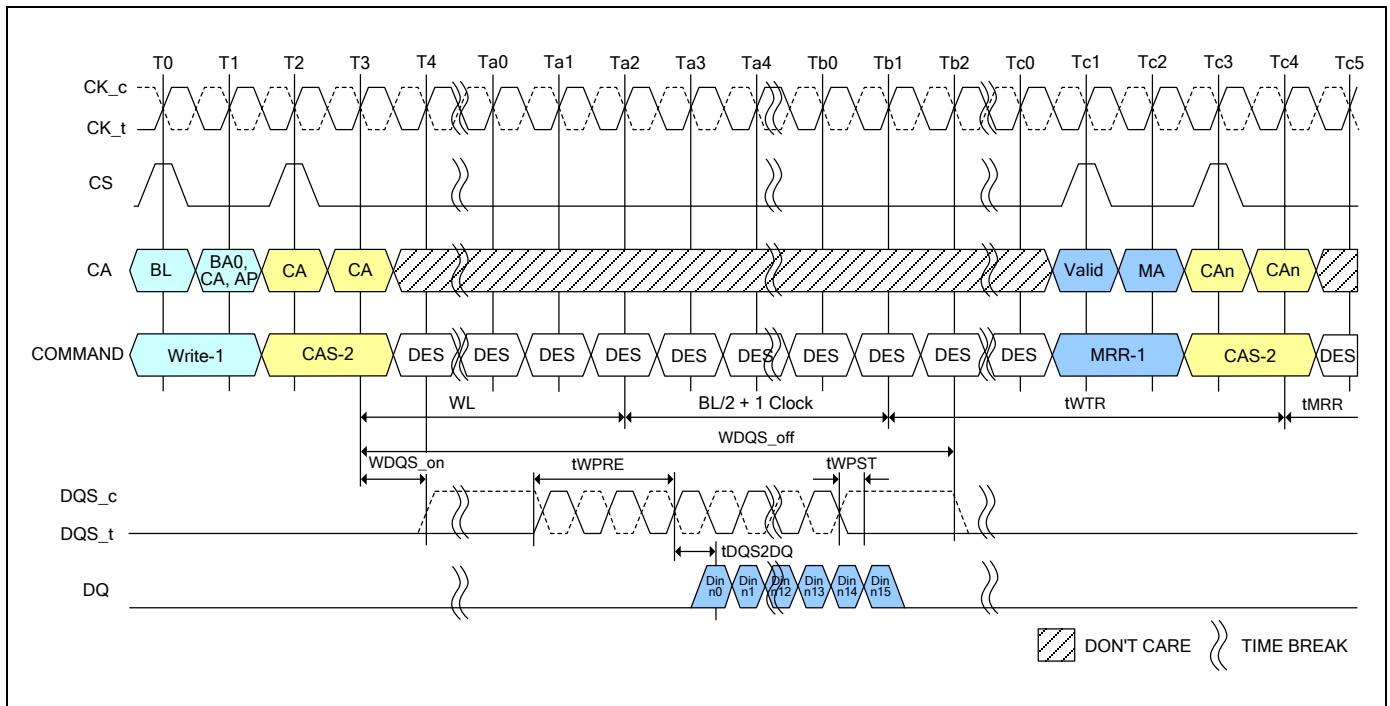
After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles, in a similar way WL + BL/2 + 1 + RU(tWTR/tCK) clock cycles after a prior Write, Write with AP, Mask Write, Mask Write with AP and MPC Write FIFO command in order to avoid the collision of Read and Write burst data on SDRAM's internal Data bus. Reference Figure 78 and Figure 79.



#### Notes:

1. The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.
2. Read BL = 32, MRR BL = 16, RL = 14, Preamble = Toggle, Postamble = 0.5nCK, DBI = Disable, DQ/DQS: VSSQ termination.
3. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

**Figure 78 - READ to MRR Timing**

**Notes:**

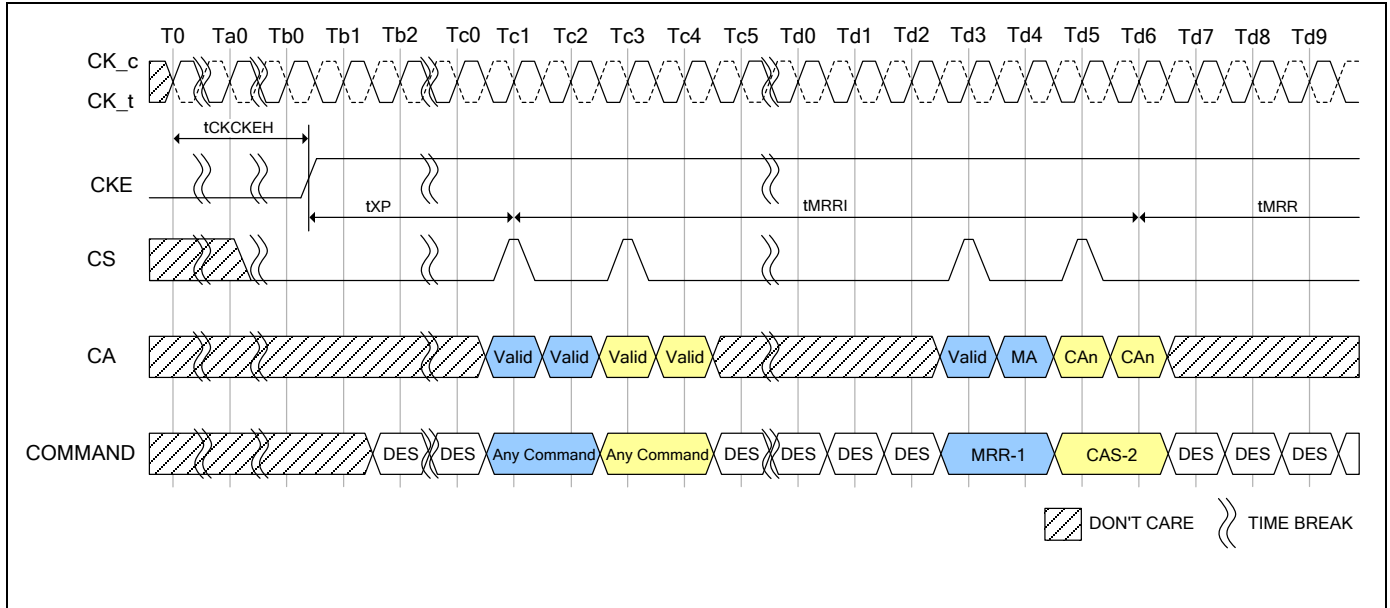
1. Write BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Only DES is allowed during tMRR period.
3. Din n = data-in to column n.
4. The minimum number of clock cycles from the burst write command to MRR command is  $WL + BL/2 + 1 + RU(tWTR/tCK)$ .
5. tWTR starts at the rising edge of CK after the last latching edge of DQS.
6. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

**Figure 79 - Write to MRR Timing**



### 7.4.23.2 MRR after Power-Down Exit

Following the power-down state, an additional time, tMRRI, is required prior to issuing the mode register read (MRR) command. This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from power down mode. Reference Figure 80 and Table 43.



#### Notes:

1. Only DES is allowed during tMRR period.
2. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

**Figure 80 - MRR Following Power-Down**

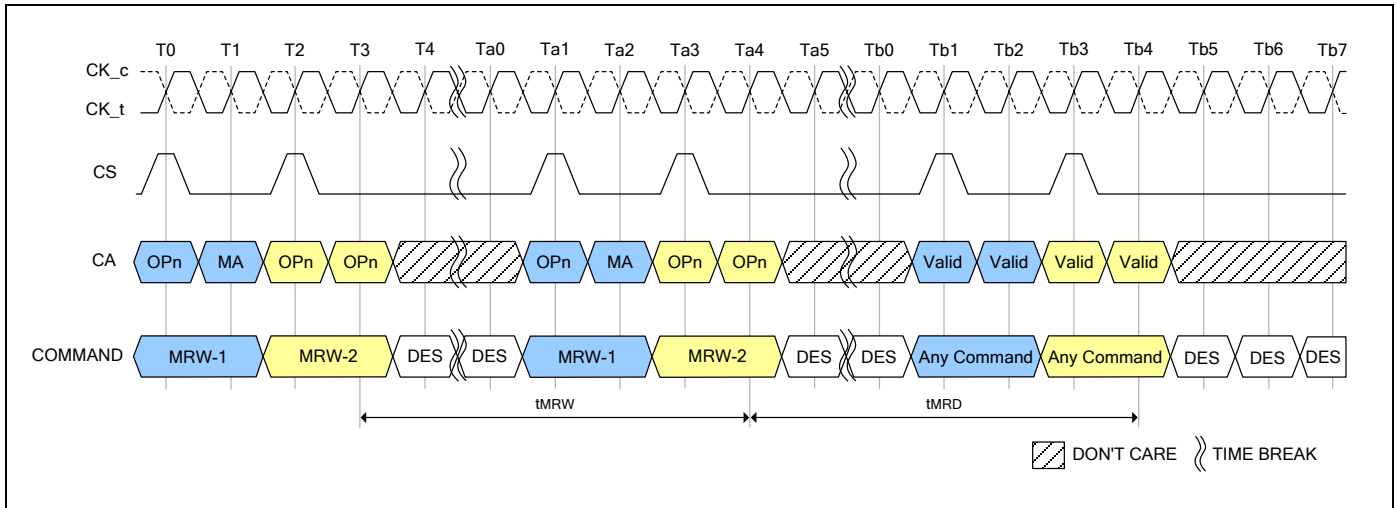
**Table 43 - Mode Register Read/Write AC timing**

| Parameter                                                             | Symbol | Min/Max | Data Rate        | Unit | Note |
|-----------------------------------------------------------------------|--------|---------|------------------|------|------|
| <b>Mode Register Read/Write Timing</b>                                |        |         |                  |      |      |
| Additional time after tXP has expired until MRR command may be issued | tMRRI  | Min     | tRCD + 3nCK      | -    |      |
| MODE REGISTER READ command period                                     | tMRR   | Min     | 8                | nCK  |      |
| MODE REGISTER WRITE command period                                    | tMRW   | Min     | Max(10nS, 10nCK) | -    |      |
| Mode register set command delay                                       | tMRD   | Min     | Max(14nS, 10nCK) | -    |      |



#### 7.4.24 Mode Register Write (MRW) Operation

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated by setting CKE, CS, and CA[5:0] to valid levels at a rising edge of the clock (See Command Truth Table, Table 87). The mode register address and the data written to the mode registers is contained in CA[5:0] according to the Command Truth Table. The MRW command period is defined by tMRW. Mode register writes to read-only registers have no impact on the functionality of the device. Reference Figure 81.



**Note:**

1. Only Deselect command is allowed during tMRW and tMRD periods.

**Figure 81 - Mode Register Write Timing**

##### 7.4.24.1 Mode Register Write

MRW can be issued from either a Bank-Idle or Bank-Active state. Certain restrictions may apply for MRW from an Active state (Reference Table 44 through Table 46).

**Table 44 - Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)**

| Current State  | Command | Intermediate State                        | Next State     |
|----------------|---------|-------------------------------------------|----------------|
| SDRAM          |         | SDRAM                                     | SDRAM          |
| All Banks Idle | MRR     | Mode Register Reading<br>(All Banks Idle) | All Banks Idle |
|                | MRW     | Mode Register Writing<br>(All Banks Idle) | All Banks Idle |
| Bank(s) Active | MRR     | Mode Register Reading                     | Bank(s) Active |
|                | MRW     | Mode Register Writing                     | Bank(s) Active |





Table 45 - MRR/MRW Timing Constraints: DQ ODT is Disable

| From Command               | To Command      | Minimum Delay between "From Command" and "To Command"                 | Unit | Notes |
|----------------------------|-----------------|-----------------------------------------------------------------------|------|-------|
| MRR                        | MRR             | tMRR                                                                  | -    |       |
|                            | RD/RDA          | tMRR                                                                  | -    |       |
|                            | WR/WRA/MWR/MWRA | $RL+RU(tDQSCK(max)/tCK)+BL/2-WL+tWPRE+RD(trPST)$                      | nCK  |       |
|                            | MRW             | $RL+RU(tDQSCK(max)/tCK)+BL/2+3$                                       | nCK  |       |
| RD/RDA                     | MRR             | BL/2                                                                  | nCK  |       |
| WR/WRA/MWR/MWRA            |                 | $WL+1+BL/2+RU(tWTR/tCK)$                                              | nCK  |       |
| MRW                        |                 | tMRD                                                                  | -    |       |
| Power Down Exit            |                 | tXP+tMRRl                                                             | -    |       |
| MRW                        | RD/RDA          | tMRD                                                                  | -    |       |
|                            | WR/WRA/MWR/MWRA | tMRD                                                                  | -    |       |
|                            | MRW             | tMRW                                                                  | -    |       |
| RD/RD FIFO/RD DQ CAL       | MRW             | $RL+BL/2+RU(tDQSCKmax/tCK)+RD(trPST)+\max(RU(7.5nS/tCK),8nCK)$        | nCK  |       |
| RD with Auto-Precharge     |                 | $RL+BL/2+RU(tDQSCKmax/tCK)+RD(trPST)+\max(RU(7.5nS/tCK),8nCK)+nRTP-8$ | nCK  |       |
| WR/MWR/WR FIFO             |                 | $WL+1+BL/2+\max(RU(7.5nS/tCK),8nCK)$                                  | nCK  |       |
| WR/MWR with Auto-Precharge |                 | $WL+1+BL/2+\max(RU(7.5nS/tCK),8nCK)+nWR$                              | nCK  |       |

Table 46 - MRR/MRW Timing Constraints: DQ ODT is Enable

| From Command               | To Command      | Minimum Delay between "From Command" and "To Command"                | Unit | Notes |
|----------------------------|-----------------|----------------------------------------------------------------------|------|-------|
| MRR                        | MRR             | Same as ODT Disable Case                                             | -    |       |
|                            | RD/RDA          |                                                                      |      |       |
|                            | WR/WRA/MWR/MWRA | $RL+RU(tDQSCK(max)/tCK)+BL/2-ODTLon-RD(tODTon(min)/tCK)+RD(trPST)+1$ | nCK  |       |
|                            | MRW             | Same as ODT Disable Case                                             | -    |       |
| RD/RDA                     | MRR             | Same as ODT Disable Case                                             | -    |       |
| WR/WRA/MWR/MWRA            |                 |                                                                      |      |       |
| MRW                        |                 |                                                                      |      |       |
| Power Down Exit            |                 |                                                                      |      |       |
| MRW                        | RD/RDA          | Same as ODT Disable Case                                             | -    |       |
|                            | WR/WRA/MWR/MWRA |                                                                      |      |       |
|                            | MRW             |                                                                      |      |       |
| RD/RD FIFO/RD DQ CAL       | MRW             | Same as ODT Disable Case                                             | -    |       |
| RD with Auto-Precharge     |                 |                                                                      |      |       |
| WR/MWR/WR FIFO             |                 |                                                                      |      |       |
| WR/MWR with Auto-Precharge |                 |                                                                      |      |       |



#### 7.4.25 VREF Current Generator (VRCG)

LPDDR4/LPDDR4X SDRAM VREF current generators (VRCG) incorporate a high current mode to reduce the settling time of the internal VREF(DQ) and VREF(CA) levels during training and when changing frequency set points during operation. The high current mode is enabled by setting MR13 OP[3] = 1. Only Deselect commands may be issued until tVRCG\_ENABLE is satisfied. tVRCG\_ENABLE timing is shown in Figure 82 and Table 47.

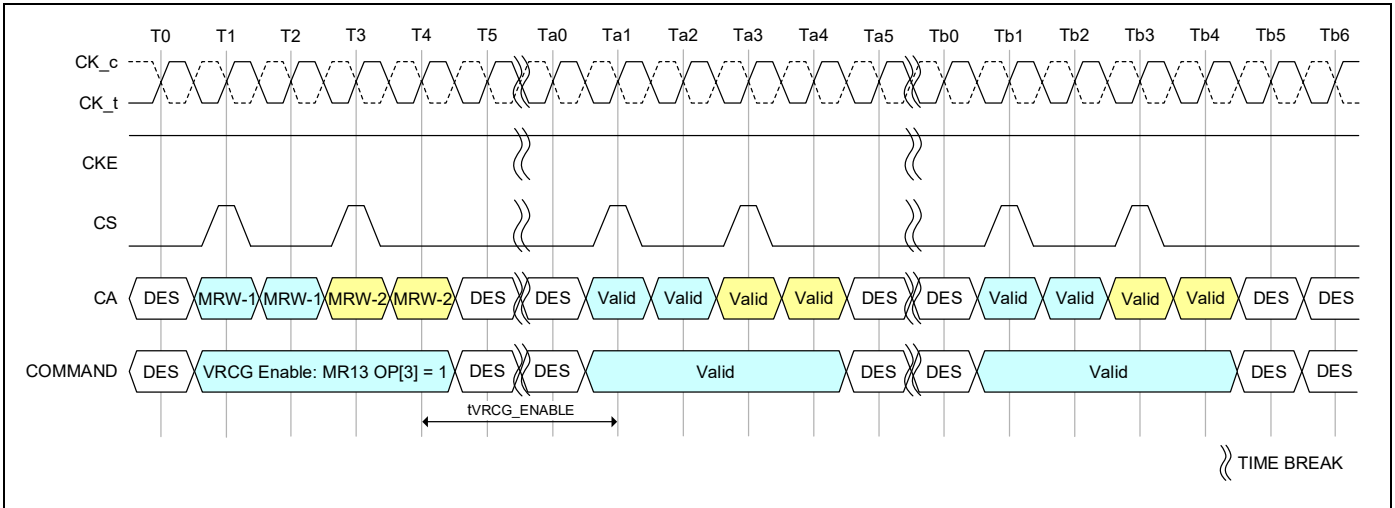


Figure 82 - VRCG Enable timing

VRCG high current mode is disabled by setting MR13 OP[3] = 0. Only Deselect commands may be issued until tVRCG\_DISABLE is satisfied. tVRCG\_DISABLE timing is shown in Figure 83 and Table 47.

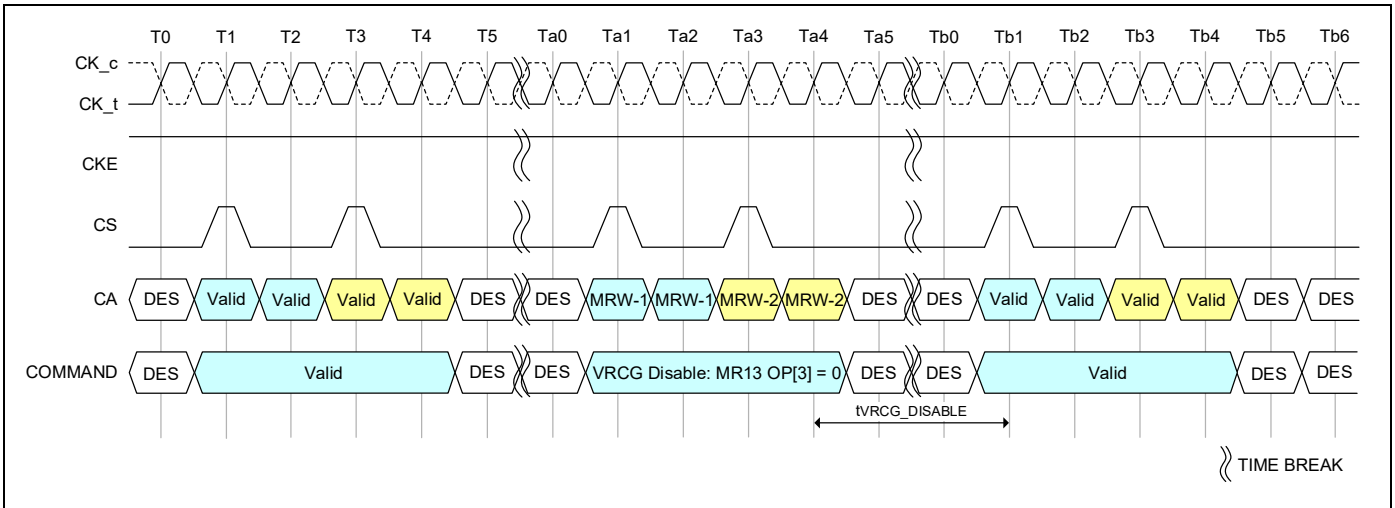


Figure 83 - VRCG Disable timing

Note that LPDDR4/LPDDR4X SDRAM devices support VREF(CA) and VREF(DQ) range and value changes without enabling VRCG high current mode.

Table 47 - VRCG Enable/Disable Timing

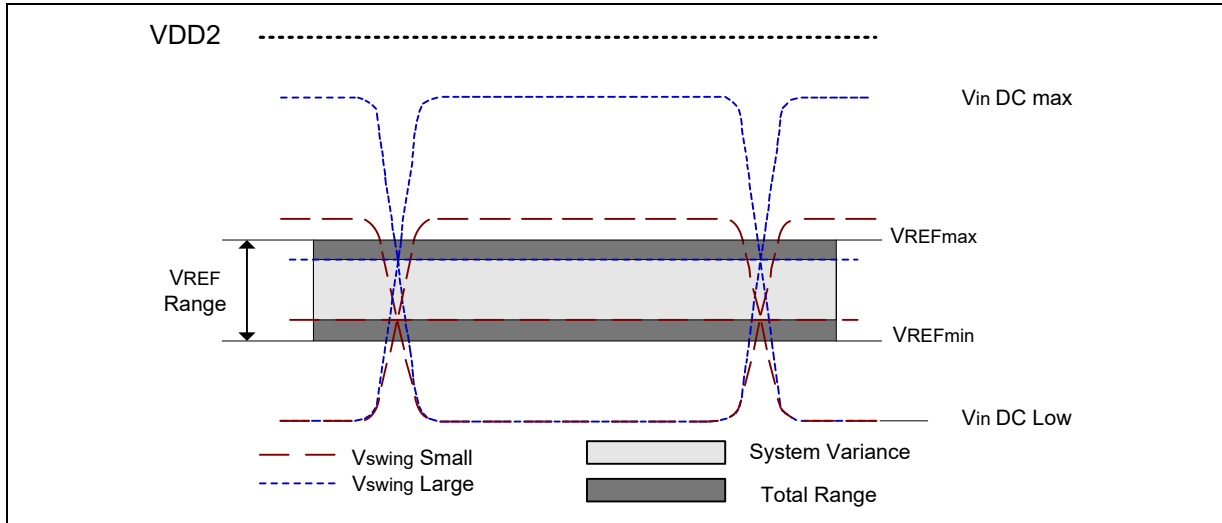
| Speed                               |               | 533, 1066, 1600, 2133, 2667, 3200, 3733, 4267 Mbps |     | Units | Note |
|-------------------------------------|---------------|----------------------------------------------------|-----|-------|------|
| Parameter                           | Symbol        | MIN                                                | MAX |       |      |
| VREF high current mode enable time  | tVRCG_ENABLE  | -                                                  | 200 | nS    |      |
| VREF high current mode disable time | tVRCG_DISABLE | -                                                  | 100 | nS    |      |



#### 7.4.26 CA VREF Training

The DRAM internal CA VREF specification parameters are voltage operating range, step size, VREF set tolerance, VREF step time and VREF valid level.

The voltage operating range specifies the minimum required VREF setting range for LPDDR4/LPDDR4X SDRAM devices. The minimum range is defined by VREFmax and VREFmin as depicted in Figure 84.

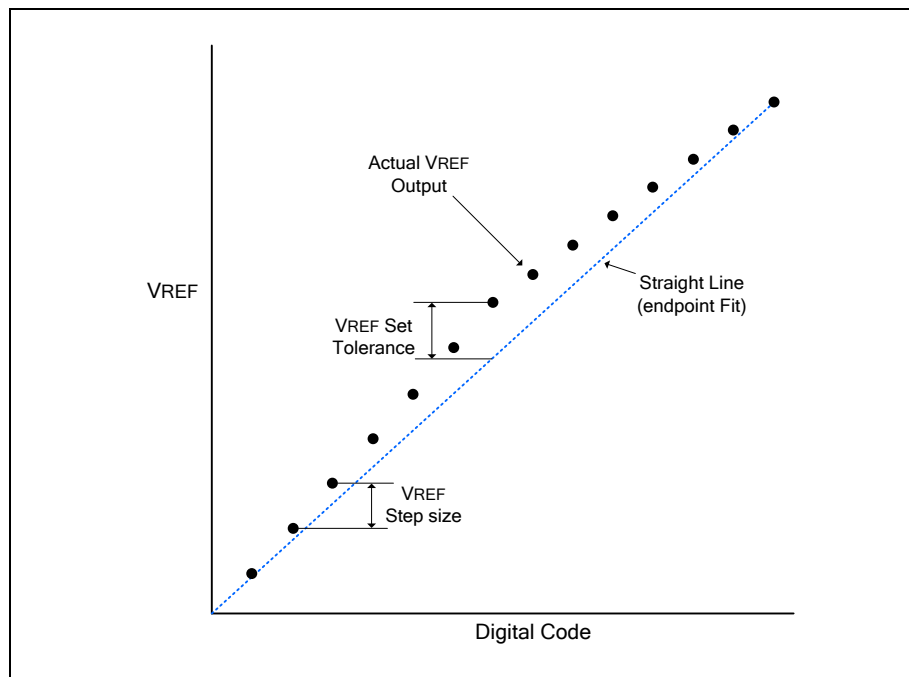


**Figure 84 – CA VREF operating range (VREFmin, VREFmax)**

The VREF step size is defined as the step size between adjacent steps. However, for a given design, DRAM has one value for VREF step size that falls within the range.

The VREF set tolerance is the variation in the VREF voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VREF set tolerance uncertainty. The range of VREF set tolerance uncertainty is a function of number of steps  $n$ .

The VREF set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max VREF values for a specified range. An example of the step size and VREF set tolerance is shown in Figure 85.



**Figure 85 - Example of VREF set tolerance (max case only shown) and step size**



The VREF increment/decrement step times are define by VREF\_time-short, Middle and long. The VREF\_time-short, VREF\_time-Middle and VREF\_time-long is defined from TS to TE as shown in Figure 86 where TE is referenced to when the VREF voltage is at the final DC level within the VREF valid tolerance(VREF\_val\_tol).

The VREF valid level is defined by VREF\_val tolerance to qualify the step time TE as shown in Figure 86.

This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VREF increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

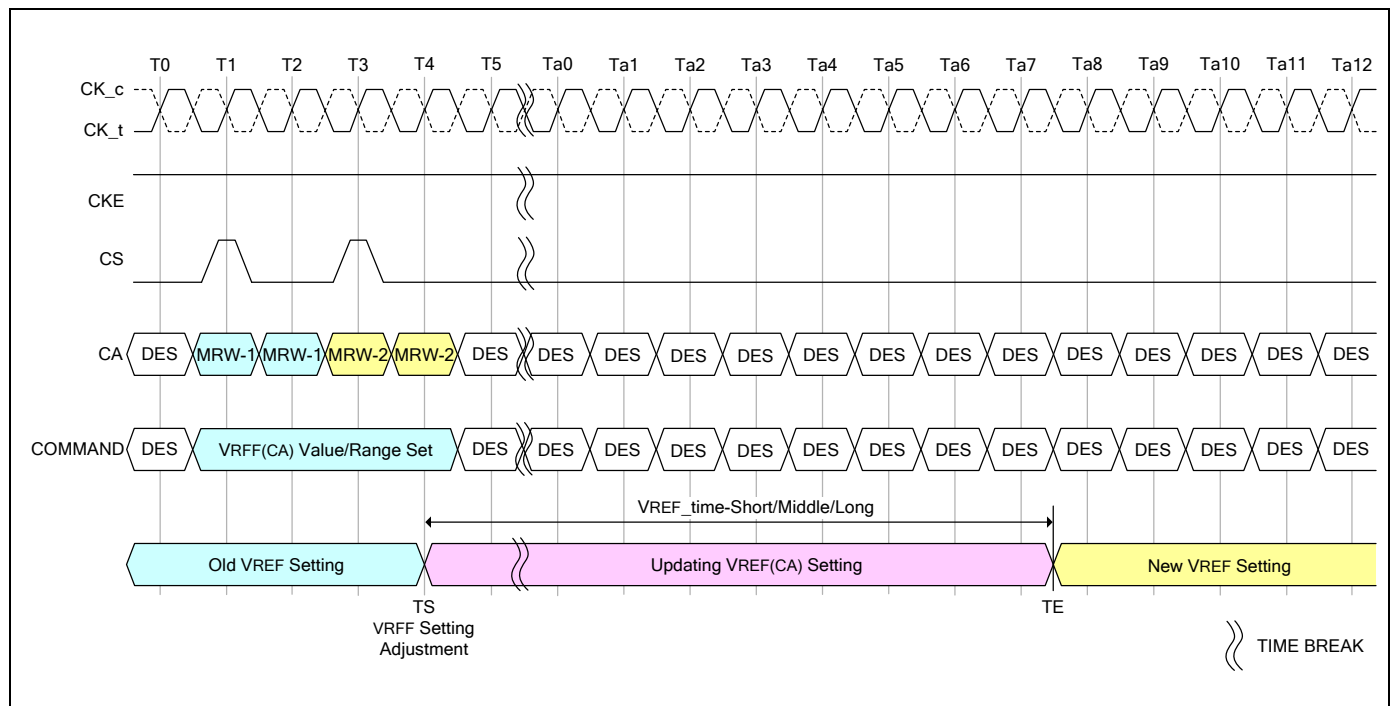
VREF\_time-Short is for a single step size increment/decrement change in VREF voltage.

VREF\_time-Middle is at least 2 step sizes increment/decrement change within the same VREFCA range in VREF voltage.

VREF\_time-Long is the time including up to VREFmin to VREFmax or VREFmax to VREFmin change across the VREFCA Range in VREF voltage.

TS - is referenced to MRS command clock

TE - is referenced to the VREF\_val\_tol



**Figure 86 - VREF\_time for Short, Middle and Long Timing Diagram**

The MRW command to the mode register bits are as follows.

MR12 OP[5:0]: VREF(CA) Setting

MR12 OP[6]: VREF(CA) Range



The minimum time required between two VREF MRS commands is VREF\_time-short for single step and VREF\_time-Middle for a full voltage range step. Reference Figure 87 through Figure 90.

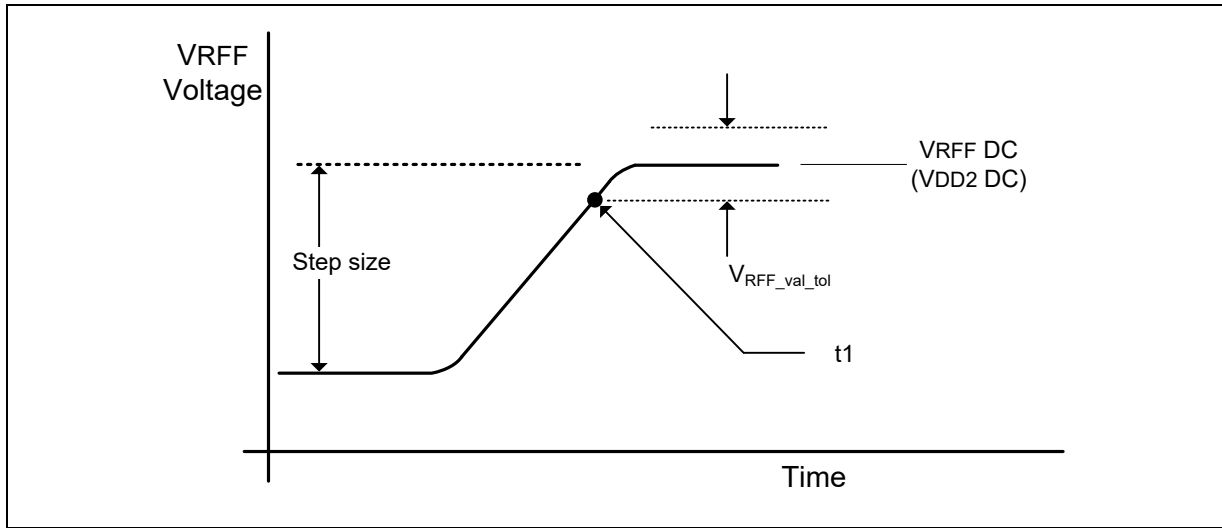


Figure 87 - VREF step single step size increment case

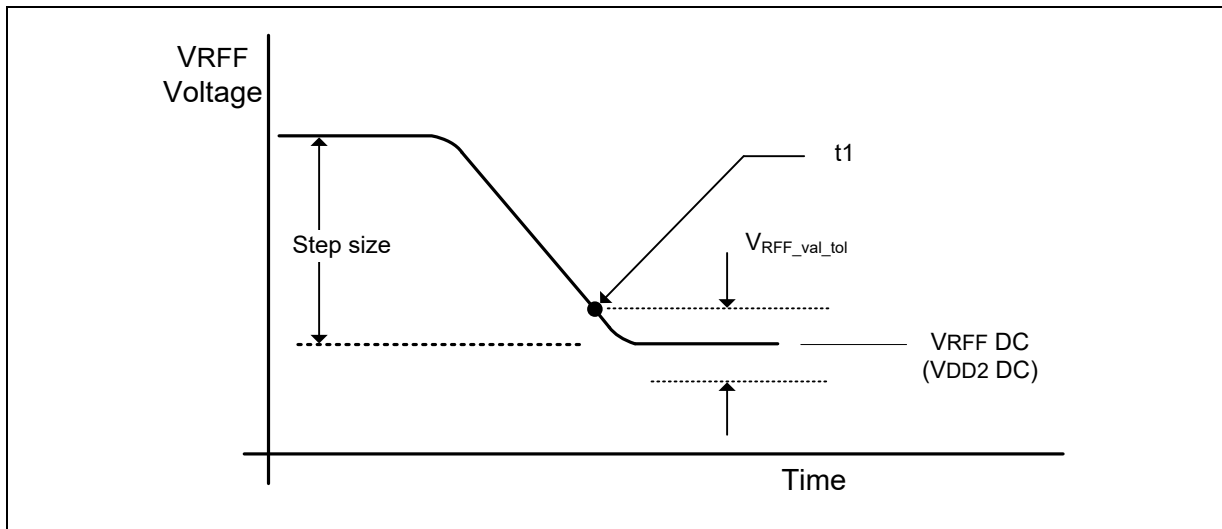


Figure 88 - VREF step single step size decrement case

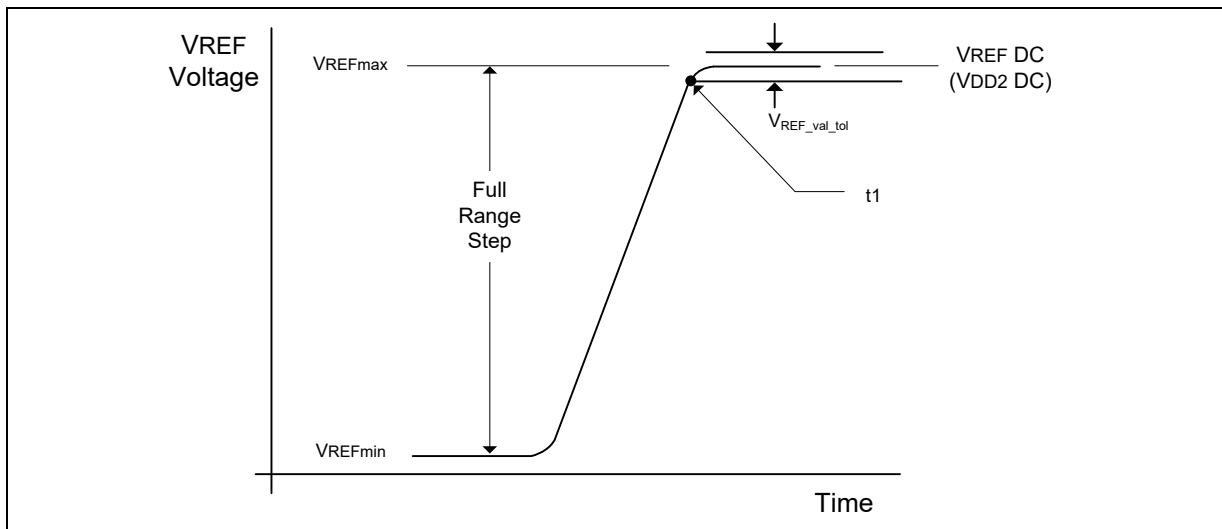


Figure 89 - VREF full step from VREFmin to VREFmax case

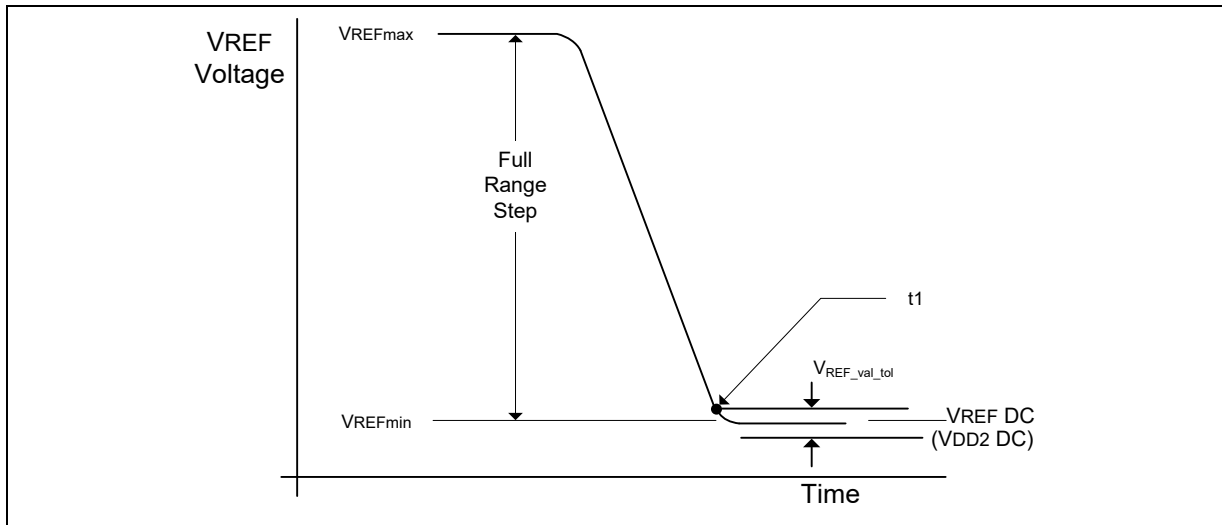


Figure 90 - VREF full step from VREFmax to VREFmin case



Table 48 contains the CA internal VREF specifications that will be characterized at the component level for compliance.

**Table 48 - CA Internal VREF Specifications for LPDDR4**

| Parameter                       | Symbol           | Min    | Typ   | Max   | Unit | Notes   |
|---------------------------------|------------------|--------|-------|-------|------|---------|
| VREF Max operating point Range0 | VREF_max_R0      | -      | -     | 30%   | VDD2 | 1, 11   |
| VREF Min operating point Range0 | VREF_min_R0      | 10%    | -     | -     | VDD2 | 1, 11   |
| VREF Max operating point Range1 | VREF_max_R1      | -      | -     | 42%   | VDD2 | 1, 11   |
| VREF Min operating point Range1 | VREF_min_R1      | 22%    | -     | -     | VDD2 | 1, 11   |
| VREF Step size                  | VREF_step        | 0.30%  | 0.40% | 0.50% | VDD2 | 2       |
| VREF Set Tolerance              | VREF_set_tol     | -1.00% | 0.00% | 1.00% | VDD2 | 3, 4, 6 |
|                                 |                  | -0.10% | 0.00% | 0.10% | VDD2 | 3, 5, 7 |
| VREF Step Time                  | VREF_time-Short  | -      | -     | 100   | nS   | 8       |
|                                 | VREF_time_Middle | -      | -     | 200   | nS   | 12      |
|                                 | VREF_time-Long   | -      | -     | 250   | nS   | 9       |
|                                 | VREF_time_weak   | -      | -     | 1     | mS   | 13, 14  |
| VREF Valid tolerance            | VREF_val_tol     | -0.10% | 0.00% | 0.10% | VDD2 | 10      |

**Notes:**

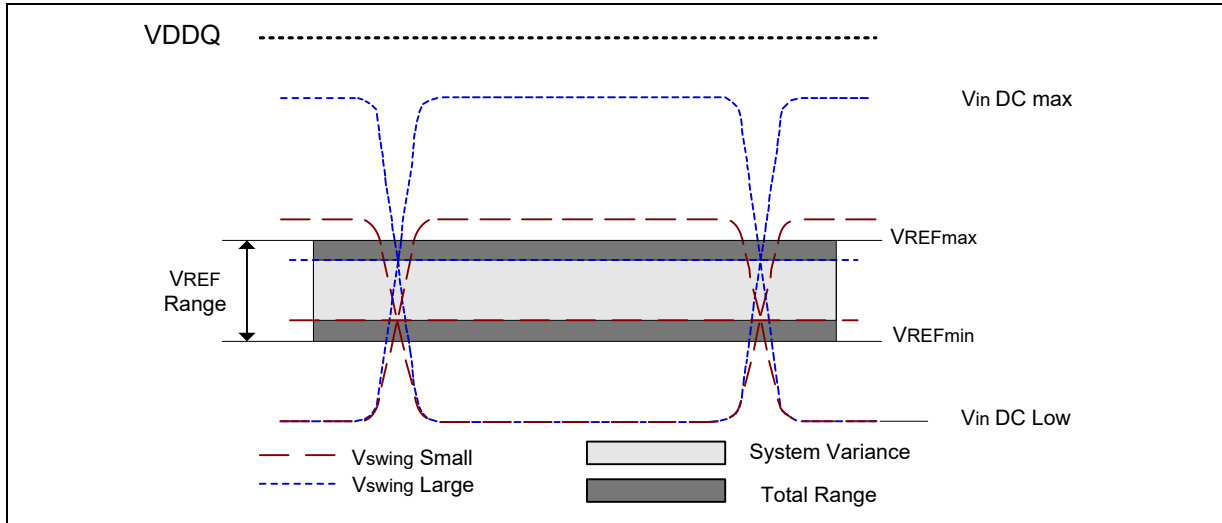
- VREF DC voltage referenced to VDD2\_DC.
- VREF step size increment/decrement range. VREF at DC level.
- $VREF\_new = VREF\_old + n \cdot VREF\_step$ ; n= number of steps; if increment use "+"; If decrement use "-".
- The minimum value of VREF setting tolerance =  $VREF\_new - 1.0\% \cdot VDD2$ . The maximum value of VREF setting tolerance =  $VREF\_new + 1.0\% \cdot VDD2$ . For  $n > 4$ .
- The minimum value of VREF setting tolerance =  $VREF\_new - 0.10\% \cdot VDD2$ . The maximum value of VREF setting tolerance =  $VREF\_new + 0.10\% \cdot VDD2$ . For  $n \leq 4$ .
- Measured by recording the min and max values of the VREF output over the range, drawing a straight line between those points and comparing all other VREF output settings to that line.
- Measured by recording the min and max values of the VREF output across 4 consecutive steps ( $n=4$ ), drawing a straight line between those points and comparing all other VREF output settings to that line.
- Time from MRS command to increment or decrement one step size for VREF.
- Time from MRS command to increment or decrement VREFmin to VREFmax or VREFmax to VREFmin change across the VREFCA Range in VREF voltage.
- Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VREF valid is to qualify the step times which will be characterized at the component level.
- DRAM range 0 or 1 set by MR12 OP[6].
- Time from MRS command to increment or decrement more than one step size up to a full range of VREF voltage within the same VREFCA range.
- Applies when VRCG high current mode is not enabled, specified by MR13 OP[3] = 0.
- VREF\_time\_weak covers all VREF(CA) Range and Value change conditions are applied to VREF\_time\_Short/Middle/Long.



#### 7.4.27 DQ VREF Training

The DRAM internal DQ VREF specification parameters are voltage operating range, step size, VREF set tolerance, VREF step time and VREF valid level.

The voltage operating range specifies the minimum required VREF setting range for LPDDR4/LPDDR4X SDRAM devices. The minimum range is defined by VREFmax and VREFmin as depicted in Figure 91.

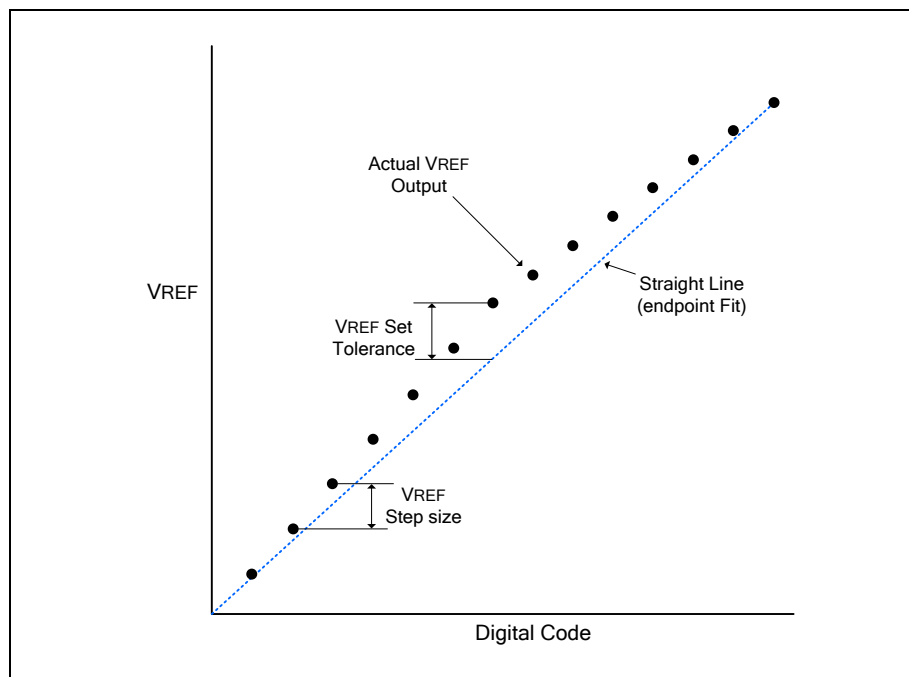


**Figure 91 – DQ VREF operating range (VREFmin, VREFmax)**

The VREF step size is defined as the step size between adjacent steps. However, for a given design, DRAM has one value for VREF step size that falls within the range.

The VREF set tolerance is the variation in the VREF voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VREF set tolerance uncertainty. The range of VREF set tolerance uncertainty is a function of number of steps  $n$ .

The VREF set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max VREF values for a specified range. An example of the step size and VREF set tolerance is shown in Figure 92.



**Figure 92 - Example of VREF set tolerance (max case only shown) and step size**





The VREF increment/decrement step times are define by VREF\_time-short, Middle and long. The VREF\_time-short, VREF\_time-Middle and VREF\_time-long is defined from TS to TE as shown in Figure 93 where TE is referenced to when the VREF voltage is at the final DC level within the VREF valid tolerance(VREF\_val\_tol).

The VREF valid level is defined by VREF\_val tolerance to qualify the step time TE as shown in Figure 93.

This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VREF increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

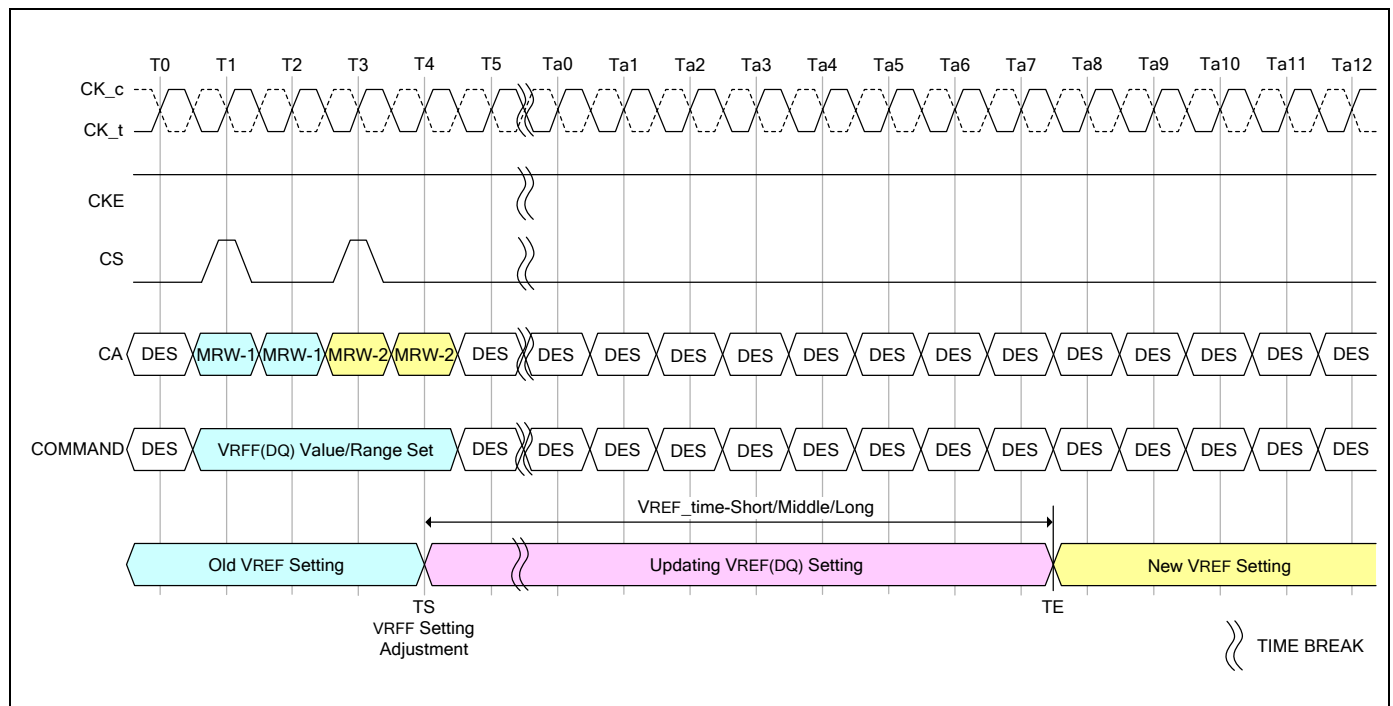
VREF\_time-Short is for a single step size increment/decrement change in VREF voltage.

VREF\_time-Middle is at least 2 step sizes increment/decrement change within the same VREFDQ range in VREF voltage.

VREF\_time-Long is the time including up to VREFmin to VREFmax or VREFmax to VREFmin change across the VREFDQ Range in VREF voltage.

TS - is referenced to MRS command clock

TE - is referenced to the VREF\_val\_tol



**Figure 93 - VREF\_time for Short, Middle and Long Timing Diagram**

The MRW command to the mode register bits are as follows.

MR14 OP[5:0]: VREF(DQ) Setting

MR14 OP[6]: VREF(DQ) Range



The minimum time required between two VREF MRS commands is VREF\_time-short for single step and VREF\_time-Middle for a full voltage range step. Reference Figure 94 through Figure 97.

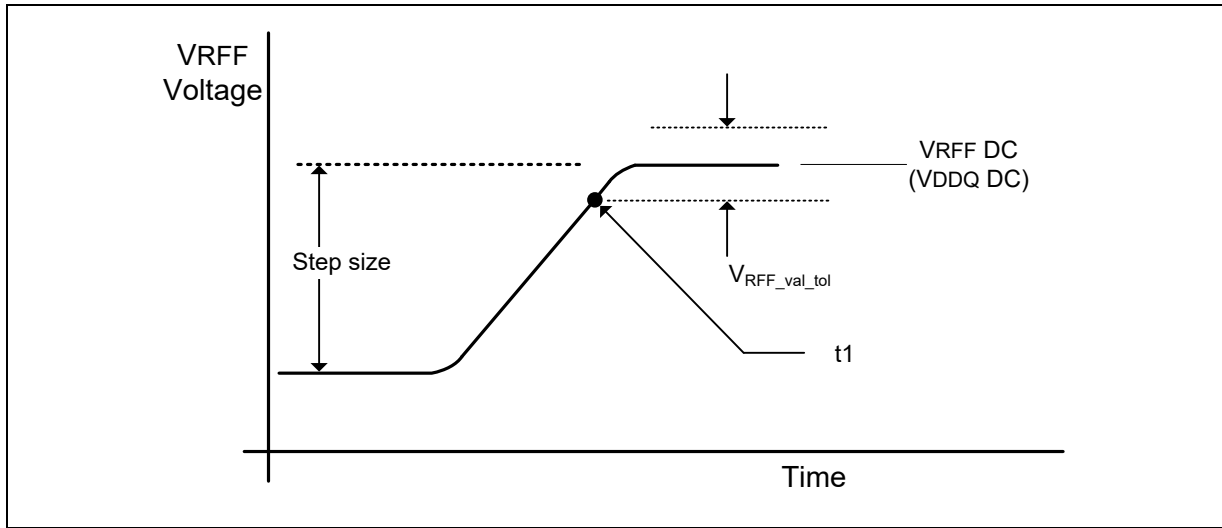


Figure 94 - VREF step single step size increment case

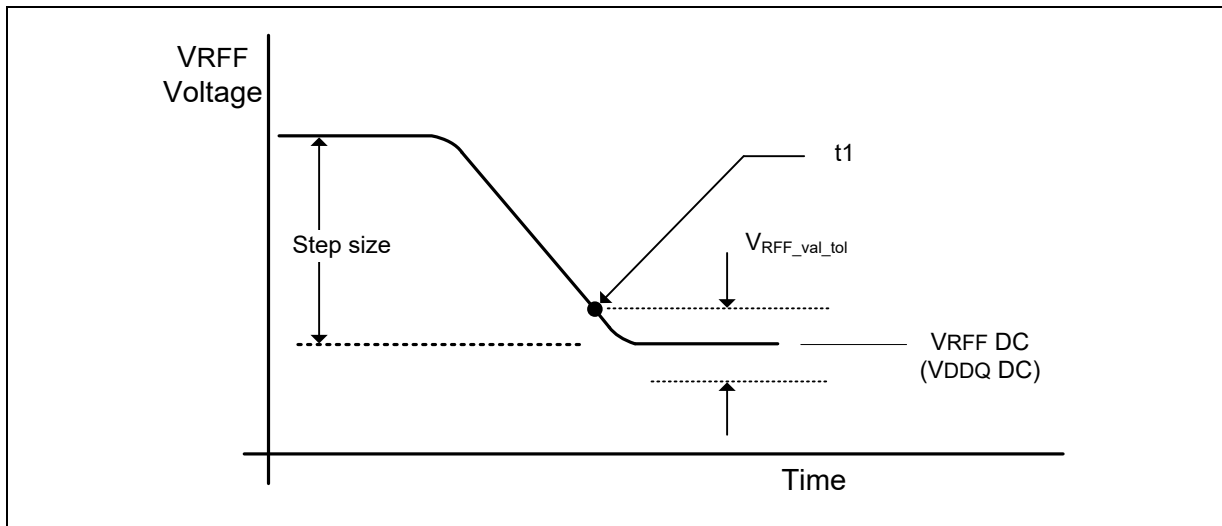


Figure 95 - VREF step single step size decrement case

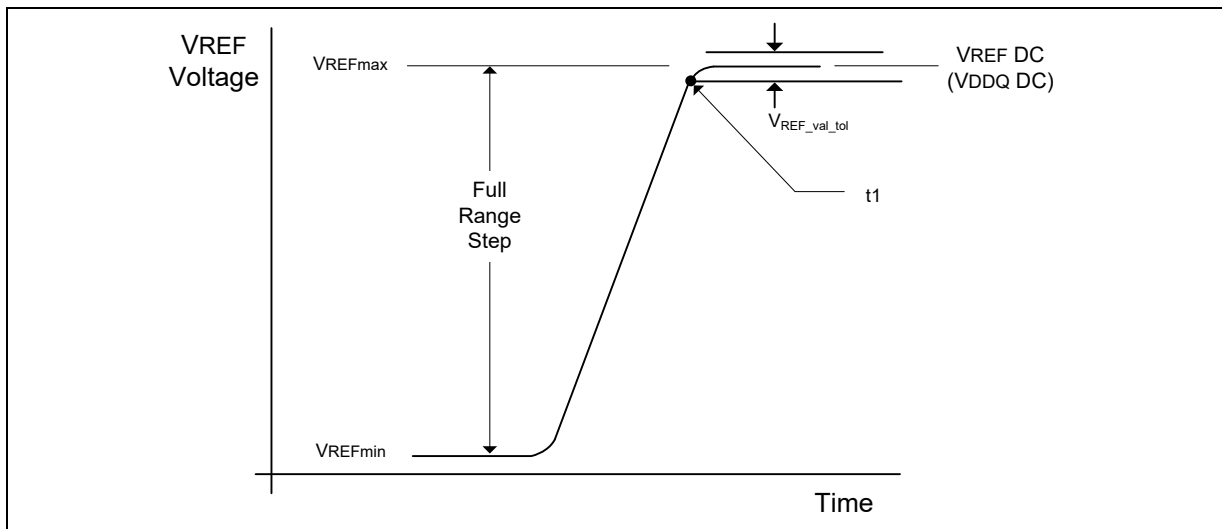


Figure 96 - VREF full step from VREFmin to VREFmax case

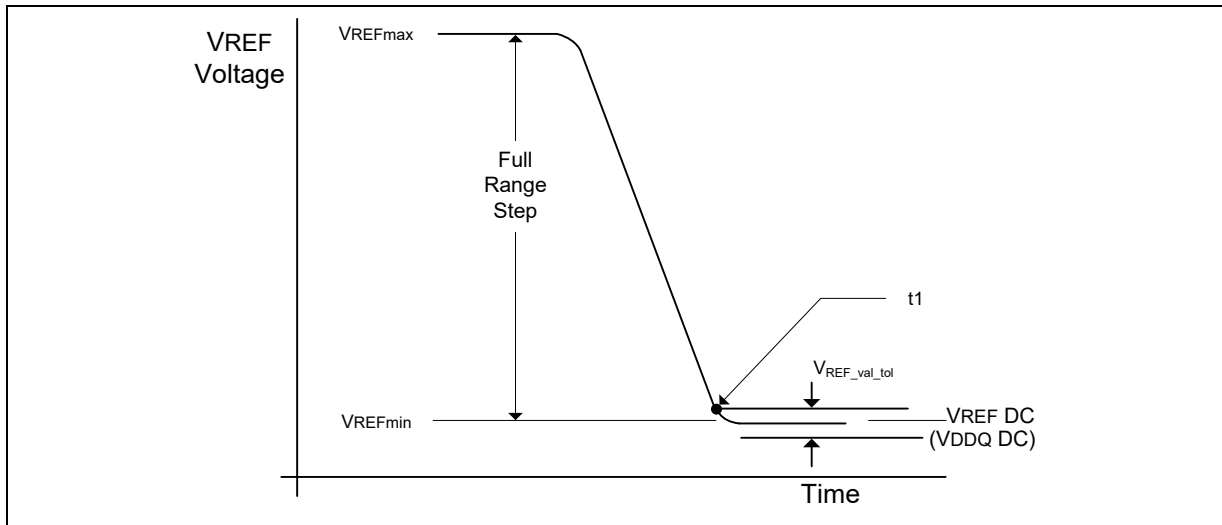


Figure 97 - VREF full step from VREFmax to VREFmin case



Table 49 contains the DQ internal VREF specifications that will be characterized at the component level for compliance.

**Table 49 - DQ Internal VREF Specifications for LPDDR4**

| Parameter                       | Symbol           | Min    | Typ   | Max   | Unit | Notes   |
|---------------------------------|------------------|--------|-------|-------|------|---------|
| VREF Max operating point Range0 | VREF_max_R0      | -      | -     | 30%   | VDDQ | 1, 11   |
| VREF Min operating point Range0 | VREF_min_R0      | 10%    | -     | -     | VDDQ | 1, 11   |
| VREF Max operating point Range1 | VREF_max_R1      | -      | -     | 42%   | VDDQ | 1, 11   |
| VREF Min operating point Range1 | VREF_min_R1      | 22%    | -     | -     | VDDQ | 1, 11   |
| VREF Step size                  | VREF Step        | 0.30%  | 0.40% | 0.50% | VDDQ | 2       |
| VREF Set Tolerance              | VREF_set_tol     | -1.00% | 0.00% | 1.00% | VDDQ | 3, 4, 6 |
|                                 |                  | -0.10% | 0.00% | 0.10% | VDDQ | 3, 5, 7 |
| VREF Step Time                  | VREF_time-Short  | -      | -     | 100   | nS   | 8       |
|                                 | VREF_time_Middle | -      | -     | 200   | nS   | 12      |
|                                 | VREF_time-Long   | -      | -     | 250   | nS   | 9       |
|                                 | VREF_time_weak   | -      | -     | 1     | mS   | 13, 14  |
| VREF Valid tolerance            | VREF_val_tol     | -0.10% | 0.00% | 0.10% | VDDQ | 10      |

**Notes:**

- VREF DC voltage referenced to VDDQ\_DC.
- VREF step size increment/decrement range. VREF at DC level.
- $VREF\_new = VREF\_old + n \cdot VREF\_step$ ; n= number of steps; if increment use "+"; If decrement use "-".
- The minimum value of VREF setting tolerance =  $VREF\_new - 1.0\% \cdot VDDQ$ . The maximum value of VREF setting tolerance =  $VREF\_new + 1.0\% \cdot VDDQ$ . For  $n > 4$ .
- The minimum value of VREF setting tolerance =  $VREF\_new - 0.10\% \cdot VDDQ$ . The maximum value of VREF setting tolerance =  $VREF\_new + 0.10\% \cdot VDDQ$ . For  $n \leq 4$ .
- Measured by recording the min and max values of the VREF output over the range, drawing a straight line between those points and comparing all other VREF output settings to that line.
- Measured by recording the min and max values of the VREF output across 4 consecutive steps ( $n=4$ ), drawing a straight line between those points and comparing all other VREF output settings to that line.
- Time from MRS command to increment or decrement one step size for VREF.
- Time from MRS command to increment or decrement VREFmin to VREFmax or VREFmax to VREFmin change across the VREFDQ Range in VREF voltage.
- Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VREF valid is to qualify the step times which will be characterized at the component level.
- DRAM range 0 or 1 set by MR14 OP[6].
- Time from MRS command to increment or decrement more than one step size up to a full range of VREF voltage within the same VREFDQ range.
- Applies when VRCG high current mode is not enabled, specified by MR13 OP[3] = 0.
- VREF\_time\_weak covers all VREF(DQ) Range and Value change conditions are applied to VREF\_time\_Short/Middle/Long.



### 7.4.28 Command Bus Training

The LPDDR4/LPDDR4X SDRAM command bus must be trained before enabling termination for high-frequency operation. LPDDR4/LPDDR4X provides an internal VREF(CA) that defaults to a level suitable for un-terminated, low frequency operation, but the VREF(CA) must be trained to achieve suitable receiver voltage margin for terminated, high-frequency operation. The training mode described here centers the internal VREF(CA) in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements. Because it can be difficult to capture commands prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the Command Bus Training mode.

**NOTE:** It is up to the system designer to determine what constitutes “low-frequency” and “high-frequency” based on the capabilities of the system. Low-frequency should then be defined as an operating frequency in which the system can reliably communicate with the SDRAM before Command Bus Training is executed.

The LPDDR4/LPDDR4X SDRAM die has a bond pad (ODT\_CA) for multi-rank operation. In a multi-rank system, the terminating rank should be trained first, followed by the non-terminating rank(s). See section 7.4.41, ODT for more information.

The LPDDR4/LPDDR4X SDRAM uses Frequency Set-Points to enable multiple operating settings for the die. The LPDDR4/LPDDR4X SDRAM defaults to FSP-OP[0] at power-up, which has the default settings to operate in unterminated, low-frequency environments. Prior to training, the mode register settings should be configured by setting MR13 OP[6]=1<sub>b</sub> (FSP-WR[1]) and setting all other mode register bits for FSP-OP[1] to the desired settings for high-frequency operation. Prior to entering Command Bus Training, the SDRAM will be operating from FSP-OP[x]. Upon Command Bus Training entry when CKE is driven LOW, the LPDDR4/LPDDR4X SDRAM will automatically switch to the alternate FSP register set (FSP-OP[y]) and use the alternate register settings during training (See note 6 in Figure 98 for more information on FSP-OP register sets). Upon training exit when CKE is driven HIGH, the LPDDR4/LPDDR4X SDRAM will automatically switch back to the original FSP register set (FSP-OP[x]), returning to the “known-good” state that was operating prior to training. The training values for VREF(CA) are not retained by the SDRAM in FSP-OP[y] registers, and must be written to the registers after training exit.

1. To enter Command Bus Training mode, issue a MRW-1 command followed by a MRW-2 command to set MR13 OP[0]=1<sub>b</sub> (Command Bus Training Mode Enabled).
2. After time tMRD, CKE may be set LOW, causing the LPDDR4/LPDDR4X SDRAM to switch from FSP-OP[x] to FSP-OP[y], and completing the entry into Command Bus Training mode.

A status of DQS<sub>t</sub>, DQS<sub>c</sub>, DQ and DMI are as follows, and ODT state of DQS<sub>t</sub>, DQS<sub>c</sub>, DQ and DMI will be followed by MR11 OP[2:0]: DQ ODT and MR13 OP[7]: FSP-OP except output pins.

- DQS<sub>t</sub>[0], DQS<sub>c</sub>[0] become input pins for capturing DQ[6:0] levels by its toggling.
- DQ[5:0] become input pins for setting VREF(CA) Level.
- DQ[6] becomes input pin for setting VREF(CA) Range.
- DQ[7] and DMI[0] become input pins and their input level is Valid level or floating, either way is fine.
- DQ[13:8] become output pins to feedback its capturing value via command bus by CS signal.
- DQS<sub>t</sub>[1], DQS<sub>c</sub>[1], DMI[1] and DQ[15:14] become output pins or disable, it means that SDRAM may drive to a valid level or left floating.

3. At time tCAENT later, LPDDR4/LPDDR4X SDRAM can accept to change its VREF(CA) Range and Value using input signals of DQS<sub>t</sub>[0], DQS<sub>c</sub>[0] and DQ[6:0] from existing value that's setting via MR12 OP[6:0]. The mapping between MR12 OP code and DQs is shown in Table 50. At least one VREFCA setting is required before proceed to next training steps.



Table 50 - Mapping of MR12 OP Code and DQ Numbers

|              | Mapping |     |     |     |     |     |     |
|--------------|---------|-----|-----|-----|-----|-----|-----|
| MR12 OP Code | OP6     | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
| DQ Number    | DQ6     | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 |

- The new VREF(CA) value must “settle” for time tVREF\_LONG before attempting to latch CA information.
- To verify that the receiver has the correct VREF(CA) setting and to further train the CA eye relative to clock (CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.
- To exit Command Bus Training mode, drive CKE HIGH, and after time tVREF\_LONG issue the MRW-1 command followed by the MRW-2 command to set MR13 OP[0]=0<sub>b</sub>. After time tMRW the LPDDR4/LPDDR4X SDRAM is ready for normal operation. After training exit the LPDDR4/LPDDR4X SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training.

Command Bus Training may be executed from IDLE or Self Refresh states. When executing CBT within the Self Refresh state, the SDRAM must not be a power down state (i.e., CKE must be HIGH prior to training entry). Command Bus Training entry and exit is the same, regardless of the SDRAM state from which CBT is initiated.

#### 7.4.28.1 Training Sequence for single-rank systems

Note that an example shown here is assuming an initial low-frequency, no-terminating operating point, training a high-frequency, terminating operating point. **The green text is low-frequency, magenta text is high-frequency.** Any operating point may be trained from any known good operating point.

- Set MR13 OP[6]=1<sub>b</sub> to enable writing to Frequency Set Point ‘y’ (FSP-WR[y]) (or FSP-OP[x], See Note).
- Write FSP-WR[y] (or FSP-WR[x]) registers for all channels to set up high-frequency operating parameters.
- Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode.
- Drive CKE LOW, and change CK frequency to the high-frequency operating point.
- Perform Command Bus Training (VREFCA, CS, and CA).
- Exit training, a change CK frequency to the low-frequency operating point prior to driving CKE HIGH, then issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the high frequency operating point. At this point the Command Bus is trained and you may proceed to other training or normal operation.

#### 7.4.28.2 Training Sequence for multi-rank systems

Note that an example shown here is assuming an initial low-frequency operating point, training a high-frequency operating point. **The green text is low-frequency, magenta text is high-frequency.** Any operating point may be trained from any known good operating point.

- Set MR13 OP[6]=1<sub>b</sub> to enable writing to Frequency Set Point ‘y’ (FSP-WR[y]) (or FSP-OP[x], See Note).
- Write FSP-WR[y] (or FSP-WR[x]) registers for all channels and ranks to set up high frequency operating parameters.
- Read MR0 OP[7] on all channels and ranks to determine which die are terminating, signified by MR0 OP[7]=1<sub>b</sub>.
- Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode on the terminating rank.



5. Drive CKE LOW on the terminating rank (or all ranks), and change CK frequency to the high-frequency operating point.
6. Perform Command Bus Training on the terminating rank (VREFCA, CS, and CA).
7. Exit training by driving CKE HIGH, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands to write the trained values to FSP-WR[y] (or FSP-WR[x]). When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
8. Issue MRW-1 and MRW-2 command to enter training mode on the non-terminating rank (but keep CKE HIGH)
9. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the high frequency operating point.
10. Drive CKE LOW on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[y] (or FSP-OP[x]).
11. Perform Command Bus Training on the non-terminating rank (VREFCA, CS, and CA).
12. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[x] (or FSP-OP[y]) to turn off termination.
13. Exit training by driving CKE HIGH on the non-terminating rank, change CK frequency to the low frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
14. Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
15. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the high frequency operating point. At this point the Command Bus is trained for both ranks and you may proceed to other training or normal operation.

#### 7.4.28.3 Relation between CA input pin DQ output pin

The relation between CA input pin DQ output pin is shown in Table 51.

**Table 51 - Mapping of CA Input pin and DQ Output pin**

|           | Mapping |      |      |      |     |     |
|-----------|---------|------|------|------|-----|-----|
| CA Number | CA5     | CA4  | CA3  | CA2  | CA1 | CA0 |
| DQ Number | DQ13    | DQ12 | DQ11 | DQ10 | DQ9 | DQ8 |

#### 7.4.28.4 Timing Diagram

The basic Timing diagrams of Command Bus Training are shown in Figure 98 through Figure 101.



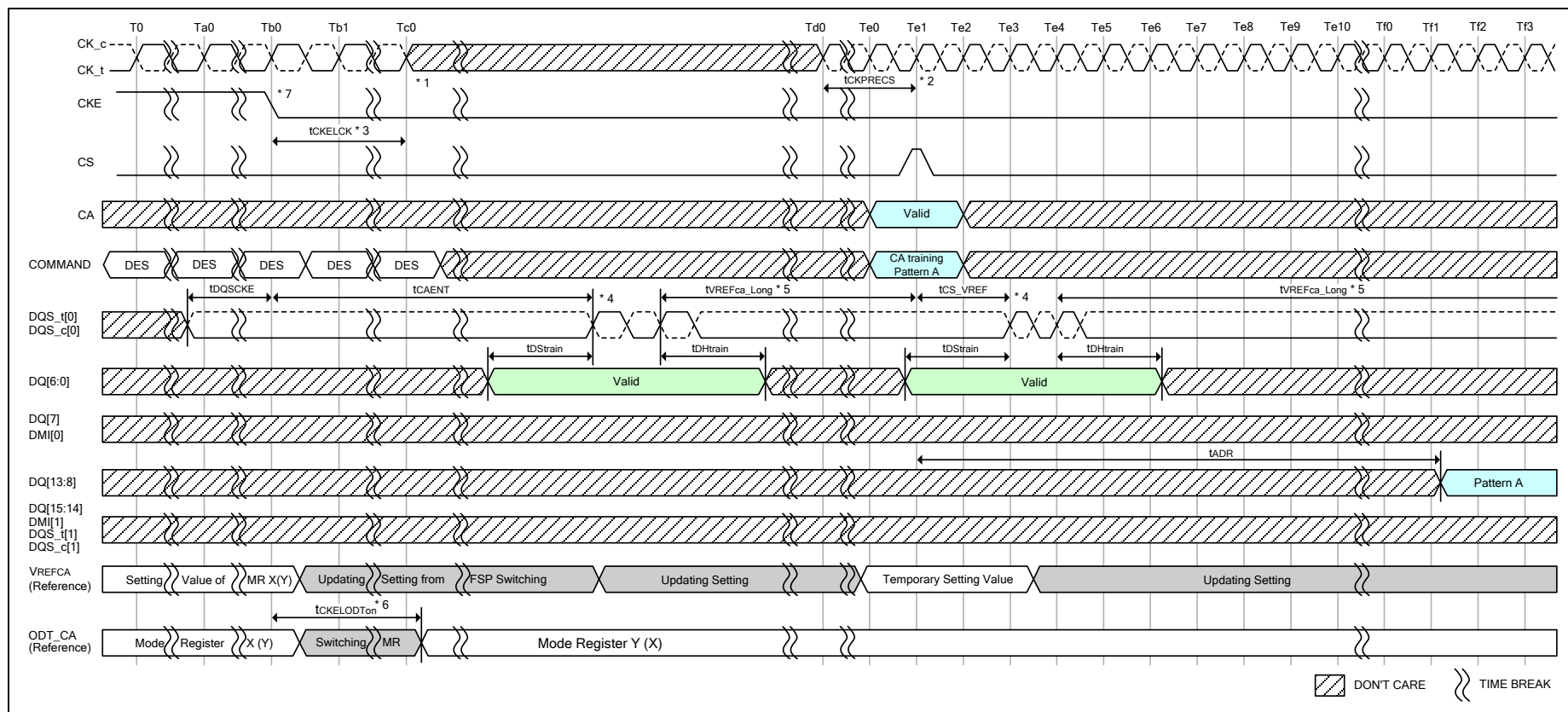


1. After tCKELCK clock can be stopped or frequency changed any time.
2. The input clock condition should be satisfied tCKPRECS and tCKPSTCS.
3. Continue to Drive CK and Hold CS pins low until tCKELCK after CKE is low (which disables command decoding).
4. DRAM may or may not capture first rising/falling edge of DQS\_t/c due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal at capturing DQ[6:0] signals. The captured value of DQ[6:0] signal level by each DQS edges are overwritten at any time and the DRAM updates its VREFCA setting of MR12 temporary after time tVREFca\_Long.
5. tVREF\_LONG may be reduced to tVREF\_SHORT if the following conditions are met: 1) The new VREF setting is a single step above or below the old VREF setting, and 2) The DQS pulses a single time, or the new VREF setting value on DQ[6:0] is static and meets tDStrain/tDHtrain for every DQS pulse applied.
6. When CKE is driven low, the SDRAM will switch its FSP-OP registers to use the alternate (*i.e.*, non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT\_CA disabled then termination will not enable in CA Bus Training mode. If the ODT\_CA pad is bonded to VSS, ODT\_CA termination will never enable for that die.
7. When CKE is driven low in Command Bus Training mode, the LPDDR4/LPDDR4X SDRAM will change operation to the alternate FSP, *i.e.*, the inverse of the FSP programmed in the FSP-OP mode register.

Publication Release Date: Dec. 30, 2024

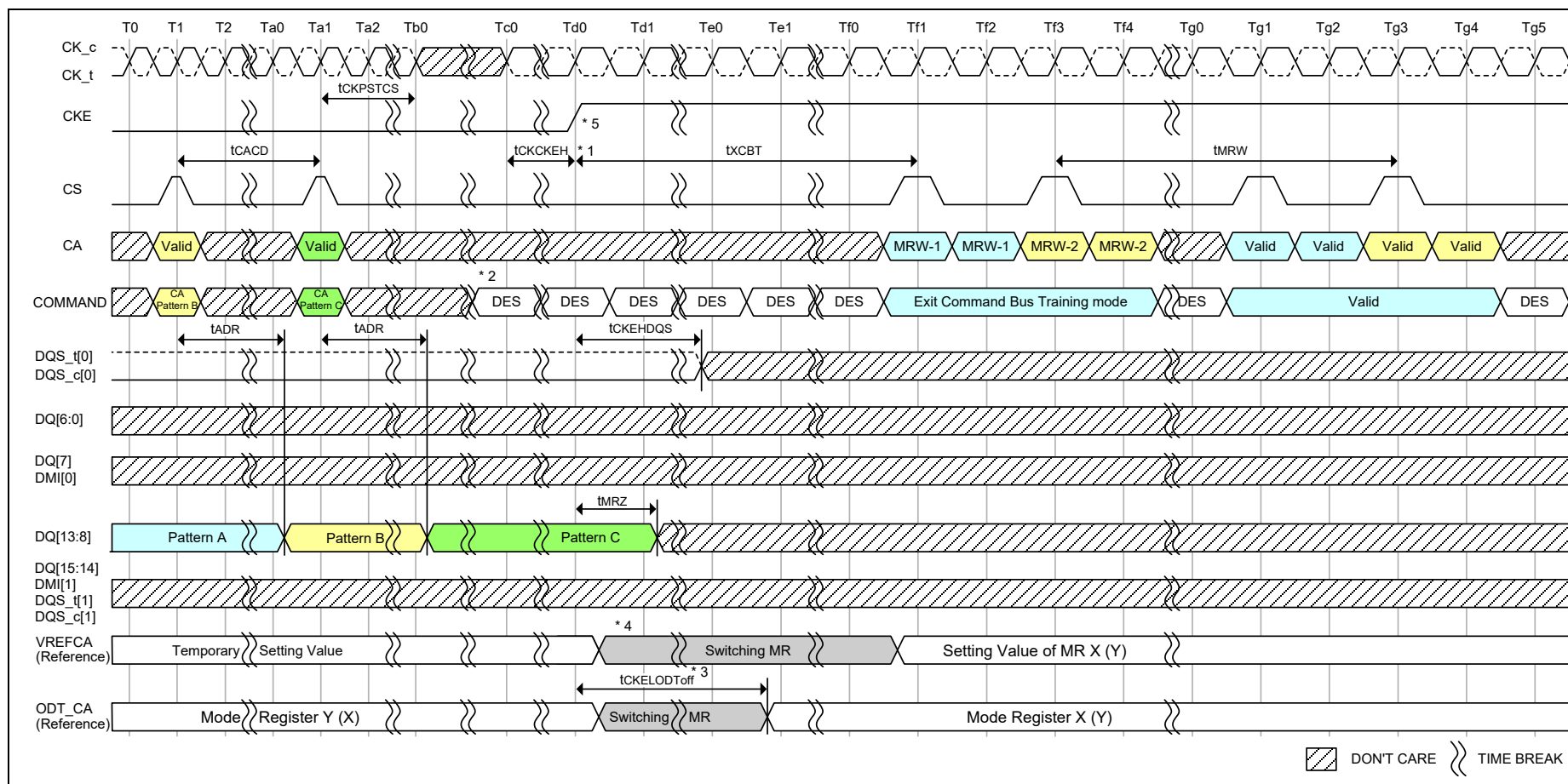
- 146 -



**Notes:**

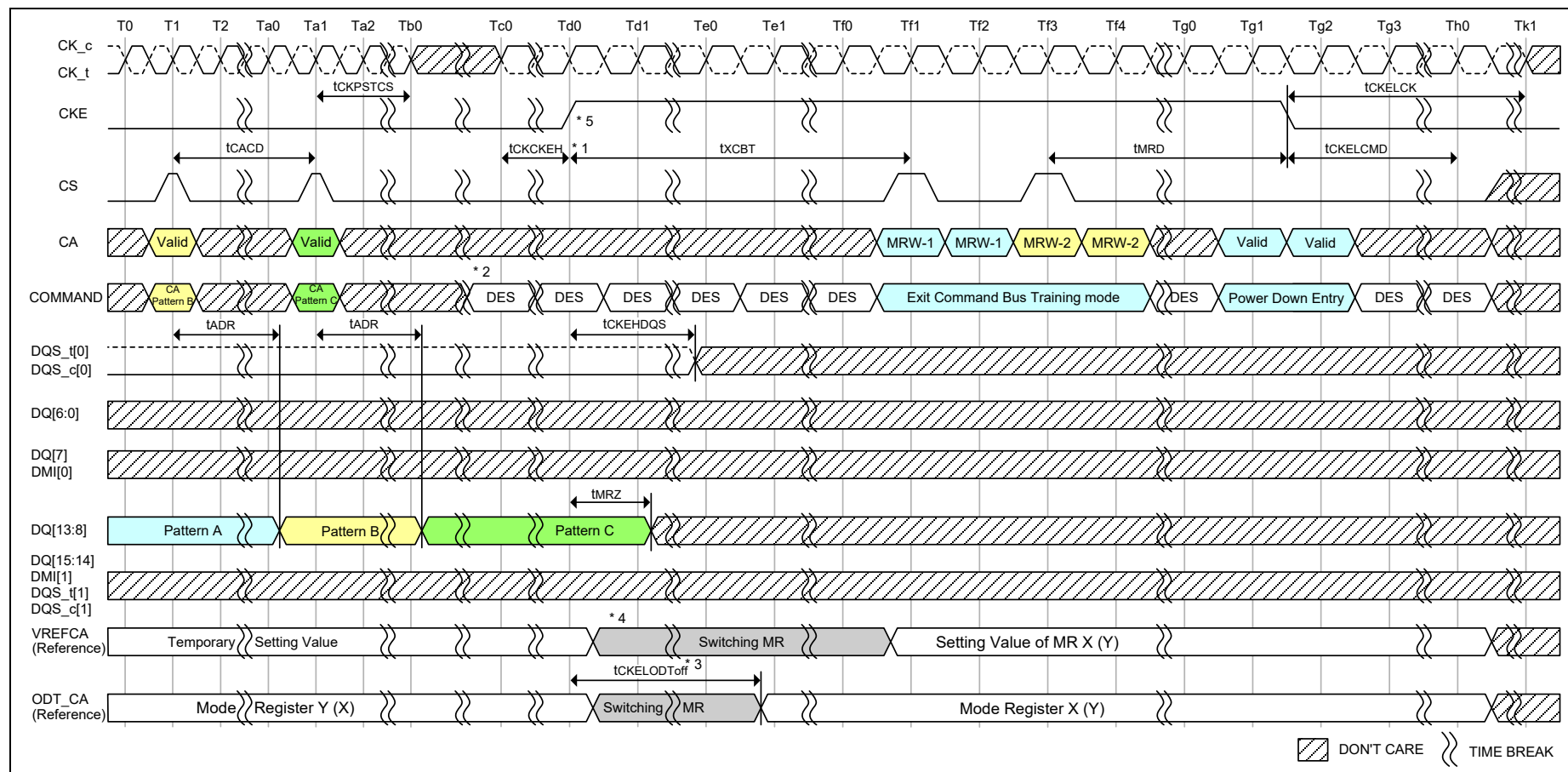
1. After tCKELCK clock can be stopped or frequency changed any time.
2. The input clock condition should be satisfied tCKPRECS.
3. Continue to Drive CK and Hold CS pins low until tCKELCK after CKE is low (which disables command decoding).
4. DRAM may or may not capture first rising/falling edge of DQS\_t/c due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal at capturing DQ[6:0] signals. The captured value of DQ[6:0] signal level by each DQS edges are overwritten at any time and the DRAM updates its VREFCA setting of MR12 temporary after time tVREFca\_Long.
5. tVREF\_LONG may be reduced to tVREF\_SHORT if the following conditions are met: 1) The new VREF setting is a single step above or below the old VREF setting, and 2) The DQS pulses a single time, or the new VREF setting value on DQ[6:0] is static and meets tDStrain/tDHtrain for every DQS pulse applied.
6. When CKE is driven LOW, the SDRAM will switch its FSP-OP registers to use the alternate (i.e., non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT\_CA disabled then termination will not enable in CA Bus Training mode. If the ODT\_CA pad is bonded to VSS, ODT\_CA termination will never enable for that die.
7. When CKE is driven low in Command Bus Training mode, the LPDDR4/LPDDR4X SDRAM will change operation to the alternate FSP, i.e., the inverse of the FSP programmed in the FSP-OP mode register.

**Figure 99 - Consecutive VREFCA Value Update**

**Notes:**

1. Clock can be stopped or frequency changed any time before tCKCKEH. CK must meet tCKCKEH before CKE is driven high.  
When CKE is driven high the clock frequency must be returned to the original frequency (the frequency corresponding to the FSP at which Command Bus Training mode was entered)
2. CS must be Deselect (low) tCKCKEH before CKE is driven high.
3. When CKE is driven high, the SDRAM's ODT\_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]).  
Example: If the SDRAM was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the SDRAM, and must be written to the FSP-OP register set before returning to operation at the trained frequency.  
Example: VREF(CA) will return to the value programmed in the original set point.
5. When CKE is driven high the LPDDR4/LPDDR4X SDRAM will revert to the FSP in operation when Command Bus Training mode was entered.

**Figure 100 - Exiting Command Bus Training Mode with Valid Command**

**Notes:**

1. Clock can be stopped or frequency changed any time before tCKCKEH. CK must meet tCKCKEH before CKE is driven high.  
When CKE is driven high the clock frequency must be returned to the original frequency (the frequency corresponding to the FSP at which Command Bus Training mode was entered)
2. CS must be Deselect (low) tCKCKEH before CKE is driven high.
3. When CKE is driven high, the SDRAM's ODT\_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]).  
Example: If the SDRAM was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the SDRAM, and must be written to the FSP-OP register set before returning to operation at the trained frequency.  
Example: VREF(CA) will return to the value programmed in the original set point.
5. When CKE is driven high the LPDDR4/LPDDR4X SDRAM will revert to the FSP in operation when Command Bus Training mode was entered.

**Figure 101 - Exiting Command Bus Training Mode with Power Down Entry**



## 7.4.28.5 Command Bus Training AC Timing Table

Table 52 - Command Bus Training AC Timing

| Parameter                                                   | Symbol        | Min/<br>Max | Data Rate                           |      |      |      |      |      |      |      | Unit | Notes |
|-------------------------------------------------------------|---------------|-------------|-------------------------------------|------|------|------|------|------|------|------|------|-------|
|                                                             |               |             | 533                                 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4267 |      |       |
| Command Bus Training Timing                                 |               |             |                                     |      |      |      |      |      |      |      |      |       |
| Valid Clock Requirement after CKE Input low                 | tCKELCK       | Min         | Max(5nS, 5nCK)                      |      |      |      |      |      |      |      | -    |       |
| Data Setup for VREF Training Mode                           | tDStrain      | Min         | 2                                   |      |      |      |      |      |      |      | nS   |       |
| Data Hold for VREF Training Mode                            | tDHtrain      | Min         | 2                                   |      |      |      |      |      |      |      | nS   |       |
| Asynchronous Data Read                                      | tADR          | Max         | 20                                  |      |      |      |      |      |      |      | nS   |       |
| CA Bus Training Command to CA Bus Training Command Delay    | tCACD         | Min         | RU(tADR/tCK)                        |      |      |      |      |      |      |      | tCK  | 2     |
| Valid Strobe Requirement before CKE Low                     | tDQSCKE       | Min         | 10                                  |      |      |      |      |      |      |      | nS   | 1     |
| First CA Bus Training Command Following CKE Low             | tCAENT        | Min         | 250                                 |      |      |      |      |      |      |      | nS   |       |
| VREF Step Time – multiple steps                             | tVREFCA_LONG  | Max         | 250                                 |      |      |      |      |      |      |      | nS   |       |
| VREF Step Time – one step                                   | tVREFCA_SHORT | Max         | 80                                  |      |      |      |      |      |      |      | nS   |       |
| Valid Clock Requirement before CS High                      | tCKPRECS      | Min         | 2tCK + tXP (tXP = Max(7.5nS, 5nCK)) |      |      |      |      |      |      |      | -    |       |
| Valid Clock Requirement after CS High                       | tCKPSTCS      | Min         | Max(7.5nS, 5nCK)                    |      |      |      |      |      |      |      | -    |       |
| Minimum delay from CS to DQS toggle in command bus training | tCS_VREF      | Min         | 2                                   |      |      |      |      |      |      |      | tCK  |       |
| Minimum delay from CKE High to Strobe High Impedance        | tCKEHDQS      |             | 10                                  |      |      |      |      |      |      |      | nS   |       |
| Valid Clock Requirement before CKE Input High               | tCKCKEH       | Min         | Max(1.75nS, 3nCK)                   |      |      |      |      |      |      |      | -    |       |
| CA Bus Training CKE High to DQ Tri-state                    | tMRZ          | Min         | 1.5                                 |      |      |      |      |      |      |      | nS   |       |
| ODT turn-on Latency from CKE                                | tCKELODTon    | Min         | 20                                  |      |      |      |      |      |      |      | nS   |       |
| ODT turn-off Latency from CKE                               | tCKELODToff   | Min         | 20                                  |      |      |      |      |      |      |      | nS   |       |
| Exit Command Bus Training Mode to next valid command delay  | tXCBT_Short   | Min         | Max(5nCK, 200nS)                    |      |      |      |      |      |      |      | -    | 3     |
|                                                             | tXCBT_Middle  | Min         | Max(5nCK, 200nS)                    |      |      |      |      |      |      |      | -    | 3     |
|                                                             | tXCBT_Long    | Min         | Max(5nCK, 250nS)                    |      |      |      |      |      |      |      | -    | 3     |

**Notes:**

1. DQS<sub>t</sub> has to retain a low level during tDQSCKE period, as well as DQS<sub>c</sub> has to retain a high level.
2. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
3. Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in Table 56. Additionally exit Command Bus Training Mode to next valid command delay Time may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.



### 7.4.29 Frequency Set Point

Frequency Set-Points allow the LPDDR4/LPDDR4X SDRAM CA Bus to be switched between two differing operating frequencies, with changes in voltage swings and termination values, without ever being in an untrained state which could result in a loss of communication to the DRAM. This is accomplished by duplicating all CA Bus mode register parameters, as well as other mode register parameters commonly changed with operating frequency. These duplicated registers form two sets that use the same mode register addresses, with read/write access controlled by MR bit FSP-WR (Frequency Set-Point Write/Read) and the DRAM operating point controlled by another MR bit FSP-OP (Frequency Set-Point Operation). Changing the FSPWR bit allows MR parameters to be changed for an alternate Frequency Set-Point without affecting the LPDDR4/LPDDR4X SDRAM's current operation. Once all necessary parameters have been written to the alternate Set-Point, changing the FSP-OP bit will switch operation to use all of the new parameters simultaneously (within tFC), eliminating the possibility of a loss of communication that could be caused by a partial configuration change.

Parameters which have two physical registers controlled by FSP-WR and FSP-OP are shown in the following table.

**Table 53 - Mode Register Function with two physical registers**

| MR#  | Operand | Function                                           | Note |
|------|---------|----------------------------------------------------|------|
| MR1  | OP[2]   | WR-PRE (WR Pre-amble Length)                       |      |
|      | OP[3]   | RD-PRE (RD Pre-amble Type)                         |      |
|      | OP[6:4] | nWR (Write-Recovery for Auto-Precharge commands)   |      |
|      | OP[7]   | PST (RD Post-Amble Length)                         |      |
| MR2  | OP[2:0] | RL (Read latency)                                  |      |
|      | OP[5:3] | WL (Write latency)                                 |      |
|      | OP[6]   | WLS (Write Latency Set)                            |      |
| MR3  | OP[0]   | PU-Cal (Pull-up Calibration Point)                 | 1    |
|      | OP[1]   | WR PST(WR Post-Amble Length)                       |      |
|      | OP[5:3] | PDDS (Pull-Down Drive Strength)                    |      |
|      | OP[6]   | DBI-RD (DBI-Read Enable)                           |      |
|      | OP[7]   | DBI-WR (DBI-Write Enable)                          |      |
| MR11 | OP[2:0] | DQ ODT (DQ Bus Receiver On-Die-Termination)        |      |
|      | OP[6:4] | CA ODT (CA Bus Receiver On-Die-Termination)        |      |
| MR12 | OP[5:0] | VREF(CA) (VREF(CA) Setting)                        |      |
|      | OP[6]   | VR-CA (VREF(CA) Range)                             |      |
| MR14 | OP[5:0] | VREF(DQ) (VREF(DQ) Setting)                        |      |
|      | OP[6]   | VR(dq) (VREF(DQ) Range)                            |      |
| MR21 | OP[5]   | Low Speed CA buffer                                |      |
| MR22 | OP[2:0] | SoC ODT (Controller ODT Value for VOH calibration) |      |
|      | OP[3]   | ODTE-CK (CK ODT enabled for non-terminating rank)  |      |
|      | OP[4]   | ODTE-CS (CS ODT enable for non-terminating rank)   |      |
|      | OP[5]   | ODTD-CA (CA ODT termination disable)               |      |
| MR51 | OP[1]   | SE_QE_RD (Single Ended Read DQS Enable)            |      |
|      | OP[2]   | SE_QE_WR (Single Ended Write DQS Enable)           |      |
|      | OP[3]   | SE_CE (Single Ended CK Enable)                     |      |

**Note:**

1. For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.

See Mode Register Definition for more details.



Table 54 shows how the two mode registers for each of the parameters above can be modified by setting the appropriate FSP-WR value, and how device operation can be switched between operating points by setting the appropriate FSP-OP value. The FSP-WR and FSP-OP functions operate completely independently.

**Table 54 - Relation between MR Setting and DRAM Operation**

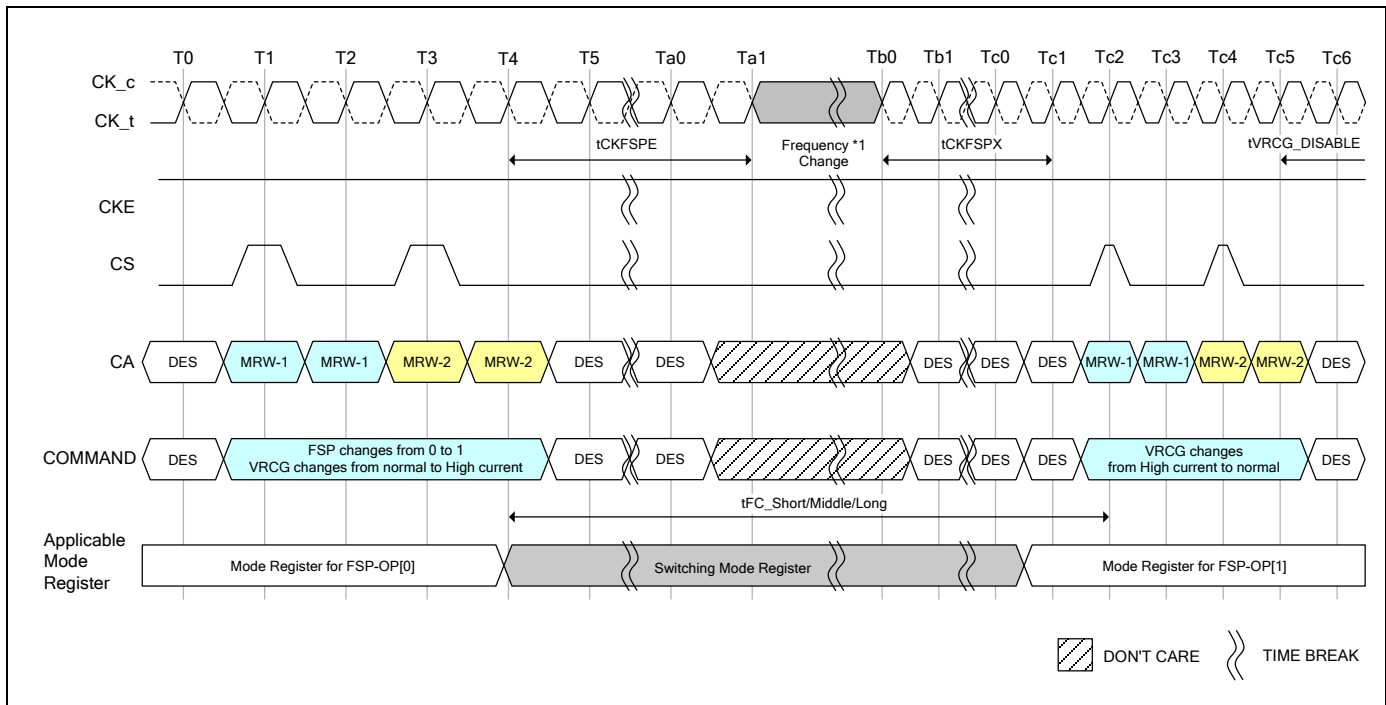
| Function | MR# & Operand | Data        | Operation                                                                                                                 | Notes |
|----------|---------------|-------------|---------------------------------------------------------------------------------------------------------------------------|-------|
| FSP-WR   | MR13 OP[6]    | 0 (Default) | Data write to Mode Register N for FSP-OP[0] by MRW Command<br>Data read from Mode Register N for FSP-OP[0] by MRR Command | 1     |
|          |               | 1           | Data write to Mode Register N for FSP-OP[1] by MRW Command<br>Data read from Mode Register N for FSP-OP[1] by MRR Command |       |
| FSP-OP   | MR13 OP[7]    | 0 (Default) | DRAM operates with Mode Register N for FSP-OP[0] setting                                                                  | 2     |
|          |               | 1           | DRAM operates with Mode Register N for FSP-OP[1] setting                                                                  |       |

**Notes:**

1. FSP-WR stands for Frequency Set Point Write/Read.
2. FSP-OP stands for Frequency Set Point Operating Point.

#### 7.4.29.1 Frequency set point update Timing

The Frequency set point update timing is shown in Figure 102 and Table 55. When changing the frequency set point via MR13 OP[7], the VRCG setting: MR13 OP[3] have to be changed into VREF Fast Response (high current) mode at the same time. After Frequency change time ( $t_{FC}$ ) is satisfied. VRCG can be changed into Normal Operation mode via MR13 OP[3].



**Note:**

1. The definition that is Clock frequency change during CKE HIGH should be followed at the frequency change operation. For more information, refer to section 7.4.45 Input Clock Stop and Frequency Change.

**Figure 102 - Frequency Set Point Switching Timing**



Table 55 - Frequency Set Point AC Timing

| Parameter                                                               | Symbol     | Min/<br>Max | Data Rate        |      |      |      |      |      |      |      | Unit | Note |
|-------------------------------------------------------------------------|------------|-------------|------------------|------|------|------|------|------|------|------|------|------|
|                                                                         |            |             | 533              | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4267 |      |      |
| Frequency Set Point parameters                                          |            |             |                  |      |      |      |      |      |      |      |      |      |
| Frequency Set Point<br>Switching Time                                   | tFC_Short  | Min         | 200              |      |      |      |      |      |      |      | nS   | 1    |
|                                                                         | tFC_Middle | Min         | 200              |      |      |      |      |      |      |      | nS   | 1    |
|                                                                         | tFC_Long   | Min         | 250              |      |      |      |      |      |      |      | nS   | 1    |
| Valid Clock Requirement<br>after Entering FSP Change                    | tCKFSPE    | Min         | max(7.5nS, 4nCK) |      |      |      |      |      |      |      | -    |      |
| Valid Clock Requirement<br>before 1st Valid Command<br>after FSP change | tCKFSPX    | Min         | max(7.5nS, 4nCK) |      |      |      |      |      |      |      | -    |      |

**Note:**

1. Frequency Set Point Switching Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in Table 56.

Additionally change of Frequency Set Point may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

Table 56 - tFC value mapping

| Application | Step Size       |                                           | Range           |               |
|-------------|-----------------|-------------------------------------------|-----------------|---------------|
|             | From<br>FSP-OP0 | To<br>FSP-OP1                             | From<br>FSP-OP0 | To<br>FSP-OP1 |
| tFC_Short   | Base            | A single step size increment/decrement    | Base            | No Change     |
| tFC_Middle  | Base            | Two or more step size increment/decrement | Base            | No Change     |
| tFC_Long    | -               | -                                         | Base            | Change        |

**Note:**

1. As well as change from FSP-OP1 to FSP-OP0.

Table 57 provides an example of tFC value mapping when FSP-OP moves from OP0 to OP1.

Table 57 - tFC value mapping example

| Case | From/To | FSP-OP:<br>MR13 OP[7] | VREF(CA) Setting:<br>MR12 OP[5:0] | VREF(CA) Range:<br>MR12 OP[6] | Application | Note |
|------|---------|-----------------------|-----------------------------------|-------------------------------|-------------|------|
| 1    | From    | 0                     | 001100                            | 0                             | tFC_Short   | 1    |
|      | To      | 1                     | 001101                            | 0                             |             |      |
| 2    | From    | 0                     | 001100                            | 0                             | tFC_Middle  | 2    |
|      | To      | 1                     | 001110                            | 0                             |             |      |
| 3    | From    | 0                     | Don't Care                        | 0                             | tFC_Long    | 3    |
|      | To      | 1                     | Don't Care                        | 1                             |             |      |

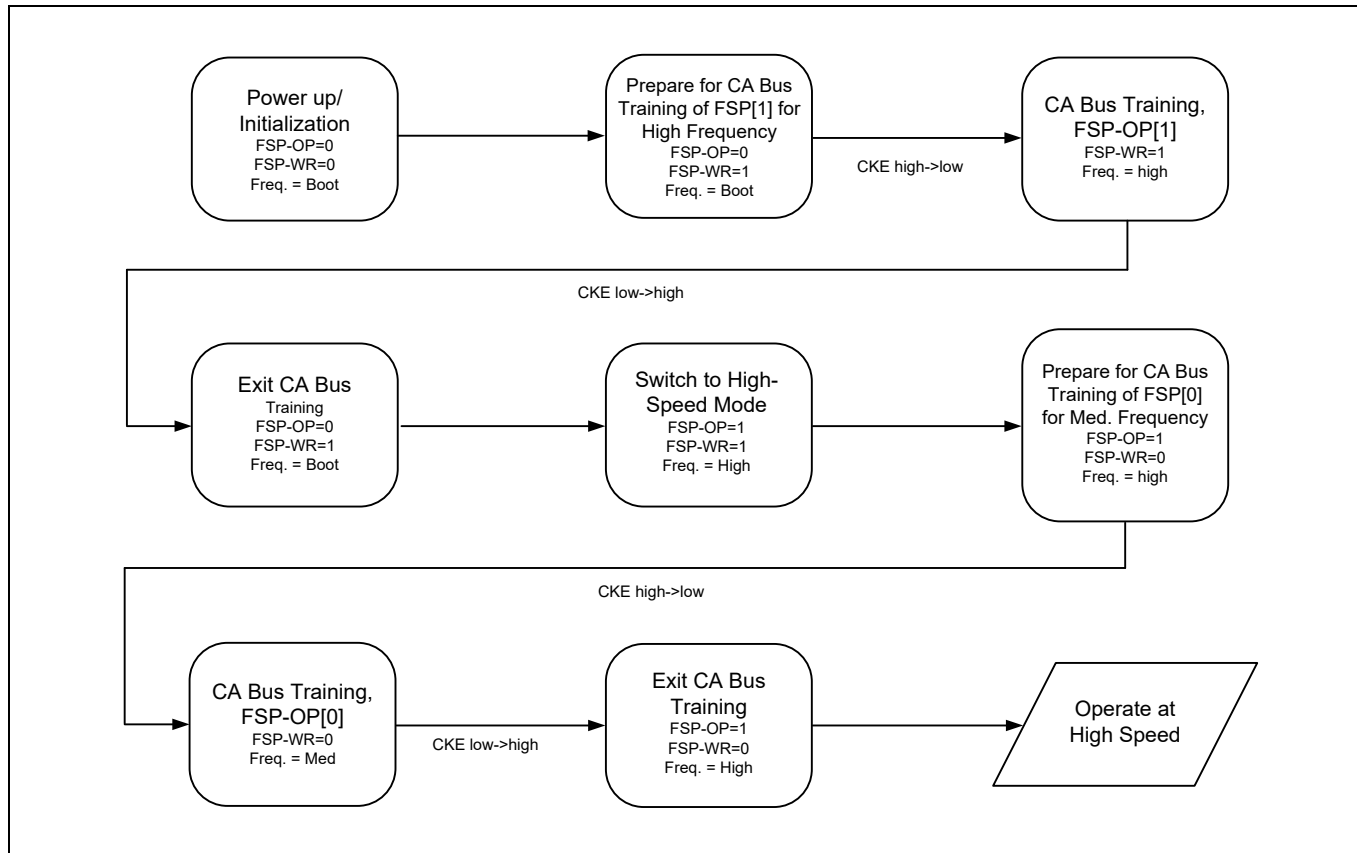
**Notes:**

1. A single step size increment/decrement for VREF(CA) Setting Value.
2. Two or more step size increment/decrement for VREF(CA) Setting Value.
3. VREF(CA) Range is changed. In this case changing VREF(CA) Setting doesn't affect tFC value.



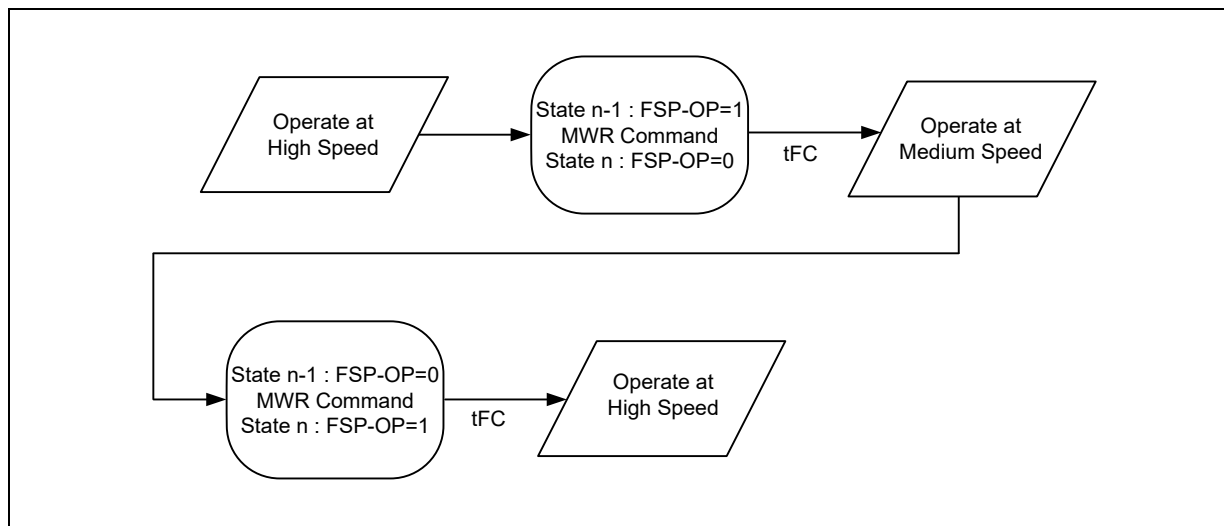


The LPDDR4/LPDDR4X SDRAM defaults to FSP-OP[0] at power-up. Both Set-Points default to settings needed to operate in un-terminated, low-frequency environments. To enable the LPDDR4/LPDDR4X SDRAM to operate at higher frequencies, Command Bus Training mode should be utilized to train the alternate Frequency Set-Point (Figure 103). See the section Command Bus Training for more details on this training mode.



**Figure 103 - Training Two Frequency Set-Points**

Once both Frequency Set-Points have been trained, switching between points can be performed by a single MRW followed by waiting for tFC (Figure 104).

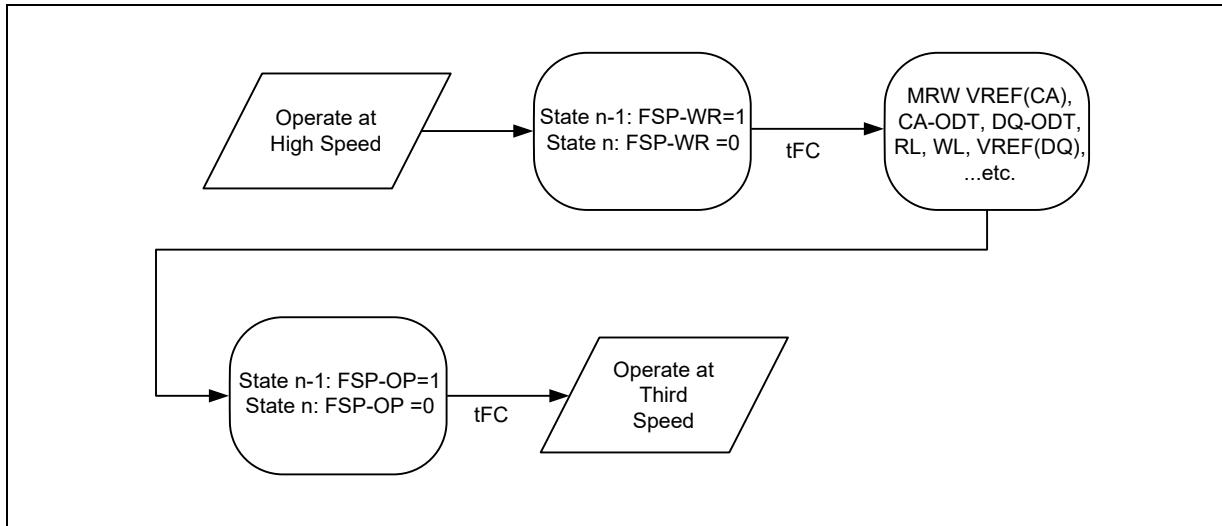


**Figure 104 - Switching Between Two Trained Frequency Set-Points**





Switching to a third (or more) Set-Point can be accomplished if the memory controller has stored the previously-trained values (in particular the VREF(CA) calibration value) and re-writes these to the alternate Set-Point before switching FSP-OP (Figure 105).



**Figure 105 - Switching to a Third Trained Frequency Set-Point**



### 7.4.30 Mode Register Write-WR Leveling Mode

To improve signal-integrity performance, the LPDDR4/LPDDR4X SDRAM provides a write-leveling feature to compensate CK-to-DQS timing skew affecting timing parameters such as tDQSS, tDSS, and tDSH. The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS\_t/DQS\_c signal pair.

All data bits (DQ[7:0] for DQS\_t/DQS\_c[0], and DQ[15:8] for DQS\_t/DQS\_c[1]) carry the training feedback to the controller. Both DQS signals in each channel must be leveled independently. Write-leveling entry/exit is independent between channels for dual channel devices.

The LPDDR4/LPDDR4X SDRAM enters into write-leveling mode when mode register MR2-OP[7] is set HIGH. When entering write-leveling mode, the state of the DQ pins is undefined. During write-leveling mode, only DESELECT commands are allowed, or a MRW command to exit the write-leveling operation. Depending on the absolute values of tDQSL and tDQSH in the application, the value of tDQSS may have to be better than the limits provided in the Write AC Timing Table in order to satisfy the tDSS and tDSH specifications.

Upon completion of the write-leveling operation, the DRAM exits from write-leveling mode when MR2-OP[7] is reset LOW.

Write Leveling should be performed before Write Training (DQS2DQ Training).

#### 7.4.30.1 Write Leveling Procedure

1. Enter into Write-leveling mode by setting MR2-OP[7]=1.
2. Once entered into Write-leveling mode, DQS\_t must be driven LOW and DQS\_c HIGH after a delay of tWLDQSEN.
3. Wait for a time tWLMRD before providing the first DQS signal input. The delay time tWLMRD(MAX) is controller dependent.
4. DRAM may or may not capture first rising edge of DQS\_t due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal during Write Training Mode. The captured clock level by each DQS edges are overwritten at any time and the DRAM provides asynchronous feedback on all the DQ bits after time tWLO.
5. The feedback provided by the DRAM is referenced by the controller to increment or decrement the DQS\_t and/or DQS\_c delay settings.
6. Repeat step 4 through step 5 until the proper DQS\_t/DQS\_c delay is established.
7. Exit from Write-leveling mode by setting MR2-OP[7]=0.



A Write Leveling timing example is shown in Figure 106, and Figure 107.

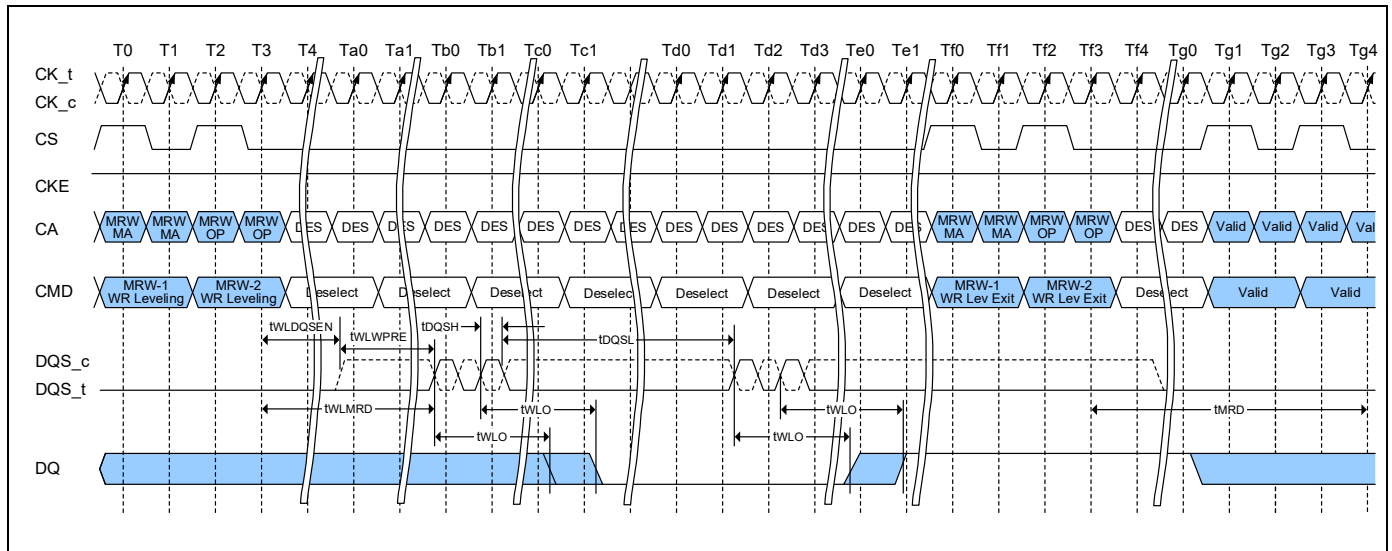


Figure 106 - Write Leveling Timing,  $t_{DQSL(max)}$

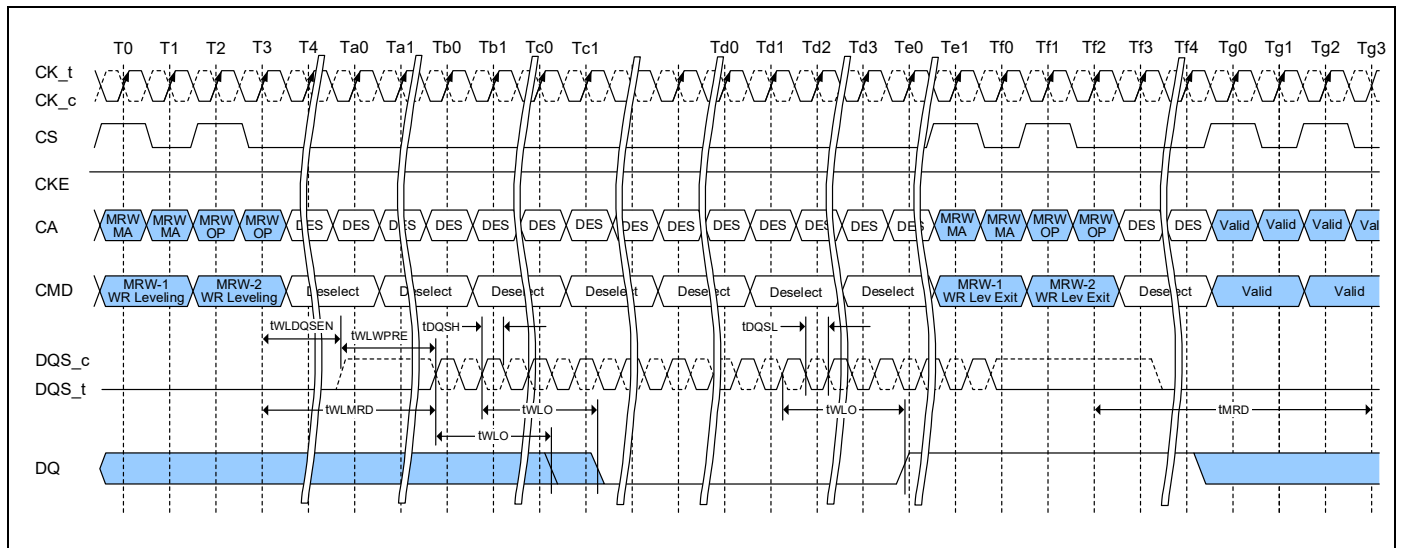


Figure 107 - Write Leveling Timing,  $t_{DQSL(min)}$

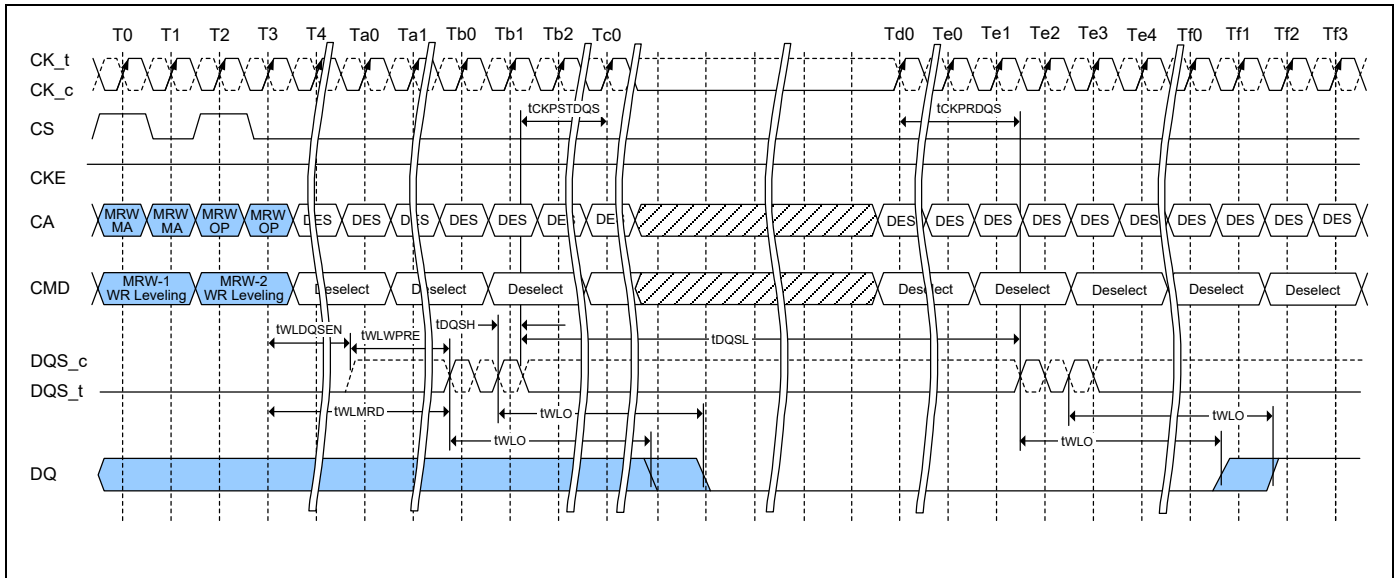


### 7.4.30.2 Input Clock Frequency Stop and Change

The input clock frequency can be stopped or changed from one stable clock rate to another stable clock rate during Write Leveling mode.

The Frequency stop or change timing is shown in Figure 108.

The timing parameters are provided in Table 58.



#### Notes:

1. CK\_t is held LOW and CK\_c is held HIGH during clock stop.
2. CS shall be held LOW during clock stop.

**Figure 108 - Clock Stop and Timing during Write Leveling**

**Table 58 - Write Leveling Timing Parameters**

| Parameter                                                      | Symbol    | Min/Max | Value            | Units | Notes |
|----------------------------------------------------------------|-----------|---------|------------------|-------|-------|
| DQS_t/DQS_c delay after write leveling mode is programmed      | tWLDQSEN  | Min     | 20               | tCK   |       |
|                                                                |           | Max     | -                |       |       |
| Write preamble for Write Leveling                              | tWLWPRE   | Min     | 20               | tCK   |       |
|                                                                |           | Max     | -                |       |       |
| First DQS_t/DQS_c edge after write leveling mode is programmed | tWLMRD    | Min     | 40               | tCK   |       |
|                                                                |           | Max     | -                |       |       |
| Write leveling output delay                                    | tWLO      | Min     | 0                | nS    |       |
|                                                                |           | Max     | 20               |       |       |
| Mode register set command delay                                | tMRD      | Min     | max(14nS, 10nCK) | nS    |       |
|                                                                |           | Max     | -                |       |       |
| Valid Clock Requirement before DQS Toggle                      | tCKPRDQS  | Min     | max(7.5nS, 4nCK) | -     |       |
|                                                                |           | Max     | -                |       |       |
| Valid Clock Requirement after DQS Toggle                       | tCKPSTDQS | Min     | max(7.5nS, 4nCK) | -     |       |
|                                                                |           | Max     | -                |       |       |



### 7.4.30.3 Write Leveling Setup and Hold Time

Table 59 - Write Leveling Setup and Hold Time

| Parameter                         | Symbol | Min/Max | Data Rate |      |       |      |      |      | Unit |
|-----------------------------------|--------|---------|-----------|------|-------|------|------|------|------|
|                                   |        |         | 1600      | 2400 | 2667  | 3200 | 3733 | 4267 |      |
| Write Leveling Parameters         |        |         |           |      |       |      |      |      |      |
| Write leveling hold time          | tWLH   | Min     | 150       | 100  | 91.7  | 75   | 62.5 | 50   | pS   |
| Write leveling setup time         | tWLS   | Min     | 150       | 100  | 91.7  | 75   | 62.5 | 50   | pS   |
| Write leveling input valid window | tWLIVW | Max     | 240       | 160  | 146.7 | 120  | 105  | 90   | pS   |

**Notes:**

1. In addition to the traditional setup and hold time specifications above, there is value in an input valid window based specification for write-leveling training. As the training is based on each device, worst case process skews for setup and hold do not make sense to close timing between CK and DQS.
2. tWLIVW is defined in a similar manner to tDIVW\_Total, except that here it is a DQS input valid window with respect to CK. This would need to account for all VT (voltage and temperature) drift terms between CK and DQS within the DRAM that affect the write-leveling input valid window.

The DQS input mask for timing with respect to CK is shown in Figure 109. The "total" mask (tWLIVW) defines the time the input signal must not encroach in order for the DQS input to be successfully captured by CK. The mask is a receiver property and it is not the valid data-eye.

DQS t/DQS\_c and CK t/CK\_c at DRAM Latch

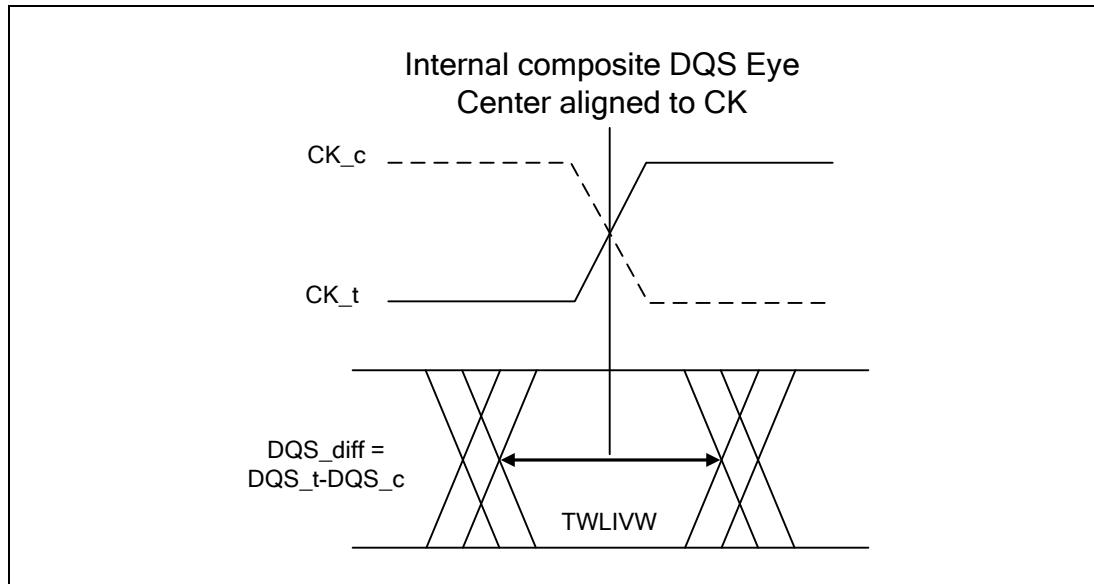


Figure 109 - DQS\_t/DQS\_c to CK\_t/CK\_c timings at the DRAM pins referenced from the internal latch



### 7.4.31 RD DQ Calibration

LPDDR4/LPDDR4X SDRAMs feature a RD DQ Calibration training function that outputs a 16-bit user-defined pattern on the DQ pins. RD DQ Calibration is initiated by issuing a MPC-1 [RD DQ Calibration] command followed by a CAS-2 command, cause the LPDDR4/LPDDR4X SDRAM to drive the contents of MR32 followed by the contents of MR40 on each of DQ[15:0] and DMI[1:0]. The pattern can be inverted on selected DQ pins according to user-defined invert masks written to MR15 and MR20.

#### 7.4.31.1 RD DQ Calibration Training Procedure

Reference Figure 110 and Figure 111.

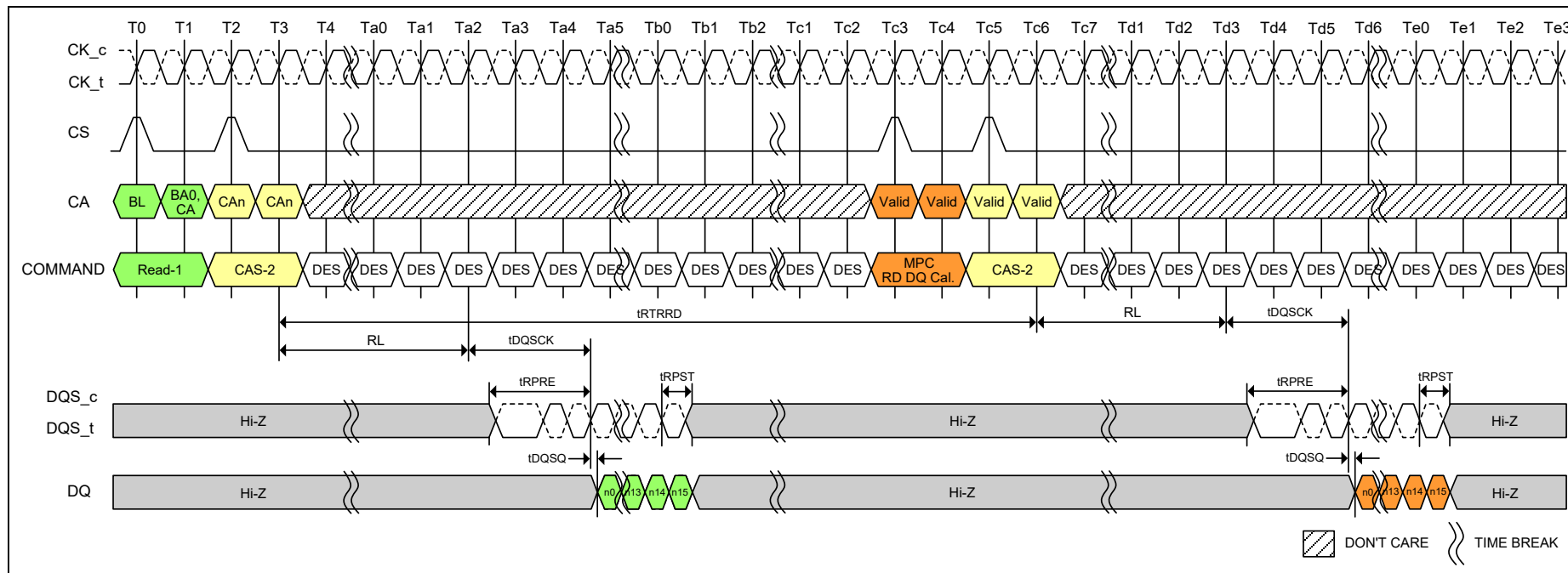
The procedure for executing RD DQ Calibration is:

- Issue MRW commands to write MR32 (first eight bits), MR40 (second eight bits), MR15 (eight-bit invert mask for byte 0), and MR20 (eight-bit invert mask for byte 1).
- Optionally this step could be skipped to use the default patterns
  - MR32 default = 5A<sub>H</sub>
  - MR40 default = 3C<sub>H</sub>
  - MR15 default = 55<sub>H</sub>
  - MR20 default = 55<sub>H</sub>
- Issue an MPC-1 [RD DQ Calibration] command followed immediately by a CAS-2 command.
  - Each time an MPC-1 [RD DQ Calibration] command followed by a CAS-2 is received by the LPDDR4/LPDDR4X SDRAM, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins.
  - The data pattern will be inverted for I/O pins with a '1' programmed in the corresponding invert mask mode register bit (see Table 60).
  - Note that the pattern is driven on the DMI pins, but no data bus inversion function is enabled, even if Read DBI is enabled in the DRAM mode register.
  - The MPC-1 [RD DQ Calibration] command can be issued every tCCD seamlessly, and tRTRRD delay is required between Array Read command and the MPC-1 [RD DQ Calibration] command as well the delay required between the MPC-1 [RD DQ Calibration] command and an array read.
  - The operands received with the CAS-2 command must be driven LOW.
- DQ Read Training can be performed with any or no banks active, during Refresh, or during SREF with CKE high.

**Table 60 - Invert Mask Assignments**

| DQ Pin   | 0 | 1 | 2 | 3 | DMI0 | 4 | 5 | 6 | 7 |
|----------|---|---|---|---|------|---|---|---|---|
| MR15 bit | 0 | 1 | 2 | 3 | N/A  | 4 | 5 | 6 | 7 |

| DQ Pin   | 8 | 9 | 10 | 11 | DMI1 | 12 | 13 | 14 | 15 |
|----------|---|---|----|----|------|----|----|----|----|
| MR20 bit | 0 | 1 | 2  | 3  | N/A  | 4  | 5  | 6  | 7  |

**Notes:**

1. Read-1 to MPC [RD DQ Calibration] Operation is shown as an example of command-to-command timing.  
Timing from Read-1 to MPC [RD DQ Calibration] command is  $t_{RTRRD}$ .
2. MPC [RD DQ Calibration] uses the same command-to-data timing relationship ( $RL$ ,  $t_{DQSCK}$ ,  $t_{DQSQ}$ ) as a Read-1 command.
3. BL = 16, Read Preamble: Toggle, Read Postamble: 0.5nCK.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 110 - DQ Read Training Timing: Read to Read DQ Calibration**



- Figure 111 - DQ Read Training Timing: Read DQ Cal. to Read DQ Cal. / Read**





### 7.4.31.2 DQ Read Training Example

An example of DQ Read Training output is shown in Table 61. This shows the 16-bit data pattern that will be driven on each DQ in byte 0 when one DQ Read Training command is executed. This output assumes the following mode register values are used:

- MR32 = 1C<sub>H</sub>
- MR40 = 59<sub>H</sub>
- MR15 = 55<sub>H</sub>
- MR20 = 55<sub>H</sub>

**Table 61 - DQ Read Calibration Bit Ordering and Inversion Example**

| Pin  | Invert | Bit Sequence → |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------|--------|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
|      |        | 15             | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DQ0  | Yes    | 1              | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ1  | No     | 0              | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ2  | Yes    | 1              | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ3  | No     | 0              | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DMI0 | Never  | 0              | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ4  | Yes    | 1              | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ5  | No     | 0              | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ6  | Yes    | 1              | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ7  | No     | 0              | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ8  | Yes    | 1              | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ9  | No     | 0              | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ10 | Yes    | 1              | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ11 | No     | 0              | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DMI1 | Never  | 0              | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ12 | Yes    | 1              | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ13 | No     | 0              | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ14 | Yes    | 1              | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ15 | No     | 0              | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

#### Notes:

1. The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and DMI[1:0] when RD DQ Calibration is initiated via a MPC-1 [RD DQ Calibration] command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern is 27<sub>H</sub>, then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111 →.
2. MR15 and MR20 may be used to invert the MR32/MR40 data pattern on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. DMI [1:0] outputs status follows Table 62.
4. No Data Bus Inversion (DBI) function is enacted during RD DQ Calibration, even if DBI is enabled in MR3-OP[6].



Table 62 - MR Setting vs. DMI Status

| DM Function<br>MR13 OP[5] | Write DBI dc Function<br>MR3 OP[7] | Read DBI dc Function<br>MR3 OP[6] | DMI Status                      |
|---------------------------|------------------------------------|-----------------------------------|---------------------------------|
| 1: Disable                | 0: Disable                         | 0: Disable                        | Hi-Z                            |
| 1: Disable                | 1: Enable                          | 0: Disable                        | The data pattern is transmitted |
| 1: Disable                | 0: Disable                         | 1: Enable                         | The data pattern is transmitted |
| 1: Disable                | 1: Enable                          | 1: Enable                         | The data pattern is transmitted |
| 0: Enable                 | 0: Disable                         | 0: Disable                        | The data pattern is transmitted |
| 0: Enable                 | 1: Enable                          | 0: Disable                        | The data pattern is transmitted |
| 0: Enable                 | 0: Disable                         | 1: Enable                         | The data pattern is transmitted |
| 0: Enable                 | 1: Enable                          | 1: Enable                         | The data pattern is transmitted |

#### 7.4.31.3 MPC of Read DQ Calibration after Power-Down Exit

Following the power-down state, an additional time, tMRRI, is required prior to issuing the MPC of Read DQ Calibration command (Figure 112). This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the Read DQ data in MR32 and MR40 data path after exit from standby, power-down mode.

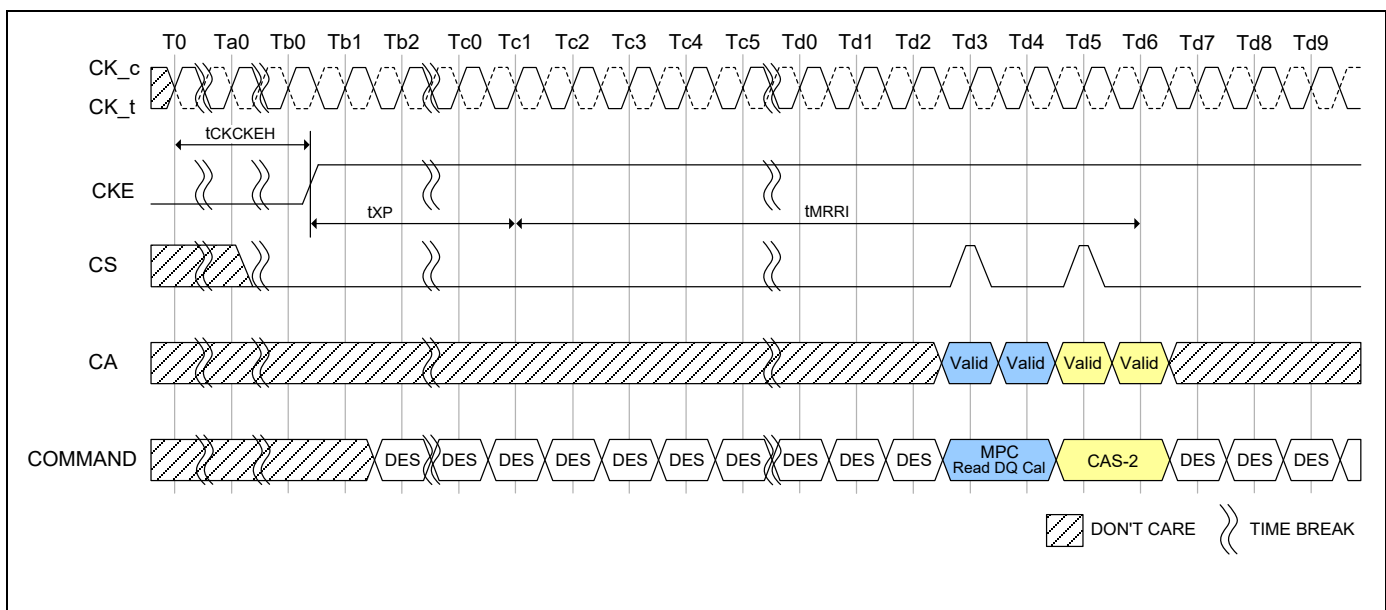


Figure 112 - MPC Read DQ Calibration Following Power-Down State



#### 7.4.32 DQS-DQ Training

The LPDDR4/LPDDR4X SDRAM uses an un-matched DQS-DQ path to enable high speed performance and save power in the DRAM. As a result, the DQS strobe must be trained to arrive at the DQ latch center-aligned with the Data eye. The SDRAM DQ receiver is located at the DQ pad, and has a shorter internal delay in the SDRAM than does the DQS signal. The SDRAM DQ receiver will latch the data present on the DQ bus when DQS reaches the latch, and training is accomplished by delaying the DQ signals relative to DQS such that the Data eye arrives at the receiver latch centered on the DQS transition.

Two modes of training are available in LPDDR4/LPDDR4X SDRAM:

- Command-based FIFO WR/RD with user patterns
- An internal DQS clock-tree oscillator, to determine the need for, and the magnitude of required training.

The command-based FIFO WR/RD uses the MPC command with operands to enable this special mode of operation. When issuing the MPC command, if OP[6] is set LOW then the DRAM will perform a NOP command. When OP[6] is set HIGH, then OP[5:0] enable training functions or are reserved for future use (RFU). MPC commands that initiate a Read FIFO, READ DQ Calibration or Write FIFO to the SDRAM must be followed immediately by a CAS-2 command. See section **7.4.35 “Multi-Purpose Command (MPC)”** for more information.

To perform Write Training, the controller can issue a MPC [Write DQ FIFO] command with OP[6:0] set as described in the MPC Definition section, followed immediately by a CAS-2 command (CAS-2 operands should be driven LOW) to initiate a Write DQ FIFO. Timings for MPC [Write DQ FIFO] are identical to a Write command, with WL (Write Latency) timed from the 2nd rising clock edge of the CAS-2 command. Up to 5 consecutive MPC [Write DQ FIFO] commands with user defined patterns may be issued to the SDRAM to store up to 80 values (BL16 x5) per pin that can be read back via the MPC [Read DQ FIFO] command. Write/Read FIFO Pointer operation is described later in this section.

After writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC [Read DQ FIFO] command and results compared with “expect” data to see if further training (DQ delay) is needed. MPC [Read DQ FIFO] is initiated by issuing a MPC command with OP[6:0] set as described in the MPC Definition section, followed immediately by a CAS-2 command (CAS-2 operands must be driven LOW). Timings for the MPC [Read DQ FIFO] command are identical to a Read command, with RL (Read Latency) timed from the 2nd rising clock edge of the CAS-2 command.

Read DQ FIFO is non-destructive to the data captured in the FIFO, so data may be read continuously until it is either overwritten by a Write DQ FIFO command or disturbed by CKE LOW or any of the following commands; Write, Masked Write, Read, Read DQ Calibration and a MRR. If fewer than 5 Write DQ FIFO commands were executed, then unwritten registers will have un-defined (but valid) data when read back.

The following command about MRW is only allowed from MPC [Write DQ FIFO] command to MPC [Read DQ FIFO].

Allowing MRW command is for OP[7]:FSP-OP, OP[6]:FSP-WR and OP[3]:VRCG of MR13 and MR14. And the rest of MRW command is prohibited.

For example: If 5 Write DQ FIFO commands are executed sequentially, then a series of Read DQ FIFO commands will read valid data from FIFO[0], FIFO[1]....FIFO[4], and will then wrap back to FIFO[0] on the next Read DQ FIFO.

On the other hand, if fewer than 5 Write DQ FIFO commands are executed sequentially (example=3), then a series of Read DQ FIFO commands will return valid data for FIFO[0], FIFO[1], and FIFO[2], but the next two Read DQ FIFO commands will return un-defined data for FIFO[3] and FIFO[4] before wrapping back to the valid data in FIFO[0].



#### 7.4.32.1 FIFO Pointer Reset and Synchronism

(Reference Figure 113 through Figure 117 and Table 63.)

The Read and Write DQ FIFO pointers are reset under the following conditions:

- Power-up initialization
- RESET\_n asserted
- Power-down entry
- Self Refresh Power-Down entry

The MPC [Write DQ FIFO] command advances the WR-FIFO pointer, and the MPC [Read DQ FIFO] advances the RD-FIFO pointer. Also any normal (non-FIFO) Read Operation (RD, RDA) advances both WR-FIFO pointer and RD-FIFO pointer. Issuing (non-FIFO) Read Operation command is inhibited during Write training period. To keep the pointers aligned, the SoC memory controller must adhere to the following restriction at the end of Write training period:

- $b = a + (n \times c)$

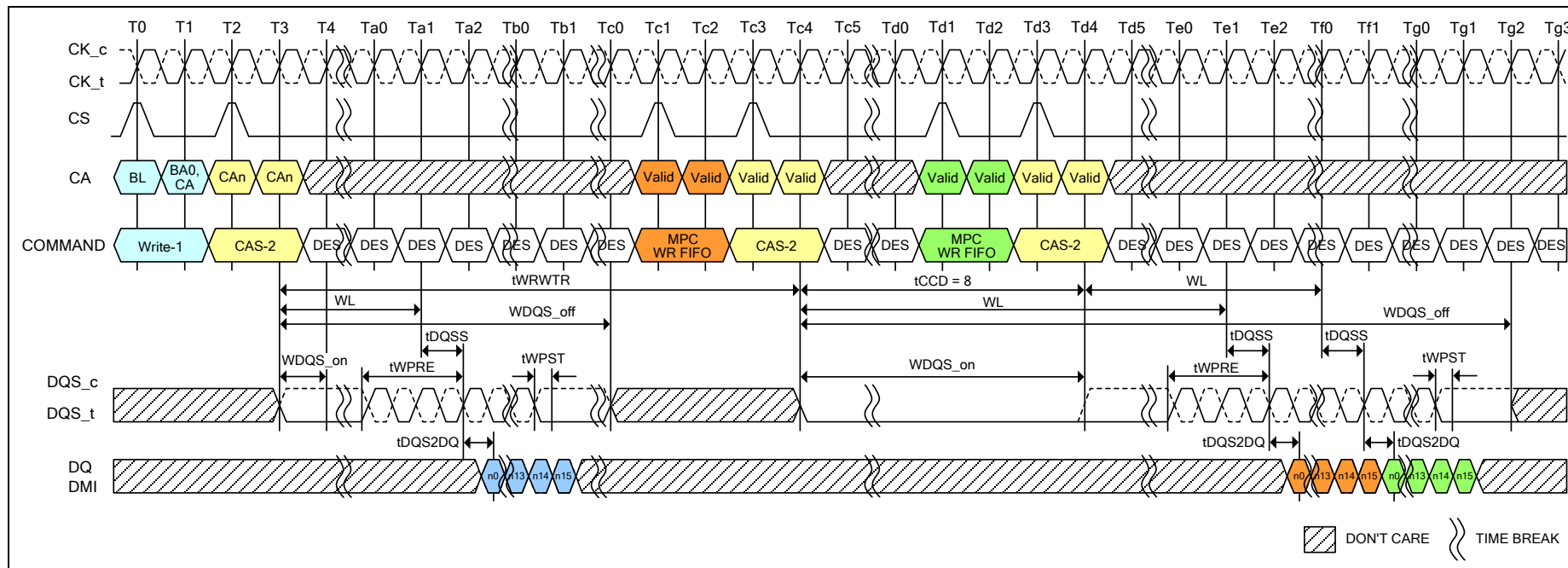
Where:

'a' is the number of MPC [Write DQ FIFO] commands

'b' is the number of MPC [Read DQ FIFO] commands

'c' is the FIFO depth (=5 for LPDDR4/LPDDR4X SDRAM)

'n' is a positive integer,  $\geq 0$



#### Notes:

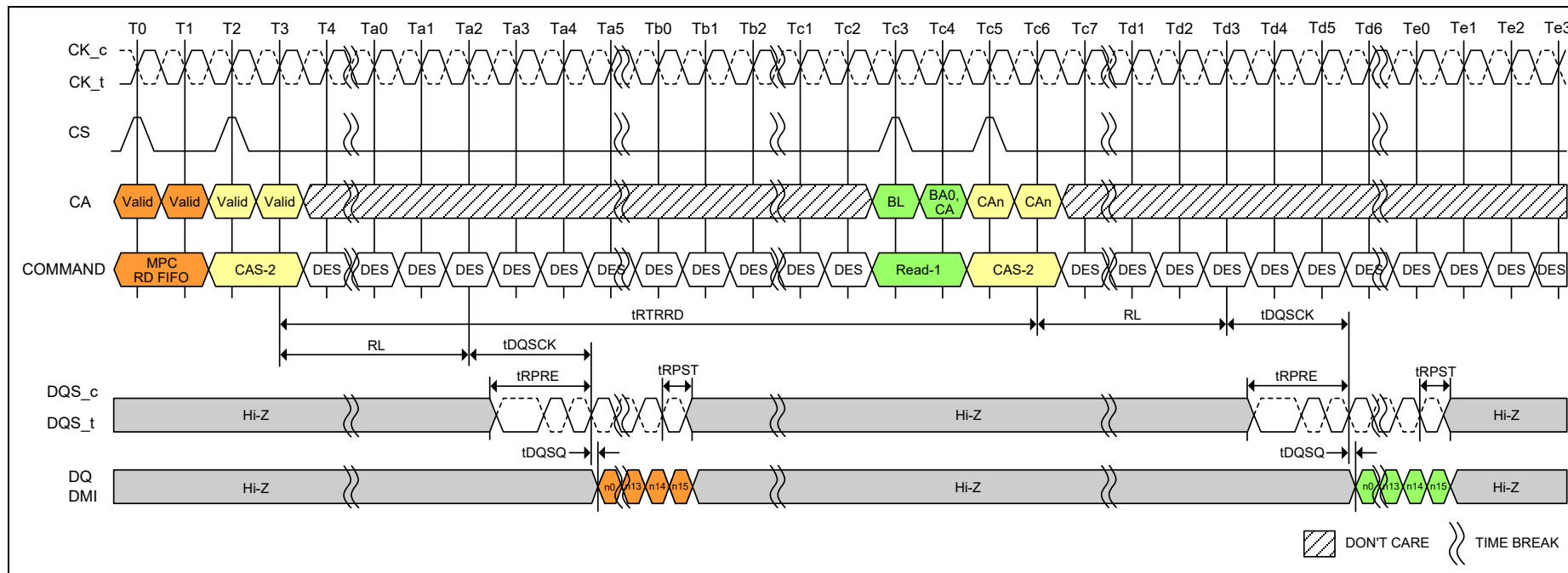
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC [WR-FIFO] is tWRWTR.
3. Seamless MPC [WR-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [WR-FIFO] uses the same command-to-data timing relationship (WL, tDQSS, tDQS2DQ) as a Write-1 command.
5. A maximum of 5 MPC [WR-FIFO] commands may be executed consecutively without corrupting FIFO data.  
The 6th MPC [WR-FIFO] command will overwrite the FIFO data from the first command. If fewer than 5 MPC [WR-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
6. For the CAS-2 command following a MPC command, the CAS-2 operands must be driven "LOW".
7. To avoid corrupting the FIFO contents, MPC [RD-FIFO] must immediately follow MPC [WR-FIFO]/CAS-2 without any other command disturbing FIFO pointers in-between.  
FIFO pointers are disturbed by CKE Low, Write, Masked Write, Read, Read DQ Calibration and MRR.
8. BL = 16, Write Postamble = 0.5nCK.
9. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 113 - Write to MPC [Write FIFO] Operation Timing**



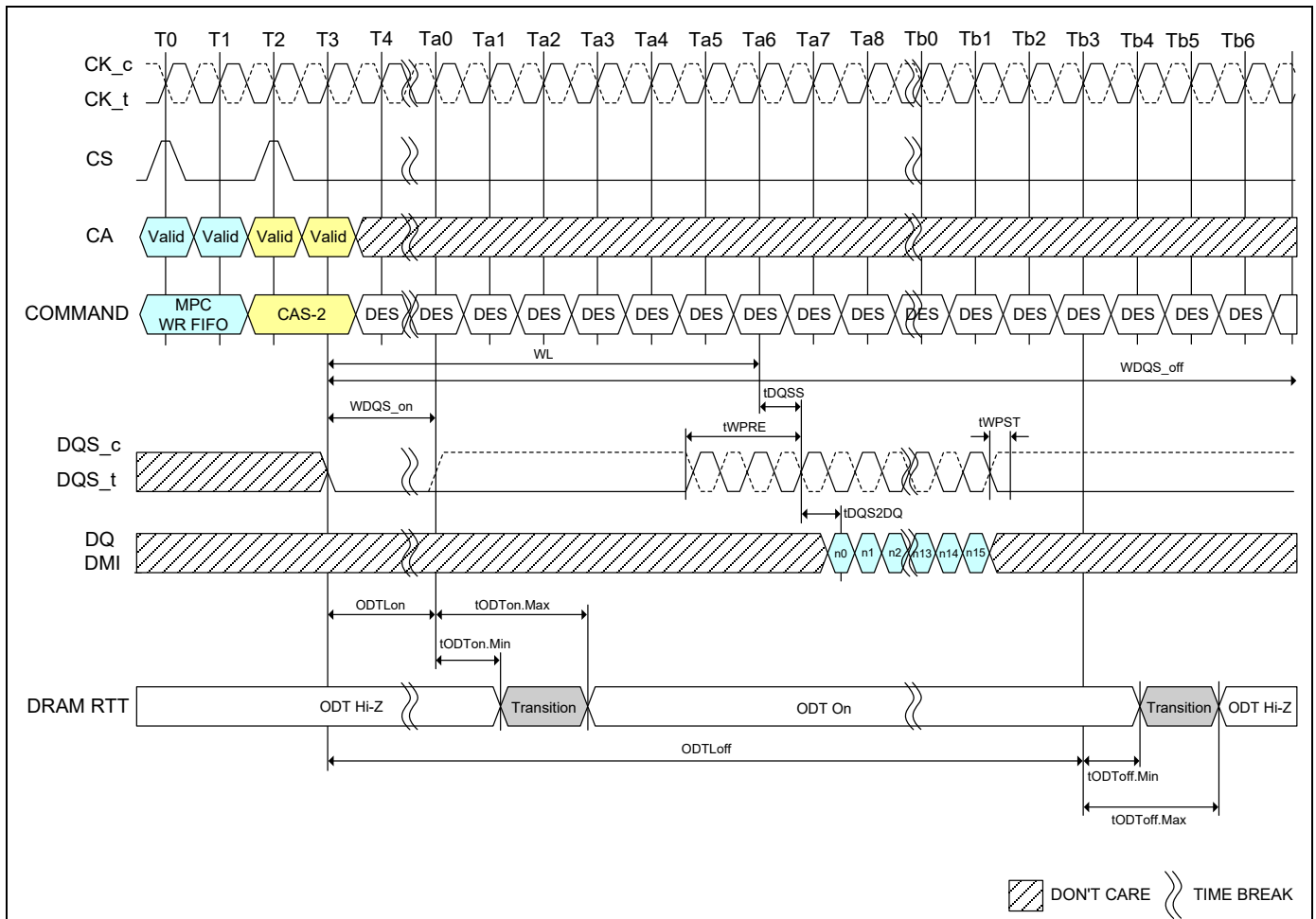
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [WR-FIFO] to MPC [RD-FIFO] is shown as an example of command-to-command timing for MPC. Timing from MPC [WR-FIFO] to MPC [RD-FIFO] is specified in the command-to-command timing table.
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSK, tDQSQ) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW".
7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.
8. BL = 16, Write Postamble = 0.5nCK, Read Preamble: Toggle, Read Postamble: 0.5nCK.
9. DES commands are shown for ease of illustration; other commands may be valid at these times.

### Figure 114 - MPC [Write FIFO] to MPC [Read FIFO] Timing

**Notes:**

1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [RD-FIFO] to Read-1 Operation is shown as an example of command-to-command timing for MPC. Timing from MPC [RD-FIFO] command to Read is tRTRRD.
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK, tDQSQ) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW".
7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.
8. BL = 16, Read Preamble: Toggle, Read Postamble: 0.5nCK.
9. DES commands are shown for ease of illustration; other commands may be valid at these times.

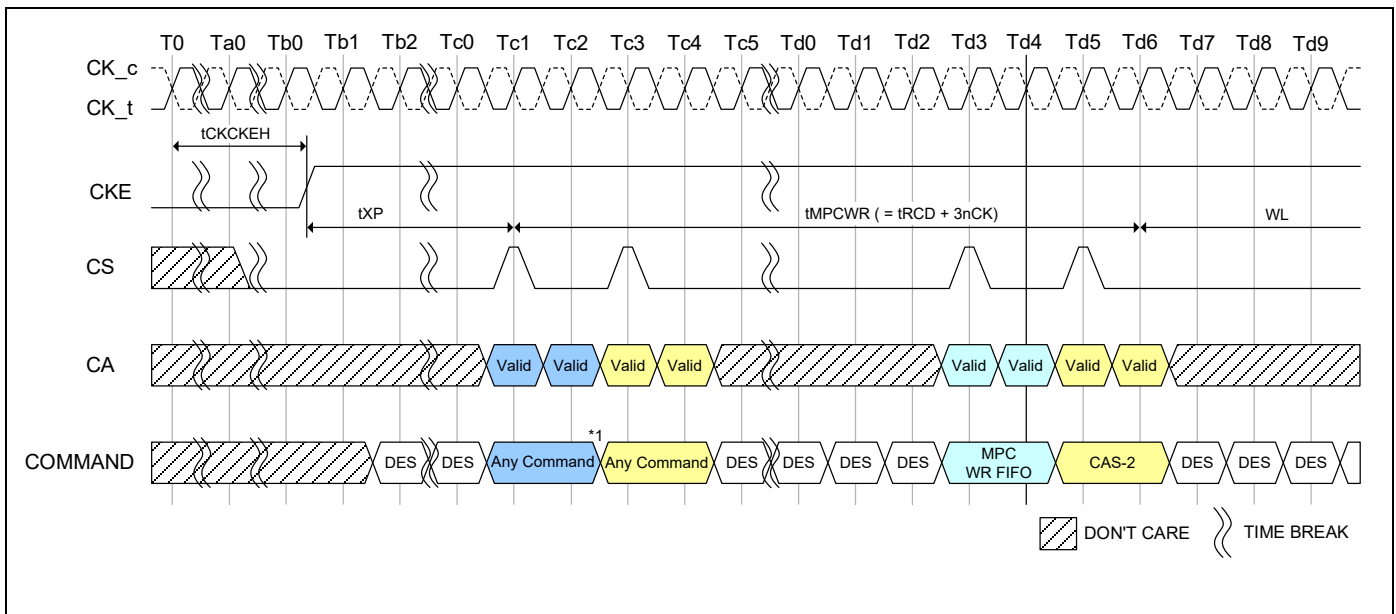
**Figure 115 - MPC [Read FIFO] to Read Timing**

**Notes:**

1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [WR-FIFO] uses the same command-to-data/ODT timing relationship (WL, tDQSS, tDQS2DQ, ODTLon, ODTLoff, tODTOn, tODTOff) as a Write-1 command.
3. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW".
4. BL = 16, Write Postamble = 0.5nCK.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 116 - MPC [Write FIFO] with DQ ODT Timing**



**Notes:**

- Any commands except MPC WR FIFO and other exception commands defined other section in this document (i.e., MPC Read DQ Calibration).
- DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 117 - Power Down Exit to MPC [Write FIFO] Timing****Table 63 - MPC [Write FIFO] AC Timing**

| Parameter                                                                                      | Symbol             | Min/Max | Data Rate               | Unit | Note |
|------------------------------------------------------------------------------------------------|--------------------|---------|-------------------------|------|------|
| MPC Write FIFO Timing                                                                          |                    |         |                         |      |      |
| Additional time after t <sub>XP</sub> has expired until MPC [Write FIFO] command may be issued | t <sub>MPCWR</sub> | Min     | t <sub>RCD</sub> + 3nCK |      |      |

**7.4.33 DQS Interval Oscillator**

As voltage and temperature change on the SDRAM die, the DQS clock tree delay will shift and may require re-training. The LPDDR4/LPDDR4X SDRAM includes an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The DQS Oscillator will provide the controller with important information regarding the need to re-train, and the magnitude of potential error.

The DQS Interval Oscillator is started by issuing a MPC [Start DQS Osc] command with OP[6:0] set as described in the MPC Operation section, which will start an internal ring oscillator that counts the number of time a signal propagates through a copy of the DQS clock tree.

The DQS Oscillator may be stopped by issuing a MPC [Stop DQS Osc] command with OP[6:0] set as described in the MPC Operation section, or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MR23 for more information). If MR23 is set to automatically stop the DQS Oscillator, then the MPC [Stop DQS Osc] command should not be used (illegal). When the DQS Oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MR18 and MR19.



The controller may adjust the accuracy of the result by running the DQS Interval Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\text{DQS Oscillator Granularity Error} = \frac{2 * (\text{DQS delay})}{\text{Run Time}}$$

Where:

Run Time = total time between start and stop commands

DQS delay = the value of the DQS clock tree delay (tDQS2DQ min/max)

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific.

Therefore, the total accuracy of the DQS Oscillator counter is given by:

$$\text{DQS Oscillator Accuracy} = 1 - \text{Granularity Error} - \text{Matching Error}$$

**Example:** If the total time between start and stop commands is 100nS, and the maximum DQS clock tree delay is 800pS (tDQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\text{DQS Oscillator Granularity Error} = \frac{2 * (0.8\text{nS})}{100\text{nS}} = 1.6\%$$

This equates to a granularity timing error of 12.8pS.

Assuming a circuit Matching Error of 5.5pS across voltage and temperature, then the accuracy is:

$$\text{DQS Oscillator Accuracy} = 1 - \frac{12.8 + 5.5}{800} = 97.7\%$$

**Example:** Running the DQS Oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 500nS, and the maximum DQS clock tree delay is 800pS (tDQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\text{DQS Oscillator Granularity Error} = \frac{2 * (0.8\text{nS})}{500\text{nS}} = 0.32\%$$

This equates to a granularity timing error or 2.56pS.

Assuming a circuit Matching Error of 5.5pS across voltage and temperature, then the accuracy is:

$$\text{DQS Oscillator Accuracy} = 1 - \frac{2.56 + 5.5}{800} = 99.0\%$$

The result of the DQS Interval Oscillator is defined as the number of DQS Clock Tree Delays that can be counted within the “run time,” determined by the controller. The result is stored in MR18-OP[7:0] and MR19-OP[7:0]. MR18 contains the least significant bits (LSB) of the result, and MR19 contains the most significant bits (MSB) of the result. MR18 and MR19 are overwritten by the SDRAM when a MPC-1 [Stop DQS Osc] command is received. The SDRAM counter will count to its maximum value (=2<sup>16</sup>) and stop. If the maximum value is read from the mode registers, then the memory controller must assume that the counter overflowed the register and discard the result. The longest “run time” for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\text{Longest Run Time Interval} = 2^{16} * \text{tDQS2DQ}(\text{min}) = 2^{16} * 0.2\text{nS} = 13.1\mu\text{S}$$



### 7.4.33.1 Interval Oscillator matching error

The interval oscillator matching error is defined as the difference between the DQS training ckt (interval oscillator) and the actual DQS clock tree across voltage and temperature.

- Parameters:
  - $t_{DQS2DQ}$ : Actual DQS clock tree delay
  - $t_{DQS_{osc}}$ : Training ckt(interval oscillator) delay
  - $OSC_{Offset}$ : Average delay difference over voltage and temp (shown in Figure118)
  - $OSC_{Match}$ : DQS oscillator matching error (Table 64)

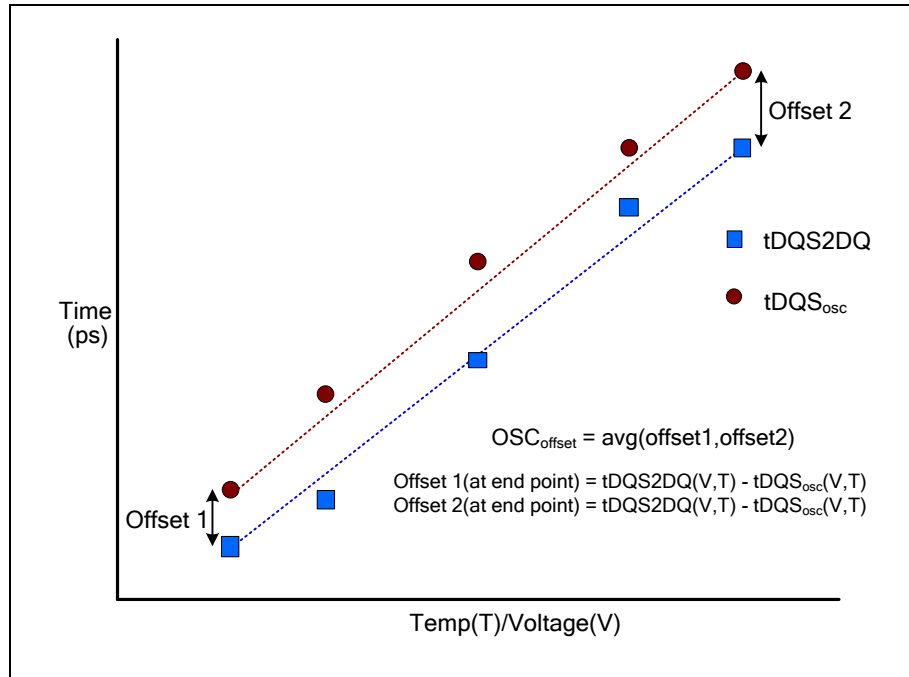


Figure 118 - Interval oscillator offset  $OSC_{Offset}$

- $OSC_{Match}$ :

$$OSC_{Match} = [t_{DQS2DQ}(V,T) - t_{DQS_{osc}}(V,T) - OSC_{Offset}]$$

- $t_{DQS_{osc}}$ :

$$t_{DQS_{osc}}(V,T) = \frac{Runtime}{2 * Count}$$



Table 64 - DQS Oscillator Matching Error Specification

| Parameter                     | Symbol    | Min  | Max | Unit | Notes         |
|-------------------------------|-----------|------|-----|------|---------------|
| DQS Oscillator Matching Error | OSCMATCH  | -20  | 20  | pS   | 1,2,3,4,5,6,7 |
| DQS Oscillator Offset         | OSCOFFSET | -100 | 100 | pS   | 2,4,7         |

**Notes:**

1. The OSCMATCH is the matching error per between the actual DQS and DQS interval oscillator over voltage and temp.
2. This parameter will be characterized or guaranteed by design.
3. The OSCMATCH is defined as the following:

$$OSCMATCH = [tDQS2DQ(V,T) - tDQSOSC(V,T) - OSCOFFSET]$$

Where  $tDQS2DQ(V,T)$  and  $tDQSOSC(V,T)$  are determined over the same voltage and temp conditions.

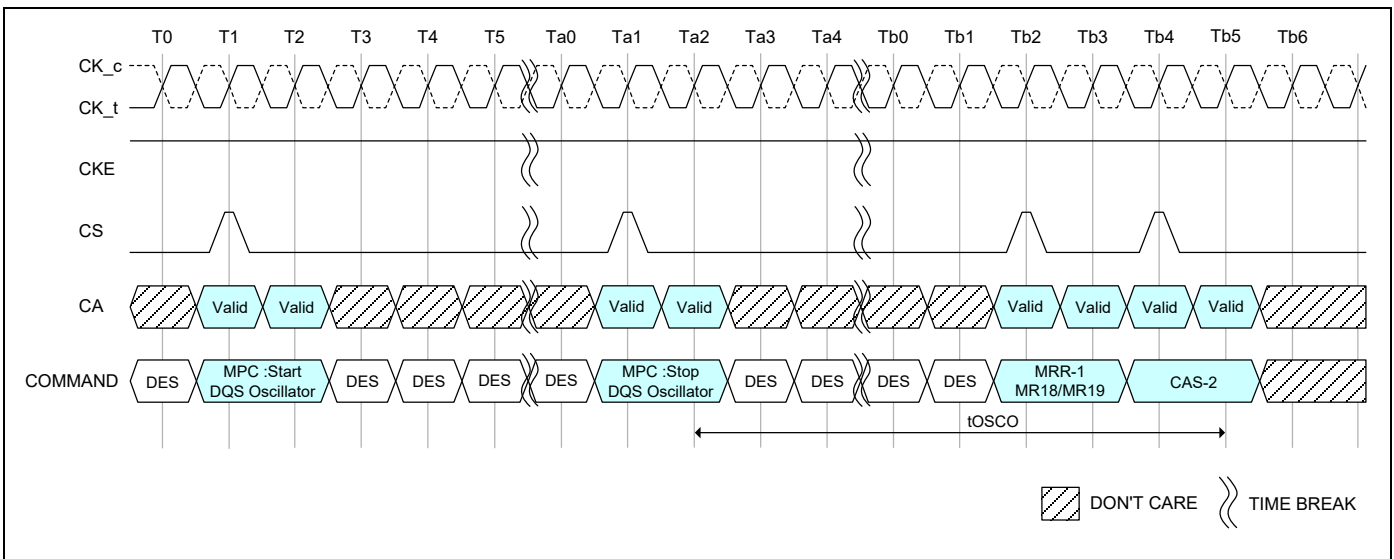
4. The runtime of the oscillator must be at least 200nS for determining  $tDQSOSC(V,T)$ .

$$tDQSOSC(V,T) = \frac{\text{Runtime}}{2 * \text{Count}}$$

5. The input stimulus for  $tDQS2DQ$  will be consistent over voltage and temp conditions.
6. The OSCOFFSET is the average difference of the endpoints across voltage and temp.
7. These parameters are defined per channel.
8.  $tDQS2DQ(V,T)$  delay will be the average of DQS to DQ delay over the runtime period.

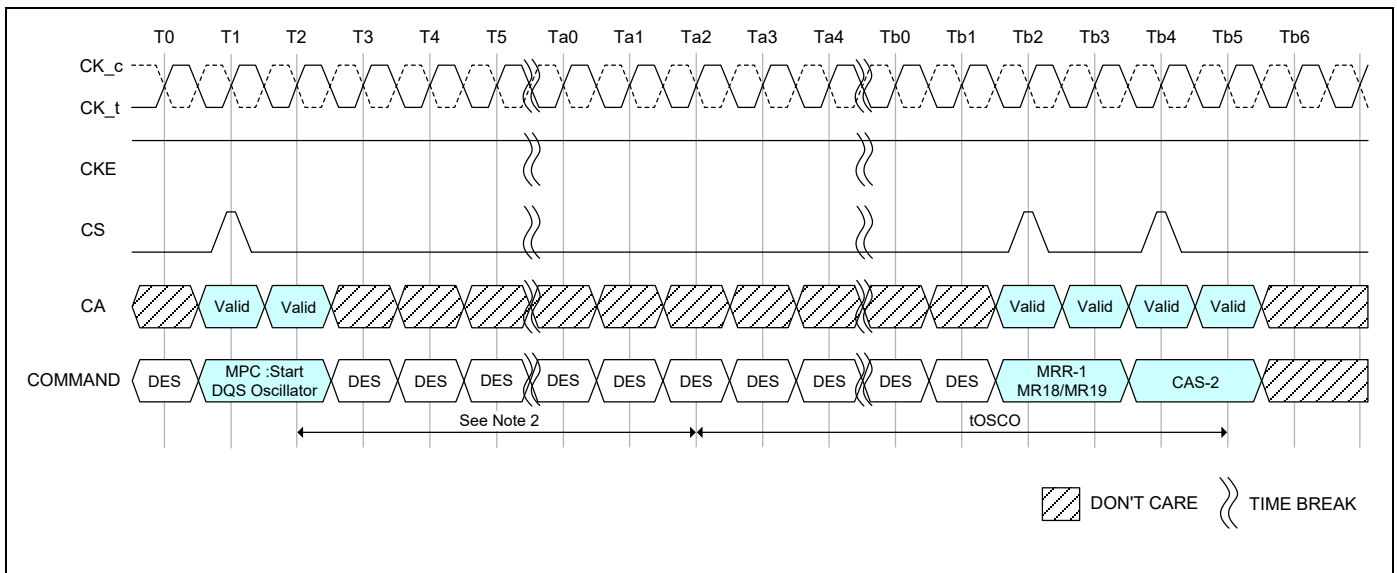
**7.4.33.2 DQS Interval Oscillator Readout Timing**

OSC Stop to its counting value readout timing is shown in Figure 119 and Figure 120 and Table 65.

**Notes:**

1. DQS interval timer run time setting: MR23 OP[7:0] = 00000000.
2. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 119 - In case of DQS Interval Oscillator is stopped by MPC Command**

**Notes:**

1. DQS interval timer run time setting: MR23 OP[7:0]  $\neq$  00000000.
2. Setting counts of MR23.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 120 - In case of DQS Interval Oscillator is stopped by DQS interval timer****Table 65 - DQS Interval Oscillator AC Timing**

| Parameter                                         | Symbol | Min/Max | Value           | Unit | Note |
|---------------------------------------------------|--------|---------|-----------------|------|------|
| Delay time from OSC stop to Mode Register Readout | tOSCO  | Min     | Max(40nS, 8nCK) | nS   |      |

**Note:**

1. Start DQS OSC command is prohibited until tOSCO(Min) is satisfied.



### 7.4.34 READ Preamble Training

LPDDR4/LPDDR4X READ Preamble Training is supported through the MPC function.

This mode can be used to train or read level the DQS receivers. Once READ Preamble Training is enabled by MR13 OP[1] = 1, the LPDDR4/LPDDR4X SDRAM will drive DQS\_t LOW, DQS\_c HIGH within tSDO and remain at these levels until an MPC DQ READ Calibration command is issued.

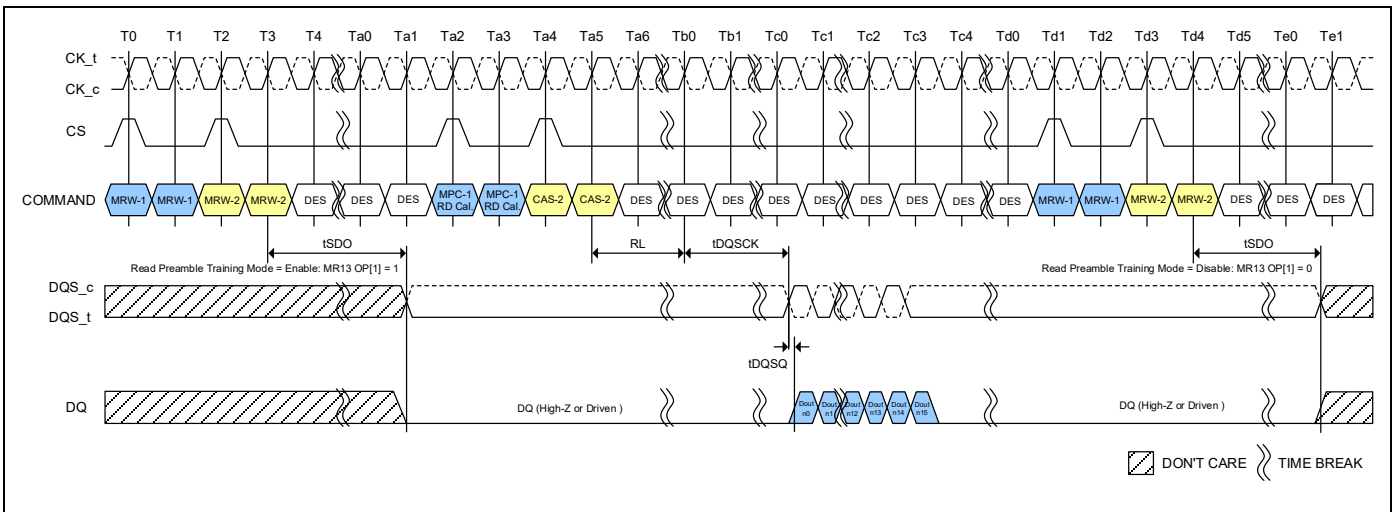
During READ Preamble Training the DQS pre-amble provided during normal operation will not be driven by the DRAM. Once the MPC DQ READ Calibration command is issued, the DRAM will drive DQS\_t/DQS\_c and DQ like a normal READ burst after RL and tDQSCK. Prior to the MPC DQ READ Calibration command, the DRAM may or may not drive DQ[15:0] in this mode.

While in READ Preamble Training Mode, only READ DQ Calibration commands may be issued.

- Issue an MPC [RD DQ Calibration] command followed immediately by a CAS-2 command.
- Each time an MPC [RD DQ Calibration] command followed by a CAS-2 is received by the LPDDR4/LPDDR4X SDRAM, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins.
- The data pattern will be inverted for I/O pins with a '1' programmed in the corresponding invert mask mode register bit.
- Note that the pattern is driven on the DMI pins, but no data bus inversion function is enabled, even if Read DBI is enabled in the DRAM mode register.
- This command can be issued every tCCD seamlessly.
- The operands received with the CAS-2 command must be driven LOW.

READ Preamble Training is exited within tSDO after setting MR13 OP[1] = 0.

Reference Figure 121 and Table 66.



**Note:**

1. Read DQ Calibration supports only BL16 operation.

**Figure 121 - Read Preamble Training**

**Table 66 - Read Preamble Training Timing Parameter**

| Parameter                            | Symbol | Min | Max              | Unit | Note |
|--------------------------------------|--------|-----|------------------|------|------|
| Delay from MRW command to DQS Driven | tSDO   | -   | Max(12nCK, 20nS) | -    |      |



### 7.4.35 Multi-Purpose Command (MPC)

LPDDR4/LPDDR4X SDRAMs use the MPC command to issue a NOP and to access various training modes. The MPC command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table (Table 87). The MPC command has seven operands (OP[6:0]) that are decoded to execute specific commands in the SDRAM. OP[6] is a special bit that is decoded on the first rising CK edge of the MPC command. When OP[6]=0 then the SDRAM executes a NOP (no operation) command, and when OP[6]=1 then the SDRAM further decodes one of several training commands.

When OP[6]=1 and when the training command includes a Read or Write operation, the MPC command must be followed immediately by a CAS-2 command. For training commands that Read or Write the SDRAM, read latency (RL) and write latency (WL) are counted from the second rising CK edge of the CAS-2 command with the same timing relationship as any normal Read or Write command. The operands of the CAS-2 command following a MPC Read/Write command must be driven LOW.

The following MPC commands must be followed by a CAS-2 command:

- Write FIFO
- Read FIFO
- Read DQ Calibration

All other MPC-1 commands do not require a CAS-2 command, including:

- NOP
- Start DQS Interval Oscillator
- Stop DQS Interval Oscillator
- Start ZQ Calibration
- Latch ZQ Calibration

See Table 67 and Table 68, and Figure 122 through Figure 124.

**Table 67 - MPC Command Definition**

| SDRAM Command       | SDR Command Pins |         |    | SDR CA Pins |     |     |     |     |     | CK_t EDGE | Notes |
|---------------------|------------------|---------|----|-------------|-----|-----|-----|-----|-----|-----------|-------|
|                     | CKE              |         | CS | CA0         | CA1 | CA2 | CA3 | CA4 | CA5 |           |       |
|                     | CK_t(n-1)        | CK_t(n) |    |             |     |     |     |     |     |           |       |
| MPC<br>(Train, NOP) | H                | H       | H  | L           | L   | L   | L   | L   | OP6 | R1        | 1, 2  |
|                     |                  |         | L  | OP0         | OP1 | OP2 | OP3 | OP4 | OP5 | R2        |       |

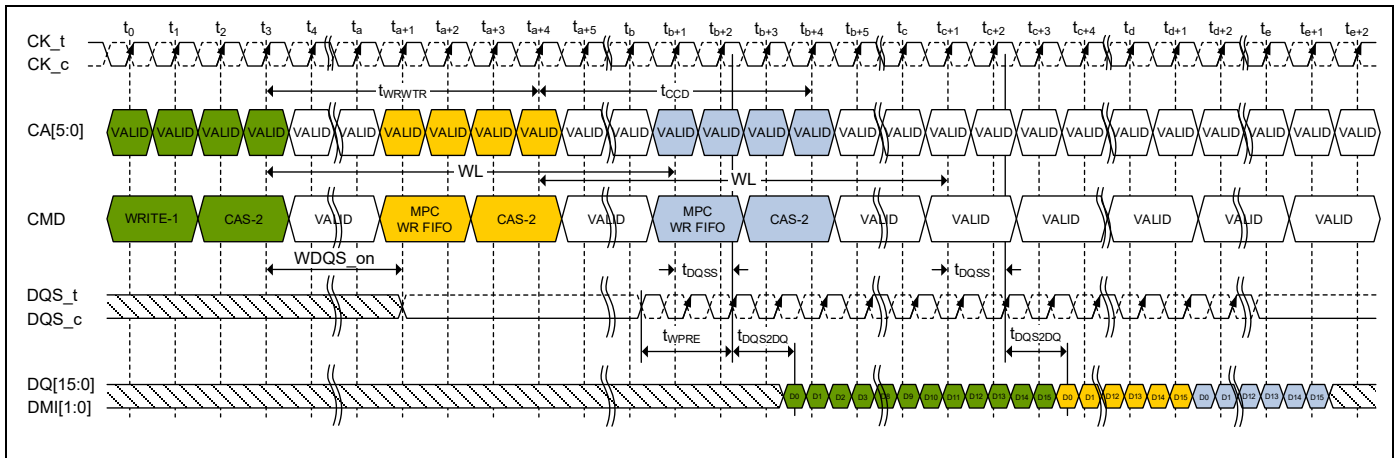
**Table 68 - MPC Command Definition for OP[6:0]**

| Function       | Operand | Data                                                                 | Notes   |
|----------------|---------|----------------------------------------------------------------------|---------|
| Training Modes | OP[6:0] | 0XXXXXX <sub>b</sub> : NOP                                           | 1, 2, 3 |
|                |         | 1000001 <sub>b</sub> : RD FIFO: RD FIFO supports only BL16 operation |         |
|                |         | 1000011 <sub>b</sub> : RD DQ Calibration (MR32/MR40)                 |         |
|                |         | 1000101 <sub>b</sub> : RFU                                           |         |
|                |         | 1000111 <sub>b</sub> : WR FIFO: WR FIFO supports only BL16 operation |         |
|                |         | 1001001 <sub>b</sub> : RFU                                           |         |
|                |         | 1001011 <sub>b</sub> : Start DQS Osc                                 |         |
|                |         | 1001101 <sub>b</sub> : Stop DQS Osc                                  |         |
|                |         | 1001111 <sub>b</sub> : ZQCal Start                                   |         |
|                |         | 1010001 <sub>b</sub> : ZQCal Latch                                   |         |
|                |         | All Others: Reserved                                                 |         |

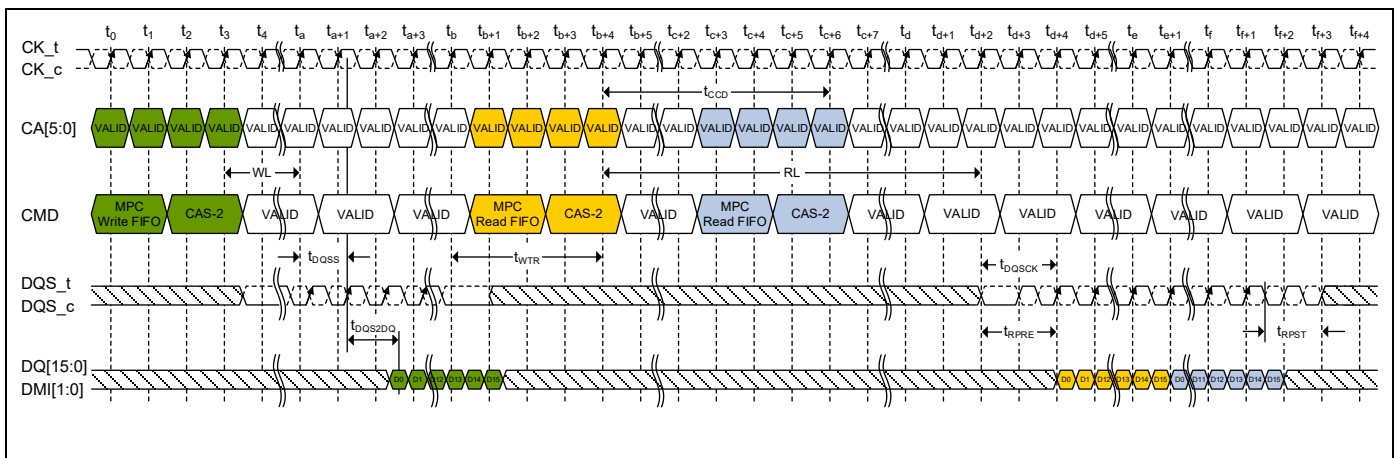
**Notes:**

1. See command truth table (Table 87) for more information.
2. MPC commands for Read or Write training operations must be immediately followed by CAS-2 command consecutively without any other commands in-between. MPC command must be issued first before issuing the CAS-2 command.
3. Write FIFO and Read FIFO commands will only operate as BL16, ignoring the burst length selected by MR1 OP[1:0].



**Notes:**

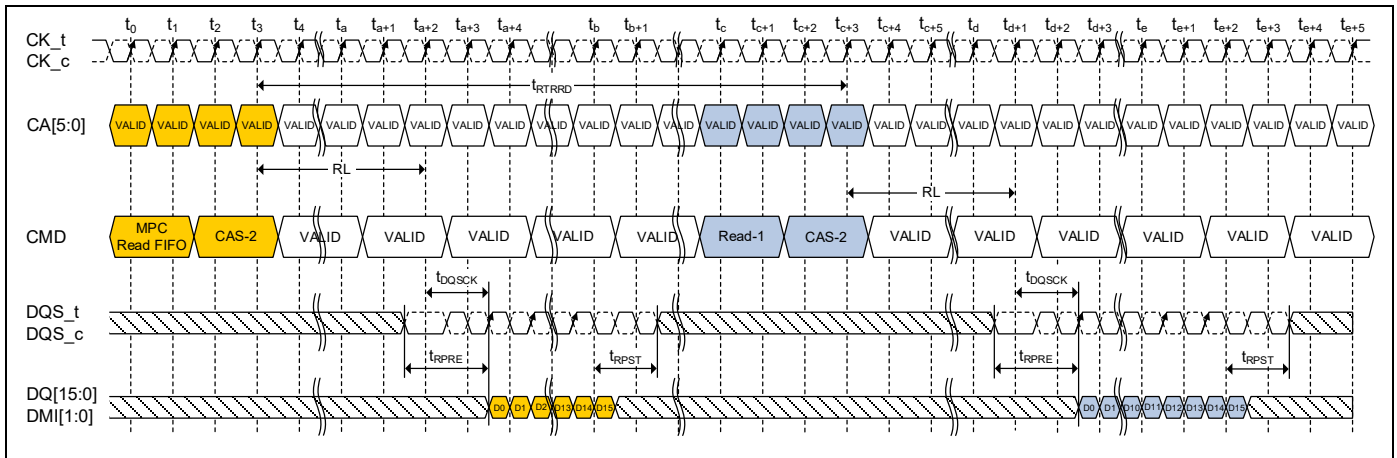
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC [WR-FIFO] is  $t_{WRWTR}$ .
3. Seamless MPC [WR-FIFO] commands may be executed by repeating the command every  $t_{CCD}$  time.
4. MPC [WR-FIFO] uses the same command-to-data timing relationship ( $WL$ ,  $t_{DQSS}$ ,  $t_{DQS2DQ}$ ) as a Write-1 command.
5. A maximum of 5 MPC [WR-FIFO] commands may be executed consecutively without corrupting FIFO data.  
The 6th MPC [WR-FIFO] command will overwrite the FIFO data from the first command. If fewer than 5 MPC [WR-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
6. For the CAS-2 command following a MPC command, the CAS-2 operands must be driven "LOW".
7. To avoid corrupting the FIFO contents, MPC-1 [RD-FIFO] must immediately follow MPC-1 [WR-FIFO]/CAS-2 without any other command disturbing FIFO pointers in-between. FIFO pointers are disturbed by CKE Low, Write, Masked Write, Read, Read DQ Calibration and MRR. See Write Training section for more information on FIFO pointer behavior.

**Figure 122 - MPC [WRITE FIFO] Operation:  $t_{WPST}=2nCK$ ,  $t_{WPRE}=0.5nCK$** **Notes:**

1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every  $t_{CCD}$  time.
3. MPC [RD-FIFO] uses the same command-to-data timing relationship ( $RL$ ,  $t_{DQSS}$ ) as a Read-1 command.
4. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
5. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW".
6. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.

**Figure 123 - MPC [RD FIFO] Read Operation:  $t_{WPST}=2nCK$ ,  $t_{WPRE}=0.5nCK$ ,  $t_{RPST}=1.5nCK$**



**Notes:**

1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [RD-FIFO] to Read-1 Operation is shown as an example of command-to-command timing for MPC. Timing from MPC-1 [RD-FIFO] command to Read is  $t_{RTRRD}$ .
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every  $t_{CCD}$  time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship ( $RL$ ,  $t_{DQSCK}$ ) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW".
7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.

**Figure 124 - MPC [RD FIFO] Operation:  $t_{RPRE}$ =toggling,  $t_{RPST}$ =1.5nCK**



Table 69 - Timing Constraints for Training Commands

| Previous Command           | Next Command               | Minimum Delay                            | Unit | Notes |
|----------------------------|----------------------------|------------------------------------------|------|-------|
| WR/MWR                     | MPC<br>[WR FIFO]           | tWRWTR                                   | nCK  | 1     |
|                            | MPC<br>[RD FIFO]           | Not Allowed                              | -    | 2     |
|                            | MPC<br>[RD DQ Calibration] | WL+RU(tDQSS(max)/tCK) +BL/2+RU(tWTR/tCK) | nCK  |       |
| RD/MRR                     | MPC<br>[WR FIFO]           | tRTRRD                                   | nCK  | 3     |
|                            | MPC<br>[RD FIFO]           | Not Allowed                              | -    | 2     |
|                            | MPC<br>[RD DQ Calibration] | tRTRRD                                   | nCK  | 3     |
| MPC<br>[WR FIFO]           | WR/MWR                     | Not Allowed                              | -    | 2     |
|                            | MPC<br>[WR FIFO]           | tCCD                                     | nCK  |       |
|                            | RD/MRR                     | Not Allowed                              | -    | 2     |
|                            | MPC<br>[RD FIFO]           | WL+RU(tDQSS(max)/tCK) +BL/2+RU(tWTR/tCK) | nCK  |       |
|                            | MPC<br>[RD DQ Calibration] | Not Allowed                              | -    | 2     |
| MPC<br>[RD FIFO]           | WR/MWR                     | tRTRRD                                   | nCK  | 3     |
|                            | MPC<br>[WR FIFO]           | tRTW                                     | nCK  | 4     |
|                            | RD/MRR                     | tRTRRD                                   | nCK  | 3     |
|                            | MPC<br>[RD FIFO]           | tCCD                                     | nCK  |       |
|                            | MPC<br>[RD DQ Calibration] | tRTRRD                                   | nCK  | 3     |
| MPC<br>[RD DQ Calibration] | WR/MWR                     | tRTRRD                                   | nCK  | 3     |
|                            | MPC<br>[WR FIFO]           | tRTRRD                                   | nCK  | 3     |
|                            | RD/MRR                     | tRTRRD                                   | nCK  | 3     |
|                            | MPC<br>[RD FIFO]           | Not Allowed                              | -    | 2     |
|                            | MPC<br>[RD DQ Calibration] | tCCD                                     | nCK  |       |

**Notes:**

1.  $tWRWTR = WL + BL/2 + RU(tDQSS(max)/tCK) + \max(RU(7.5nS/tCK), 8nCK)$ .
2. No commands are allowed between MPC [WR FIFO] and MPC-1 [RD FIFO] except MRW commands related to training parameters.
3.  $tRTRRD = RL + RU(tDQSS(max)/tCK) + BL/2 + RD(tRPST) + \max(RU(7.5nS/tCK), 8nCK)$ .
4. tRTW:  
In Case of DQ ODT Disable MR11 OP[2:0] = 000<sub>b</sub>:  
 $RL + RU(tDQSS(max)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)$   
In Case of DQ ODT Enable MR11 OP[2:0] ≠ 000<sub>b</sub>:  
 $RL + RU(tDQSS(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODT_{on,min}/tCK) + 1$



### 7.4.36 Thermal Offset

Because of their tight thermal coupling with the LPDDR4/LPDDR4X SDRAM, hot spots on an SOC can induce thermal gradients across the LPDDR4/LPDDR4X SDRAM. As these hot spots may not be located near the device thermal sensor, the devices' temperature compensated Self Refresh circuit may not generate enough refresh cycles to guarantee memory retention. To address this shortcoming, the controller can provide a thermal offset that the memory uses to adjust its TCSR circuit to ensure reliable operation.

This offset is provided through MR4 OP[6:5] to each channel. This temperature offset may modify refresh behavior for the channel to which the offset is provided. It will take a max of 200µs to have the change reflected in MR4[2:0] for the channel to which the offset is provided. If the induced thermal gradient from the device temperature sensor location to the hot spot location of the controller is larger than 15 degrees C, then Self Refresh mode will not reliably maintain memory contents.

To accurately determine the temperature gradient between the memory thermal sensor and the induced hot spot, the memory thermal sensor location must be provided to the LPDDR4/LPDDR4X SDRAM memory controller.

### 7.4.37 Temperature Sensor

LPDDR4/LPDDR4X SDRAMs feature a temperature sensor whose status can be read from MR4 (see Table 70 and Figure 125.). This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device TOPER may be used to determine whether operating temperature requirements are being met.

LPDDR4/LPDDR4X SDRAMs shall monitor device temperature and update MR4 according to tTSI. Upon assertion of CKE (Low to High transition), the device temperature status bits shall be no older than tTSI. MR4 will be updated even when device is in Self Refresh state with CKE HIGH.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification that applies for the standard or elevated temperature ranges. For example, TCASE may be above 85°C when MR4[2:0] equals 'b011'. LPDDR4/LPDDR4X SDRAMs shall allow for 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller reconfigures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

To assure proper operation using the temperature sensor, applications should consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + \text{tTSI} + \text{SysRespDelay}) \leq 2^{\circ}\text{C}$$

Table 70 - Temperature Sensor

| Parameter                   | Symbol       | Min/Max | Value            | Unit | Notes |
|-----------------------------|--------------|---------|------------------|------|-------|
| System Temperature Gradient | TempGradient | Max     | System Dependent | °C/s |       |
| MR4 Read Interval           | ReadInterval | Max     | System Dependent | mS   |       |
| Temperature Sensor Interval | tTSI         | Max     | 32               | mS   |       |
| System Response Delay       | SysRespDelay | Max     | System Dependent | mS   |       |
| Device Temperature Margin   | TempMargin   | Max     | 2                | °C   |       |



For example, if TempGradient is 10°C/s and the SysRespDelay is 1 mS:

$$(10^{\circ}\text{C/s}) \times (\text{ReadInterval} + 32\text{mS} + 1\text{mS}) \leq 2^{\circ}\text{C}$$

In this case, ReadInterval shall be no greater than 167 mS.

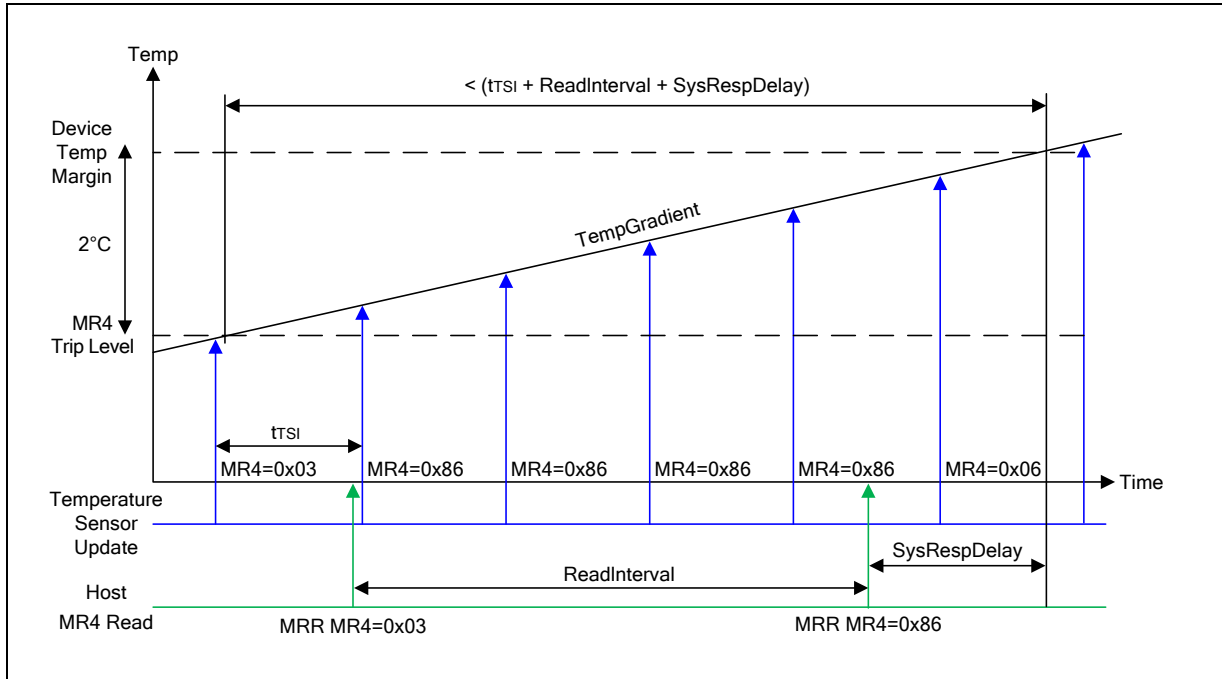


Figure 125 - Temperature Sensor Timing



### 7.4.38 ZQ Calibration

The MPC command is used to initiate ZQ Calibration, which calibrates the output driver impedance across process, temperature, and voltage. ZQ Calibration occurs in the background of device operation.

There are two ZQ Calibration modes initiated with the MPC command: ZQCal Start, and ZQCal Latch. ZQCal Start initiates the SDRAM's calibration procedure, and ZQCal Latch captures the result and loads it into the SDRAM's drivers.

A ZQCal Start command may be issued anytime the LPDDR4/LPDDR4X SDRAM is not in a power-down state. A ZQCal Latch Command may be issued anytime outside of power-down after  $t_{ZQCAL}$  has expired and all DQ bus operations have completed. The CA Bus must maintain a Deselect state during  $t_{ZQLAT}$  to allow CA ODT calibration settings to be updated. The following mode register fields that modify I/O parameters cannot be changed following a ZQCal Start command and before  $t_{ZQCAL}$  has expired:

- PU-Cal (Pull-up Calibration VOH Point)
- PDDS (Pull Down Drive Strength and Rx Termination)
- DQ-ODT (DQ ODT Value)
- CA-ODT (CA ODT Value)

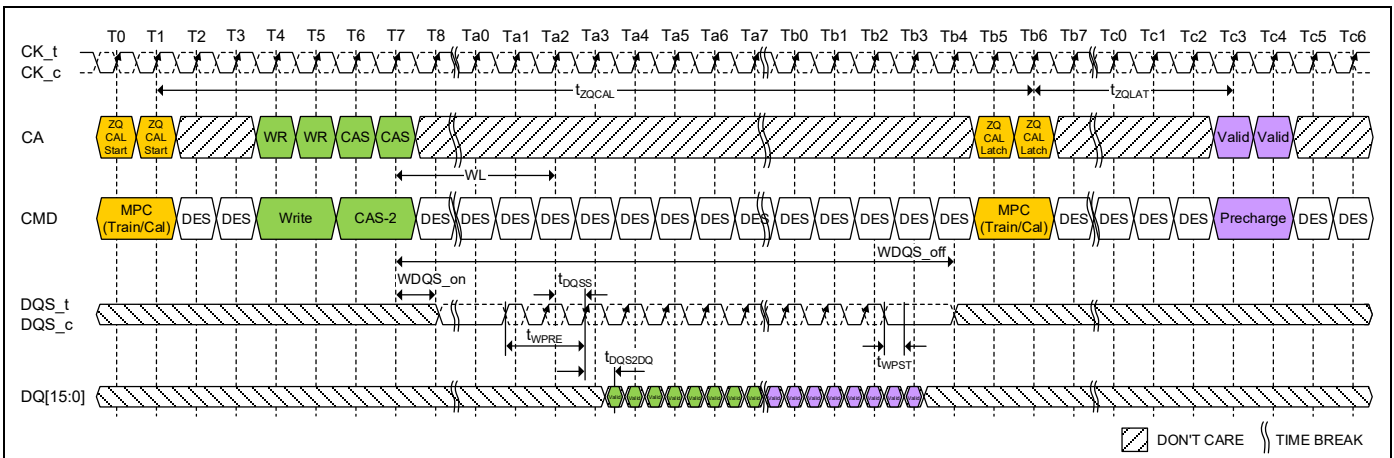
#### 7.4.38.1 ZQCal Reset

The ZQCal Reset command resets the output impedance calibration to a default accuracy of +/- 30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to +/- 30% when ZQCal Start and ZQCal Latch commands are not used. See Table 71 and Figure 126.

The ZQCal Reset command is executed by writing MR10 OP[0]= 1<sub>b</sub>.

**Table 71 - ZQCal Timing Parameters**

| Parameter                 | Symbol        | Min/Max | Value                            | Unit    |
|---------------------------|---------------|---------|----------------------------------|---------|
| ZQ Calibration Time       | $t_{ZQCAL}$   | Min     | 1                                | $\mu$ S |
| ZQ Calibration Latch Time | $t_{ZQLAT}$   | Min     | $\max(30\text{nS}, 8\text{nCK})$ | nS      |
| ZQ Calibration Reset Time | $t_{ZQRESET}$ | Min     | $\max(50\text{nS}, 3\text{nCK})$ | nS      |



#### Notes:

1. Write and Precharge operations shown for illustrative purposes.  
Any single or multiple valid commands may be executed within the  $t_{ZQCAL}$  time and prior to latching the results.
2. Before the ZQ-Latch command can be executed, any prior commands utilizing the DQ bus must have completed.  
Write commands with DQ Termination must be given enough time to turn off the DQ-ODT before issuing the ZQ-Latch command.  
See the ODT section for ODT timing.

**Figure 126 - ZQCal Timing**



#### 7.4.38.2 ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm  $\pm 1\%$  tolerance external resistor must be connected between the ZQ pin and VDDQ.

If the system configuration shares the CA bus to form an x32 (or wider) channel, the ZQ pin of each die's x16 channel shall use a separate ZQCal resistor.

If the system configuration has more than one rank, and if the ZQ pins of both ranks are attached to a single resistor, then the SDRAM controller must ensure that the ZQCal's don't overlap.

The total capacitive loading on the ZQ pin must be limited to 25pF.

Example: If a system configuration shares a CA bus between 'n' channels to form a n \* 16 wide bus, and no means are available to control the ZQCal separately for each channel (i.e., separate CS, CKE, or CK), then each x16 channel must have a separate ZQCal resistor.

Example: For an x32, two rank system, each x16 channel must have its own ZQCal resistor, but the ZQCal resistor can be shared between ranks on each x16 channel. In this configuration, the CS signal can be used to ensure that the ZQCal commands for Rank[0] and Rank[1] don't overlap.

#### 7.4.39 Pull Up/Pull Down Driver Characteristics and Calibration – LPDDR4

The characteristics and calibration are shown in Table 72 through Table 74.

**Table 72 - Pull-down Driver Characteristics, with ZQ Calibration**

| RONPD,nom | Resistor | Min | Nom | Max | Unit  |
|-----------|----------|-----|-----|-----|-------|
| 40 Ohm    | RON40PD  | 0.9 | 1   | 1.1 | RZQ/6 |
| 48 Ohm    | RON48PD  | 0.9 | 1   | 1.1 | RZQ/5 |
| 60 Ohm    | RON60PD  | 0.9 | 1   | 1.1 | RZQ/4 |
| 80 Ohm    | RON80PD  | 0.9 | 1   | 1.1 | RZQ/3 |
| 120 Ohm   | RON120PD | 0.9 | 1   | 1.1 | RZQ/2 |
| 240 Ohm   | RON240PD | 0.9 | 1   | 1.1 | RZQ/1 |

**Note:**

1. All value are after ZQ Calibration. Without ZQ Calibration RONPD values are  $\pm 30\%$ .

**Table 73 - Pull-Up Characteristics, with ZQ Calibration – LPDDR4**

| VOHPU,nom | VOH,nom(mV) | Min | Nom | Max | Unit    |
|-----------|-------------|-----|-----|-----|---------|
| VDDQ/2.5  | 440         | 0.9 | 1   | 1.1 | VOH,nom |
| VDDQ/3    | 367         | 0.9 | 1   | 1.1 | VOH,nom |

**Notes:**

1. All values are after ZQ Calibration. Without ZQ Calibration VOH(nom) values are  $\pm 30\%$ .
2. VOH,nom (mV) values are based on a nominal VDDQ = 1.1V.

**Table 74 - Valid Calibration Points – LPDDR4**

| VOHPU,nom | ODT Value |       |       |       |       |       |
|-----------|-----------|-------|-------|-------|-------|-------|
|           | 240       | 120   | 80    | 60    | 48    | 40    |
| VDDQ/2.5  | VALID     | VALID | VALID | DNU   | DNU   | DNU   |
| VDDQ/3    | VALID     | VALID | VALID | VALID | VALID | VALID |

**Notes:**

1. Once the output is calibrated for a given VOH(nom) calibration point, the ODT value may be changed without recalibration.
2. If the VOH(nom) calibration point is changed, then re-calibration is required.
3. DNU = Do Not Use.



#### 7.4.40 On Die Termination for Command/Address Bus – LPDDR4

ODT (On-Die Termination) is a feature of the LPDDR4 SDRAM that allows the SDRAM to turn on/off termination resistance for CK<sub>t</sub>, CK<sub>c</sub>, CS and CA[5:0] signals without the ODT control pin.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via Mode Register setting.

A simple functional representation of the DRAM ODT feature is shown in Figure 127.

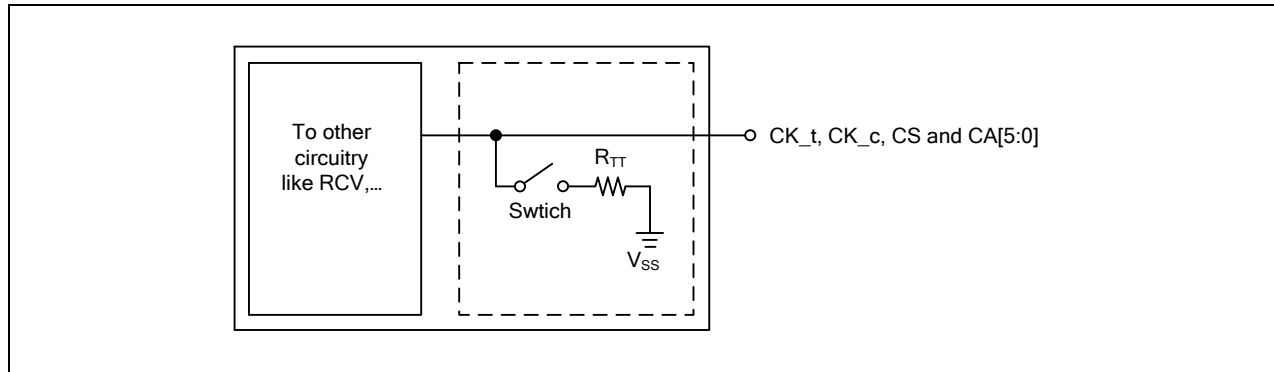


Figure 127 - Functional Representation of CA ODT

##### 7.4.40.1 ODT Mode Register and ODT State Table – LPDDR4

ODT termination values are set and enabled via MR11. The CA bus (CK<sub>t</sub>, CK<sub>c</sub>, CS, CA[5:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA is ODT disabled.

ODT is applied on the CA bus to the CK<sub>t</sub>, CK<sub>c</sub>, CS and CA[5:0] signals. The CA ODT of the device is designed to enable one rank to terminate the entire command bus in a multi-rank system, so only one termination load will be present even if multiple devices are sharing the command signals. For this reason, CA ODT remains on even when the device is in the power-down or Self Refresh power-down states.

The die has a bond pad (ODT<sub>CA</sub>) for multi-rank operations. When the ODT<sub>CA</sub> pad is LOW, the die will not terminate the CA bus regardless of the state of the mode register CA ODT bits (MR11 OP[6:4]). If, however, the ODT<sub>CA</sub> bond pad is HIGH, and the mode register CA ODT bits are enabled, the die will terminate the CA bus with the ODT values found in MR11 OP[6:4]. In a multi-rank system, the terminating rank should be trained first, followed by the non-terminating rank(s). See Table 75.

Table 75 - Command Bus ODT State – LPDDR4

| ODTE-CA<br>MR11[6:4]   | ODT <sub>CA</sub><br>bond pad | ODTD-CA<br>MR22[5]  | ODTF-CK<br>MR22[3]  | ODTF-CS<br>MR22[4]  | ODT State<br>for CA | ODT State<br>for CK <sub>t</sub> /CK <sub>c</sub> | ODT State<br>for CS |
|------------------------|-------------------------------|---------------------|---------------------|---------------------|---------------------|---------------------------------------------------|---------------------|
| Disabled* <sup>1</sup> | Valid* <sup>2</sup>           | Valid* <sup>3</sup> | Valid* <sup>3</sup> | Valid* <sup>3</sup> | Off                 | Off                                               | Off                 |
| Valid* <sup>3</sup>    | 0                             | Valid* <sup>3</sup> | 0                   | 0                   | Off                 | Off                                               | Off                 |
| Valid* <sup>3</sup>    | 0                             | Valid* <sup>3</sup> | 0                   | 1                   | Off                 | Off                                               | On                  |
| Valid* <sup>3</sup>    | 0                             | Valid* <sup>3</sup> | 1                   | 0                   | Off                 | On                                                | Off                 |
| Valid* <sup>3</sup>    | 0                             | Valid* <sup>3</sup> | 1                   | 1                   | Off                 | On                                                | On                  |
| Valid* <sup>3</sup>    | 1                             | 0                   | Valid* <sup>3</sup> | Valid* <sup>3</sup> | On                  | On                                                | On                  |
| Valid* <sup>3</sup>    | 1                             | 1                   | Valid* <sup>3</sup> | Valid* <sup>3</sup> | Off                 | On                                                | On                  |

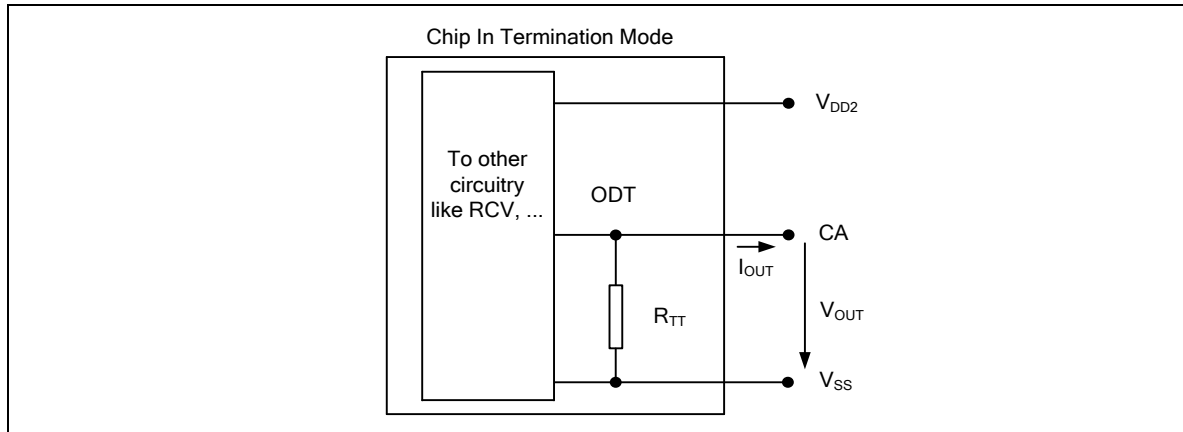
#### Notes:

1. Default Value.
2. "Valid" means "H or L (but a defined logic level)".
3. "Valid" means "0 or 1".
4. The state of ODT<sub>CA</sub> is not changed when the DRAM enters power-down mode. This maintains termination for alternate ranks in multi-rank systems.



#### 7.4.40.2 ODT Mode Register and ODT Characteristics – LPDDR4

The characteristics are provided in Figure 128 and Table 76 and Table 77.



**Figure 128 - On Die Termination for CA**

$$R_{TT} = \frac{V_{out}}{|I_{out}|}$$





**Table 76 - ODT DC Electrical Characteristics, assuming RZQ = 240 Ω ±1% over the entire operating temperature range after a proper ZQ calibration up to 3200 Mbps – LPDDR4**

| MR11[6:4]                       | RTT   | Vout               | Min | Nom | Max | Unit  | Notes   |
|---------------------------------|-------|--------------------|-----|-----|-----|-------|---------|
| 001                             | 240 Ω | VOLdc= 0.1 * VDD2  | 0.8 | 1.0 | 1.1 | RZQ   | 1, 2    |
|                                 |       | VOMdc= 0.33 * VDD2 | 0.9 | 1.0 | 1.1 | RZQ   | 1, 2    |
|                                 |       | VOHdc= 0.5 * VDD2  | 0.9 | 1.0 | 1.2 | RZQ   | 1, 2    |
| 010                             | 120 Ω | VOLdc= 0.1 * VDD2  | 0.8 | 1.0 | 1.1 | RZQ/2 | 1, 2    |
|                                 |       | VOMdc= 0.33 * VDD2 | 0.9 | 1.0 | 1.1 | RZQ/2 | 1, 2    |
|                                 |       | VOHdc= 0.5 * VDD2  | 0.9 | 1.0 | 1.2 | RZQ/2 | 1, 2    |
| 011                             | 80 Ω  | VOLdc= 0.1 * VDD2  | 0.8 | 1.0 | 1.1 | RZQ/3 | 1, 2    |
|                                 |       | VOMdc= 0.33 * VDD2 | 0.9 | 1.0 | 1.1 | RZQ/3 | 1, 2    |
|                                 |       | VOHdc= 0.5 * VDD2  | 0.9 | 1.0 | 1.2 | RZQ/3 | 1, 2    |
| 100                             | 60 Ω  | VOLdc= 0.1 * VDD2  | 0.8 | 1.0 | 1.1 | RZQ/4 | 1, 2    |
|                                 |       | VOMdc= 0.33 * VDD2 | 0.9 | 1.0 | 1.1 | RZQ/4 | 1, 2    |
|                                 |       | VOHdc= 0.5 * VDD2  | 0.9 | 1.0 | 1.2 | RZQ/4 | 1, 2    |
| 101                             | 48 Ω  | VOLdc= 0.1 * VDD2  | 0.8 | 1.0 | 1.1 | RZQ/5 | 1, 2    |
|                                 |       | VOMdc= 0.33 * VDD2 | 0.9 | 1.0 | 1.1 | RZQ/5 | 1, 2    |
|                                 |       | VOHdc= 0.5 * VDD2  | 0.9 | 1.0 | 1.2 | RZQ/5 | 1, 2    |
| 110                             | 40 Ω  | VOLdc= 0.1 * VDD2  | 0.8 | 1.0 | 1.1 | RZQ/6 | 1, 2    |
|                                 |       | VOMdc= 0.33 * VDD2 | 0.9 | 1.0 | 1.1 | RZQ/6 | 1, 2    |
|                                 |       | VOHdc= 0.5 * VDD2  | 0.9 | 1.0 | 1.2 | RZQ/6 | 1, 2    |
| Mismatch CA-CA within clk group |       | 0.33 * VDD2        | -   |     | 2   | %     | 1, 2, 3 |

**Notes:**

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at 0.33\*V<sub>DD2</sub>. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.5\*V<sub>DD2</sub> and 0.1\*V<sub>DD2</sub>.
3. CA to CA mismatch within clock group (CA, CS) variation for a given component including CK<sub>t</sub> and CK<sub>c</sub> (characterized).

$$\text{CA - CA Mismatch} = \frac{\text{RODT(max)} - \text{RODT(min)}}{\text{RODT(avg)}}$$



**Table 77 - ODT DC Electrical Characteristics, assuming RZQ = 240 Ω ±1% over the entire operating temperature range after a proper ZQ calibration for beyond 3200 Mbps – LPDDR4**

| MR11[6:4]                       | RTT   | Vout               | Min | Nom | Max | Unit  | Notes   |
|---------------------------------|-------|--------------------|-----|-----|-----|-------|---------|
| 001                             | 240 Ω | VOLdc= 0.1 * VDD2  | 0.8 | 1.0 | 1.1 | RZQ   | 1, 2    |
|                                 |       | VOMdc= 0.33 * VDD2 | 0.9 | 1.0 | 1.1 | RZQ   | 1, 2    |
|                                 |       | VOHdc= 0.5 * VDD2  | 0.9 | 1.0 | 1.3 | RZQ   | 1, 2    |
| 010                             | 120 Ω | VOLdc= 0.1 * VDD2  | 0.8 | 1.0 | 1.1 | RZQ/2 | 1, 2    |
|                                 |       | VOMdc= 0.33 * VDD2 | 0.9 | 1.0 | 1.1 | RZQ/2 | 1, 2    |
|                                 |       | VOHdc= 0.5 * VDD2  | 0.9 | 1.0 | 1.3 | RZQ/2 | 1, 2    |
| 011                             | 80 Ω  | VOLdc= 0.1 * VDD2  | 0.8 | 1.0 | 1.1 | RZQ/3 | 1, 2    |
|                                 |       | VOMdc= 0.33 * VDD2 | 0.9 | 1.0 | 1.1 | RZQ/3 | 1, 2    |
|                                 |       | VOHdc= 0.5 * VDD2  | 0.9 | 1.0 | 1.3 | RZQ/3 | 1, 2    |
| 100                             | 60 Ω  | VOLdc= 0.1 * VDD2  | 0.8 | 1.0 | 1.1 | RZQ/4 | 1, 2    |
|                                 |       | VOMdc= 0.33 * VDD2 | 0.9 | 1.0 | 1.1 | RZQ/4 | 1, 2    |
|                                 |       | VOHdc= 0.5 * VDD2  | 0.9 | 1.0 | 1.3 | RZQ/4 | 1, 2    |
| 101                             | 48 Ω  | VOLdc= 0.1 * VDD2  | 0.8 | 1.0 | 1.1 | RZQ/5 | 1, 2    |
|                                 |       | VOMdc= 0.33 * VDD2 | 0.9 | 1.0 | 1.1 | RZQ/5 | 1, 2    |
|                                 |       | VOHdc= 0.5 * VDD2  | 0.9 | 1.0 | 1.3 | RZQ/5 | 1, 2    |
| 110                             | 40 Ω  | VOLdc= 0.1 * VDD2  | 0.8 | 1.0 | 1.1 | RZQ/6 | 1, 2    |
|                                 |       | VOMdc= 0.33 * VDD2 | 0.9 | 1.0 | 1.1 | RZQ/6 | 1, 2    |
|                                 |       | VOHdc= 0.5 * VDD2  | 0.9 | 1.0 | 1.3 | RZQ/6 | 1, 2    |
| Mismatch CA-CA within clk group |       | 0.33 * VDD2        | -   |     | 2   | %     | 1, 2, 3 |

**Notes:**

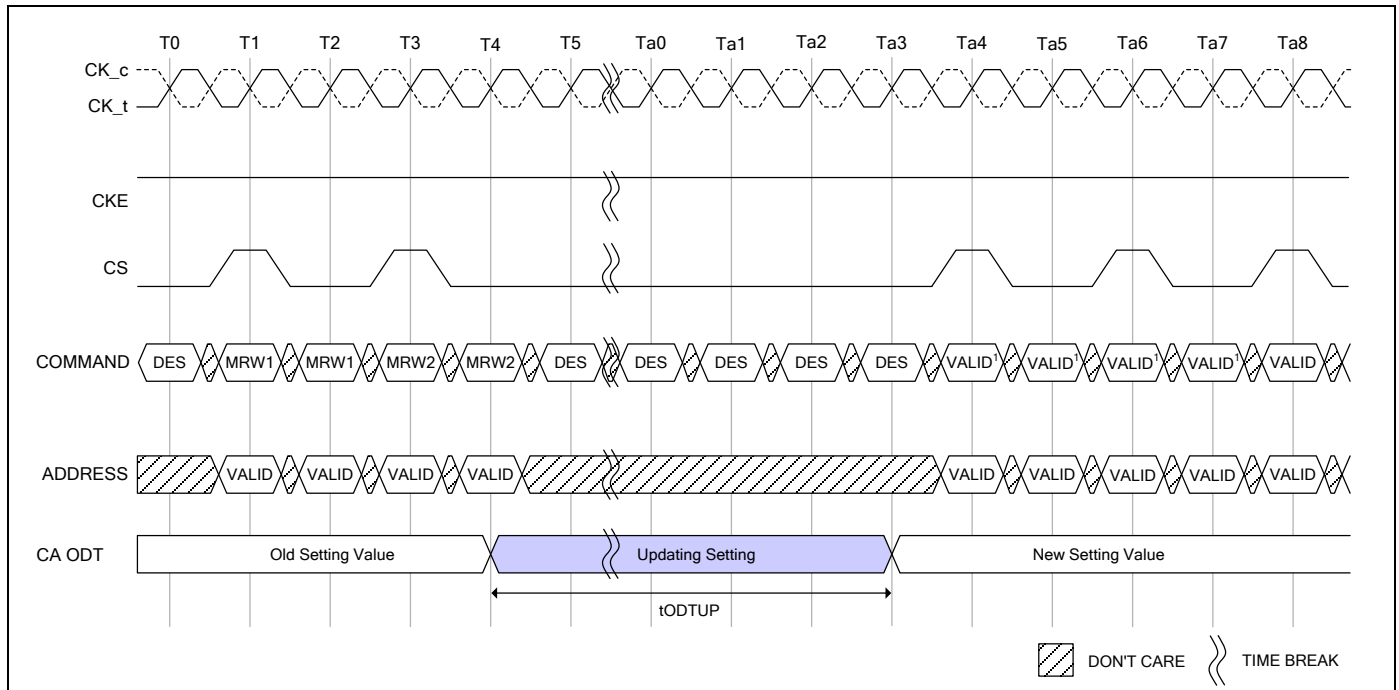
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at 0.33\*V<sub>DD2</sub>. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.5\*V<sub>DD2</sub> and 0.1\*V<sub>DD2</sub>.
3. CA to CA mismatch within clock group (CA, CS) variation for a given component including CK<sub>t</sub> and CK<sub>c</sub> (characterized).

$$\text{CA - CA Mismatch} = \frac{\text{RODT(max)} - \text{RODT(min)}}{\text{RODT(avg)}}$$



### 7.4.40.3 ODT for Command/Address update time

ODT for Command/Address update time after Mode Register set are shown in Figure 129 and Table 78.



**Note:** 1. 4 Clock Cycle Command.

**Figure 129 - ODT for Command/Address setting update timing in 4 Clock Cycle Command**

**Table 78 - ODT CA AC Timing**

| Speed                    |        | Data Rate                          |     | Unit | Note |
|--------------------------|--------|------------------------------------|-----|------|------|
|                          |        | 1600/1866/2133/2400/3200/3733/4267 |     |      |      |
| Parameter                | Symbol | MIN                                | MAX |      |      |
| ODT CA Value Update Time | tODTUP | RU(20nS/tCK(avg))                  | -   |      |      |

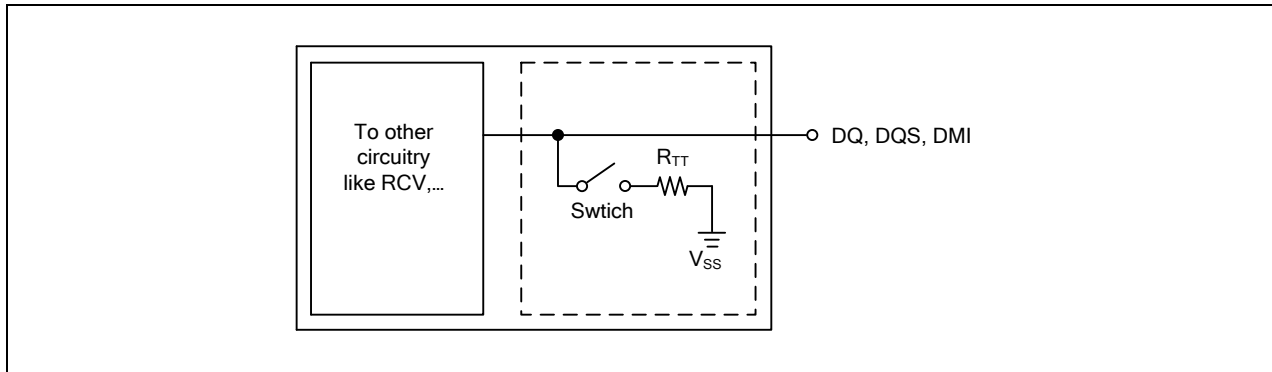


#### 7.4.41 On-Die Termination

ODT (On-Die Termination) is a feature of the LPDDR4/LPDDR4X SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS<sub>t</sub>, DQS<sub>c</sub> and DMI signals without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices during Write or Mask Write operation.

The ODT feature is off and cannot be supported in Power Down and Self Refresh modes.

A simple functional representation of the DRAM ODT feature is shown in Figure 130.



**Figure 130 - Functional Representation of ODT**

The switch is enabled by the internal ODT control logic, which uses the Write-1 or Mask Write-1 command and other mode register control information. The value of  $R_{TT}$  is determined by the settings of Mode Register bits.

##### 7.4.41.1 ODT Mode Register

The ODT Mode is enabled if MR11 OP[2:0] are non-zero. In this case, the value of  $R_{TT}$  is determined by the settings of those bits. The ODT Mode is disabled if MR11 OP[2:0] = 0.

##### 7.4.41.2 Asynchronous ODT

When ODT Mode is enabled in MR11 OP[2:0], DRAM ODT is always Hi-Z. DRAM ODT feature is automatically turned ON asynchronously based on the Write-1 or Mask Write-1 command that DRAM samples. After the write burst is complete, DRAM ODT featured is automatically turned OFF asynchronously.

Following timing parameters apply when DRAM ODT mode is enabled:

- ODTLon, tODTon,min, tODTon,max
- ODTLoff, tODToff,min, tODToff,max

ODTLon is a synchronous parameter and it is the latency from CAS-2 command to tODTon reference.

ODTLon latency is a fixed latency value for each speed bin. Each speed bin has a different ODTLon latency. Minimum  $R_{TT}$  turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on.

Maximum  $R_{TT}$  turn on time (tODTon,max) is the point in time when the ODT resistance is fully on. tODTon,min and tODTon,max are measured once ODTLon latency is satisfied from CAS-2 command.

ODTLoff is a synchronous parameter and it is the latency from CAS-2 command to tODToff reference.

ODTLoff latency is a fixed latency value for each speed bin. Each speed bin has a different ODTLoff latency.

Minimum  $R_{TT}$  turn-off time (tODToff,min) is the point in time when the device termination circuit starts to turn off the ODT resistance.

Maximum ODT turn off time (tODToff,max) is the point in time when the on-die termination has reached high impedance.

tODToff,min and tODToff,max are measured once ODTLoff latency is satisfied from CAS-2 command. See Table 79 and Table 80, and Figure 131.



Table 79 - ODTLon and ODTLoff Latency Values

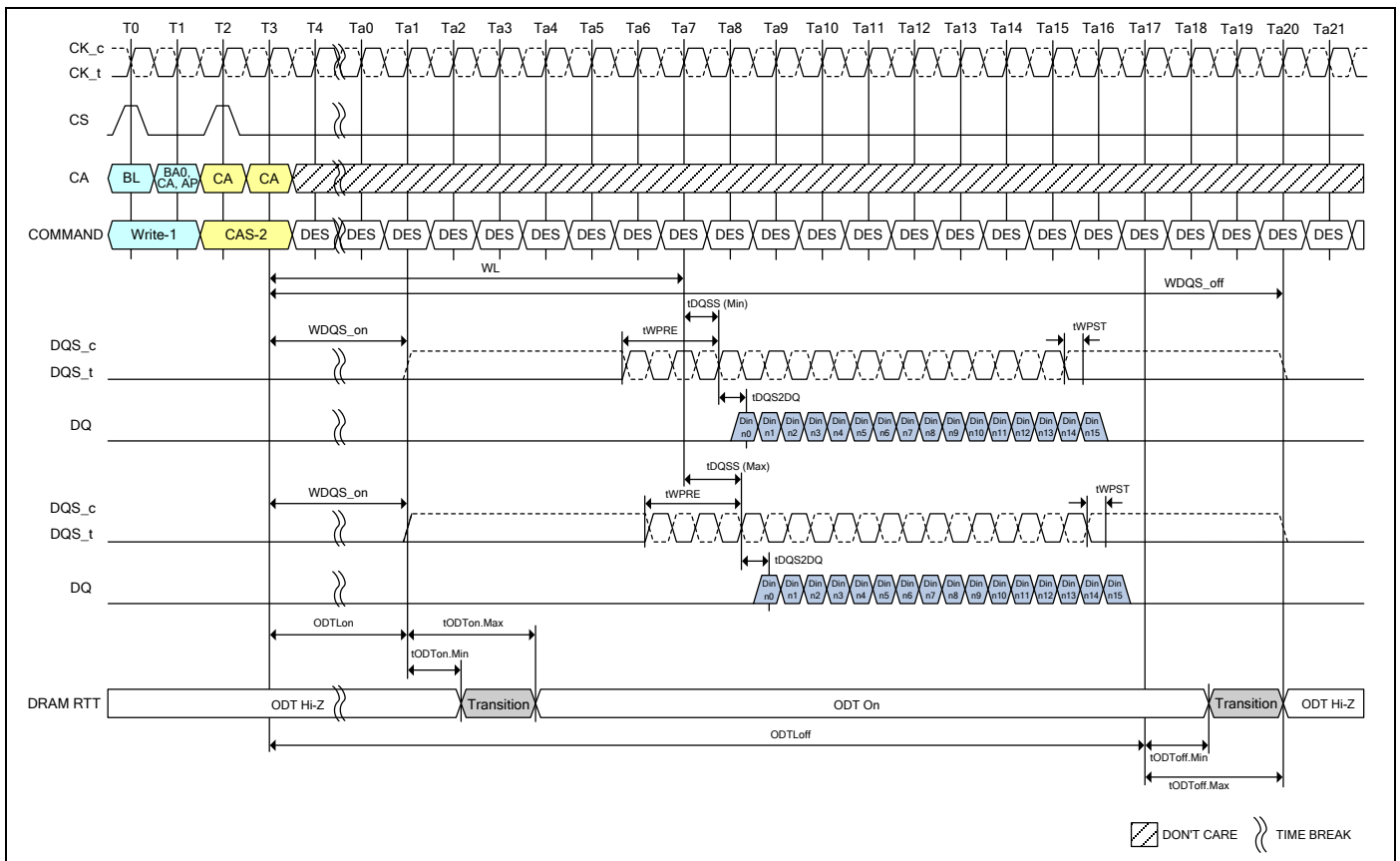
| ODTLon Latency* <sup>1</sup> |            | ODTLoff Latency* <sup>2</sup> |            | Lower Clock<br>Frequency Limit<br>(>) | Upper Clock<br>Frequency Limit<br>(≤) |
|------------------------------|------------|-------------------------------|------------|---------------------------------------|---------------------------------------|
| tWPRE = 2 tCK                |            |                               |            |                                       |                                       |
| WL Set “A”                   | WL Set “B” | WL Set “A”                    | WL Set “B” |                                       |                                       |
| 2                            | 2          | 14                            | 14         | 10                                    | 266                                   |
| 2                            | 2          | 16                            | 18         | 266                                   | 533                                   |
| 2                            | 6          | 18                            | 22         | 533                                   | 800                                   |
| 4                            | 12         | 20                            | 28         | 800                                   | 1066                                  |
| 4                            | 14         | 22                            | 32         | 1066                                  | 1333                                  |
| 6                            | 18         | 24                            | 36         | 1333                                  | 1600                                  |
| 6                            | 20         | 26                            | 40         | 1600                                  | 1866                                  |
| 8                            | 24         | 28                            | 44         | 1866                                  | 2133                                  |
| nCK                          | nCK        | nCK                           | nCK        | MHz                                   | MHz                                   |

**Notes:**

1. ODTLon is referenced from CAS-2 command. See Figure 131.
2. ODTLoff as shown in table assumes BL=16. For BL32, 8 tCK should be added.

Table 80 - Asynchronous ODT Turn On and Turn Off Timing

| Parameter    | 10 - 2133 MHz | Unit |
|--------------|---------------|------|
| tODTon, min  | 1.5           | nS   |
| tODTon, max  | 3.5           | nS   |
| tODToff, min | 1.5           | nS   |
| tODToff, max | 3.5           | nS   |

**Notes:**

1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Din n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 131 - Asynchronous ODTon/ODTOff Timing****7.4.41.3 ODT during Write Leveling**

If ODT is enabled in MR11 OP[2:0], in Write Leveling mode, DRAM always provides the termination on DQS<sub>t</sub>/DQS<sub>c</sub> signals. DQ termination is always off in Write Leveling mode regardless.

**Table 81 - DRAM Termination Function in Write Leveling Mode**

| ODT Enabled in MR11 OP[2:0] | DQS <sub>t</sub> /DQS <sub>c</sub> termination | DQ termination |
|-----------------------------|------------------------------------------------|----------------|
| Disabled                    | OFF                                            | OFF            |
| Enabled                     | ON                                             | OFF            |



#### 7.4.42 On Die Termination for DQ, DQS and DMI

On-Die Termination effective resistance  $R_{TT}$  is defined by MR11 OP[2:0].

ODT is applied to the DQ, DMI, DQS\_t and DQS\_c pins.

A functional representation of the on-die termination is shown in Figure 132.

Electrical characteristics are provided in Table 82 and Table 83.

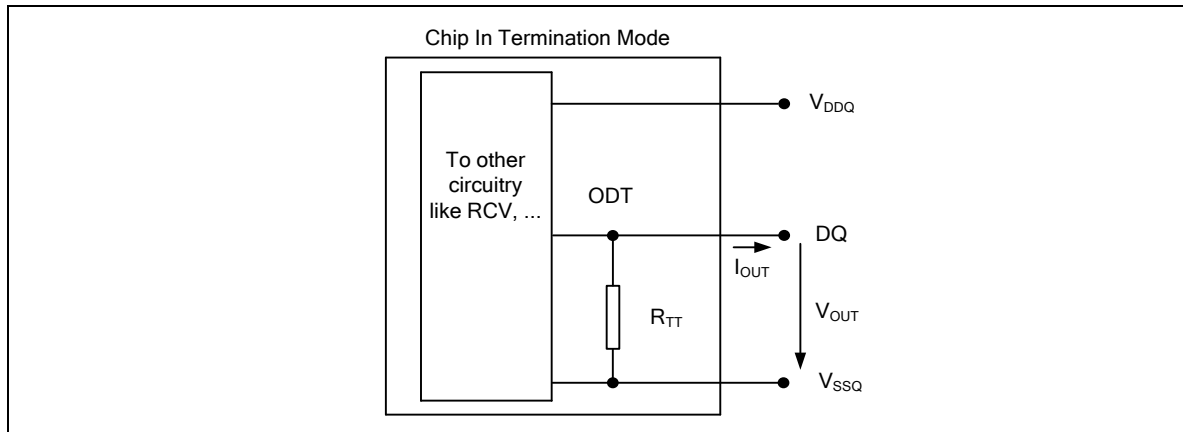


Figure 132 - On Die Termination

$$R_{TT} = \frac{V_{out}}{|I_{out}|}$$



**Table 82 - ODT DC Electrical Characteristics, assuming RZQ = 240 Ω ±1% over the entire operating temperature range after a proper ZQ calibration up to 3200 Mbps – LPDDR4**

| MR11[2:0]                  | R <sub>TT</sub> | V <sub>out</sub>               | Min | Nom | Max | Unit  | Notes   |
|----------------------------|-----------------|--------------------------------|-----|-----|-----|-------|---------|
| 001                        | 240 Ω           | VOLdc= 0.1 * V <sub>DDQ</sub>  | 0.8 | 1.0 | 1.1 | RZQ   | 1, 2    |
|                            |                 | VOMdc= 0.33 * V <sub>DDQ</sub> | 0.9 | 1.0 | 1.1 | RZQ   | 1, 2    |
|                            |                 | VOHdc= 0.5 * V <sub>DDQ</sub>  | 0.9 | 1.0 | 1.2 | RZQ   | 1, 2    |
| 010                        | 120 Ω           | VOLdc= 0.1 * V <sub>DDQ</sub>  | 0.8 | 1.0 | 1.1 | RZQ/2 | 1, 2    |
|                            |                 | VOMdc= 0.33 * V <sub>DDQ</sub> | 0.9 | 1.0 | 1.1 | RZQ/2 | 1, 2    |
|                            |                 | VOHdc= 0.5 * V <sub>DDQ</sub>  | 0.9 | 1.0 | 1.2 | RZQ/2 | 1, 2    |
| 011                        | 80 Ω            | VOLdc= 0.1 * V <sub>DDQ</sub>  | 0.8 | 1.0 | 1.1 | RZQ/3 | 1, 2    |
|                            |                 | VOMdc= 0.33 * V <sub>DDQ</sub> | 0.9 | 1.0 | 1.1 | RZQ/3 | 1, 2    |
|                            |                 | VOHdc= 0.5 * V <sub>DDQ</sub>  | 0.9 | 1.0 | 1.2 | RZQ/3 | 1, 2    |
| 100                        | 60 Ω            | VOLdc= 0.1 * V <sub>DDQ</sub>  | 0.8 | 1.0 | 1.1 | RZQ/4 | 1, 2    |
|                            |                 | VOMdc= 0.33 * V <sub>DDQ</sub> | 0.9 | 1.0 | 1.1 | RZQ/4 | 1, 2    |
|                            |                 | VOHdc= 0.5 * V <sub>DDQ</sub>  | 0.9 | 1.0 | 1.2 | RZQ/4 | 1, 2    |
| 101                        | 48 Ω            | VOLdc= 0.1 * V <sub>DDQ</sub>  | 0.8 | 1.0 | 1.1 | RZQ/5 | 1, 2    |
|                            |                 | VOMdc= 0.33 * V <sub>DDQ</sub> | 0.9 | 1.0 | 1.1 | RZQ/5 | 1, 2    |
|                            |                 | VOHdc= 0.5 * V <sub>DDQ</sub>  | 0.9 | 1.0 | 1.2 | RZQ/5 | 1, 2    |
| 110                        | 40 Ω            | VOLdc= 0.1 * V <sub>DDQ</sub>  | 0.8 | 1.0 | 1.1 | RZQ/6 | 1, 2    |
|                            |                 | VOMdc= 0.33 * V <sub>DDQ</sub> | 0.9 | 1.0 | 1.1 | RZQ/6 | 1, 2    |
|                            |                 | VOHdc= 0.5 * V <sub>DDQ</sub>  | 0.9 | 1.0 | 1.2 | RZQ/6 | 1, 2    |
| Mismatch DQ-DQ within byte |                 | 0.33 * V <sub>DDQ</sub>        | -   |     | 2   | %     | 1, 2, 3 |

**Notes:**

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at 0.33\*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.5\*VDDQ and 0.1\*VDDQ.
3. DQ to DQ mismatch within byte variation for a given component including DQS\_t and DQS\_c (characterized).

$$\text{DQ - DQ Mismatch} = \frac{\text{RODT(max)} - \text{RODT(min)}}{\text{RODT(avg)}}$$





**Table 83 - ODT DC Electrical Characteristics, assuming RZQ = 240  $\Omega$   $\pm$ 1% over the entire operating temperature range after a proper ZQ calibration for beyond 3200 Mbps – LPDDR4**

| MR11[2:0]                  | R <sub>TT</sub> | Vout               | Min | Nom | Max | Unit  | Notes   |
|----------------------------|-----------------|--------------------|-----|-----|-----|-------|---------|
| 001                        | 240 Ω           | VOLdc= 0.1 * VDDQ  | 0.8 | 1.0 | 1.1 | RZQ   | 1, 2    |
|                            |                 | VOMdc= 0.33 * VDDQ | 0.9 | 1.0 | 1.1 | RZQ   | 1, 2    |
|                            |                 | VOHdc= 0.5 * VDDQ  | 0.9 | 1.0 | 1.3 | RZQ   | 1, 2    |
| 010                        | 120 Ω           | VOLdc= 0.1 * VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/2 | 1, 2    |
|                            |                 | VOMdc= 0.33 * VDDQ | 0.9 | 1.0 | 1.1 | RZQ/2 | 1, 2    |
|                            |                 | VOHdc= 0.5 * VDDQ  | 0.9 | 1.0 | 1.3 | RZQ/2 | 1, 2    |
| 011                        | 80 Ω            | VOLdc= 0.1 * VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/3 | 1, 2    |
|                            |                 | VOMdc= 0.33 * VDDQ | 0.9 | 1.0 | 1.1 | RZQ/3 | 1, 2    |
|                            |                 | VOHdc= 0.5 * VDDQ  | 0.9 | 1.0 | 1.3 | RZQ/3 | 1, 2    |
| 100                        | 60 Ω            | VOLdc= 0.1 * VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/4 | 1, 2    |
|                            |                 | VOMdc= 0.33 * VDDQ | 0.9 | 1.0 | 1.1 | RZQ/4 | 1, 2    |
|                            |                 | VOHdc= 0.5 * VDDQ  | 0.9 | 1.0 | 1.3 | RZQ/4 | 1, 2    |
| 101                        | 48 Ω            | VOLdc= 0.1 * VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/5 | 1, 2    |
|                            |                 | VOMdc= 0.33 * VDDQ | 0.9 | 1.0 | 1.1 | RZQ/5 | 1, 2    |
|                            |                 | VOHdc= 0.5 * VDDQ  | 0.9 | 1.0 | 1.3 | RZQ/5 | 1, 2    |
| 110                        | 40 Ω            | VOLdc= 0.1 * VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/6 | 1, 2    |
|                            |                 | VOMdc= 0.33 * VDDQ | 0.9 | 1.0 | 1.1 | RZQ/6 | 1, 2    |
|                            |                 | VOHdc= 0.5 * VDDQ  | 0.9 | 1.0 | 1.3 | RZQ/6 | 1, 2    |
| Mismatch DQ-DQ within byte |                 | 0.33 * VDDQ        | -   |     | 2   | %     | 1, 2, 3 |

**Notes:**

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at 0.33\*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.5\*VDDQ and 0.1\*VDDQ.
3. DQ to DQ mismatch within byte variation for a given component including DQS\_t and DQS\_c (characterized).

$$\text{DQ - DQ Mismatch} = \frac{\text{RODT(max)} - \text{RODT(min)}}{\text{RODT(avg)}}$$



#### 7.4.43 Output Driver and Termination Resistor Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 84 and Table 85.

**Table 84 - Output Driver and Termination Resistor Sensitivity Definition – LPDDR4**

| Resistor      | Definition Point   | Min                                                                  | Max                                                                   | Unit | Notes   |
|---------------|--------------------|----------------------------------------------------------------------|-----------------------------------------------------------------------|------|---------|
| $R_{ONPD}$    | $0.33 \times VDDQ$ | $90 - (dR_{ondT} \times  \Delta T ) - (dR_{onDV} \times  \Delta V )$ | $110 + (dR_{ondT} \times  \Delta T ) + (dR_{onDV} \times  \Delta V )$ | %    | 1, 2    |
| $VOH_{PU}$    | $0.33 \times VDDQ$ | $90 - (dVOHdT \times  \Delta T ) - (dVOHdV \times  \Delta V )$       | $110 + (dVOHdT \times  \Delta T ) + (dVOHdV \times  \Delta V )$       | %    | 1, 2, 5 |
| $R_{TT(I/O)}$ | $0.33 \times VDDQ$ | $90 - (dR_{ondT} \times  \Delta T ) - (dR_{onDV} \times  \Delta V )$ | $110 + (dR_{ondT} \times  \Delta T ) + (dR_{onDV} \times  \Delta V )$ | %    | 1, 2, 3 |
| $R_{TT(In)}$  | $0.33 \times VDD2$ | $90 - (dR_{ondT} \times  \Delta T ) - (dR_{onDV} \times  \Delta V )$ | $110 + (dR_{ondT} \times  \Delta T ) + (dR_{onDV} \times  \Delta V )$ | %    | 1, 2, 4 |

**Notes:**

- $\Delta T = T - T(@ \text{Calibration})$ ,  $\Delta V = V - V(@ \text{Calibration})$ .
- $dR_{ondT}$ ,  $dR_{onDV}$ ,  $dVOHdT$ ,  $dVOHdV$ ,  $dR_{TTdV}$ , and  $dR_{TTdT}$  are not subject to production test but are verified by design and characterization.
- This parameter applies to Input/Output pin such as DQS, DQ and DMI.
- This parameter applies to Input pin such as CK, CA and CS.
- Refer to section 7.4.39 Pull Up/Pull Down Driver Characteristics for  $VOH_{PU}$ .

**Table 85 - Output Driver and Termination Resistor Temperature and Voltage Sensitivity**

| Symbol      | Parameter                        | Min  | Max  | Unit |
|-------------|----------------------------------|------|------|------|
| $dR_{ondT}$ | $R_{ON}$ Temperature Sensitivity | 0.00 | 0.75 | %/°C |
| $dR_{onDV}$ | $R_{ON}$ Voltage Sensitivity     | 0.00 | 0.20 | %/mV |
| $dVOHdT$    | $VOH$ Temperature Sensitivity    | 0.00 | 0.75 | %/°C |
| $dVOHdV$    | $VOH$ Voltage Sensitivity        | 0.00 | 0.35 | %/mV |
| $dR_{TTdT}$ | $R_{TT}$ Temperature Sensitivity | 0.00 | 0.75 | %/°C |
| $dR_{TTdV}$ | $R_{TT}$ Voltage Sensitivity     | 0.00 | 0.20 | %/mV |



#### 7.4.44 Power-Down Mode

##### 7.4.44.1 Power-Down Entry and Exit

(Reference Figure 133 through Figure 143 and Table 86.)

Power-down is asynchronously entered when CKE is driven LOW. CKE must not go LOW while the following operations are in progress:

- Mode Register Read
- Mode Register Write
- Read
- Write
- VREF(CA) Range and Value setting via MRW
- VREF(DQ) Range and Value setting via MRW
- Command Bus Training mode Entering/Exiting via MRW
- VRCG High Current mode Entering/Exiting via MRW

And the LPDDR4/LPDDR4X SDRAM cannot be placed in power-down state during “Start DQS Interval Oscillator” operation.

CKE can go LOW while any other operations such as row activation, Precharge, Auto-Precharge, or Refresh are in progress. The power-down IDD specification will not be applied until such operations are complete. Power-down entry and exit are shown in Figure 133.

Entering power-down deactivates the input and output buffers, excluding CKE and Reset\_n. To ensure that there is enough time to account for internal delay on the CKE signal path, CS input is required stable Low level and CA input level is don't care after CKE is driven LOW, this timing period is defined as tCKELCS.

Clock input is required after CKE is driven LOW, this timing period is defined as tCKELCK. CKE LOW will result in deactivation of all input receivers except Reset\_n after tCKELCK has expired. In power-down mode, CKE must be held LOW; all other input signals except Reset\_n are “Don't Care”. CKE LOW must be maintained until tCKE,min is satisfied.

No refresh operations are performed in power-down mode except Self Refresh power-down. The maximum duration in non-Self Refresh power-down mode is only limited by the refresh requirements outlined in the Refresh command section.

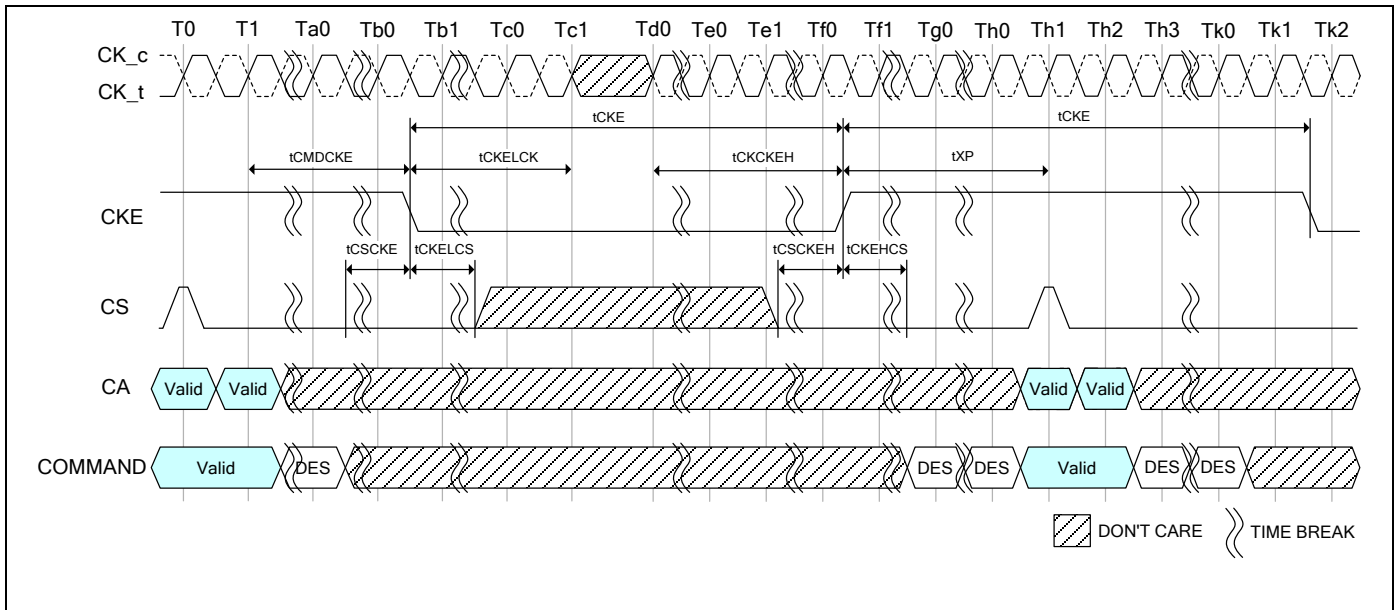
The power-down state is asynchronously exited when CKE is driven HIGH. CKE HIGH must be maintained until tCKE,min is satisfied. A valid, executable command can be applied with power-down exit latency tXP after CKE goes HIGH. Power-down exit latency is defined in the AC timing parameter table.

Clock frequency change or Clock Stop is inhibited during tCMDCKE, tCKELCK, tCKCKEH, tXP, tMRWCKEL and tZQCKE periods.

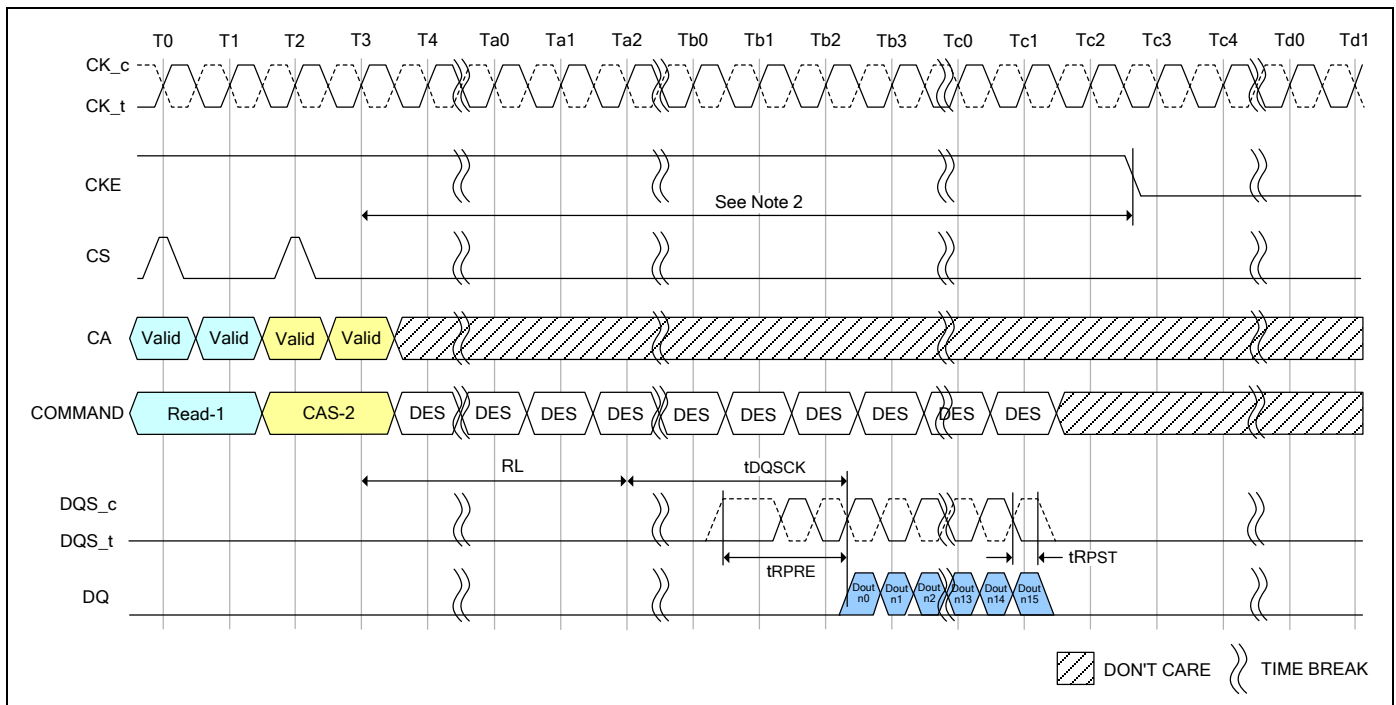
If power-down occurs when all banks are idle, this mode is referred to as idle power-down. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. And if power-down occurs when Self Refresh is in progress, this mode is referred to as Self Refresh power-down in which the internal refresh is continuing in the same way as Self Refresh mode.

VDDQ may be turned off during power-down after tCKELCK(Max(5nS,5nCK)) is satisfied (Refer to Figure 133 about tCKELCK). Prior to exiting power-down, VDDQ must be within its minimum/maximum operating range.

When CA, CK and/or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or CA-ODT pad setting, the rank providing ODT will continue to terminate the command bus in all DRAM states including power-down when VDDQ is stable and within its minimum/maximum operating range.

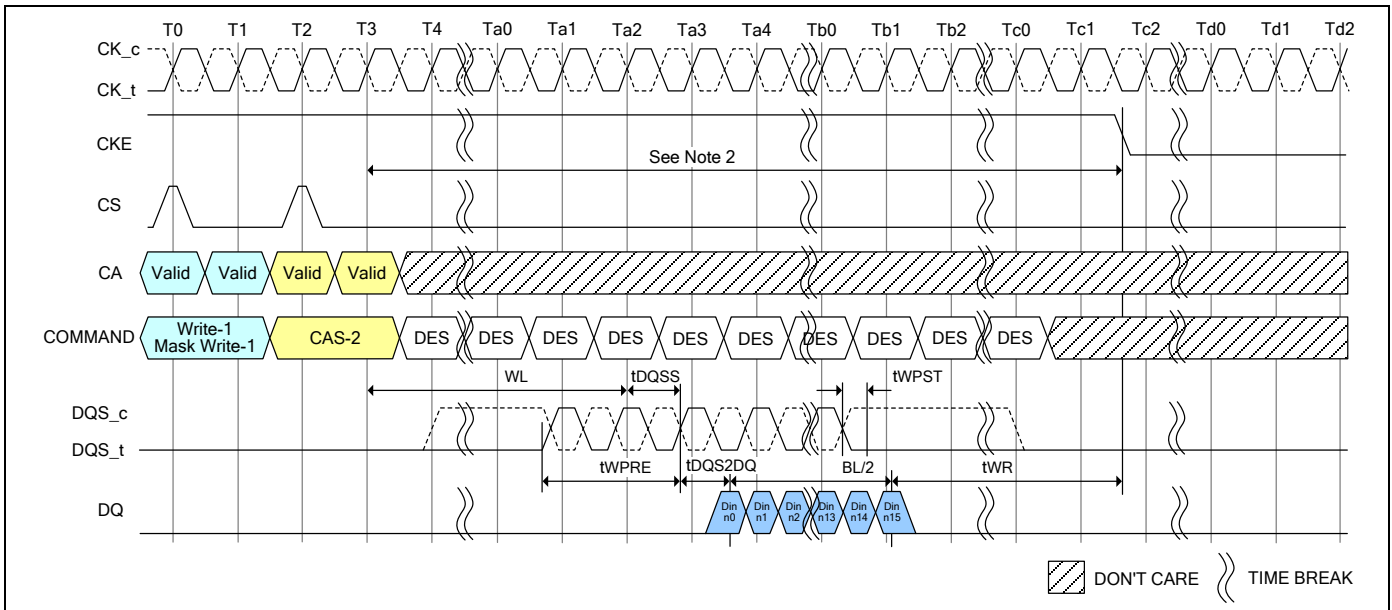
**Note:**

- Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of  $t_{CKCKEH}$  of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

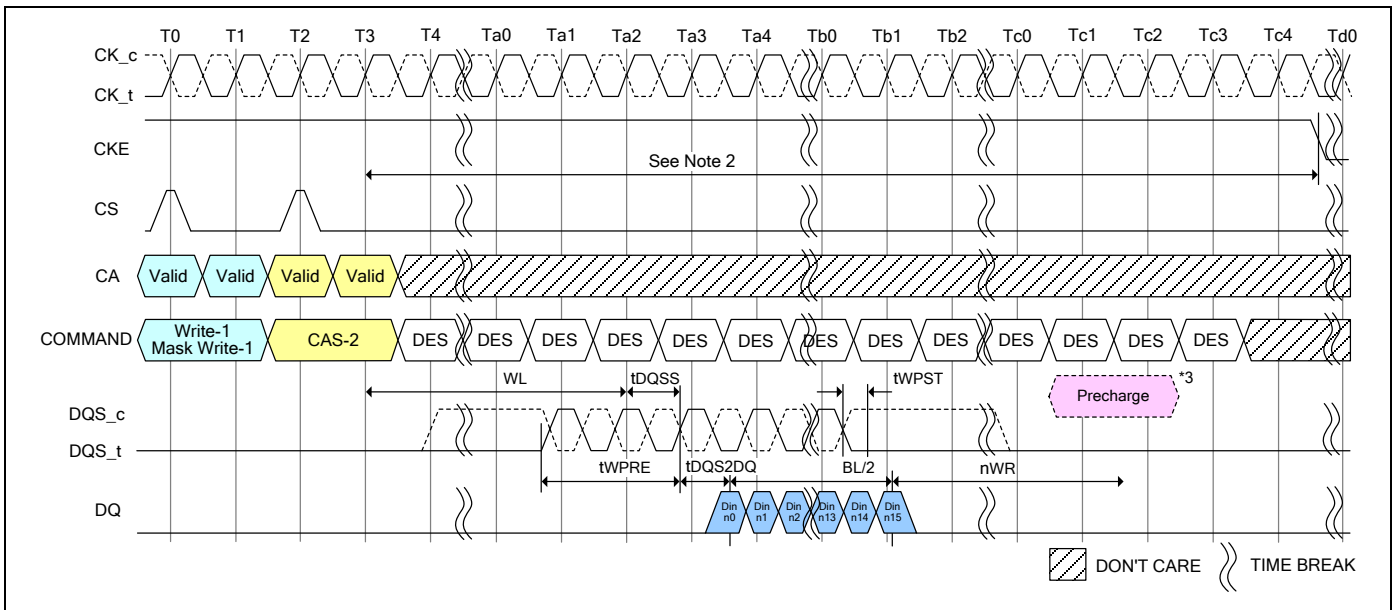
**Figure 133 - Basic Power-Down Entry and Exit Timing****Notes:**

- CKE must be held HIGH until the end of the burst operation.
- Minimum Delay time from Read Command or Read with Auto-Precharge Command to falling edge of CKE signal is as follows.  
 Read Post-amble =  $0.5nCK$  : MR1 OP[7]=[0] :  $(RL \times tCK) + tDQSCK(Max) + ((BL/2) \times tCK) + 1tCK$   
 Read Post-amble =  $1.5nCK$  : MR1 OP[7]=[1] :  $(RL \times tCK) + tDQSCK(Max) + ((BL/2) \times tCK) + 2tCK$

**Figure 134 - Read and Read with Auto-Precharge to Power-Down Entry**

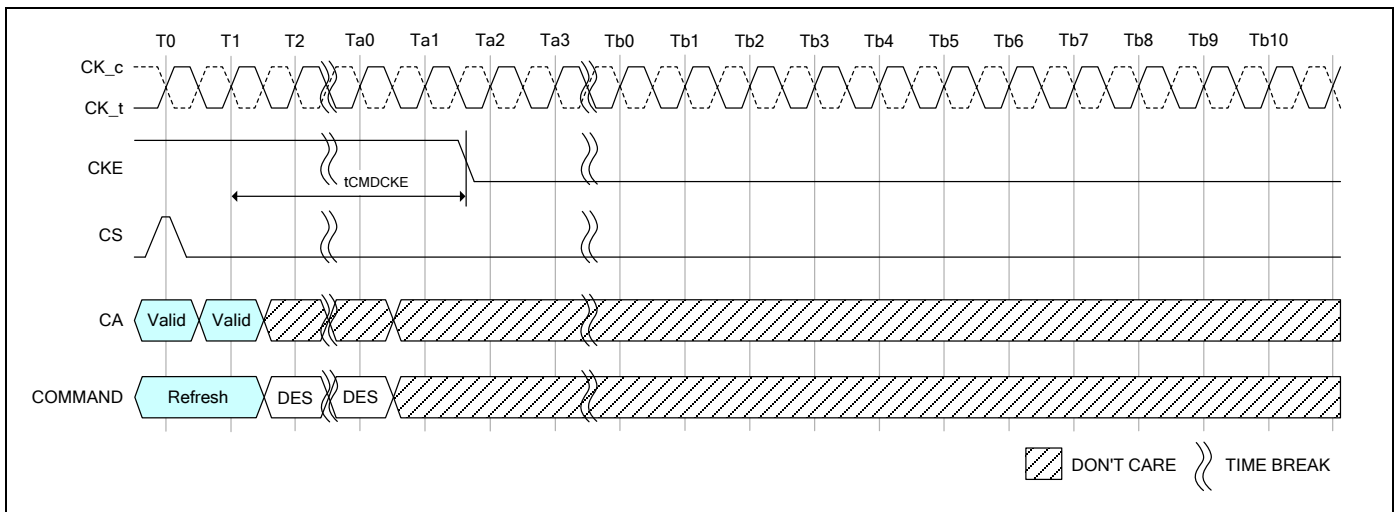
**Notes:**

1. CKE must be held HIGH until the end of the burst operation.
2. Minimum Delay time from Write Command or Mask Write Command to falling edge of CKE signal is as follows.  
 $(WL \times tCK) + tDQSS(Max) + tDQS2DQ(Max) + ((BL/2) \times tCK) + tWR$
3. This timing is applied regardless of DQ ODT Disable/Enable setting: MR11 OP[2:0].
4. This timing diagram only applies to the Write and Mask Write Commands without Auto-Precharge.

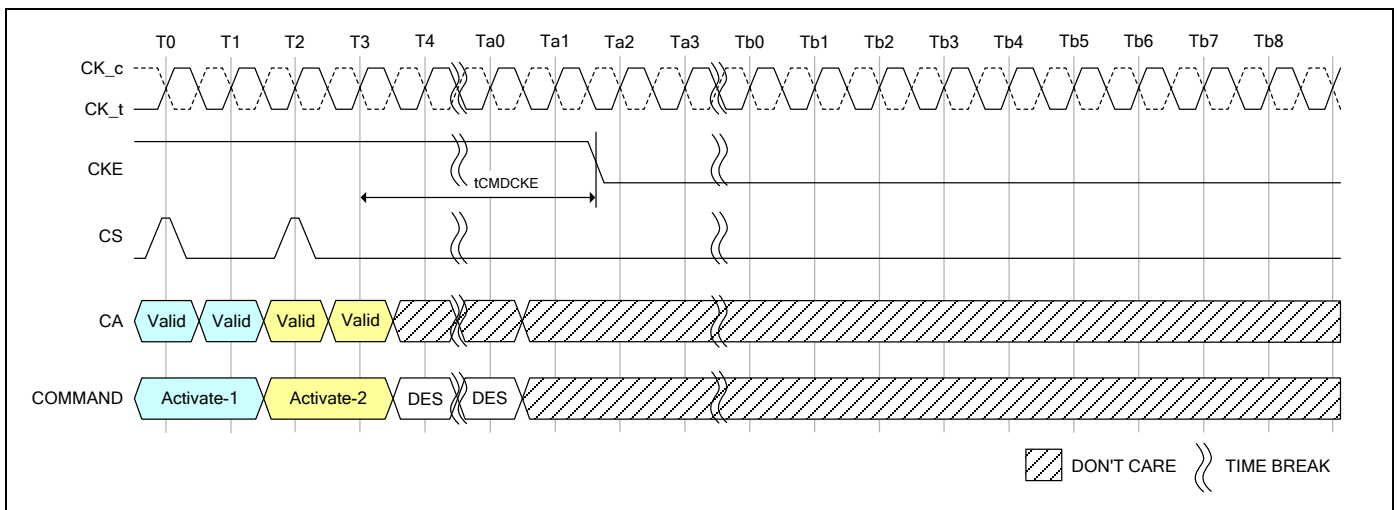
**Figure 135 - Write and Mask Write to Power-Down Entry****Notes:**

1. CKE must be held HIGH until the end of the burst operation.
2. Delay time from Write with Auto-Precharge Command or Mask Write with Auto-Precharge Command to falling edge of CKE signal is more than  
 $(WL \times tCK) + tDQSS(Max) + tDQS2DQ(Max) + ((BL/2) \times tCK) + (nWR \times tCK) + (2 \times tCK)$
3. Internal Precharge Command.
4. This timing is applied regardless of DQ ODT Disable/Enable setting: MR11 OP[2:0].

**Figure 136 - Write with Auto-Precharge and Mask Write with Auto-Precharge to Power-Down Entry**

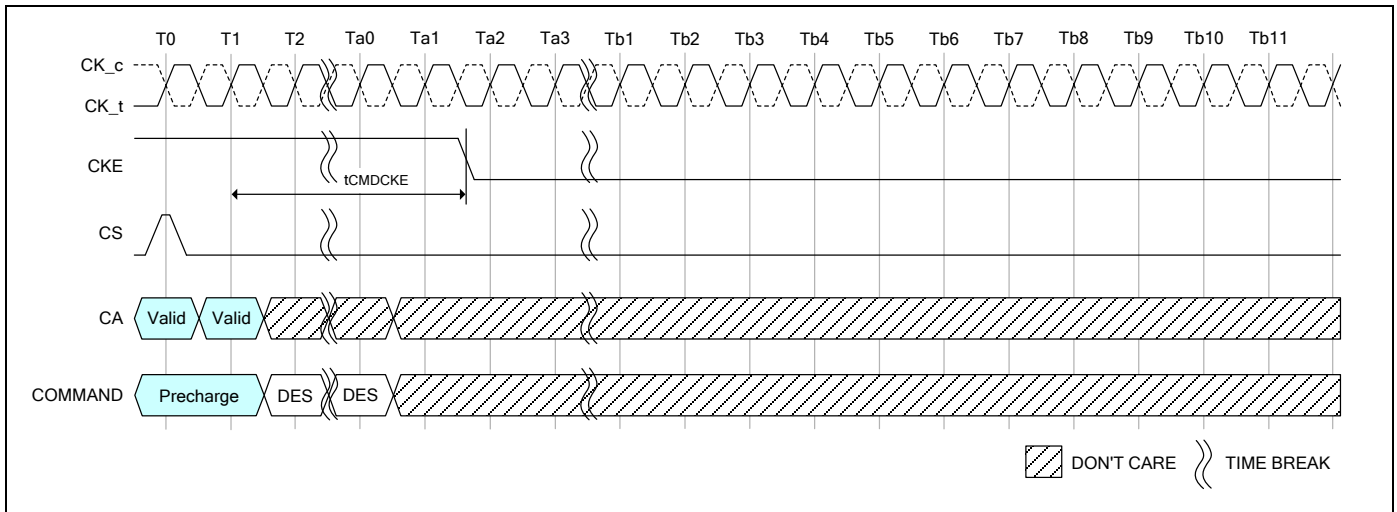
**Note:**

1. CKE must be held HIGH until  $t_{CMDCKE}$  is satisfied.

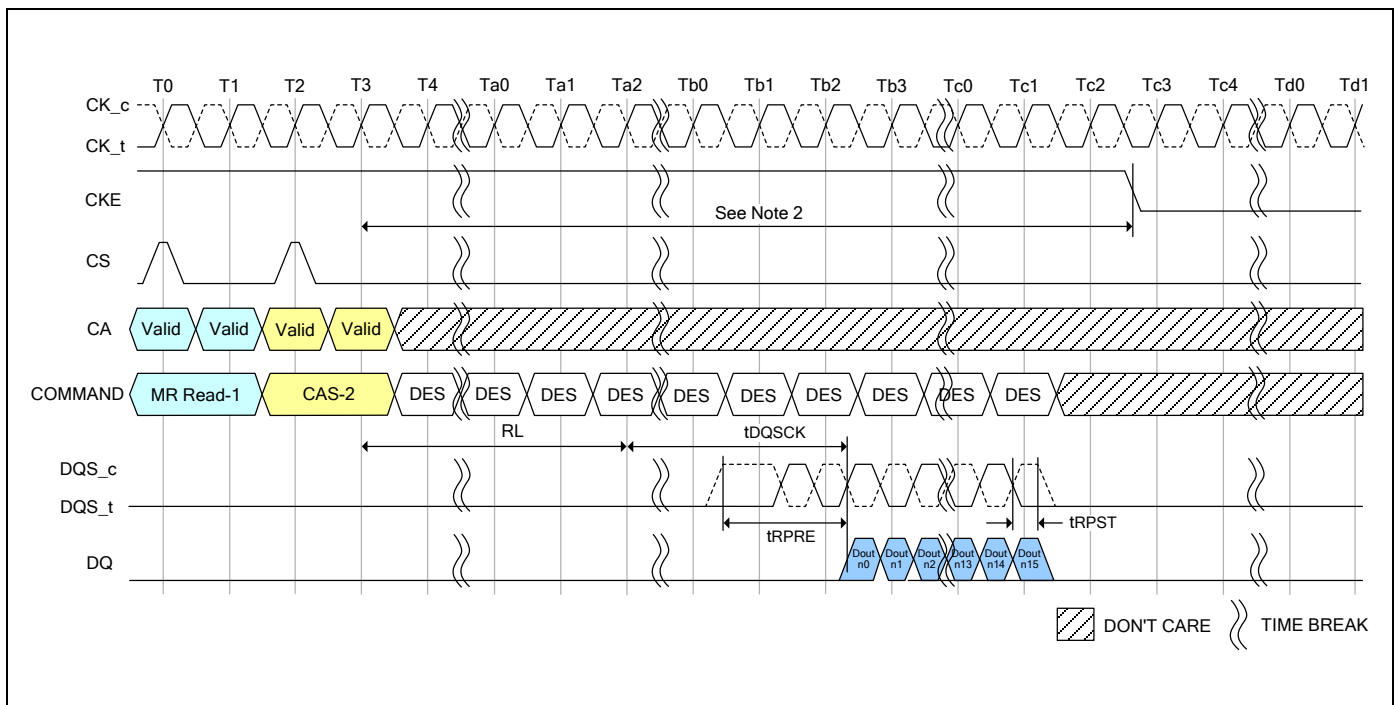
**Figure 137 - Refresh entry to Power-Down Entry****Note:**

1. CKE must be held HIGH until  $t_{CMDCKE}$  is satisfied.

**Figure 138 - Activate Command to Power-Down Entry**

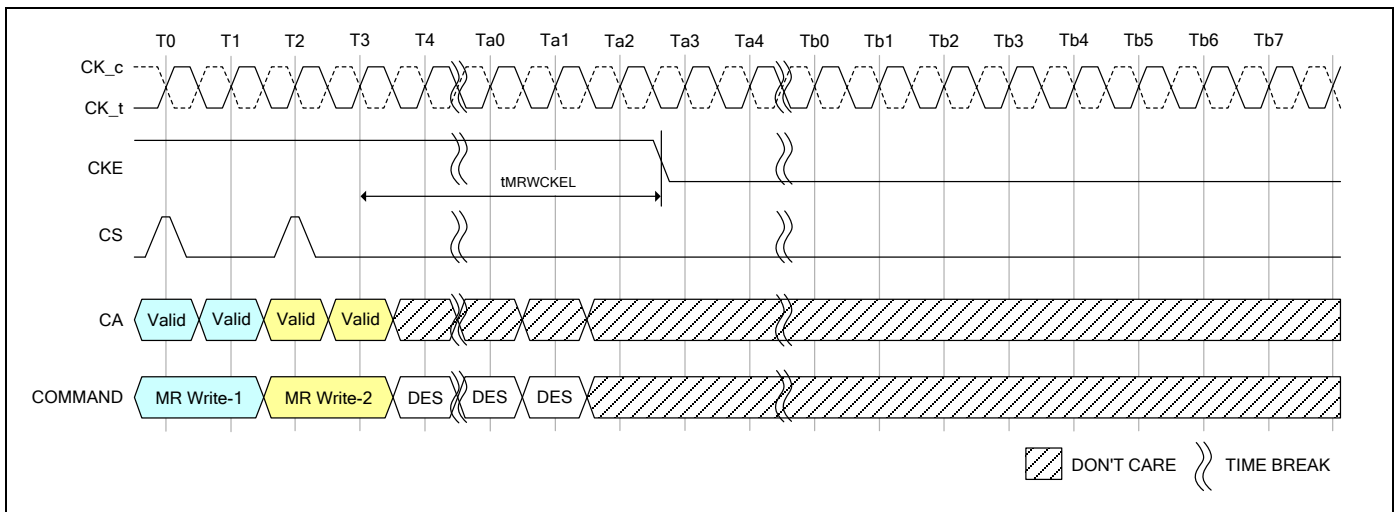
**Note:**

1. CKE must be held HIGH until  $t_{CMDCKE}$  is satisfied.

**Figure 139 - Precharge Command to Power-Down Entry****Notes:**

1. CKE must be held HIGH until the end of the burst operation.
2. Minimum Delay time from Mode Register Read Command to falling edge of CKE signal is as follows:  
 Read Post-amble = 0.5nCK : MR1 OP[7]=[0] :  $(RL \times t_{CK}) + t_{DQSCK}(\text{Max}) + ((BL/2) \times t_{CK}) + 1t_{CK}$   
 Read Post-amble = 1.5nCK : MR1 OP[7]=[1] :  $(RL \times t_{CK}) + t_{DQSCK}(\text{Max}) + ((BL/2) \times t_{CK}) + 2t_{CK}$

**Figure 140 - Mode Register Read to Power-Down Entry**

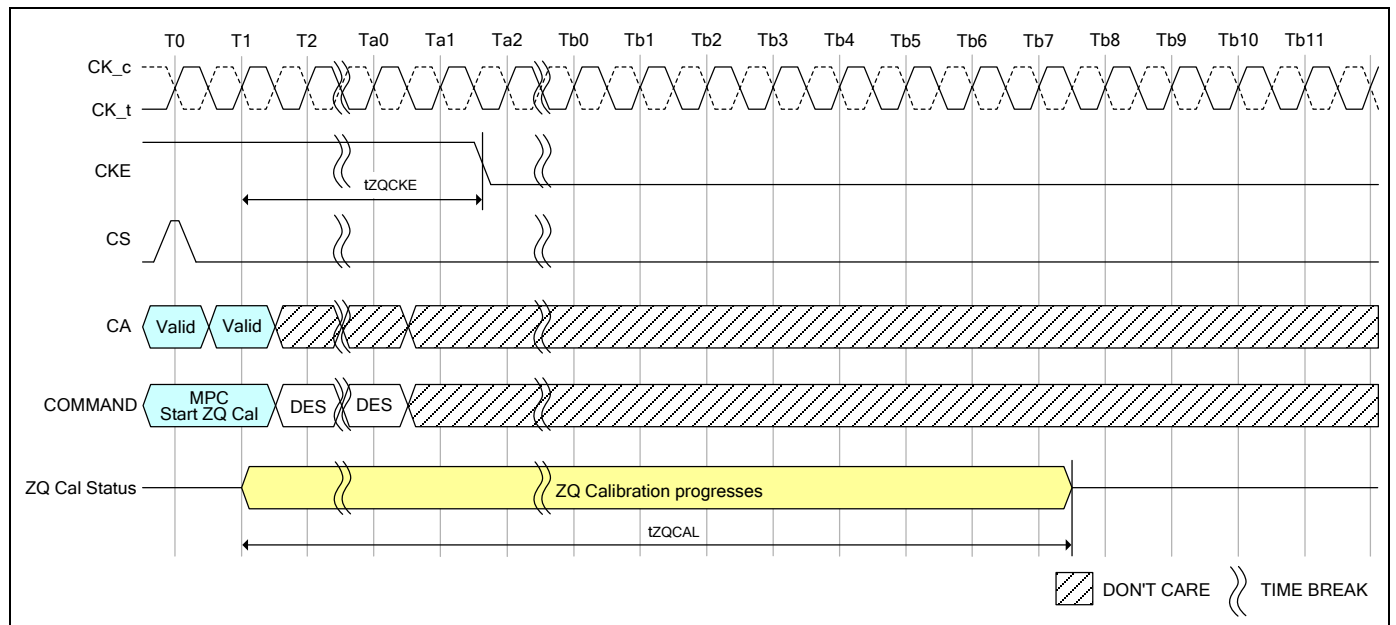
**Notes:**

1. CKE must be held HIGH until tMRWCKEL is satisfied.
2. This timing is the general definition for Power Down Entry after Mode Register Write Command.

When a Mode Register Write Command changes a parameter or starts an operation that requires special timing longer than tMRWCKEL, that timing must be satisfied before CKE is driven low.

Changing the VREF(DQ) value is one example, in this case the appropriate VREF\_time-Short/Middle/Long must be satisfied.

**Figure 141 - Mode Register Write to Power-Down Entry**

**Note:**

1. ZQ Calibration continues if CKE goes low after tZQCKE is satisfied.

**Figure 142 - Multi-Purpose Command for Start ZQ Calibration to Power-Down Entry**





Table 86 - Power-Down AC Timing

| Parameter                                                                                | Symbol   | Min/<br>Max | Data Rate         | Unit | Note |
|------------------------------------------------------------------------------------------|----------|-------------|-------------------|------|------|
| <b>Power Down Timing</b>                                                                 |          |             |                   |      |      |
| CKE minimum pulse width<br>(HIGH and LOW pulse width)                                    | tCKE     | Min         | Max(7.5nS, 4nCK)  | -    |      |
| Delay from valid command to CKE input LOW                                                | tCMDCKE  | Min         | Max(1.75nS, 3nCK) | nS   | 1    |
| Valid Clock Requirement after CKE Input low                                              | tCKELCK  | Min         | Max(5nS, 5nCK)    | nS   | 1    |
| Valid CS Requirement before CKE Input Low                                                | tCSCKE   | Min         | 1.75              | nS   |      |
| Valid CS Requirement after CKE Input low                                                 | tCKELCS  | Min         | Max(5nS, 5nCK)    | nS   |      |
| Valid Clock Requirement before CKE Input High                                            | tCKCKEH  | Min         | Max(1.75nS, 3nCK) | nS   | 1    |
| Exit power- down to next valid command delay                                             | tXP      | Min         | Max(7.5nS, 5nCK)  | nS   | 1    |
| Valid CS Requirement before CKE Input High                                               | tCSCKEH  | Min         | 1.75              | nS   |      |
| Valid CS Requirement after CKE Input High                                                | tCKEHCS  | Min         | Max(7.5nS, 5nCK)  | nS   |      |
| Valid Clock and CS Requirement after CKE Input low<br>after MRW Command                  | tMRWCKEL | Min         | Max(14nS, 10nCK)  | nS   | 1    |
| Valid Clock and CS Requirement after CKE Input low<br>after ZQ Calibration Start Command | tZQCKE   | Min         | Max(1.75nS, 3nCK) | nS   | 1    |

**Note:**

1. Delay time has to satisfy both analog time (nS) and clock count (nCK).

For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3 \*tCK) and 1.75nS has transpired. The case which 3nCK is applied to is shown In Figure 143.

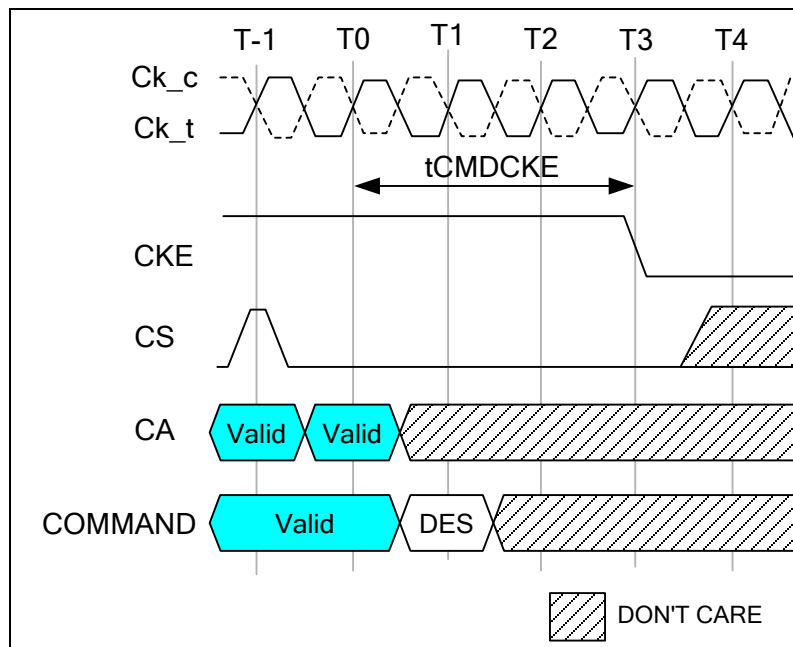


Figure 143 - tCMDCKE Timing



#### 7.4.45 Input Clock Stop and Frequency Change

##### Clock Frequency Change during CKE LOW

LPDDR4/LPDDR4X SDRAMs support input clock frequency change during CKE LOW under the following conditions:

- $t_{CK(ABS)min}$  is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions ( $t_{RCD}$ ,  $t_{RP}$ ) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of  $t_{CKELCK}$  after CKE goes LOW;
- The clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $t_{CKCKEH}$  prior to CKE going HIGH

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

##### Clock Stop during CKE LOW

LPDDR4/LPDDR4X SDRAMs support clock stop during CKE LOW under the following conditions:

- CK\_t and CK\_c are don't care during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions ( $t_{RCD}$ ,  $t_{RP}$ ) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of  $t_{CKELCK}$  after CKE goes LOW;
- The clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $t_{CKCKEH}$  prior to CKE going HIGH



### Clock Frequency Change during CKE HIGH

LPDDR4/LPDDR4X SDRAMs support input clock frequency change during CKE HIGH under the following conditions:

- $t_{CK(ABS)min}$  is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- Any Activate, Read, Read with auto Precharge, Write, Write with auto Precharge, MPC(WRFIFO, RDFIFO, RDDQCAL), Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions ( $t_{RCD}$ ,  $t_{WR}$ ,  $t_{RP}$ ,  $t_{MRW}$ ,  $t_{MRR}$ , etc.) have been met prior to changing the frequency;
- CS shall be held LOW during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR4/LPDDR4X SDRAM is ready for normal operation after the clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $2 \cdot t_{CK} + t_{XP}$ .

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL, etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

### Clock Stop during CKE HIGH

LPDDR4/LPDDR4X SDRAMs support clock stop during CKE HIGH under the following conditions:

- CK<sub>t</sub> is held LOW and CK<sub>c</sub> is held HIGH during clock stop;
- CS shall be held LOW during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Read, Write, MPC(WRFIFO, RDFIFO, RDDQCAL), Precharge, Mode Register Write or Mode Register Read commands must have executed to completion, including any associated data bursts and extra 4 clock cycles must be provided prior to stopping the clock;
- The related timing conditions ( $t_{RCD}$ ,  $t_{WR}$ ,  $t_{RP}$ ,  $t_{MRW}$ ,  $t_{MRR}$ ,  $t_{ZQLAT}$ , etc.) have been met prior to stopping the clock;
- Read with auto precharge and write with auto precharge commands need extra 4 clock cycles in addition to the related timing constraints, nWR and nRTP, to complete the operations.
- REFab, REFpb, SRE, SRX and MPC(Zqcal Start) commands are required to have 4 additional clocks prior to stopping the clock same as CKE=L case.
- The LPDDR4/LPDDR4X SDRAM is ready for normal operation after the clock is restarted and satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $2 \cdot t_{CK} + t_{XP}$ .



#### 7.4.46 Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR4/LPDDR4X SDRAM must be reset or power-cycled and then restarted through the specified initialization sequence before normal operation can continue.

CKE signal has to be held HIGH when the commands listed in Table 87 input.

**Table 87 - Command Truth Table**

|                                                    | SDR Command Pins | SDR CA Pins (6) |     |     |     |     |     |           |             |
|----------------------------------------------------|------------------|-----------------|-----|-----|-----|-----|-----|-----------|-------------|
| SDRAM Command                                      | CS               | CA0             | CA1 | CA2 | CA3 | CA4 | CA5 | CK_t edge | Notes       |
| Deselect (DES)                                     | L                | X               |     |     |     |     |     | R1        | 1,2         |
| Multi-Purpose Command (MPC)                        | H                | L               | L   | L   | L   | L   | OP6 | R1        | 1,9         |
|                                                    | L                | OP0             | OP1 | OP2 | OP3 | OP4 | OP5 | R2        |             |
| Precharge (PRE)<br>(Per Bank, All Bank)            | H                | L               | L   | L   | L   | H   | AB  | R1        | 1,2,3,4     |
|                                                    | L                | BA0             | BA1 | BA2 | V   | V   | V   | R2        |             |
| Refresh (REF)<br>(Per Bank, All Bank)              | H                | L               | L   | L   | H   | L   | AB  | R1        | 1,2,3,4     |
|                                                    | L                | BA0             | BA1 | BA2 | V   | V   | V   | R2        |             |
| Self Refresh Entry (SRE)                           | H                | L               | L   | L   | H   | H   | V   | R1        | 1,2         |
|                                                    | L                | V               |     |     |     |     |     | R2        |             |
| Write -1 (WR-1)                                    | H                | L               | L   | H   | L   | L   | BL  | R1        | 1,2,3,6,7,9 |
|                                                    | L                | BA0             | BA1 | BA2 | V   | C9  | AP  | R2        |             |
| Self Refresh Exit (SRX)                            | H                | L               | L   | H   | L   | H   | V   | R1        | 1,2         |
|                                                    | L                | V               |     |     |     |     |     | R2        |             |
| Mask Write -1 (MWR-1)                              | H                | L               | L   | H   | H   | L   | L   | R1        | 1,2,3,5,6,9 |
|                                                    | L                | BA0             | BA1 | BA2 | V   | C9  | AP  | R2        |             |
| RFU                                                | H                | L               | L   | H   | H   | H   | V   | R1        | 1,2         |
|                                                    | L                | V               |     |     |     |     |     | R2        |             |
| Read -1 (RD-1)                                     | H                | L               | H   | L   | L   | L   | BL  | R1        | 1,2,3,6,7,9 |
|                                                    | L                | BA0             | BA1 | BA2 | V   | C9  | AP  | R2        |             |
| CAS-2 (Write-2, Mask Write -2, Read-2, MRR-2, MPC) | H                | L               | H   | L   | L   | H   | C8  | R1        | 1,8,9       |
|                                                    | L                | C2              | C3  | C4  | C5  | C6  | C7  | R2        |             |
| RFU                                                | H                | L               | H   | L   | H   | L   | V   | R1        | 1,2         |
|                                                    | L                | V               |     |     |     |     |     | R2        |             |
| RFU                                                | H                | L               | H   | L   | H   | H   | V   | R1        | 1,2         |
|                                                    | L                | V               |     |     |     |     |     | R2        |             |
| Mode Register Write-1 (MRW-1)                      | H                | L               | H   | H   | L   | L   | OP7 | R1        | 1,11        |
|                                                    | L                | MA0             | MA1 | MA2 | MA3 | MA4 | MA5 | R2        |             |
| Mode Register Write-2 (MRW-2)                      | H                | L               | H   | H   | L   | H   | OP6 | R1        | 1,11        |
|                                                    | L                | OP0             | OP1 | OP2 | OP3 | OP4 | OP5 | R2        |             |
| Mode Register Read-1 (MRR-1)                       | H                | L               | H   | H   | H   | L   | V   | R1        | 1,2,12      |
|                                                    | L                | MA0             | MA1 | MA2 | MA3 | MA4 | MA5 | R2        |             |
| RFU                                                | H                | L               | H   | H   | H   | H   | V   | R1        | 1,2         |
|                                                    | L                | V               |     |     |     |     |     | R2        |             |
| Activate-1 (ACT-1)                                 | H                | H               | L   | R12 | R13 | R14 | X   | R1        | 1,2,3,10    |
|                                                    | L                | BA0             | BA1 | BA2 | X   | R10 | R11 | R2        |             |
| Activate-2 (ACT-2)                                 | H                | H               | H   | R6  | R7  | R8  | R9  | R1        | 1,10        |
|                                                    | L                | R0              | R1  | R2  | R3  | R4  | R5  | R2        |             |

**Notes:**

1. All LPDDR4/LPDDR4X commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.
2. "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CA[5:0] can be floated.
3. Bank addresses BA[2:0] determine which bank is to be operated upon.
4. AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address are don't care.
5. Mask Write-1 command supports only BL 16. For Mask Write-1 command, CA5 must be driven LOW on first rising clock cycle (R1).
6. AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an Auto-Precharge will occur to the bank associated with the Write, Mask Write or Read command.
7. If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".
8. For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.
9. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
10. Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.
11. MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.
12. MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.



#### 7.4.47 TRR Mode - Target Row Refresh

A LPDDR4/LPDDR4X SDRAM's row has a limited number of times a given row can be accessed within a refresh period ( $t_{REFW} * 2$ ) prior to requiring adjacent rows to be refreshed. The Maximum Activate Count (MAC) is the maximum number of activates that a single row can sustain within a refresh period before the adjacent rows need to be refreshed. The row receiving the excessive activates is the Target Row ( $TR_n$ ), the adjacent rows to be refreshed are the victim rows. When the MAC limit is reached on  $TR_n$ , either the LPDDR4/LPDDR4X SDRAM receive all ( $R * 2$ ) Refresh Commands before another row activate is issued, or the LPDDR4/LPDDR4X SDRAM should be placed into Targeted Row Refresh (TRR) mode. The TRR Mode will re-refresh the rows adjacent to the  $TR_n$  that encountered tMAC limit.

If LPDDR4/LPDDR4X SDRAM supports Unlimited MAC value: MR24 OP[2:0]=000 and MR24 OP[3]=1, Target Row Refresh operation is not required. Even though LPDDR4/LPDDR4X SDRAM allows to set MR24 OP[7]=1: TRR mode enable, in this case LPDDR4/LPDDR4X SDRAM's behavior is vendor specific.

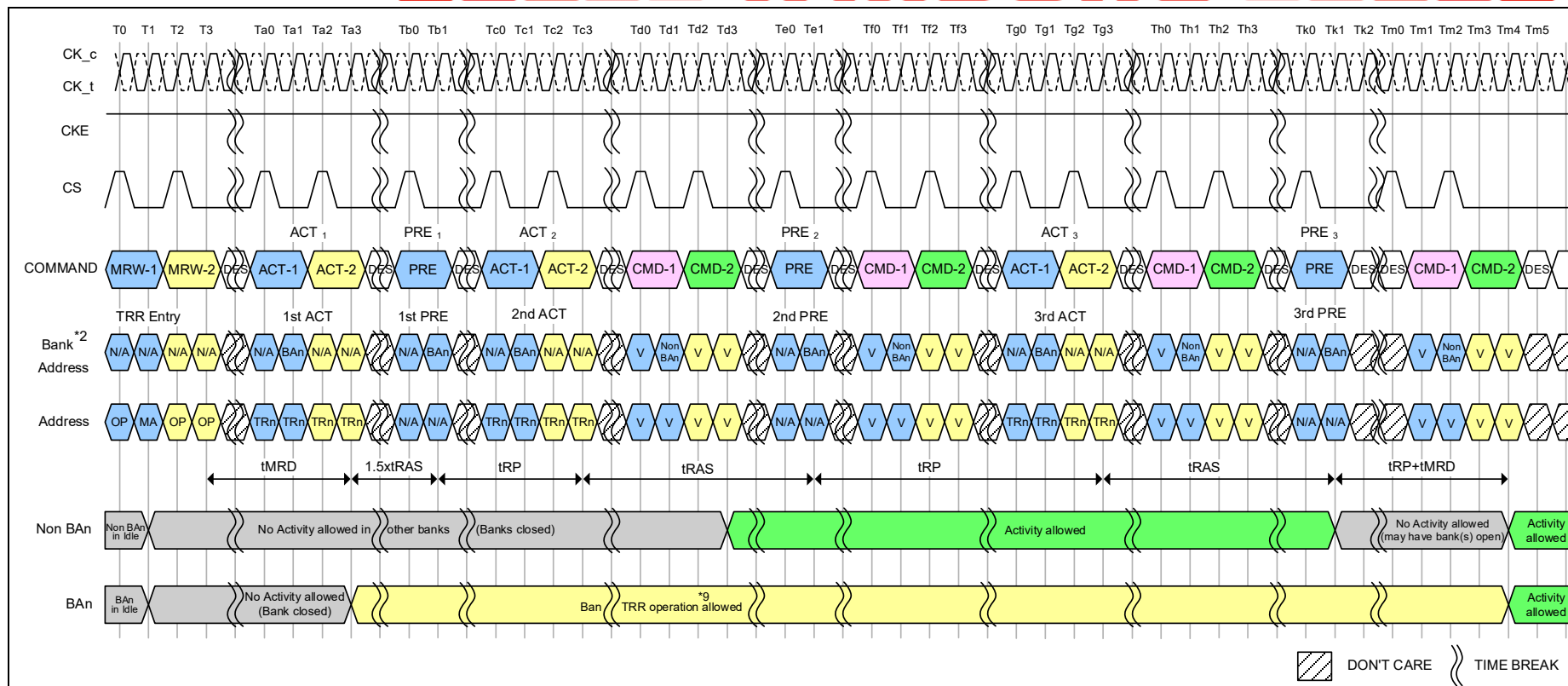
There could be a maximum of two target rows to a victim row in a bank. The cumulative value of the activation from the two target rows on a victim row in a bank should not exceed MAC value as well. MR24 fields required to support the new TRR settings. Setting MR24 OP[7] = 1 enables TRR Mode and setting MR24 OP[7] = 0 disables TRR Mode. MR24 OP[6:4] defines which bank (BAn) the target row is located in (See MR24 table for details).

The TRR mode must be disabled during initialization as well as any other LPDDR4/LPDDR4X SDRAM calibration modes. The TRR mode is entered from a DRAM Idle State, once TRR mode has been entered, no other Mode Register commands are allowed until TRR mode is completed, except setting MR24 OP[7] = 0 to interrupt and reissue the TRR mode is allowed.

When enabled; TRR Mode is self-clearing; the mode will be disabled automatically after the completion of defined TRR flow; after the 3rd BAn precharge has completed plus tMRD. The TRR mode can also be exited via another MRS command at the completion of TRR by setting MR24 OP[7] = 0; if the TRR is exited via another MRS command, the value written to MR24 OP[6:4] are don't cares.

##### 7.4.47.1 TRR Mode Operation

1. The timing diagram in Figure 144 depicts TRR mode. The following steps must be performed when TRR mode is enabled. This mode requires all three ACT (ACT1, ACT2 and ACT3) and three corresponding PRE commands (PRE1, PRE2 and PRE3) to complete TRR mode. A Precharge All (PREA) commands issued while LPDDR4/LPDDR4X SDRAM is in TRR mode will also perform precharge to BAn and counts towards a PREn command.
2. Prior to issuing the MRW command to enter TRR mode, the device should be in the idle state. A MRW command must be issued with MR24 OP[7] = 1 and MR24 OP[6:4] defining the bank in which the targeted row is located. All other MR24 bits should remain unchanged.
3. No activity is to occur in the DRAM until tMRD has been satisfied. Once tMRD has been satisfied, the only commands to BAn allowed are ACT and PRE until the TRR mode has been completed.
4. The first ACT to the BAn with the  $TR_n$  address can now be applied, no other command is allowed at this point. All other banks must remain inactive from when the first BAn ACT command is issued until  $[(1.5 * t_{RAS}) + t_{RP}]$  is satisfied.
5. After the first ACT to the BAn with the  $TR_n$  address is issued, a PRE to BAn is to be issued ( $1.5 * t_{RAS}$ ) later; and then followed tRP later by the second ACT to the BAn with the  $TR_n$  address. Once the 2nd activate to the BAn is issued, non BAn banks are allowed to have activity.
6. After the second ACT to the BAn with the  $TR_n$  address is issued, a PRE to BAn is to be issued tRAS later and then followed tRP later by the third ACT to the BAn with the  $TR_n$  address.
7. After the third ACT to the BAn with the  $TR_n$  address is issued, a PRE to BAn would be issued tRAS later; and once the third PRE has been issued, non BAn banks are not allowed to have activity until TRR mode is exited. The TRR mode is completed once tRP plus tMRD is satisfied.
8. TRR mode must be completed as specified to guarantee that adjacent rows are refreshed. Any-time the TRR mode is interrupted and not completed; the interrupted TRR Mode must be cleared and then subsequently performed again. To clear an interrupted TRR mode, an MR24 change is required with setting MR24 OP[7] = 0, MR24 OP[6:4] are don't care, followed by three PRE to BAn, tRP time in between each PRE command. The complete TRR sequence (Steps 2-7) must be then re-issued and completed to guarantee that the adjacent rows are refreshed.
9. Refresh command to the LPDDR4/LPDDR4X SDRAM or entering Self Refresh mode is not allowed while the DRAM is in TRR mode.



#### Notes:

1. TRn is targeted row.
2. Bank BAn represents the bank in which the targeted row is located.
3. TRR mode self-clears after tMRD + tRP measured from 3rd BAn precharge PRE3 at clock edge Tm4.
4. TRR mode or any other activity can be re-engaged after tRP + tMRD from 3rd BAn precharge PRE3.  
PRE\_ALL also counts if issued instead of PREn. TRR mode is cleared by DRAM after PRE3 to the BAn bank.
5. Activate commands to BAn during TRR mode do not provide refreshing support, i.e., the Refresh counter is unaffected.
6. The DRAM must restore the degraded row(s) caused by excessive activation of the targeted row (TRn) necessary to meet refresh requirements.
7. A new TRR mode must wait tMRD+tRP time after the third precharge.
8. BAn may not be used with any other command.
9. ACT and PRE are the only allowed commands to BAn during TRR Mode.
10. Refresh commands are not allowed during TRR mode.
11. All DRAM timings are to be met by DRAM during TRR mode such as tFAW. Issuing of ACT1, ACT2 and ACT3 counts towards tFAW budget

**Figure 144 - TRR Mode**





#### 7.4.48 Post Package Repair (PPR)

LPDDR4/LPDDR4X supports Fail Row address repair and it is readable through MR25 OP[7:0] PPR provides simple and easy repair method in the system and Fail Row address can be repaired by the electrical programming of Electrical-fuse scheme.

With PPR, LPDDR4/LPDDR4X can correct 1Row per Bank.

Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended the PPR mode entry and repair.

##### 7.4.48.1 Fail Row Address Repair

The following is procedure of PPR.

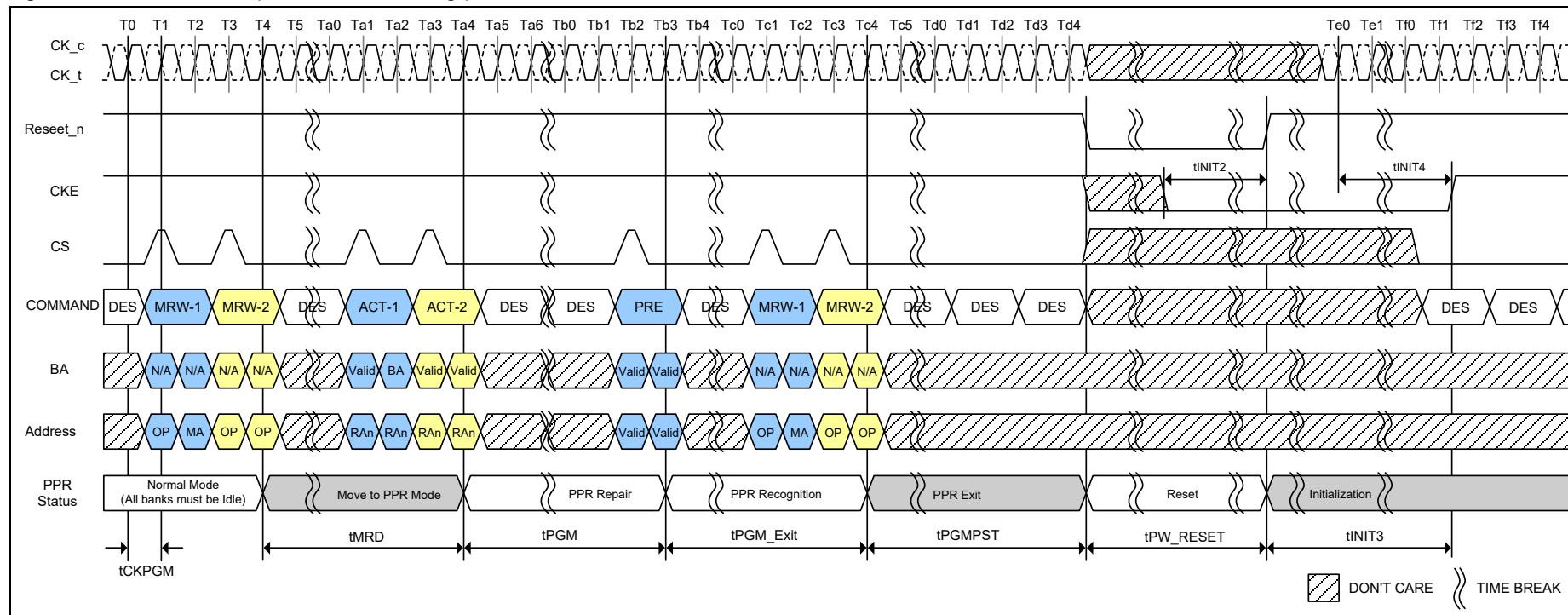
1. Before entering 'PPR' mode, All banks must be Precharged.
2. Enable PPR using MR4 OP[4] = 1 and wait tMRD.
3. Issue ACT command with Fail Row address.
4. Wait tPGM to allow DRAM repair target Row Address internally then issue PRE.
5. Wait tPGM\_Exit after PRE which allow DRAM to recognize repaired Row address RAn.
6. Exit PPR with setting MR4 OP[4] = 0.
7. Issue RESET command after tPGMPST.
8. Repeat steps in section **7.2.2 Reset Initialization with Stable Power**.
9. In more than one fail address repair case, Repeat Step 2 to 8.

Once PPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back after PPR exit with MR4 OP[4] = 0 and tPGMPST.





Figure 145 shows PPR operation. The timing parameters are shown in Table 88.



**Notes:**

1. During tPGM, any other commands (including refresh) are not allowed on each die.
2. With one PPR command, only one row can be repaired at one time per die.
3. RESET command is required at the end of every PPR procedure.
4. During PPR, memory contents are not refreshed and may be lost.
5. Assert Reset\_n below 0.2 X VDD2. Reset\_n needs to be maintained LOW for minimum tPW\_RESET. CKE must be pulled LOW at least 10nS before deasserting Reset\_n.
6. After RESET command, follow steps 4 to 10 in section 7.2.1 "Voltage Ramp and Device Initialization".
7. Only DES command is allowed during tMRD.

**Figure 145 - PPR Timing**  
**Table 88 - PPR Timing Parameters**

| Parameter                | Symbol    | Min  | Max | Unit | Note |
|--------------------------|-----------|------|-----|------|------|
| PPR Programming Time     | tPGM      | 1000 | -   | mS   |      |
| PPR Exit Time            | tPGM_Exit | 15   | -   | nS   |      |
| New Address Setting time | tPGMPST   | 50   | -   | μS   |      |
| PPR Programming Clock    | tCKPGM    | 1.25 | -   | nS   |      |



## 8. ELECTRICAL CHARACTERISTIC

### 8.1 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device.

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

| Parameter                                       | Symbol    | Min  | Max  | Units | Notes |
|-------------------------------------------------|-----------|------|------|-------|-------|
| VDD1 supply voltage relative to VSS             | VDD1      | -0.4 | +2.1 | V     | 1     |
| VDD2 supply voltage relative to VSS             | VDD2      | -0.4 | +1.4 | V     | 1     |
| VDDQ supply voltage relative to VSS             | VDDQ      | -0.4 | +1.4 | V     | 1     |
| Voltage on any ball except VDD1 relative to VSS | VIN, VOUT | -0.4 | +1.4 | V     |       |
| Storage Temperature                             | TSTG      | -55  | +125 | °C    | 2     |

#### Notes:

- See "Voltage Ramp" in section 7.2 for relationships between power supplies.
- Storage Temperature is the case surface temperature on the center/top side of the LPDDR4/LPDDR4X SDRAM. For the measurement conditions, please refer to JESD51-2.

### 8.2 AC & DC Operating Conditions

#### 8.2.1 Recommended DC Operating Conditions – LPDDR4

| DRAM                             | Symbol | Min  | Typ  | Max  | Unit | Notes   |
|----------------------------------|--------|------|------|------|------|---------|
| Core 1 Power                     | VDD1   | 1.70 | 1.80 | 1.95 | V    | 1, 2    |
| Core 2 Power/ Input Buffer Power | VDD2   | 1.06 | 1.10 | 1.17 | V    | 1, 2, 3 |
| I/O Buffer Power                 | VDDQ   | 1.06 | 1.10 | 1.17 | V    | 2, 3    |

#### Notes:

- VDD1 uses significantly less power than VDD2.
- The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
- VdIVW and TdIVW limits described elsewhere in this document apply for voltage noise on supply voltages of up to 45 mV (peak-to-peak) from DC to 20MHz.
- All parts list in ordering information table (section 3) will not guarantee to meet functional and AC specification if the DC operation conditions out of range mentioned in above table.

#### 8.2.2 Input Leakage Current

| Parameter/Condition   | Symbol | Min | Max | Unit | Notes |
|-----------------------|--------|-----|-----|------|-------|
| Input Leakage current | IL     | -4  | 4   | μA   | 1, 2  |

#### Notes:

- For CK\_t, CK\_c, CKE, CS, CA, ODT\_CA and RESET\_n. Any input  $0V \leq V_{IN} \leq V_{DD2}$  (All other pins not under test = 0V).
- CA ODT is disabled for CK\_t, CK\_c, CS, and CA.

#### 8.2.3 Input/Output Leakage Current

| Parameter/Condition          | Symbol | Min | Max | Unit | Notes   |
|------------------------------|--------|-----|-----|------|---------|
| Input/Output Leakage current | IOZ    | -5  | 5   | μA   | 1, 2, 3 |

#### Notes:

- For DQ, DQS\_t, DQS\_c and DMI. Any I/O  $0V \leq V_{OUT} \leq V_{DDQ}$ .
- I/Os status are disabled: High Impedance and ODT Off.
- It is only for typical value @ 85°C.



## 8.2.4 Operating Temperature Range

| Parameter/Condition | Symbol | Min | Max | Unit |
|---------------------|--------|-----|-----|------|
| Standard            | TOPER  | -40 | 85  | °C   |
| Elevated            |        | 85  | 105 | °C   |

### Notes:

- Operating Temperature is the case surface temperature on the center-top side of the LPDDR4/LPDDR4X SDRAM. For the measurement conditions, please refer to JESD51-2 standard.
- Some applications require operation of LPDDR4/LPDDR4X in the maximum temperature conditions in the Elevated Temperature Range between 85°C and 105°C case temperature. For LPDDR4/LPDDR4X SDRAMs, derating may be necessary to operate in this range. See MR4.
- Either the device case temperature rating or the temperature sensor (see section 7.4.37) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Elevated Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.
- All parts list in ordering information table (section 3) will not guarantee to meet functional and AC specification if operating temperature out of the range in order information table.

## 8.3 AC and DC Input/Output Measurement levels

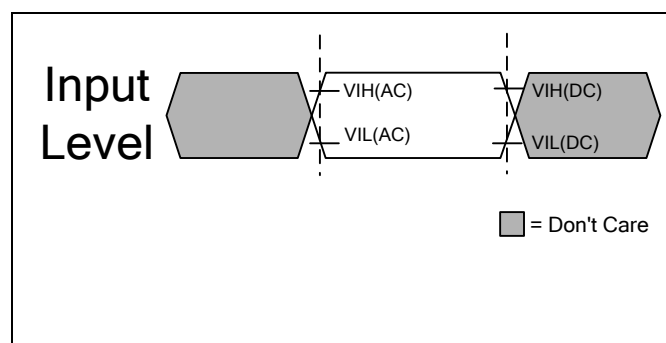
### 8.3.1 DC electrical characteristics

#### 8.3.1.1 Input Level for CKE

| Parameter             | Symbol  | Min                  | Max                  | Unit | Note |
|-----------------------|---------|----------------------|----------------------|------|------|
| Input high level (AC) | VIH(AC) | $0.75 \cdot V_{DD2}$ | $V_{DD2} + 0.2$      | V    | 1    |
| Input low level (AC)  | VIL(AC) | -0.2                 | $0.25 \cdot V_{DD2}$ | V    | 1    |
| Input high level (DC) | VIH(DC) | $0.65 \cdot V_{DD2}$ | $V_{DD2} + 0.2$      | V    |      |
| Input low level (DC)  | VIL(DC) | -0.2                 | $0.35 \cdot V_{DD2}$ | V    |      |

### Note:

- Refer LPDDR4/LPDDR4X AC Over/Undershoot section.



### Notes:

- AC level is guaranteed transition point.
- DC level is hysteresis.

Figure 146 - LPDDR4/LPDDR4X Input AC timing definition for CKE



### 8.3.1.2 Input Level for Reset\_n and ODT\_CA

This definition applies to Reset\_n and ODT\_CA. Below table provides the input level; Figure 147 shows the timing.

| Parameter        | Symbol          | Min                   | Max                   | Unit | Note |
|------------------|-----------------|-----------------------|-----------------------|------|------|
| Input high level | V <sub>IH</sub> | 0.80*V <sub>DD2</sub> | V <sub>DD2</sub> +0.2 | V    | 1    |
| Input low level  | V <sub>IL</sub> | -0.2                  | 0.20*V <sub>DD2</sub> | V    | 1    |

**Note:**  
1. Refer LPDDR4/LPDDR4X AC Over/Undershoot section.

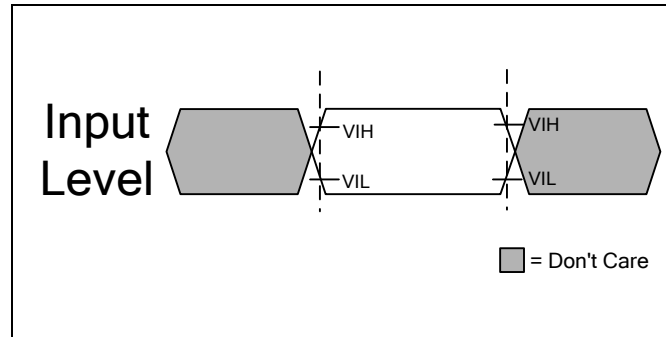


Figure 147 - LPDDR4/LPDDR4X Input AC timing definition for Reset\_n and ODT\_CA

### 8.3.2 AC Over/Undershoot

#### 8.3.2.1 LPDDR4/LPDDR4X AC Over/Undershoot

Table 89 provides the specifications; Figure 148 shows the address and control pins.

Table 89 - LPDDR4/LPDDR4X AC Over/Undershoot

| Parameter                                                       | Specification |
|-----------------------------------------------------------------|---------------|
| Maximum peak Amplitude allowed for overshoot area               | 0.35 V        |
| Maximum peak Amplitude allowed for undershoot area              | 0.35 V        |
| Maximum overshoot area above V <sub>DD</sub> /V <sub>DDQ</sub>  | 0.8 V-nS      |
| Maximum undershoot area below V <sub>SS</sub> /V <sub>SSQ</sub> | 0.8 V-nS      |

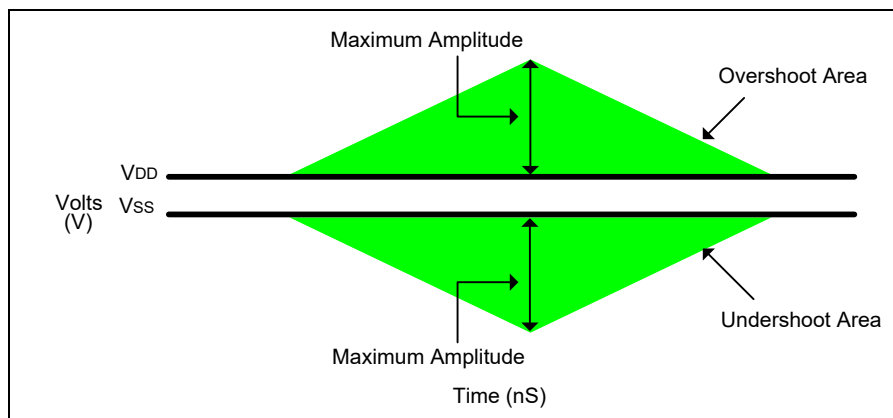


Figure 148 - AC Overshoot and Undershoot Definition for Address and Control Pins



### 8.3.3 Differential Input Voltage

#### 8.3.3.1 Differential Input Voltage for CK

The minimum input voltage need to satisfy both Vindiff\_CK and Vindiff\_CK /2 specification at input receiver and their measurement period is 1 tCK. Vindiff\_CK is the peak to peak voltage centered on 0 volts differential and Vindiff\_CK /2 is max and min peak voltage from 0V.

Figure 149 and Table 90 show the input voltage.

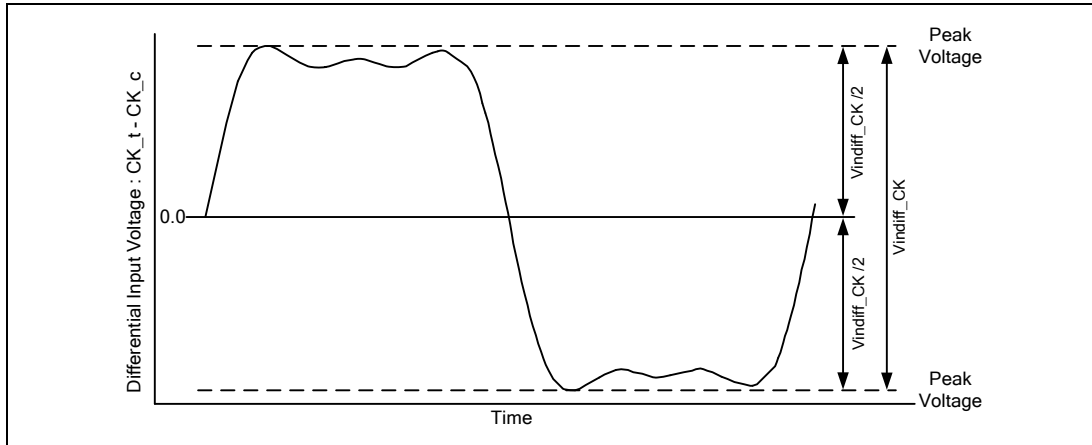


Figure 149 - CK Differential Input Voltage

Table 90 - CK differential input voltage

| Parameter                     | Symbol     | Data Rate |     |                |     |           |     | Unit | Notes |
|-------------------------------|------------|-----------|-----|----------------|-----|-----------|-----|------|-------|
|                               |            | 1600/1867 |     | 2133/2400/3200 |     | 3733/4267 |     |      |       |
|                               |            | Min       | Max | Min            | Max | Min       | Max |      |       |
| CK differential input voltage | Vindiff_CK | 420       | -   | 380            | -   | 360       | -   | mV   | 1, 2  |

**Notes:**

- The requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.
- The peak voltage of Differential CK signals is calculated in a following equation.  

$$\text{Vindiff\_CK} = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$$

$$\text{Max Peak Voltage} = \text{Max}(f(t))$$

$$\text{Min Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = \text{VCK\_t} - \text{VCK\_c}$$



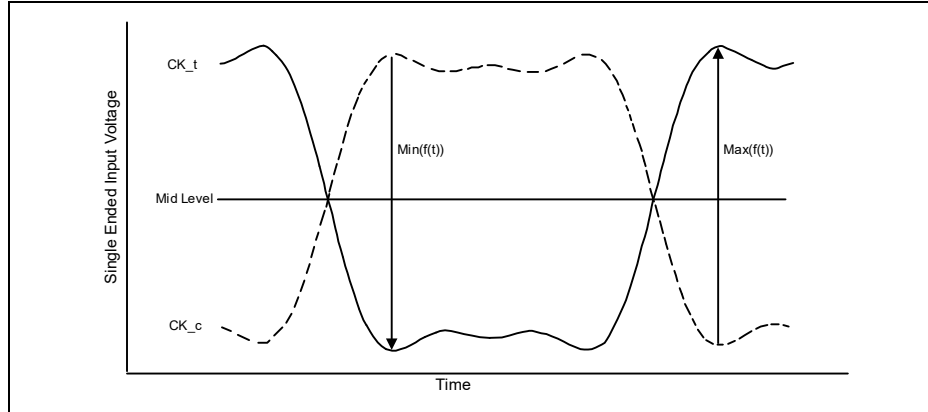
### 8.3.3.2 Peak voltage calculation method

The peak voltage of Differential Clock signals are calculated in a following equation (See Figure 150).

$$V_{IH.DIFF.PEAK} = \text{Max}(f(t))$$

$$V_{IL.DIFF.PEAK} = \text{Min}(f(t))$$

$$f(t) = V_{CK\_t} - V_{CK\_c}$$



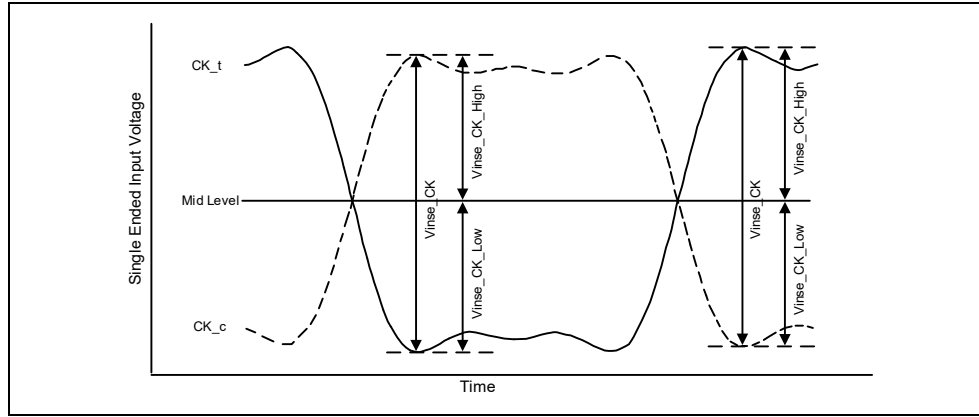
**Note:** 1.  $V_{REFCA}$  is LPDDR4/LPDDR4X SDRAM internal setting value by  $V_{REF}$  Training.

**Figure 150 - Definition of Differential Clock Peak Voltage**



### 8.3.3.3 Single-Ended Input Voltage for Clock

The minimum input voltage needs to satisfy both  $V_{inse\_CK}$ ,  $V_{inse\_CK\_High/Low}$  specification at input receiver. (See Figure 151 and Table 91.)



**Note:** 1.  $V_{REFCA}$  is LPDDR4/LPDDR4X SDRAM internal setting value by  $V_{REF}$  Training.

**Figure 151 - Clock Single-Ended Input Voltage**

**Table 91 - Clock Single-Ended input voltage**

| Parameter                                                     | Symbol        | Data Rate |     |                |     |           |     | Unit | Note |
|---------------------------------------------------------------|---------------|-----------|-----|----------------|-----|-----------|-----|------|------|
|                                                               |               | 1600/1867 |     | 2133/2400/3200 |     | 3733/4267 |     |      |      |
|                                                               |               | Min       | Max | Min            | Max | Min       | Max |      |      |
| Clock Single-Ended input voltage                              | Vinse_CK      | 210       | -   | 190            | -   | 180       | -   | mV   | 1    |
| Clock Single-Ended input voltage High from V <sub>REFDQ</sub> | Vinse_CK_High | 105       | -   | 95             | -   | 90        | -   | mV   | 1    |
| Clock Single-Ended input voltage Low from V <sub>REFDQ</sub>  | Vinse_CK_Low  | 105       | -   | 95             | -   | 90        | -   | mV   | 1    |

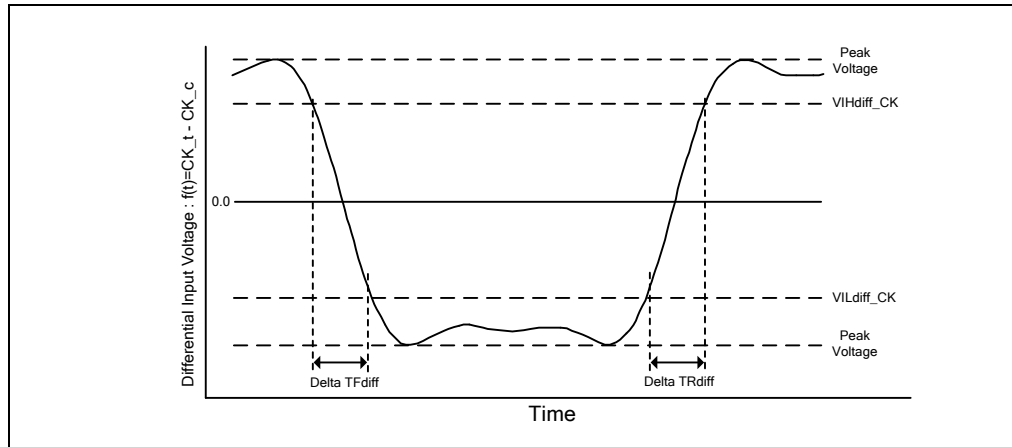
**Note:**

1. The requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.



### 8.3.3.4 Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK\_t, CK\_c) are defined and measured as shown in Figure 152 and Table 92 through Table 94.



**Notes:**

1. Differential signal rising edge from VILdiff\_CK to VIHdiff\_CK must be monotonic slope.
2. Differential signal falling edge from VIHdiff\_CK to VILdiff\_CK must be monotonic slope.

**Figure 152 - Differential Input Slew Rate Definition for CK\_t, CK\_c**

**Table 92 - Differential Input Slew Rate Definition for CK\_t, CK\_c**

| Description                                                | From       | To         | Defined by                                  |
|------------------------------------------------------------|------------|------------|---------------------------------------------|
|                                                            |            |            |                                             |
| Differential input slew rate for rising edge(CK_t - CK_c)  | VILdiff_CK | VIHdiff_CK | $ VILdiff\_CK - VIHdiff\_CK /\Delta TRdiff$ |
| Differential input slew rate for falling edge(CK_t - CK_c) | VIHdiff_CK | VILdiff_CK | $ VILdiff\_CK - VIHdiff\_CK /\Delta TFdiff$ |

**Table 93 - Differential Input Level for CK\_t, CK\_c**

| Parameter               | Symbol     | Data Rate |      |                |      |           |      | Unit | Note |
|-------------------------|------------|-----------|------|----------------|------|-----------|------|------|------|
|                         |            | 1600/1867 |      | 2133/2400/3200 |      | 3733/4267 |      |      |      |
|                         |            | Min       | Max  | Min            | Max  | Min       | Max  |      |      |
| Differential Input High | VIHdiff_CK | 175       | -    | 155            | -    | 145       | -    | mV   | 1    |
| Differential Input Low  | VILdiff_CK | -         | -175 | -              | -155 | -         | -145 | mV   | 1    |

**Note:**

1. The requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.

**Table 94 - Differential Input Slew Rate for CK\_t, CK\_c**

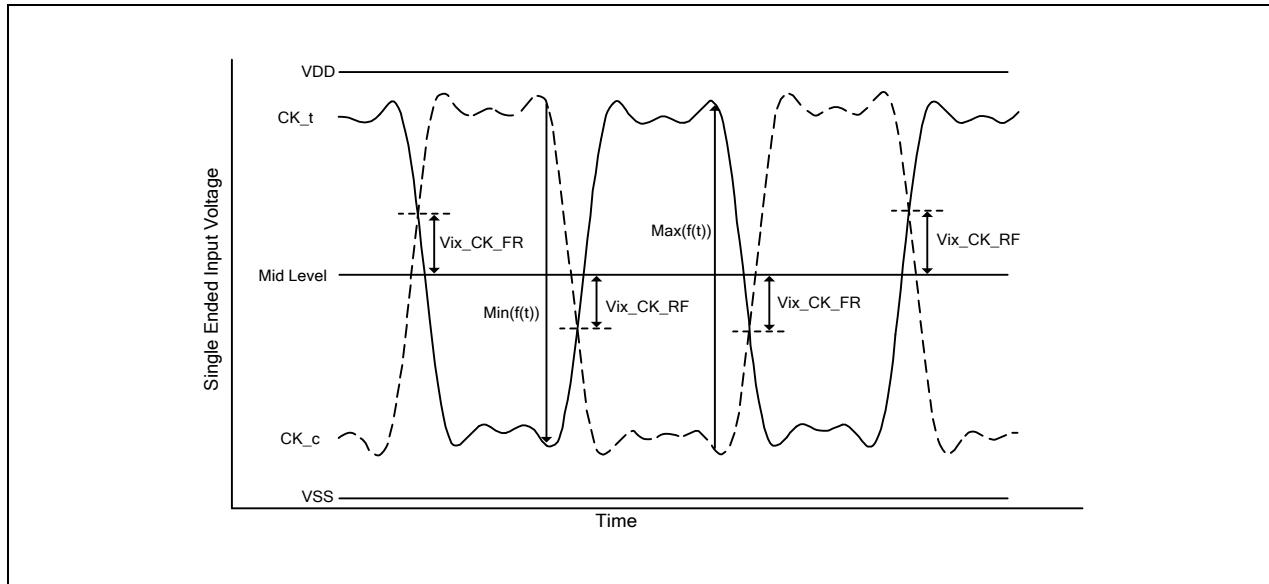
| Parameter                              | Symbol     | Data Rate |     |                |     |           |     | Unit | Note |
|----------------------------------------|------------|-----------|-----|----------------|-----|-----------|-----|------|------|
|                                        |            | 1600/1867 |     | 2133/2400/3200 |     | 3733/4267 |     |      |      |
|                                        |            | Min       | Max | Min            | Max | Min       | Max |      |      |
| Differential Input Slew Rate for Clock | SRIdiff_CK | 2         | 14  | 2              | 14  | 2         | 14  | V/nS |      |





### 8.3.3.5 Differential Input Cross Point Voltage – LPDDR4

The cross point voltage of differential input signals (CK<sub>t</sub>, CK<sub>c</sub>) are shown in Figure 153 and must meet the requirements in Table 95. The differential input cross point voltage V<sub>IX</sub> is measured from the actual cross point of true and complement signals to the mid level.



**Note:** 1. The base level of V<sub>ix\_CK\_FR/RF</sub> is V<sub>REFCA</sub> that is LPDDR4 SDRAM internal setting value by V<sub>REF</sub> Training.

**Figure 153 - Vix Definition (Clock)**

**Table 95 - Cross point voltage for differential input signals (Clock) – LPDDR4**

| Parameter                                          | Symbol       | Data Rate |     |                |     |           |     | Unit | Note             |
|----------------------------------------------------|--------------|-----------|-----|----------------|-----|-----------|-----|------|------------------|
|                                                    |              | 1600/1867 |     | 2133/2400/3200 |     | 3733/4267 |     |      |                  |
|                                                    |              | Min       | Max | Min            | Max | Min       | Max |      |                  |
| Clock Differential input cross point voltage ratio | Vix_CK_ratio | -         | 25  | -              | 25  | -         | 25  | %    | 1, 2, 3, 4, 5, 6 |

**Notes:**

- The requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.
- V<sub>ix\_CK\_Ratio</sub> is defined by this equation:  $V_{ix\_CK\_Ratio} = V_{ix\_CK\_FR}/|Min(f(t))|$ .
- V<sub>ix\_CK\_Ratio</sub> is defined by this equation:  $V_{ix\_CK\_Ratio} = V_{ix\_CK\_RF}/Max(f(t))$ .
- V<sub>ix\_CK\_FR</sub> is defined as delta between cross point (CK<sub>t</sub> fall, CK<sub>c</sub> rise) to Min(f(t))/2.
- V<sub>ix\_CK\_RF</sub> is defined as delta between cross point (CK<sub>t</sub> rise, CK<sub>c</sub> fall) to Max(f(t))/2.
- In LPDDR4 un-terminated case, CK mid-level is calculated as:  
High level = VDDQ, Low level = VSS, Mid-level must be equal or lower than 369mV (33.6% of VDD2).



### 8.3.3.6 Differential Input Voltage for DQS

The minimum input voltage need to satisfy both Vindiff\_DQS and Vindiff\_DQS /2 specification at input receiver and their measurement period is 1UI(tCK/2). Vindiff\_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff\_DQS /2 is max and min peak voltage from 0V. See Figure 154 and Table 96.

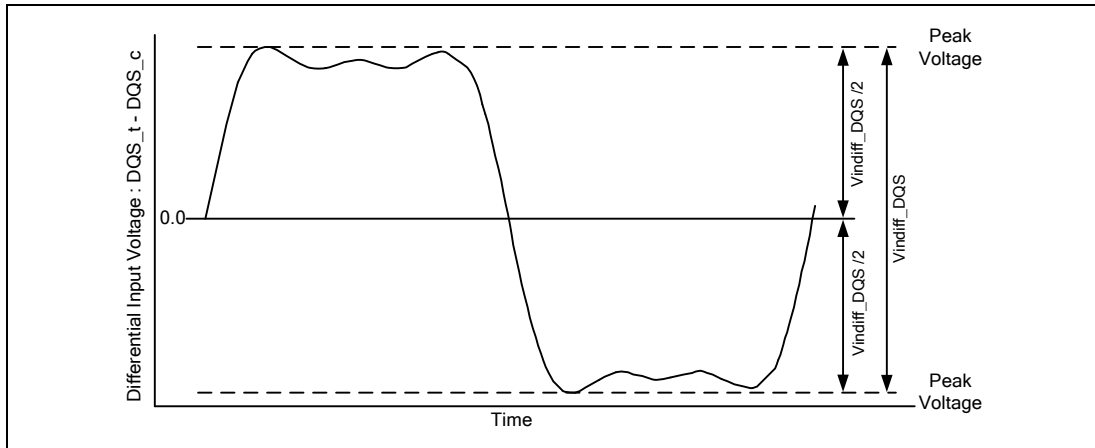


Figure 154 - DQS Differential Input Voltage

Table 96 - DQS differential input voltage

| Parameter              | Symbol      | Data Rate |     |                |     |           |     | Unit | Note |
|------------------------|-------------|-----------|-----|----------------|-----|-----------|-----|------|------|
|                        |             | 1600/1867 |     | 2133/2400/3200 |     | 3733/4267 |     |      |      |
|                        |             | Min       | Max | Min            | Max | Min       | Max |      |      |
| DQS differential input | Vindiff_DQS | 360       | -   | 360            | -   | 340       | -   | mV   | 1, 2 |

#### Notes:

- The requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.
- The peak voltage of Differential DQS signals is calculated in a following equation.

$$Vindiff\_DQS = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$$

$$\text{Max Peak Voltage} = \text{Max}(f(t))$$

$$\text{Min Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = VDQS\_t - VDQS\_c$$



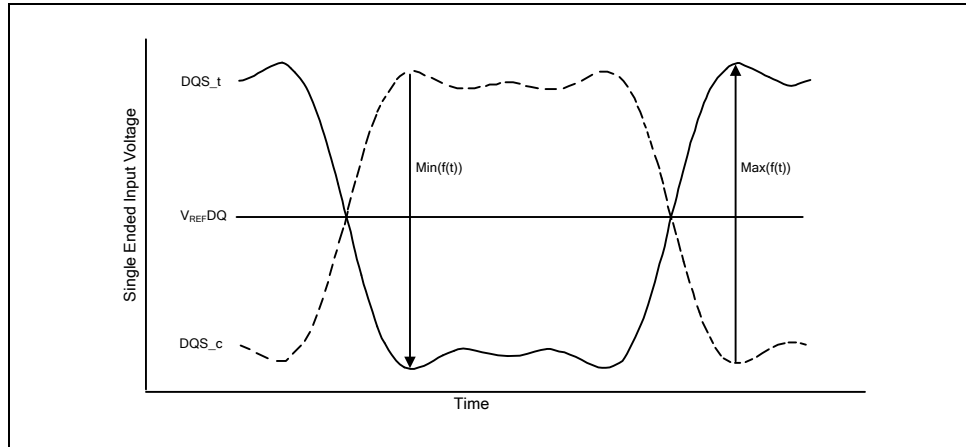
### 8.3.3.7 Peak voltage calculation method

The peak voltage of Differential DQS signals, shown in Figure 155, are calculated in a following equation.

$$V_{IH.DIFF.Peak Voltage} = \text{Max}(f(t))$$

$$V_{IL.DIFF.Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = VDQS\_t - VDQS\_c$$



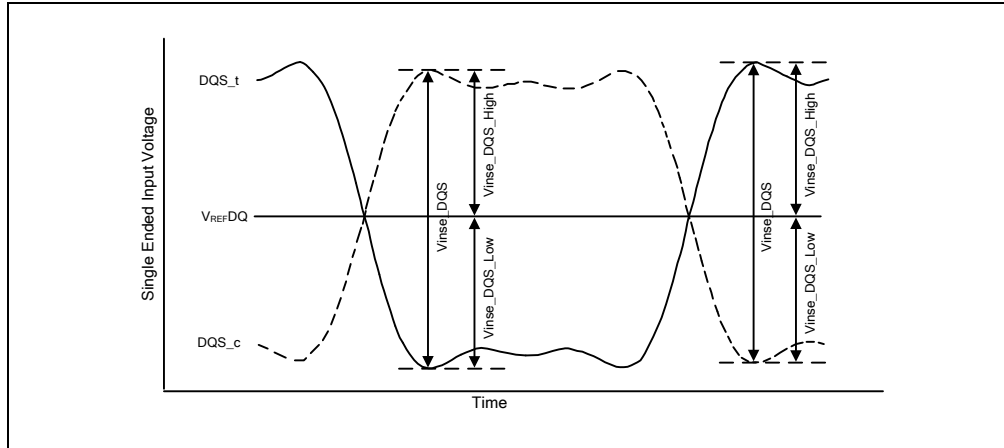
**Note:** 1.  $V_{REFDQ}$  is LPDDR4/LPDDR4X SDRAM internal setting value by  $V_{REF}$  Training.

**Figure 155 - Definition of differential DQS Peak Voltage**



### 8.3.3.8 Single-Ended Input Voltage for DQS

The minimum input voltage needs to satisfy both  $V_{inse\_DQS}$ ,  $V_{inse\_DQS\_High/Low}$  specification at input receiver, as shown in Figure 156 and Table 97.



**Note:** 1.  $V_{REFDQ}$  is LPDDR4/LPDDR4X SDRAM internal setting value by  $V_{REF}$  Training.

**Figure 156 - DQS Single-Ended Input Voltage**

**Table 97 - DQS Single-Ended input voltage**

| Parameter                                       | Symbol         | Data Rate |     |                |     |           |     | Unit | Note |
|-------------------------------------------------|----------------|-----------|-----|----------------|-----|-----------|-----|------|------|
|                                                 |                | 1600/1867 |     | 2133/2400/3200 |     | 3733/4267 |     |      |      |
|                                                 |                | Min       | Max | Min            | Max | Min       | Max |      |      |
| DQS Single-Ended input voltage                  | Vinse_DQS      | 180       | -   | 180            | -   | 170       | -   | mV   | 1    |
| DQS Single-Ended input voltage High from VREFDQ | Vinse_DQS_High | 90        | -   | 90             | -   | 85        | -   | mV   | 1    |
| DQS Single-Ended input voltage Low from VREFDQ  | Vinse_DQS_Low  | 90        | -   | 90             | -   | 85        | -   | mV   | 1    |

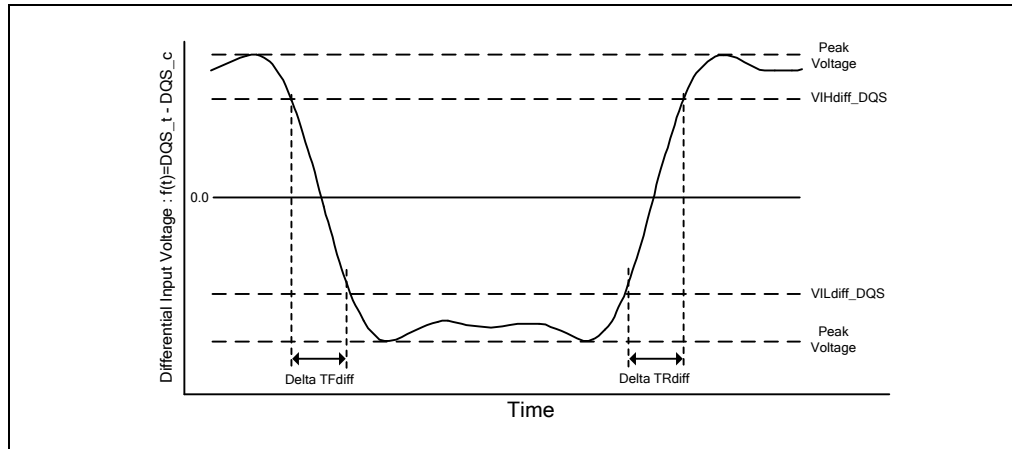
**Note:**

- These requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.



### 8.3.3.9 Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS<sub>t</sub>, DQS<sub>c</sub>) are defined and measured as shown in Figure 157 and Table 98 through Table 100.



**Notes:**

1. Differential signal rising edge from VILdiff\_DQS to VIHdiff\_DQS must be monotonic slope.
2. Differential signal falling edge from VIHdiff\_DQS to VILdiff\_DQS must be monotonic slope.

**Figure 157 - Differential Input Slew Rate Definition for DQS<sub>t</sub>, DQS<sub>c</sub>**

**Table 98 - Differential Input Slew Rate Definition for DQS<sub>t</sub>, DQS<sub>c</sub>**

| Description                                                                         | From        | To          | Defined by                                      |
|-------------------------------------------------------------------------------------|-------------|-------------|-------------------------------------------------|
|                                                                                     |             |             |                                                 |
| Differential input slew rate for rising edge(DQS <sub>t</sub> - DQS <sub>c</sub> )  | VILdiff_DQS | VIHdiff_DQS | $ VILdiff\_DQS - VIHdiff\_DQS  / \Delta TRdiff$ |
| Differential input slew rate for falling edge(DQS <sub>t</sub> - DQS <sub>c</sub> ) | VIHdiff_DQS | VILdiff_DQS | $ VILdiff\_DQS - VIHdiff\_DQS  / \Delta TFdiff$ |

**Table 99 - Differential Input Level for DQS<sub>t</sub>, DQS<sub>c</sub>**

| Parameter               | Symbol      | Data Rate |      |                |      |           |      | Unit | Note |
|-------------------------|-------------|-----------|------|----------------|------|-----------|------|------|------|
|                         |             | 1600/1867 |      | 2133/2400/3200 |      | 3733/4267 |      |      |      |
|                         |             | Min       | Max  | Min            | Max  | Min       | Max  |      |      |
| Differential Input High | VIHdiff_DQS | 140       | -    | 140            | -    | 120       | -    | mV   | 1    |
| Differential Input Low  | VILdiff_DQS | -         | -140 | -              | -140 | -         | -120 | mV   | 1    |

**Note:**

1. The requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.

**Table 100 - Differential Input Slew Rate for DQS<sub>t</sub>, DQS<sub>c</sub>**

| Parameter                    | Symbol  | Data Rate |     |                |     |           |     | Unit | Note |
|------------------------------|---------|-----------|-----|----------------|-----|-----------|-----|------|------|
|                              |         | 1600/1867 |     | 2133/2400/3200 |     | 3733/4267 |     |      |      |
|                              |         | Min       | Max | Min            | Max | Min       | Max |      |      |
| Differential Input Slew Rate | SRIdiff | 2         | 14  | 2              | 14  | 2         | 14  | V/nS | 1    |

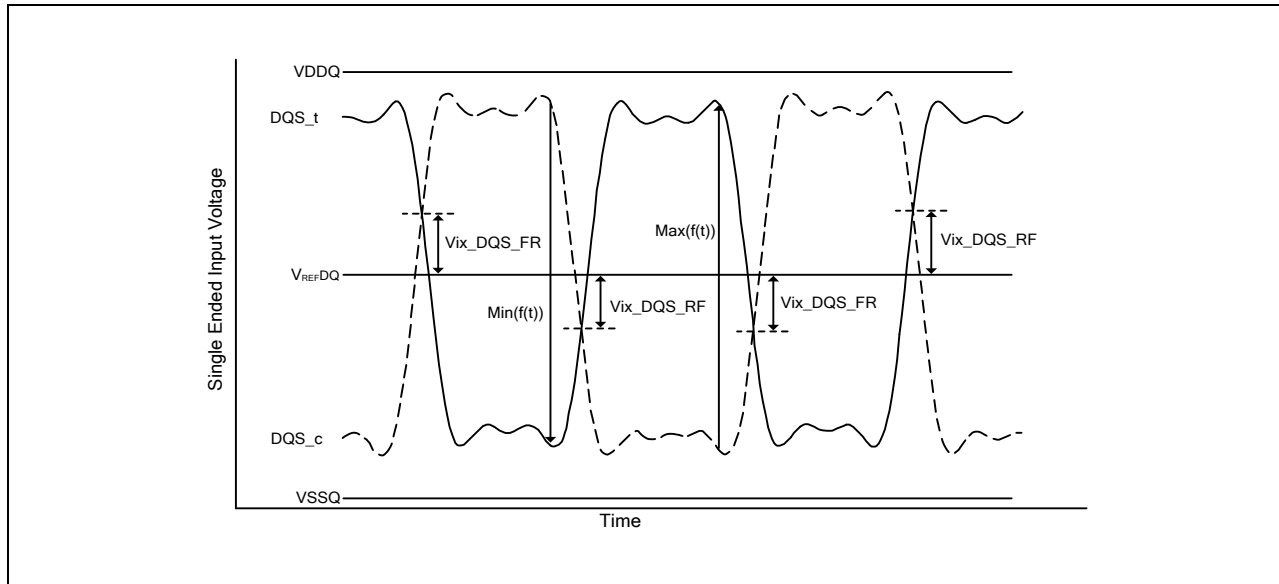
**Note:**

1. The requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.



### 8.3.3.10 Differential Input Cross Point Voltage

The cross point voltage of differential input signals (DQS\_t, DQS\_c) must meet the requirements in Table 101. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is VREFDQ as shown in Figure 158.



**Note:** 1. The base level of Vix\_DQS\_FR/RF is VREFDQ that is LPDDR4/LPDDR4X SDRAM internal setting value by VREF Training.

**Figure 158 - Vix Definition (DQS)**

**Table 101 - Cross point voltage for differential input signals (DQS)**

| Parameter                                        | Symbol        | Data Rate |     |                |     |           |     | Unit | Note    |
|--------------------------------------------------|---------------|-----------|-----|----------------|-----|-----------|-----|------|---------|
|                                                  |               | 1600/1867 |     | 2133/2400/3200 |     | 3733/4267 |     |      |         |
|                                                  |               | Min       | Max | Min            | Max | Min       | Max |      |         |
| DQS Differential input cross point voltage ratio | Vix_DQS_ratio | -         | 20  | -              | 20  | -         | 20  | %    | 1, 2, 3 |

**Notes:**

1. The requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.
2. Vix\_DQS\_Ratio is defined by this equation:  $Vix\_DQS\_Ratio = Vix\_DQS\_FR / |Min(f(t))|$ .
3. Vix\_DQS\_Ratio is defined by this equation:  $Vix\_DQS\_Ratio = Vix\_DQS\_RF / Max(f(t))$ .



### 8.3.4 Input level for ODT\_CA input

The levels are provided in Table 102.

Table 102 - Input Level for ODT\_CA

| Symbol |                      | Min       | Max       | Unit | Note |
|--------|----------------------|-----------|-----------|------|------|
| VIHODT | ODT Input High Level | 0.75*VDD2 | VDD2+0.2  | V    |      |
| VILODT | ODT Input Low Level  | -0.2      | 0.25*VDD2 | V    |      |

### 8.3.5 Single Ended Output Slew Rate

The slew rate is provided in Figure 159 and Table 103.

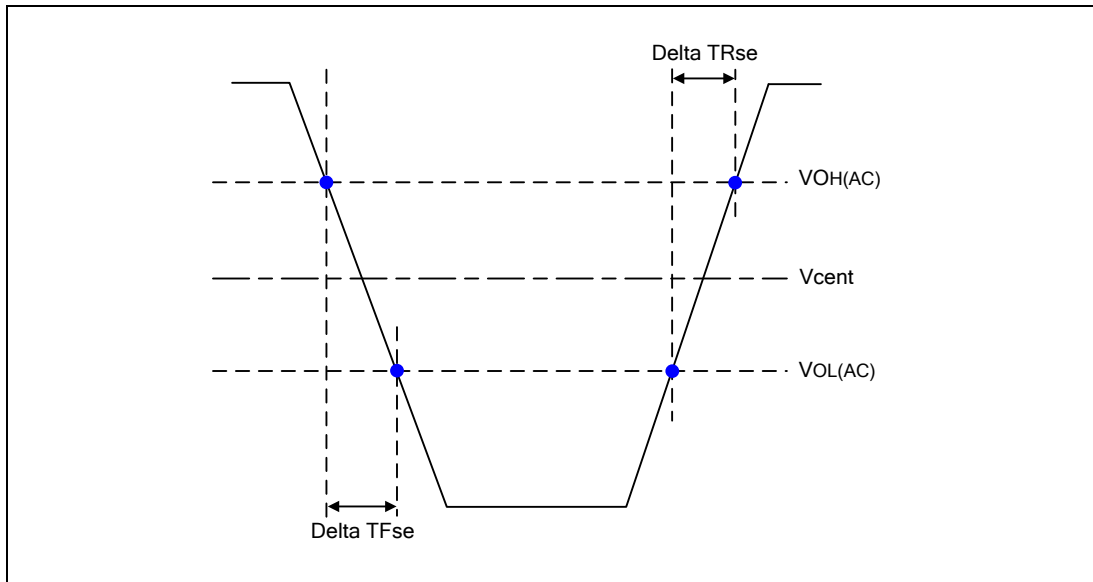


Figure 159 - Single Ended Output Slew Rate Definition

Table 103 - Output Slew Rate (Single-ended) for 1.1V VDDQ

| Parameter                                              | Symbol | Value             |                   | Units |
|--------------------------------------------------------|--------|-------------------|-------------------|-------|
|                                                        |        | Min <sup>*1</sup> | Max <sup>*2</sup> |       |
| Single-ended Output Slew Rate ( $V_{OH} = V_{DDQ}/3$ ) | SRQse  | 3.5               | 9                 | V/nS  |
| Output slew-rate matching Ratio (Rise to Fall)         | -      | 0.8               | 1.2               | -     |

#### Description:

**SR:** Slew Rate

**Q:** Query Output (like in DQ, which stands for Data-in, Query-Output)

**se:** Single-ended Signals

#### Notes:

1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between  $V_{OL}(AC) = 0.2 \cdot V_{OH}(DC)$  and  $V_{OH}(AC) = 0.8 \cdot V_{OH}(DC)$ .
4. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.



### 8.3.6 Differential Output Slew Rate

The slew rate is provided in Figure 160 and Table 104.

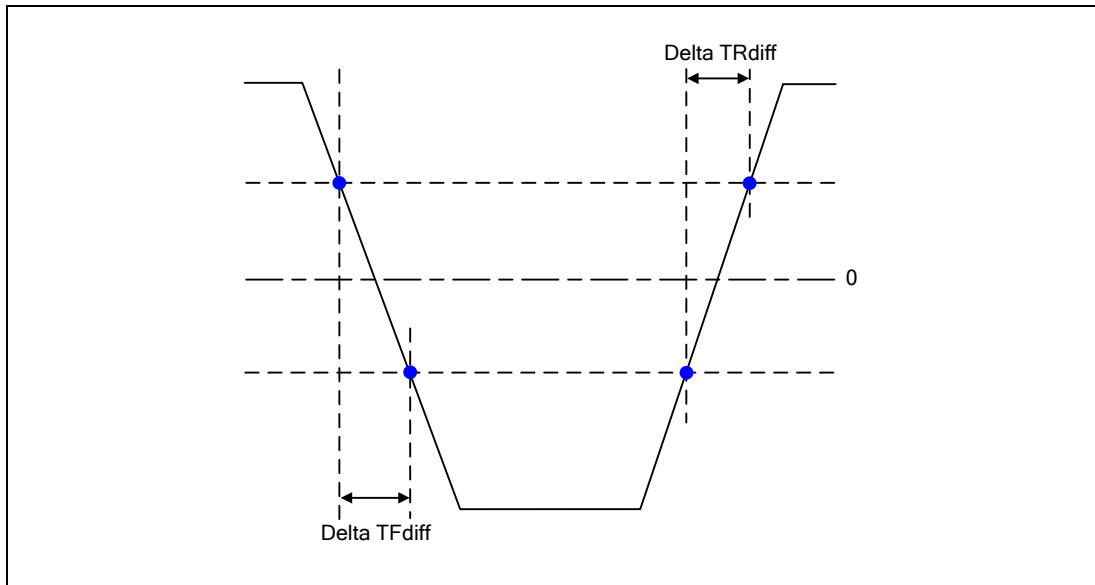


Figure 160 - Differential Output Slew Rate Definition

Table 104 - Differential Output Slew Rate for 1.1V VDDQ

| Parameter                                            | Symbol  | Value |     | Units |
|------------------------------------------------------|---------|-------|-----|-------|
|                                                      |         | Min   | Max |       |
| Differential Output Slew Rate ( $V_{OH}=V_{DDQ}/3$ ) | SRQdiff | 7     | 18  | V/nS  |

**Description:**

**SR:** Slew Rate

**Q:** Query Output (like in DQ, which stands for Data-in, Query-Output)

**diff:** Differential Signals

**Notes:**

1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between  $V_{OL}(AC) = -0.8 \cdot V_{OH}(DC)$  and  $V_{OH}(AC) = 0.8 \cdot V_{OH}(DC)$ .
3. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.





### 8.3.7 Overshoot and Undershoot for LVSTL

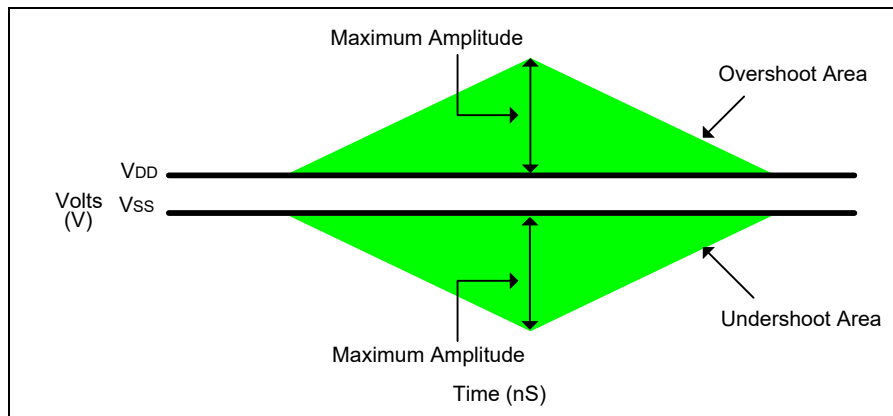
The levels are provided in Table 105 and Figure 161.

**Table 105 - AC Overshoot/Undershoot Specification**

| Parameter                                                               |     | Data Rate |      |      |      |      |      | Unit |
|-------------------------------------------------------------------------|-----|-----------|------|------|------|------|------|------|
|                                                                         |     | 1600      | 1866 | 2667 | 3200 | 3733 | 4267 |      |
| Maximum peak amplitude allowed for overshoot area.<br>(See Figure 161)  | Max | 0.3       | 0.3  | 0.3  | 0.3  | 0.3  | 0.3  | V    |
| Maximum peak amplitude allowed for undershoot area.<br>(See Figure 161) | Max | 0.3       | 0.3  | 0.3  | 0.3  | 0.3  | 0.3  | V    |
| Maximum area above VDD.<br>(See Figure 161)                             | Max | 0.1       | 0.1  | 0.1  | 0.1  | 0.1  | 0.1  | V-nS |
| Maximum area below VSS.<br>(See Figure 161)                             | Max | 0.1       | 0.1  | 0.1  | 0.1  | 0.1  | 0.1  | V-nS |

**Notes:**

1. VDD2 stands for VDD for CA[5:0], CK\_t, CK\_c, CS\_n, CKE and ODT. VDD stands for VDDQ for DQ, DMI, DQS\_t and DQS\_c.
2. Vss stands for Vss for CA[5:0], CK\_t, CK\_c, CS\_n, CKE and ODT. Vss stands for Vssq for DQ, DMI, DQS\_t and DQS\_c.
3. Maximum peak amplitude values are referenced from actual VDD and Vss values.
4. Maximum area values are referenced from maximum operating VDD and Vss values.

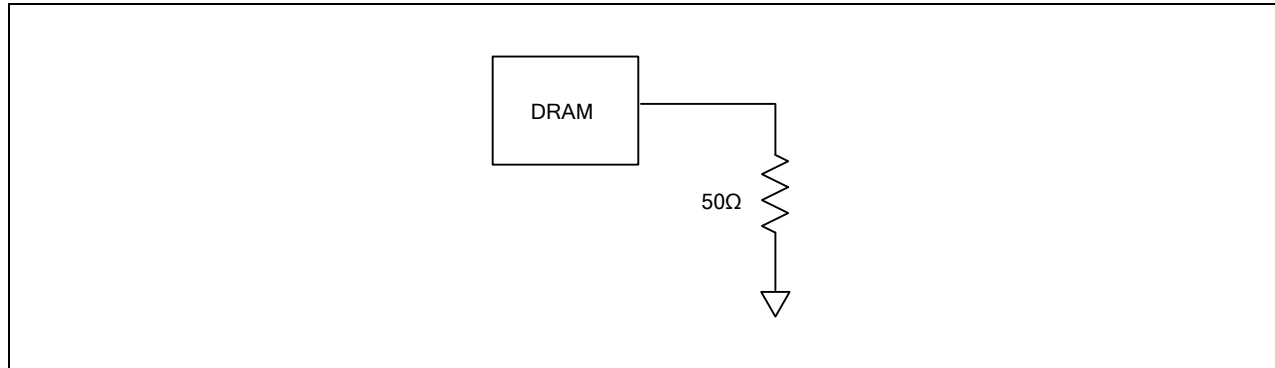


**Figure 161 - Overshoot and Undershoot Definition**



### 8.3.8 Driver Output Timing Reference load

These 'Timing Reference Loads' (Figure 162) are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



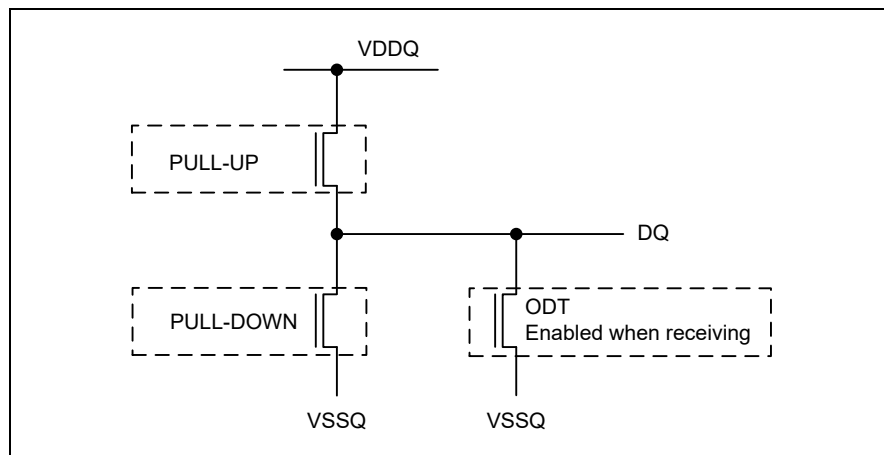
**Note:**

1. All output timing parameter values are reported with respect to this reference load.  
This reference load is also used to report slew rate.

**Figure 162 - Driver Output Reference Load for Timing and Slew Rate**

### 8.3.9 LVSTL (Low Voltage Swing Terminated Logic) IO System for 1.1V VDDQ

LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in Figure 163.



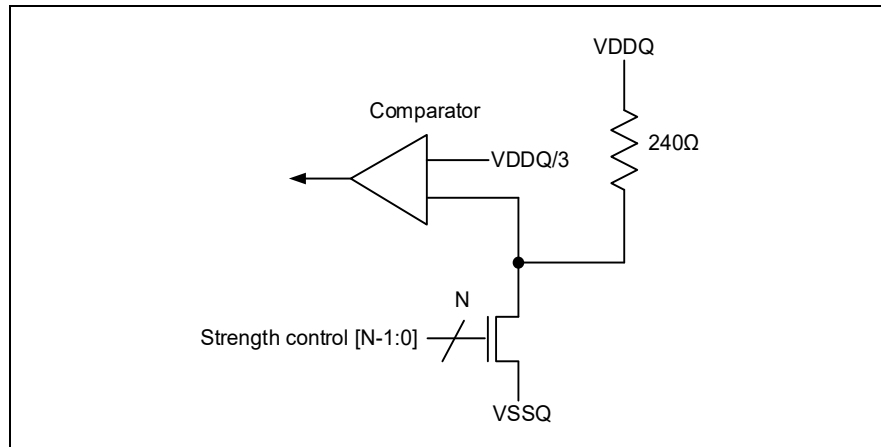
**Figure 163 - LVSTL I/O Cell**



To ensure that the target impedance is achieved the LVSTL I/O cell is designed to be calibrated as below procedure.

1. First calibrate the pull-down device against a  $240\ \Omega$  resistor to VDDQ via the ZQ pin. (Figure 164.)

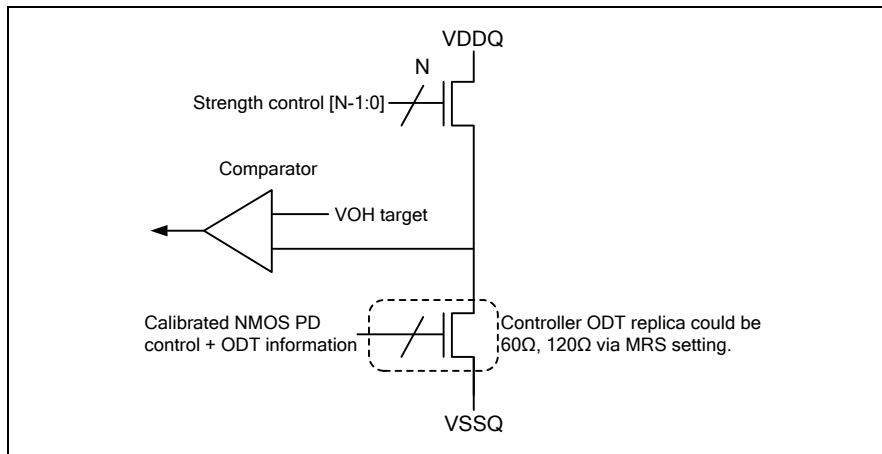
- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is less than  $VDDQ/3$
- NMOS pull-down device is calibrated to  $120\ \Omega$



**Figure 164 - Pull-down calibration for LPDDR4**

2. Then calibrate the pull-up device against the calibrated pull-down device. (Figure 165.)

- Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS)
- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is greater than VOH target
- NMOS pull-up device is now calibrated to VOH target



**Figure 165 - Pull-up calibration**



## 8.4 Input/Output Capacitance

Table 106 - Input/Output Capacitance

| Parameter                                                                 | Symbol |     | LPDDR4/LPDDR4X<br>533-3200 | LPDDR4/LPDDR4X<br>3733-4267 | Units | Notes   |
|---------------------------------------------------------------------------|--------|-----|----------------------------|-----------------------------|-------|---------|
| Input capacitance,<br>CK <sub>t</sub> and CK <sub>c</sub>                 | CCK    | Min | 0.5                        | 0.5                         | pF    | 1, 2    |
|                                                                           |        | Max | 0.9                        | 0.9                         |       | 1, 2    |
| Input capacitance delta,<br>CK <sub>t</sub> and CK <sub>c</sub>           | CDCK   | Min | 0                          | 0                           | pF    | 1, 2, 3 |
|                                                                           |        | Max | 0.09                       | 0.09                        |       | 1, 2, 3 |
| Input capacitance,<br>all other input-only pins                           | CI     | Min | 0.5                        | 0.5                         | pF    | 1, 2, 4 |
|                                                                           |        | Max | 0.9                        | 0.9                         |       | 1, 2, 4 |
| Input capacitance delta,<br>all other input-only pins                     | CDI    | Min | -0.1                       | -0.1                        | pF    | 1, 2, 5 |
|                                                                           |        | Max | 0.1                        | 0.1                         |       | 1, 2, 5 |
| Input/output capacitance, DQ,<br>DMI, DQS <sub>t</sub> , DQS <sub>c</sub> | CIO    | Min | 0.7                        | 0.7                         | pF    | 1, 2, 6 |
|                                                                           |        | Max | 1.3                        | 1.3                         |       | 1, 2, 6 |
| Input/output capacitance delta,<br>DQS <sub>t</sub> , DQS <sub>c</sub>    | CDDQS  | Min | 0                          | 0                           | pF    | 1, 2, 7 |
|                                                                           |        | Max | 0.1                        | 0.1                         |       | 1, 2, 7 |
| Input/output capacitance delta,<br>DQ, DMI                                | CDIO   | Min | -0.1                       | -0.1                        | pF    | 1, 2, 8 |
|                                                                           |        | Max | 0.1                        | 0.1                         |       | 1, 2, 8 |
| Input/output capacitance,<br>ZQ pin                                       | CZQ    | Min | 0                          | 0                           | pF    | 1, 2    |
|                                                                           |        | Max | 5                          | 5                           |       | 1, 2    |

### Notes:

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating).
3. Absolute value of CCK<sub>t</sub> . CCK<sub>c</sub>.
4. CI applies to CS<sub>n</sub>, CKE, CA0~CA5.
5. CDI = CI - 0.5 \* (CCK<sub>t</sub> + CCK<sub>c</sub>).
6. DMI loading matches DQ and DQS.
7. Absolute value of CDQS<sub>t</sub> and CDQS<sub>c</sub>.
8. CDIO = CIO - Average(CDQn, CDMI, CDQS<sub>t</sub>, CDQS<sub>c</sub>) in byte-lane.



## 8.5 IDD Specification Parameters and Test Conditions

### 8.5.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW:  $V_{IN} \leq V_{IL(DC)} \text{ MAX}$

HIGH:  $V_{IN} \geq V_{IH(DC)} \text{ MIN}$

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See Table 107 and Table 108.

Table 107 through Table 119 provide the IDD measurement conditions.

**Table 107 - Definition of Switching for CA Input Signals**

| Switching for CA |      |      |      |      |      |      |      |      |
|------------------|------|------|------|------|------|------|------|------|
| CK_t edge        | R1   | R2   | R3   | R4   | R5   | R6   | R7   | R8   |
| CKE              | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH |
| CS               | LOW  | LOW  | LOW  | LOW  | LOW  | LOW  | LOW  | LOW  |
| CA0              | HIGH | LOW  | LOW  | LOW  | LOW  | HIGH | HIGH | HIGH |
| CA1              | HIGH | HIGH | HIGH | LOW  | LOW  | LOW  | LOW  | HIGH |
| CA2              | HIGH | LOW  | LOW  | LOW  | LOW  | HIGH | HIGH | HIGH |
| CA3              | HIGH | HIGH | HIGH | LOW  | LOW  | LOW  | LOW  | HIGH |
| CA4              | HIGH | LOW  | LOW  | LOW  | LOW  | HIGH | HIGH | HIGH |
| CA5              | HIGH | HIGH | HIGH | LOW  | LOW  | LOW  | LOW  | HIGH |

**Notes:**

1. CS must always be driven LOW.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

**Table 108 - CA pattern for ldd4R for BL=16**

| Clock Cycle Number | CKE  | CS   | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|---------|-----|-----|-----|-----|-----|-----|
| N                  | HIGH | HIGH | Read-1  | L   | H   | L   | L   | L   | L   |
| N+1                | HIGH | LOW  |         | L   | H   | L   | L   | L   | L   |
| N+2                | HIGH | HIGH | CAS-2   | L   | H   | L   | L   | H   | L   |
| N+3                | HIGH | LOW  |         | L   | L   | L   | L   | L   | L   |
| N+4                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+5                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+6                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+7                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+8                | HIGH | HIGH | Read-1  | L   | H   | L   | L   | L   | L   |
| N+9                | HIGH | LOW  |         | L   | H   | L   | L   | H   | L   |
| N+10               | HIGH | HIGH | CAS-2   | L   | H   | L   | L   | H   | H   |
| N+11               | HIGH | LOW  |         | H   | H   | H   | H   | H   | H   |
| N+12               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+13               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+14               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+15               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |

**Notes:**

1. BA[2:0] = 010, C[9:4] = 000000 or 111111, Burst Order C[3:2] = 00 or 11 (Same as LPDDR3 IDD4R Spec).
2. Difference from LPDDR3 Spec: CA pins are kept low with DES CMD to reduce ODT current.



Table 109 - CA pattern for IDD4W for BL=16

| Clock Cycle Number | CKE  | CS   | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|---------|-----|-----|-----|-----|-----|-----|
| N                  | HIGH | HIGH | Write-1 | L   | L   | H   | L   | L   | L   |
| N+1                | HIGH | LOW  |         | L   | H   | L   | L   | L   | L   |
| N+2                | HIGH | HIGH | CAS-2   | L   | H   | L   | L   | H   | L   |
| N+3                | HIGH | LOW  |         | L   | L   | L   | L   | L   | L   |
| N+4                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+5                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+6                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+7                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+8                | HIGH | HIGH | Write-1 | L   | L   | H   | L   | L   | L   |
| N+9                | HIGH | LOW  |         | L   | H   | L   | L   | H   | L   |
| N+10               | HIGH | HIGH | CAS-2   | L   | H   | L   | L   | H   | H   |
| N+11               | HIGH | LOW  |         | L   | L   | H   | H   | H   | H   |
| N+12               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+13               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+14               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+15               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |

**Notes:**

1. BA[2:0] = 010, C[9:4] = 000000 or 111111 (Same as LPDDR3 IDD4W Spec).
2. Difference from LPDDR3 Spec:
  - 1-No burst ordering.
  - 2-CA pins are kept low with DES CMD to reduce ODT current.



Table 110 - Data pattern for Idd4W (DBI off) for BL=16

| DBI OFF Case |       |       |       |       |       |       |       |       |     | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|              | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL0          | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL1          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL2          | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL3          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL4          | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL5          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL6          | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL7          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL8          | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL9          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL10         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL11         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL12         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL13         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL14         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL15         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
|              |       |       |       |       |       |       |       |       |     |            |
| BL16         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL17         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL18         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL19         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL20         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL21         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL22         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL23         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL24         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL25         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL26         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL27         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL28         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL29         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL30         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL31         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| No. of 1's   | 16    | 16    | 16    | 16    | 16    | 16    | 16    | 16    |     |            |

**Note:**

1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for Idd4W/R pattern programming.



Table 111 - Data pattern for IDD4R (DBI off) for BL=16

| DBI OFF Case |       |       |       |       |       |       |       |       |     | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|              | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL0          | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL1          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL2          | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL3          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL4          | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL5          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL6          | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL7          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL8          | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL9          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL10         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL11         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL12         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL13         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL14         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL15         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
|              |       |       |       |       |       |       |       |       |     |            |
| BL16         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL17         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL18         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL19         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL20         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL21         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL22         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL23         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL24         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL25         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL26         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL27         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL28         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL29         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL30         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL31         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| No. of 1's   | 16    | 16    | 16    | 16    | 16    | 16    | 16    | 16    |     |            |

**Note:**

1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.





Table 112 - Data pattern for Idd4W (DBI on) for BL=16

| DBI ON Case |       |       |       |       |       |       |       |       |     | No. of 1's |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|             | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL0         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL1         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL2         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL3         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL4         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL5         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL6         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL7         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL8         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL9         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL10        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL11        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL12        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL13        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL14        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL15        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
|             |       |       |       |       |       |       |       |       |     |            |
| BL16        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL17        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL18        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL19        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL20        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL21        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL22        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL23        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL24        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL25        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL26        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL27        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL28        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL29        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL30        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL31        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| No. of 1's  | 8     | 8     | 8     | 8     | 8     | 8     | 16    | 16    | 8   |            |

 DBI enabled burst



Table 113 - Data pattern for IDD4R (DBI on) for BL=16

| DBI ON Case |       |       |       |       |       |       |       |       |     | No. of 1's |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|             | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL0         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL1         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL2         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL3         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL4         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL5         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL6         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL7         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL8         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL9         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL10        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL11        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL12        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL13        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL14        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL15        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
|             |       |       |       |       |       |       |       |       |     |            |
| BL16        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL17        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL18        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL19        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL20        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL21        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL22        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL23        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL24        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL25        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL26        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL27        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL28        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL29        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL30        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL31        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| No. of 1's  | 8     | 8     | 8     | 8     | 8     | 8     | 16    | 16    | 8   |            |

 DBI enabled burst



Table 114 - CA Pattern for IDD4R for BL=32

| Clock Cycle Number | CKE  | CS   | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|---------|-----|-----|-----|-----|-----|-----|
| N                  | HIGH | HIGH | Read-1  | L   | H   | L   | L   | L   | L   |
| N+1                | HIGH | LOW  |         | L   | H   | L   | L   | L   | L   |
| N+2                | HIGH | HIGH | CAS-2   | L   | H   | L   | L   | H   | L   |
| N+3                | HIGH | LOW  |         | L   | L   | L   | L   | L   | L   |
| N+4                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+5                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+6                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+7                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+8                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+9                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+10               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+11               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+12               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+13               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+14               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+15               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+16               | HIGH | HIGH | Read-1  | L   | H   | L   | L   | L   | L   |
| N+17               | HIGH | LOW  |         | L   | H   | L   | L   | H   | L   |
| N+18               | HIGH | HIGH | CAS-2   | L   | H   | L   | L   | H   | H   |
| N+19               | HIGH | LOW  |         | H   | H   | L   | H   | H   | H   |
| N+20               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+21               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+22               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+23               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+24               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+25               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+26               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+27               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+28               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+29               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+30               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+31               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |

**Note:**

1. BA[2:0] = 010, C[9:5] = 00000 or 11111, Burst Order C[4:2] = 000 or 111.



Table 115 - CA Pattern for Idd4W for BL=32

| Clock Cycle Number | CKE  | CS   | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|---------|-----|-----|-----|-----|-----|-----|
| N                  | HIGH | HIGH | Write-1 | L   | L   | H   | L   | L   | L   |
| N+1                | HIGH | LOW  |         | L   | H   | L   | L   | L   | L   |
| N+2                | HIGH | HIGH | CAS-2   | L   | H   | L   | L   | H   | L   |
| N+3                | HIGH | LOW  |         | L   | L   | L   | L   | L   | L   |
| N+4                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+5                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+6                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+7                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+8                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+9                | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+10               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+11               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+12               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+13               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+14               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+15               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+16               | HIGH | HIGH | Write-1 | L   | L   | H   | L   | L   | L   |
| N+17               | HIGH | LOW  |         | L   | H   | L   | L   | H   | L   |
| N+18               | HIGH | HIGH | CAS-2   | L   | H   | L   | L   | H   | H   |
| N+19               | HIGH | LOW  |         | L   | L   | L   | H   | H   | H   |
| N+20               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+21               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+22               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+23               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+24               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+25               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+26               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+27               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+28               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+29               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+30               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |
| N+31               | HIGH | LOW  | DES     | L   | L   | L   | L   | L   | L   |

**Note:**

1. BA[2:0] = 010, C[9:5] = 00000 or 11111.



Table 116 - Data Pattern for Idd4W (DBI off) for BL=32

| DBI OFF Case |       |       |       |       |       |       |       |       |     | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|              | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL0          | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL1          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL2          | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL3          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL4          | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL5          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL6          | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL7          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL8          | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL9          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL10         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL11         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL12         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL13         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL14         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL15         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
|              |       |       |       |       |       |       |       |       |     |            |
| BL16         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL17         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL18         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL19         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL20         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL21         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL22         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL23         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL24         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL25         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL26         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL27         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL28         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL29         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL30         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL31         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |



Table 116 - Data Pattern for ID4W (DBI off) for BL=32 (Cont'd)

| DBI OFF Case |       |       |       |       |       |       |       |       |     | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|              | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL32         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL33         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL34         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL35         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL36         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL37         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL38         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL39         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL40         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL41         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL42         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL43         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL44         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL45         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL46         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL47         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
|              |       |       |       |       |       |       |       |       |     |            |
| BL48         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL49         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL50         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL51         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL52         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL53         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL54         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL55         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL56         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL57         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL58         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL59         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL60         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL61         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL62         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL63         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| No. of 1's   | 32    | 32    | 32    | 32    | 32    | 32    | 32    | 32    |     |            |

**Note:**

1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for ID4W/R pattern programming.



Table 117 - Data Pattern for IDD4R (DBI off) for BL=32

| DBI OFF Case |       |       |       |       |       |       |       |       |     | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|              | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL0          | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL1          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL2          | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL3          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL4          | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL5          | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL6          | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL7          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL8          | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL9          | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL10         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL11         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL12         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL13         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL14         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL15         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
|              |       |       |       |       |       |       |       |       |     |            |
| BL16         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL17         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL18         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL19         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL20         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL21         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL22         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL23         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL24         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL25         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL26         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL27         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL28         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL29         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL30         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL31         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |



Table 117 - Data Pattern for ID4R (DBI off) for BL=32 (Cont'd)

| DBI OFF Case |       |       |       |       |       |       |       |       |     | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|              | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL32         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL33         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL34         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL35         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL36         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL37         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL38         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL39         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL40         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL41         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL42         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL43         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL44         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL45         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL46         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL47         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
|              |       |       |       |       |       |       |       |       |     |            |
| BL48         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL49         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL50         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL51         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL52         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL53         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL54         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL55         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL56         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL57         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL58         | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8          |
| BL59         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL60         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL61         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL62         | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6          |
| BL63         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| No. of 1's   | 32    | 32    | 32    | 32    | 32    | 32    | 32    | 32    |     |            |

**Note:**

1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for ID4W/R pattern programming.





Table 118 - Data Pattern for IDD4W (DBI on) for BL=32

| DBI ON Case |       |       |       |       |       |       |       |       |     | No. of 1's |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|             | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL0         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL1         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL2         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL3         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL4         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL5         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL6         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL7         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL8         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL9         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL10        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL11        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL12        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL13        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL14        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL15        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
|             |       |       |       |       |       |       |       |       |     |            |
| BL16        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL17        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL18        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL19        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL20        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL21        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL22        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL23        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL24        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL25        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL26        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL27        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL28        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL29        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL30        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL31        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |

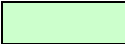
 DBI enabled burst



Table 118 - Data Pattern for IdD4W (DBI on) for BL=32 (Cont'd)

| DBI ON Case |       |       |       |       |       |       |       |       |     | No. of 1's |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|             | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL32        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL33        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL34        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL35        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL36        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL37        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL38        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL39        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL40        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL41        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL42        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL43        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL44        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL45        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL46        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL47        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
|             |       |       |       |       |       |       |       |       |     |            |
| BL48        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL49        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL50        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL51        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL52        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL53        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL54        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL55        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL56        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL57        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL58        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL59        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL60        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL61        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL62        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL63        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| No. of 1's  | 16    | 16    | 16    | 16    | 16    | 16    | 32    | 32    | 16  |            |

 DBI enabled burst



Table 119 - Data Pattern for IDD4R (DBI on) for BL=32

| DBI ON Case |       |       |       |       |       |       |       |       |     | No. of 1's |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|             | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL0         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL1         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL2         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL3         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL4         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL5         | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL6         | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL7         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL8         | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL9         | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL10        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL11        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL12        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL13        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL14        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL15        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
|             |       |       |       |       |       |       |       |       |     |            |
| BL16        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL17        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL18        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL19        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL20        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL21        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL22        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL23        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL24        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL25        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL26        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL27        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL28        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL29        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL30        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL31        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |

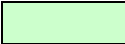
 DBI enabled burst



Table 119 - Data Pattern for IDD4R (DBI on) for BL=32 (Cont'd)

| DBI ON Case |       |       |       |       |       |       |       |       |     | No. of 1's |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
|             | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |            |
| BL32        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL33        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL34        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL35        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL36        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL37        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL38        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL39        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL40        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL41        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL42        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL43        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL44        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL45        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL46        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL47        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
|             |       |       |       |       |       |       |       |       |     |            |
| BL48        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL49        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL50        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL51        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL52        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL53        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL54        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL55        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL56        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0          |
| BL57        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL58        | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1          |
| BL59        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| BL60        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2          |
| BL61        | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4          |
| BL62        | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3          |
| BL63        | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4          |
| No. of 1's  | 16    | 16    | 16    | 16    | 16    | 16    | 32    | 32    | 16  |            |

 DBI enabled burst



## 8.5.2 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range.

### 8.5.2.1 LPDDR4 IDD Specification Parameters and Operating Conditions – Single Die

(V<sub>DD1</sub> = 1.70V~1.95V; V<sub>DD2</sub>, V<sub>DDQ</sub> = 1.06V~1.17V) Notes: 1, 2 apply for all values

| Parameter/Condition                                                                                                                                                                                                     | Symbol  | Power Supply | Data Rate |       |       | Unit | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--------------|-----------|-------|-------|------|-------|
|                                                                                                                                                                                                                         |         |              | 3200      | 3733  | 4267  |      |       |
|                                                                                                                                                                                                                         |         |              | 105°C     | 105°C | 105°C |      |       |
| <b>Operating one bank active-precharge current:</b><br>tCK = tCKmin; tRC = tRCmin;<br>CKE is HIGH;<br>CS is LOW between valid commands;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled   | IDD01   | VDD1         | 9         | 9     | 9     | mA   |       |
|                                                                                                                                                                                                                         | IDD02   | VDD2         | 53        | 53    | 53    | mA   |       |
|                                                                                                                                                                                                                         | IDD0Q   | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 3     |
| <b>Idle power-down standby current:</b><br>tCK = tCKmin;<br>CKE is LOW; CS is LOW;<br>All banks are idle;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                                 | IDD2P1  | VDD1         | 0.6       | 0.6   | 0.6   | mA   |       |
|                                                                                                                                                                                                                         | IDD2P2  | VDD2         | 6.5       | 6.5   | 6.5   | mA   |       |
|                                                                                                                                                                                                                         | IDD2PQ  | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 3     |
| <b>Idle power-down standby current with clock stop:</b><br>CK_t = LOW, CK_c = HIGH;<br>CKE is LOW; CS is LOW;<br>All banks are idle;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled         | IDD2PS1 | VDD1         | 0.6       | 0.6   | 0.6   | mA   |       |
|                                                                                                                                                                                                                         | IDD2PS2 | VDD2         | 6.5       | 6.5   | 6.5   | mA   |       |
|                                                                                                                                                                                                                         | IDD2PSQ | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 3     |
| <b>Idle non power-down standby current:</b><br>tCK = tCKmin;<br>CKE is HIGH; CS is LOW;<br>All banks are idle;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                            | IDD2N1  | VDD1         | 0.6       | 0.6   | 0.6   | mA   |       |
|                                                                                                                                                                                                                         | IDD2N2  | VDD2         | 31        | 31    | 31    | mA   |       |
|                                                                                                                                                                                                                         | IDD2NQ  | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 3     |
| <b>Idle non power-down standby current with clock stopped:</b><br>CK_t = LOW, CK_c = HIGH;<br>CKE is HIGH; CS is LOW;<br>All banks are idle;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | IDD2NS1 | VDD1         | 0.6       | 0.6   | 0.6   | mA   |       |
|                                                                                                                                                                                                                         | IDD2NS2 | VDD2         | 21        | 21    | 21    | mA   |       |
|                                                                                                                                                                                                                         | IDD2NSQ | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 3     |
| <b>Active power-down standby current:</b><br>tCK = tCKmin;<br>CKE is LOW; CS is LOW;<br>One bank is active;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                               | IDD3P1  | VDD1         | 1.65      | 1.65  | 1.65  | mA   |       |
|                                                                                                                                                                                                                         | IDD3P2  | VDD2         | 11        | 11    | 11    | mA   |       |
|                                                                                                                                                                                                                         | IDD3PQ  | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 3     |

LPDDR4 I<sub>DD</sub> Specification Parameters and Operating Conditions – Single Die, (Continued)(V<sub>DD1</sub> = 1.70V~1.95V; V<sub>DD2</sub>, V<sub>DDQ</sub> = 1.06V~1.17V) Notes: 1, 2 apply for all values

| Parameter/Condition                                                                                                                                                                                                                             | Symbol              | Power Supply     | Data Rate |       |       | Unit | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------------------|-----------|-------|-------|------|-------|
|                                                                                                                                                                                                                                                 |                     |                  | 3200      | 3733  | 4267  |      |       |
|                                                                                                                                                                                                                                                 |                     |                  | 105°C     | 105°C | 105°C |      |       |
| <b>Active power-down standby current with clock stop:</b><br>CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH;<br>CKE is LOW; CS is LOW;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled         | I <sub>DD3PS1</sub> | V <sub>DD1</sub> | 1.65      | 1.65  | 1.65  | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD3PS2</sub> | V <sub>DD2</sub> | 11        | 11    | 11    | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD3PSQ</sub> | V <sub>DDQ</sub> | 0.1       | 0.1   | 0.1   | mA   | 4     |
| <b>Active non power-down standby current:</b><br>tCK = tCKmin;<br>CKE is HIGH; CS is LOW;<br>One bank is active;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                                                  | I <sub>DD3N1</sub>  | V <sub>DD1</sub> | 2         | 2     | 2     | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD3N2</sub>  | V <sub>DD2</sub> | 34.5      | 34.5  | 34.5  | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD3NQ</sub>  | V <sub>DDQ</sub> | 0.1       | 0.1   | 0.1   | mA   | 4     |
| <b>Active non power-down standby current with clock stopped:</b><br>CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH;<br>CKE is HIGH; CS is LOW;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | I <sub>DD3NS1</sub> | V <sub>DD1</sub> | 2         | 2     | 2     | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD3NS2</sub> | V <sub>DD2</sub> | 25        | 25    | 25    | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD3NSQ</sub> | V <sub>DDQ</sub> | 0.1       | 0.1   | 0.1   | mA   | 4     |
| <b>Operating burst READ current:</b><br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>One bank is active;<br>BL = 16 or 32; RL = RL (MIN);<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled       | I <sub>DD4R1</sub>  | V <sub>DD1</sub> | 2.5       | 2.5   | 2.5   | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD4R2</sub>  | V <sub>DD2</sub> | 287       | 327   | 367   | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD4RQ</sub>  | V <sub>DDQ</sub> | 105       | 105   | 105   | mA   | 6     |
| <b>Operating burst WRITE current:</b><br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>One bank is active;<br>BL = 16 or 32; WL = WLmin;<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled         | I <sub>DD4W1</sub>  | V <sub>DD1</sub> | 2         | 2     | 2     | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD4W2</sub>  | V <sub>DD2</sub> | 265       | 295   | 325   | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD4WQ</sub>  | V <sub>DDQ</sub> | 0.3       | 0.3   | 0.3   | mA   | 4     |
| <b>All-bank REFRESH Burst current:</b><br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tRFCabmin;<br>Burst refresh;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                              | I <sub>DD51</sub>   | V <sub>DD1</sub> | 31        | 31    | 31    | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD52</sub>   | V <sub>DD2</sub> | 95        | 95    | 95    | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD5Q</sub>   | V <sub>DDQ</sub> | 0.15      | 0.15  | 0.15  | mA   | 4     |



LPDDR4 IDD Specification Parameters and Operating Conditions – Single Die, (Continued)

(VDD1 = 1.70V~1.95V; VDD2, VDDQ = 1.06V~1.17V) Notes: 1, 2 apply for all values

| Parameter/Condition                                                                                                                                                                              | Symbol  |       | Power Supply | Data Rate |       |       | Unit | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-------|--------------|-----------|-------|-------|------|-------|
|                                                                                                                                                                                                  |         |       |              | 3200      | 3733  | 4267  |      |       |
|                                                                                                                                                                                                  |         |       |              | 105°C     | 105°C | 105°C |      |       |
| <b>All-bank REFRESH Average current:</b><br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tREFI;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled   | IDD5AB1 |       | VDD1         | 5         | 5     | 5     | mA   |       |
|                                                                                                                                                                                                  | IDD5AB2 |       | VDD2         | 42        | 42    | 42    | mA   |       |
|                                                                                                                                                                                                  | IDD5ABQ |       | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 4     |
| <b>Per-bank REFRESH Average current:</b><br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tREFI/8;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled | IDD5PB1 |       | VDD1         | 6         | 6     | 6     | mA   |       |
|                                                                                                                                                                                                  | IDD5PB2 |       | VDD2         | 43        | 43    | 43    | mA   |       |
|                                                                                                                                                                                                  | IDD5PBQ |       | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 4     |
| <b>Full Array Self Refresh Current:</b><br>CK_t = LOW, CK_c = HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self Refresh Rate;<br>ODT disabled  | IDD61   | 105°C | VDD1         | 1.7       | 1.7   | 1.7   | mA   | 5     |
|                                                                                                                                                                                                  | IDD62   | 105°C | VDD2         | 10        | 10    | 10    | mA   | 5     |
|                                                                                                                                                                                                  | IDD6Q   | 105°C | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 4, 5  |

**Notes:**

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000<sub>b</sub>.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. The 1x Self Refresh Rate is the rate at which the LPDDR4 SDRAM is refreshed internally during Self Refresh, before going into the elevated Temperature range.
6. IDD4Rq value is reference only. Typical value.
7. For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
8. Dual Channel devices are specified in dual channel operation (both channels operating together).



### 8.5.2.2 LPDDR4X IDD Specification Parameters and Operating Conditions – Single Die

(VDD1 = 1.70V~1.95V; VDD2 = 1.06V~1.17V; VDDQ = 0.57V~0.65V) Notes: 1, 2 apply for all values

| Parameter/Condition                                                                                                                                                                                                     | Symbol  | Power Supply | Data Rate |       |       | Unit | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--------------|-----------|-------|-------|------|-------|
|                                                                                                                                                                                                                         |         |              | 3200      | 3733  | 4267  |      |       |
|                                                                                                                                                                                                                         |         |              | 105°C     | 105°C | 105°C |      |       |
| <b>Operating one bank active-precharge current:</b><br>tCK = tCKmin; tRC = tRCmin;<br>CKE is HIGH;<br>CS is LOW between valid commands;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled   | IDD01   | VDD1         | 9         | 9     | 9     | mA   |       |
|                                                                                                                                                                                                                         | IDD02   | VDD2         | 53        | 53    | 53    | mA   |       |
|                                                                                                                                                                                                                         | IDD0Q   | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 3     |
| <b>Idle power-down standby current:</b><br>tCK = tCKmin;<br>CKE is LOW; CS is LOW;<br>All banks are idle;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                                 | IDD2P1  | VDD1         | 0.6       | 0.6   | 0.6   | mA   |       |
|                                                                                                                                                                                                                         | IDD2P2  | VDD2         | 6.5       | 6.5   | 6.5   | mA   |       |
|                                                                                                                                                                                                                         | IDD2PQ  | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 3     |
| <b>Idle power-down standby current with clock stop:</b><br>CK_t = LOW, CK_c = HIGH;<br>CKE is LOW; CS is LOW;<br>All banks are idle;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled         | IDD2PS1 | VDD1         | 0.6       | 0.6   | 0.6   | mA   |       |
|                                                                                                                                                                                                                         | IDD2PS2 | VDD2         | 6.5       | 6.5   | 6.5   | mA   |       |
|                                                                                                                                                                                                                         | IDD2PSQ | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 3     |
| <b>Idle non power-down standby current:</b><br>tCK = tCKmin;<br>CKE is HIGH; CS is LOW;<br>All banks are idle;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                            | IDD2N1  | VDD1         | 0.6       | 0.6   | 0.6   | mA   |       |
|                                                                                                                                                                                                                         | IDD2N2  | VDD2         | 31        | 31    | 31    | mA   |       |
|                                                                                                                                                                                                                         | IDD2NQ  | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 3     |
| <b>Idle non power-down standby current with clock stopped:</b><br>CK_t = LOW, CK_c = HIGH;<br>CKE is HIGH; CS is LOW;<br>All banks are idle;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | IDD2NS1 | VDD1         | 0.6       | 0.6   | 0.6   | mA   |       |
|                                                                                                                                                                                                                         | IDD2NS2 | VDD2         | 21        | 21    | 21    | mA   |       |
|                                                                                                                                                                                                                         | IDD2NSQ | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 3     |
| <b>Active power-down standby current:</b><br>tCK = tCKmin;<br>CKE is LOW; CS is LOW;<br>One bank is active;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                               | IDD3P1  | VDD1         | 1.65      | 1.65  | 1.65  | mA   |       |
|                                                                                                                                                                                                                         | IDD3P2  | VDD2         | 11        | 11    | 11    | mA   |       |
|                                                                                                                                                                                                                         | IDD3PQ  | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 3     |



LPDDR4X I<sub>DD</sub> Specification Parameters and Operating Conditions – Single Die, (Continued)(V<sub>DD1</sub> = 1.70V~1.95V; V<sub>DD2</sub> = 1.06V~1.17V; V<sub>DDQ</sub> = 0.57V~0.65V) Notes: 1, 2 apply for all values

| Parameter/Condition                                                                                                                                                                                                                             | Symbol              | Power Supply     | Data Rate |       |       | Unit | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------------------|-----------|-------|-------|------|-------|
|                                                                                                                                                                                                                                                 |                     |                  | 3200      | 3733  | 4267  |      |       |
|                                                                                                                                                                                                                                                 |                     |                  | 105°C     | 105°C | 105°C |      |       |
| <b>Active power-down standby current with clock stop:</b><br>CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH;<br>CKE is LOW; CS is LOW;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled         | I <sub>DD3PS1</sub> | V <sub>DD1</sub> | 1.65      | 1.65  | 1.65  | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD3PS2</sub> | V <sub>DD2</sub> | 11        | 11    | 11    | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD3PSQ</sub> | V <sub>DDQ</sub> | 0.1       | 0.1   | 0.1   | mA   | 4     |
| <b>Active non power-down standby current:</b><br>tCK = tCKmin;<br>CKE is HIGH; CS is LOW;<br>One bank is active;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                                                  | I <sub>DD3N1</sub>  | V <sub>DD1</sub> | 2         | 2     | 2     | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD3N2</sub>  | V <sub>DD2</sub> | 34.5      | 34.5  | 34.5  | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD3NQ</sub>  | V <sub>DDQ</sub> | 0.1       | 0.1   | 0.1   | mA   | 4     |
| <b>Active non power-down standby current with clock stopped:</b><br>CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH;<br>CKE is HIGH; CS is LOW;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | I <sub>DD3NS1</sub> | V <sub>DD1</sub> | 2         | 2     | 2     | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD3NS2</sub> | V <sub>DD2</sub> | 25        | 25    | 25    | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD3NSQ</sub> | V <sub>DDQ</sub> | 0.1       | 0.1   | 0.1   | mA   | 4     |
| <b>Operating burst READ current:</b><br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>One bank is active;<br>BL = 16 or 32; RL = RL (MIN);<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled       | I <sub>DD4R1</sub>  | V <sub>DD1</sub> | 2.5       | 2.5   | 2.5   | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD4R2</sub>  | V <sub>DD2</sub> | 287       | 327   | 367   | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD4RQ</sub>  | V <sub>DDQ</sub> | 85        | 85    | 85    | mA   | 6     |
| <b>Operating burst WRITE current:</b><br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>One bank is active;<br>BL = 16 or 32; WL = WLmin;<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled         | I <sub>DD4W1</sub>  | V <sub>DD1</sub> | 2         | 2     | 2     | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD4W2</sub>  | V <sub>DD2</sub> | 265       | 295   | 325   | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD4WQ</sub>  | V <sub>DDQ</sub> | 0.3       | 0.3   | 0.3   | mA   | 4     |
| <b>All-bank REFRESH Burst current:</b><br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tRFCabmin;<br>Burst refresh;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled                              | I <sub>DD51</sub>   | V <sub>DD1</sub> | 31        | 31    | 31    | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD52</sub>   | V <sub>DD2</sub> | 95        | 95    | 95    | mA   |       |
|                                                                                                                                                                                                                                                 | I <sub>DD5Q</sub>   | V <sub>DDQ</sub> | 0.15      | 0.15  | 0.15  | mA   | 4     |



LPDDR4X IDD Specification Parameters and Operating Conditions – Single Die, (Continued)

(VDD1 = 1.70V~1.95V; VDD2 = 1.06V~1.17V; VDDQ = 0.57V~0.65V) Notes: 1, 2 apply for all values

| Parameter/Condition                                                                                                                                                                              | Symbol  |       | Power Supply | Data Rate |       |       | Unit | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-------|--------------|-----------|-------|-------|------|-------|
|                                                                                                                                                                                                  |         |       |              | 3200      | 3733  | 4267  |      |       |
|                                                                                                                                                                                                  |         |       |              | 105°C     | 105°C | 105°C |      |       |
| <b>All-bank REFRESH Average current:</b><br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tREFI;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled   | IDD5AB1 |       | VDD1         | 5         | 5     | 5     | mA   |       |
|                                                                                                                                                                                                  | IDD5AB2 |       | VDD2         | 42        | 42    | 42    | mA   |       |
|                                                                                                                                                                                                  | IDD5ABQ |       | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 4     |
| <b>Per-bank REFRESH Average current:</b><br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tREFI/8;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled | IDD5PB1 |       | VDD1         | 6         | 6     | 6     | mA   |       |
|                                                                                                                                                                                                  | IDD5PB2 |       | VDD2         | 43        | 43    | 43    | mA   |       |
|                                                                                                                                                                                                  | IDD5PBQ |       | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 4     |
| <b>Full Array Self Refresh Current:</b><br>CK_t = LOW, CK_c = HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self Refresh Rate;<br>ODT disabled  | IDD61   | 105°C | VDD1         | 1.7       | 1.7   | 1.7   | mA   | 5     |
|                                                                                                                                                                                                  | IDD62   | 105°C | VDD2         | 10        | 10    | 10    | mA   | 5     |
|                                                                                                                                                                                                  | IDD6Q   | 105°C | VDDQ         | 0.1       | 0.1   | 0.1   | mA   | 4, 5  |

**Notes:**

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000<sub>b</sub>.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. The 1x Self Refresh Rate is the rate at which the LPDDR4X SDRAM is refreshed internally during Self Refresh, before going into the elevated Temperature range.
6. IDD4Rq value is reference only. Typical value.
7. For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
8. Dual Channel devices are specified in dual channel operation (both channels operating together).



## 8.6 Electrical Characteristics and AC Timing

### 8.6.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR4/LPDDR4X SDRAM.

#### 8.6.1.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left[ \sum_{j=1}^N tCK_j \right] / N$$

where  $N = 200$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

tCK(avg) may change by up to  $\pm 1\%$  within a 100 clock cycle window, provided that all jitter and timing specs are met.

#### 8.6.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

tCK(abs) is not subject to production test.



#### 8.6.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left[ \sum_{j=1}^N tCH_j \right] / (N \times tCK(avg))$$

where  $N = 200$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left[ \sum_{j=1}^N tCL_j \right] / (N \times tCK(avg))$$

where  $N = 200$

#### 8.6.1.4 Definition for tCH(abs) and tCL(abs)

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Both tCH(abs) and tCL(abs) are not subject to production test.

#### 8.6.1.5 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).

tJIT(per) = Min/max of {tCK<sub>i</sub> - tCK(avg) where i = 1 to 200}.

tJIT(per).act is the actual clock jitter for a given system.

tJIT(per).allowed is the specified allowed clock period jitter.

tJIT(per) is not subject to production test.

#### 8.6.1.6 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

tJIT(cc) = Max of |{tCK<sub>(i+1)</sub> - tCK<sub>(i)</sub>}|.

tJIT(cc) defines the cycle to cycle jitter.

tJIT(cc) is not subject to production test.



### 8.6.2 Clock AC Timing

Table 120 - Clock AC Timing

| Parameter                                       | Symbol    | Min/Max | Data Rate                  |       |       |       |       |       | Unit     | Note |
|-------------------------------------------------|-----------|---------|----------------------------|-------|-------|-------|-------|-------|----------|------|
|                                                 |           |         | 1600                       | 2400  | 2667  | 3200  | 3733  | 4267  |          |      |
| Clock Timing                                    |           |         |                            |       |       |       |       |       |          |      |
| Average clock period                            | tCK(avg)  | Min     | 1.25                       | 0.833 | 0.75  | 0.625 | 0.535 | 0.468 | nS       |      |
|                                                 |           | Max     | 100                        | 100   | 100   | 100   | 100   | 100   |          |      |
| Average High pulse width                        | tCH(avg)  | Min     | 0.46                       | 0.46  | 0.46  | 0.46  | 0.46  | 0.46  | tCK(avg) |      |
|                                                 |           | Max     | 0.54                       | 0.54  | 0.54  | 0.54  | 0.54  | 0.54  |          |      |
| Average Low pulse width                         | tCL(avg)  | Min     | 0.46                       | 0.46  | 0.46  | 0.46  | 0.46  | 0.46  | tCK(avg) |      |
|                                                 |           | Max     | 0.54                       | 0.54  | 0.54  | 0.54  | 0.54  | 0.54  |          |      |
| Absolute clock period                           | tCK(abs)  | Min     | tCK(avg)min + tJIT(per)min |       |       |       |       |       | nS       |      |
|                                                 |           | Max     | -                          |       |       |       |       |       |          |      |
| Absolute High clock pulse width                 | tCH(abs)  | Min     | 0.43                       | 0.43  | 0.43  | 0.43  | 0.43  | 0.43  | tCK(avg) |      |
|                                                 |           | Max     | 0.57                       | 0.57  | 0.57  | 0.57  | 0.57  | 0.57  |          |      |
| Absolute Low clock pulse width                  | tCL(abs)  | Min     | 0.43                       | 0.43  | 0.43  | 0.43  | 0.43  | 0.43  | tCK(avg) |      |
|                                                 |           | Max     | 0.57                       | 0.57  | 0.57  | 0.57  | 0.57  | 0.57  |          |      |
| Clock period jitter                             | tJIT(per) | Min     | -70                        | -50   | -46.7 | -40   | -34   | -30   | pS       |      |
|                                                 |           | Max     | 70                         | 50    | 46.7  | 40    | 34    | 30    |          |      |
| Maximum Clock Jitter between consecutive cycles | tJIT(cc)  | Min     | -                          | -     | -     | -     | -     | -     | pS       |      |
|                                                 |           | Max     | 140                        | 100   | 93.3  | 80    | 68    | 60    |          |      |

**Note:**

1. All parts list in ordering information table (section 3) will not guarantee to meet functional and AC specification if the tCK out of range mentioned in above table.

### 8.6.3 Temperature Derating for AC timing

Temperature derating is shown in Table 121.

Table 121 - Temperature Derating AC Timing

| Parameter                                       | Symbol | Min/Max | Data Rate    |      |      |      |      |      |      |      | Unit |
|-------------------------------------------------|--------|---------|--------------|------|------|------|------|------|------|------|------|
|                                                 |        |         | 533          | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4267 |      |
| Temperature Derating*                           |        |         |              |      |      |      |      |      |      |      |      |
| DQS output access time from CK_t/CK_c (derated) | tDQSK  | Max     | 3600         |      |      |      |      |      |      |      | pS   |
| RAS-to-CAS delay (derated)                      | tRCD   | Min     | tRCD + 1.875 |      |      |      |      |      |      |      | nS   |
| ACTIVATE-to- ACTIVATE command period (derated)  | tRC    | Min     | tRC + 3.75   |      |      |      |      |      |      |      | nS   |
|                                                 |        |         |              |      |      |      |      |      |      |      | nS   |
| Row active time (derated)                       | tRAS   | Min     | tRAS + 1.875 |      |      |      |      |      |      |      | nS   |
| Row precharge time (derated)                    | tRP    | Min     | tRP + 1.875  |      |      |      |      |      |      |      | nS   |
| Active bank A to active bank B (derated)        | tRRD   | Min     | tRRD + 1.875 |      |      |      |      |      |      |      | nS   |

**Note:**

At higher temperatures (>85°C), AC timing derating may be required. If derating is required the LPDDR4/LPDDR4X SDRAM will set MR4 OP[2:0]=110<sub>b</sub>.



#### 8.6.4 CA Rx voltage and timing

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in Figure 166. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in Figure 166 is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

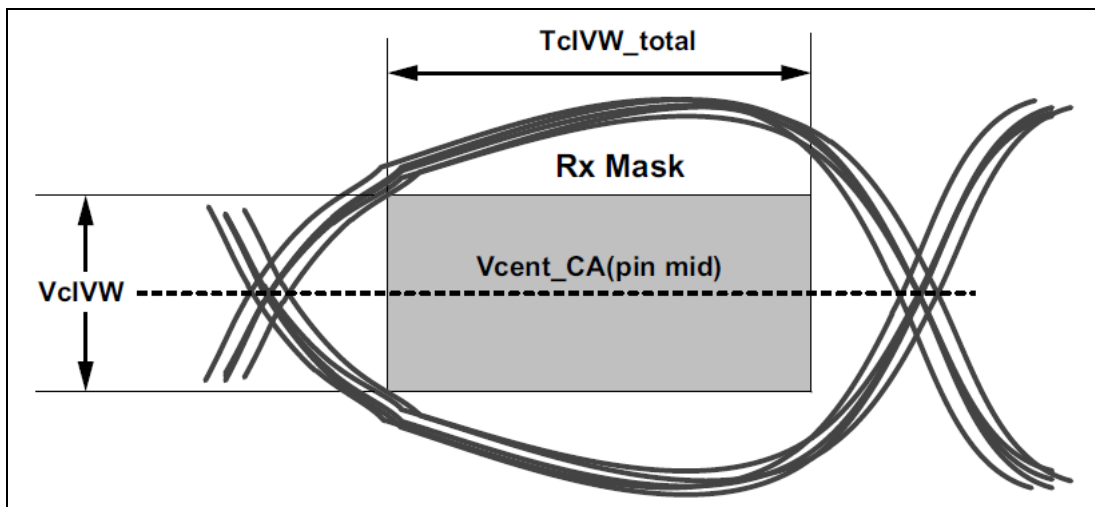


Figure 166 - CA Receiver (Rx) Mask

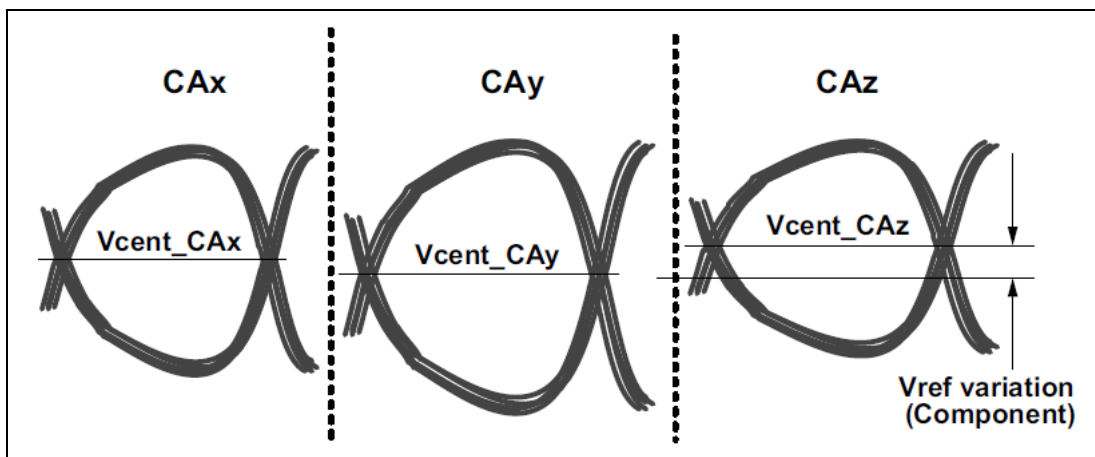
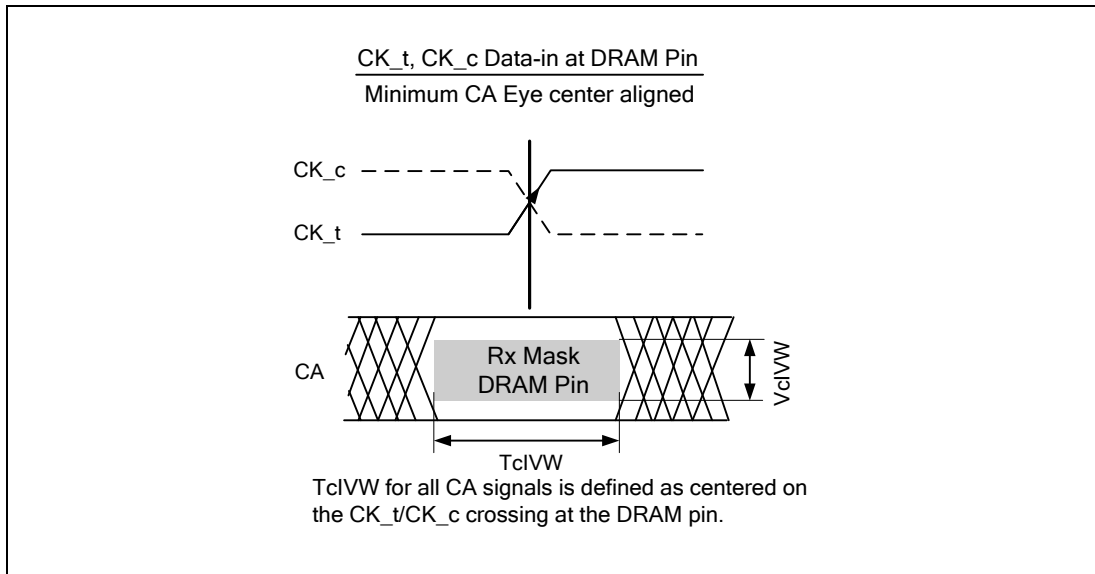


Figure 167 - Across pin VREFCA voltage variation

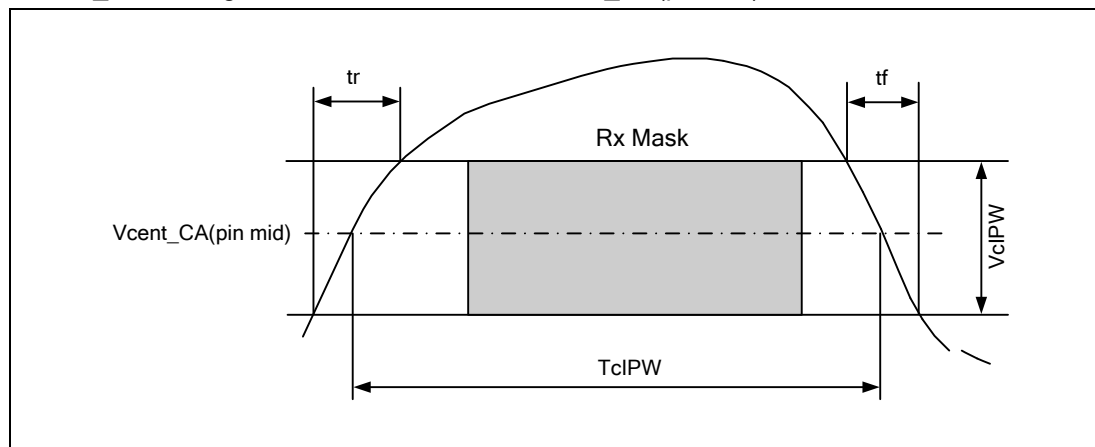
$V_{cent\_CA}(\text{pin mid})$  is defined as the midpoint between the largest  $V_{cent\_CA}$  voltage level and the smallest  $V_{cent\_CA}$  voltage level across all CA and CS pins for a given DRAM component. Each CA  $V_{cent}$  level is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 167. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask.

The component level VREF will be set by the system to account for Ron and ODT settings.



**Figure 168 - DCA Timings at the DRAM Pins**

All of the timing terms in Figure 169 are measured from the CK\_t/CK\_c to the center (midpoint) of the TcIVW window taken at the VcIVW\_total voltage levels centered around Vcent\_CA(pin mid).



**Note:**

1.  $SRIN\_cIVW = VcIVW\_Total / (tr \text{ or } tf)$ , signal must be monotonic within tr and tf range.

**Figure 169 - CA TcIPW and SRIN\_cIVW definition (for each input pulse)**



The CA VIH<sub>L</sub>\_AC definition is provided in Figure 170. The DRAM CMD/ADR, CS is shown in Table 122.

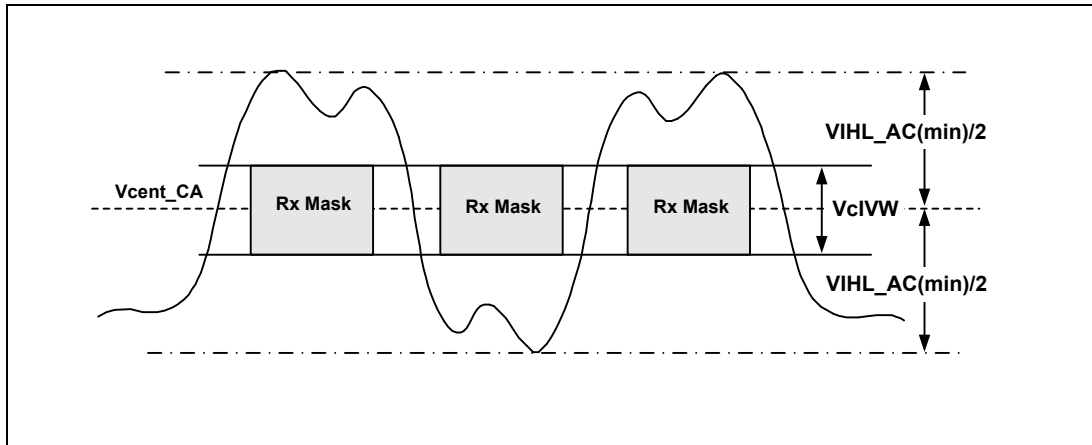


Figure 170 - CA VIH<sub>L</sub>\_AC definition (for each input pulse)

Table 122 - DRAM CMD/ADR, CS

| Symbol    | Parameter                         | Min/Max | Data Rate |           |      |      |      |      | Unit | Notes         |
|-----------|-----------------------------------|---------|-----------|-----------|------|------|------|------|------|---------------|
|           |                                   |         | 1333      | 1600/1867 | 2667 | 3200 | 3733 | 4267 |      |               |
| VcIVW     | Rx Mask voltage - p-p             | Min     | -         | -         | -    | -    | -    | -    | mV   | 1, 2, 3, 4    |
|           |                                   | Max     | 175       | 175       | 160  | 155  | 150  | 145  |      |               |
| TcIVW     | Rx timing window                  | Min     | -         | -         | -    | -    | -    | -    | UI   | 1, 2, 3, 4, 9 |
|           |                                   | Max     | 0.3       | 0.3       | 0.3  | 0.3  | 0.3  | 0.3  |      |               |
| VIHL_AC   | CA AC input pulse amplitude pk-pk | Min     | 210       | 210       | 200  | 190  | 180  | 180  | mV   | 1, 5, 8       |
|           |                                   | Max     | -         | -         | -    | -    | -    | -    |      |               |
| TcIPW     | CA input pulse width              | Min     | 0.55      | 0.55      | 0.6  | 0.6  | 0.6  | 0.6  | UI   | 2, 6, 9       |
|           |                                   | Max     |           |           |      |      |      |      |      |               |
| SRIN_cIVW | Input Slew Rate over VcIVW        | Min     | 1         | 1         | 1    | 1    | 1    | 1    | V/nS | 1, 7          |
|           |                                   | Max     | 7         | 7         | 7    | 7    | 7    | 7    |      |               |

**Notes:**

1. The Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(pS) = 450pS at or below 1333 operating frequencies.
2. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
3. Rx mask voltage VcIVW total(max) must be centered around Vcent\_CA(pin mid).
4. Vcent\_CA must be within the adjustment range of the CA internal VREF.
5. CA only input pulse signal amplitude into the receiver must meet or exceed VIH<sub>L</sub> AC at any point over the total UI. No timing requirement above level. VIH<sub>L</sub> AC is the peak to peak voltage centered around Vcent\_CA(pin mid) such that VIH<sub>L</sub>\_AC/2 min must be met both above and below Vcent\_CA.
6. CA only minimum input pulse width defined at the Vcent\_CA(pin mid).
7. Input slew rate over VcIVW Mask centered at Vcent\_CA(pin mid).
8. VIH<sub>L</sub>\_AC does not have to be met when no transitions are occurring.
9. UI=tCK(avg)min.





### 8.6.5 DRAM Data Timing

The DRAM data timing is shown in Figure 171 and Figure 172, and Table 123.

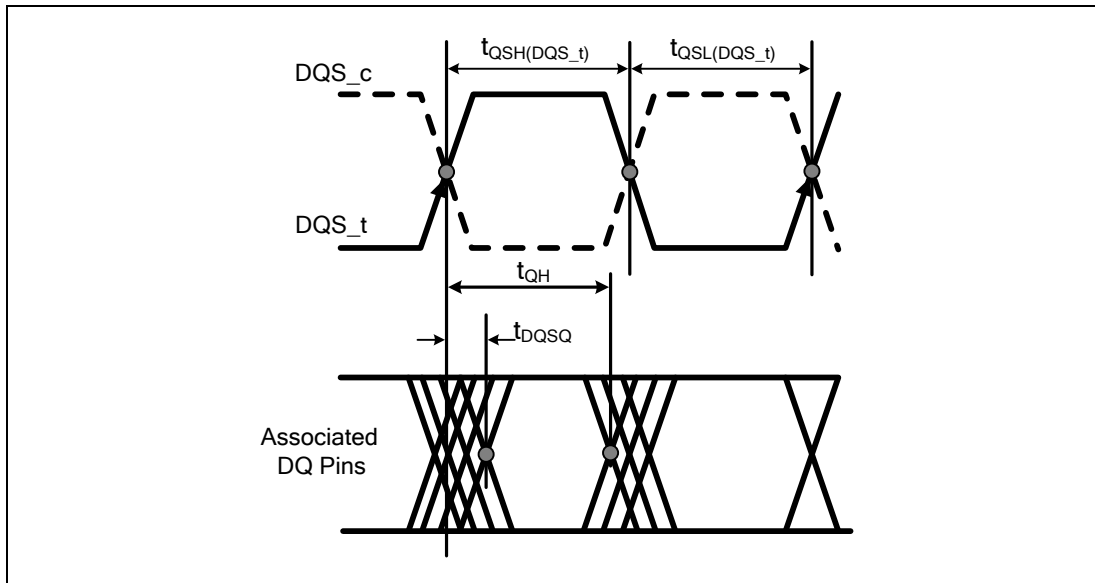


Figure 171 - Read data timing definitions  $t_{QH}$  and  $t_{DQSQ}$  across all DQ signals per DQS group

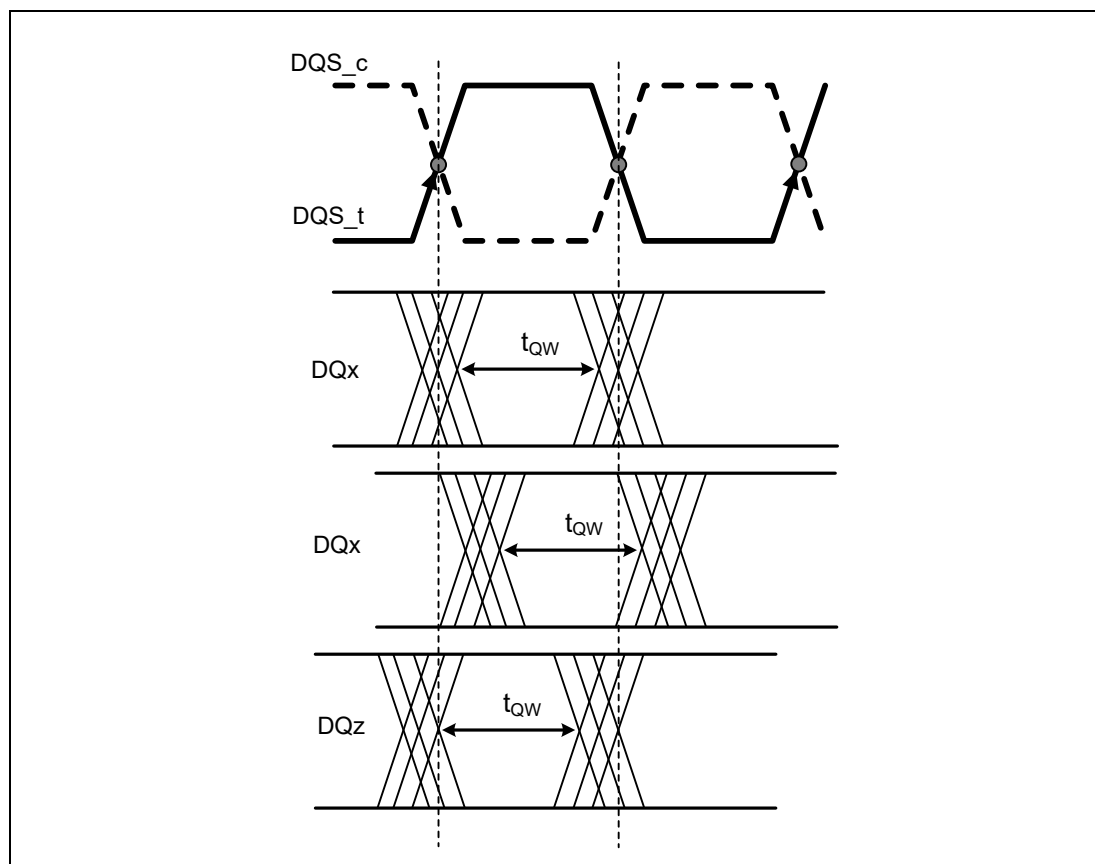


Figure 172 - Read data timing  $t_{QW}$  valid window defined per DQ signal



Table 123 - Read output timing

| Parameter                                                           | Symbol        | Min/Max | Data Rate               |           |      |      |      | Unit     | Notes |  |
|---------------------------------------------------------------------|---------------|---------|-------------------------|-----------|------|------|------|----------|-------|--|
|                                                                     |               |         | 1600/1867               | 2133/2400 | 3200 | 3733 | 4267 |          |       |  |
| Data Timing                                                         |               |         |                         |           |      |      |      |          |       |  |
| DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Disabled) | tDQSQ         | Min     | -                       |           |      |      |      | UI       | 1     |  |
|                                                                     |               | Max     | 0.18                    |           |      |      |      |          |       |  |
| DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)          | tQH           | Min     | min(tQSH, tQSL)         |           |      |      |      | UI       | 1     |  |
|                                                                     |               | Max     | -                       |           |      |      |      |          |       |  |
| DQ output window time total, per pin (DBI-Disabled)                 | tQW_total     | Min     | 0.75                    | 0.73      | 0.7  | 0.7  | 0.7  | UI       | 1, 3  |  |
|                                                                     |               | Max     | -                       | -         | -    | -    | -    |          |       |  |
| DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Enabled)  | tDQSQ_DBI     | Min     | -                       |           |      |      |      | UI       | 1     |  |
|                                                                     |               | Max     | 0.18                    |           |      |      |      |          |       |  |
| DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)           | tQH_DBI       | Min     | min(tQSH_DBI, tQSL_DBI) |           |      |      |      | UI       | 1     |  |
|                                                                     |               | Max     | -                       |           |      |      |      |          |       |  |
| DQ output window time total, per pin (DBI-Enabled)                  | tQW_total_DBI | Min     | 0.75                    | 0.73      | 0.7  | 0.7  | 0.7  | UI       | 1, 3  |  |
|                                                                     |               | Max     | -                       | -         | -    | -    | -    |          |       |  |
| Data Strobe Timing                                                  |               |         |                         |           |      |      |      |          |       |  |
| DQS_t, DQS_c differential output low time (DBI-Disabled)            | tQSL          | Min     | tCL(abs)-0.05           |           |      |      |      | tCK(avg) | 3, 4  |  |
|                                                                     |               | Max     | -                       |           |      |      |      |          |       |  |
| DQS_t, DQS_c differential output high time (DBI-Disabled)           | tQSH          | Min     | tCH(abs)-0.05           |           |      |      |      | tCK(avg) | 3, 5  |  |
|                                                                     |               | Max     | -                       |           |      |      |      |          |       |  |
| DQS_t, DQS_c differential output low time (DBI-Enabled)             | tQSL_DBI      | Min     | tCL(abs)-0.045          |           |      |      |      | tCK(avg) | 4, 6  |  |
|                                                                     |               | Max     | -                       |           |      |      |      |          |       |  |
| DQS_t, DQS_c differential output high time (DBI-Enabled)            | tQSH_DBI      | Min     | tCH(abs)-0.045          |           |      |      |      | tCK(avg) | 5, 6  |  |
|                                                                     |               | Max     | -                       |           |      |      |      |          |       |  |

**Notes:**

1.  $UI = tCK(avg)min/2$ .
2. The deterministic component of the total timing.
3. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tCK(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs)-0.04.
4. tQSL describes the instantaneous differential output low pulse width on DQS\_t - DQS\_c, as it measured the next rising edge from an arbitrary falling edge.
5. tQSH describes the instantaneous differential output high pulse width on DQS\_t - DQS\_c, as it measured the next rising edge from an arbitrary falling edge.
6. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tCK(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs)-0.04.
7. The Tx voltage and absolute timing requirements at 1600Mbps apply for all DQ operating frequencies for speed bins which is less than 1600Mbps.



### 8.6.6 DQ Rx voltage and timing

The DQ input receiver mask for voltage and timing is shown Figure 173 is applied per pin. The "total" mask ( $V_{dIVW\_total}$ ,  $T_{dIVW\_total}$ ) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property and it is not the valid data-eye.

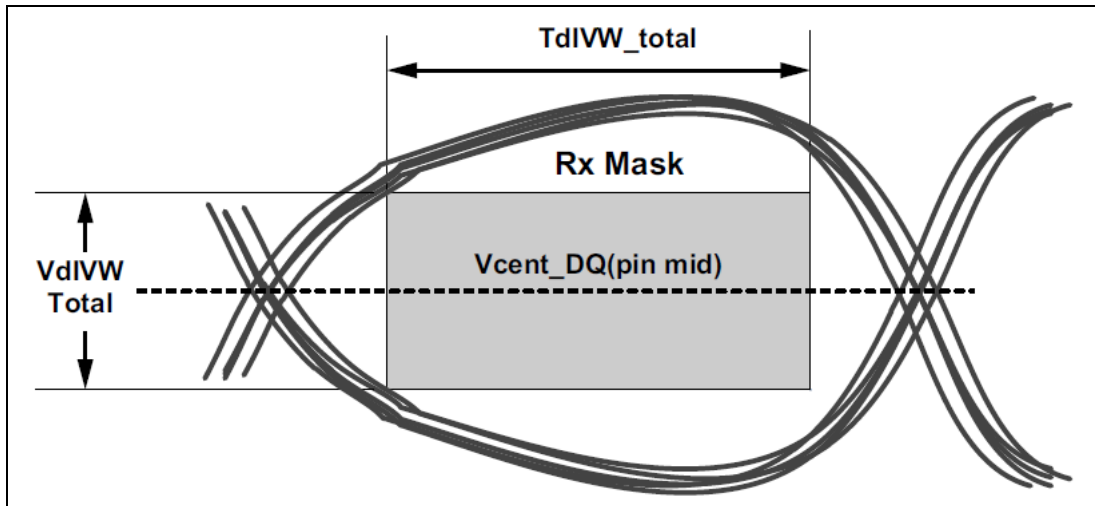


Figure 173 - DQ Receiver (Rx) mask

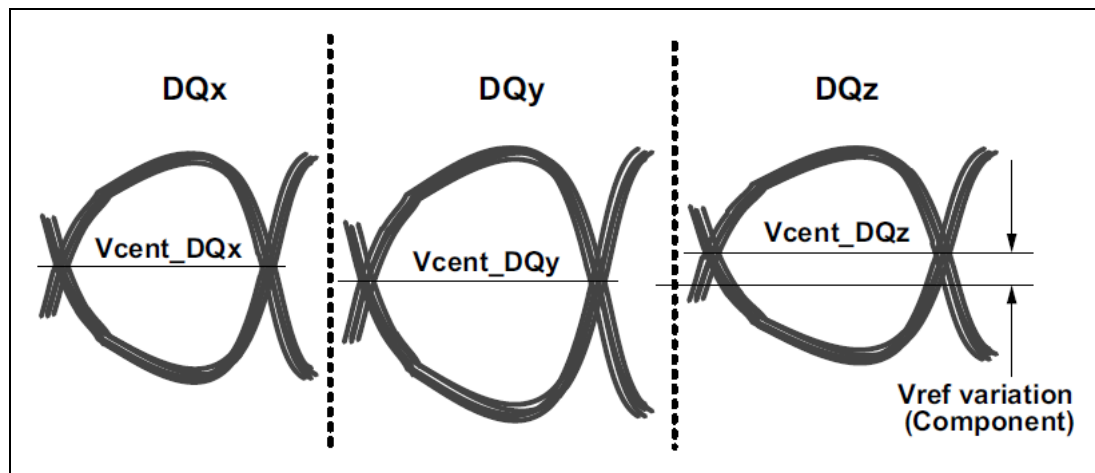


Figure 174 - Across pin VREF DQ voltage variation

$V_{cent\_DQ(pin\_mid)}$  is defined as the midpoint between the largest  $V_{cent\_DQ}$  voltage level and the smallest  $V_{cent\_DQ}$  voltage level across all DQ pins for a given DRAM component. Each DQ  $V_{cent}$  is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 174. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level VREF will be set by the system to account for Ron and ODT settings.



Figure 175 shows timing at the DRAM pins, referenced from the internal latch.

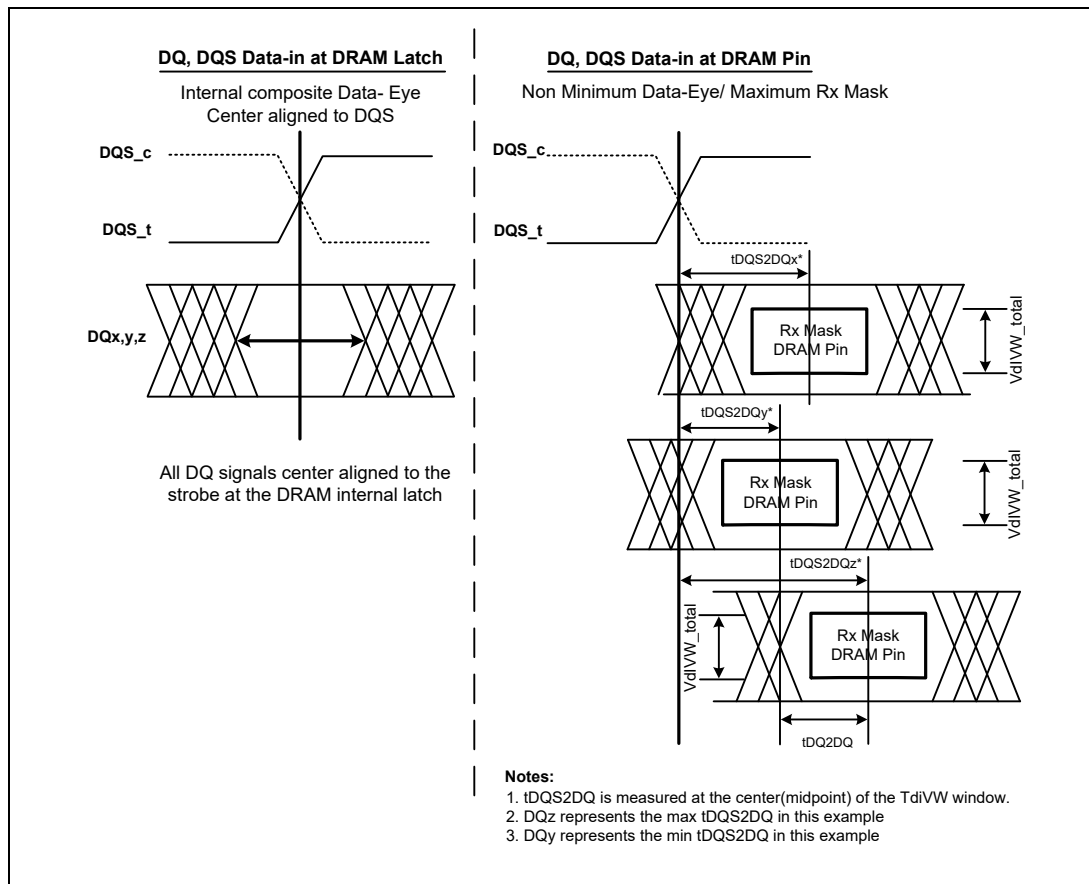


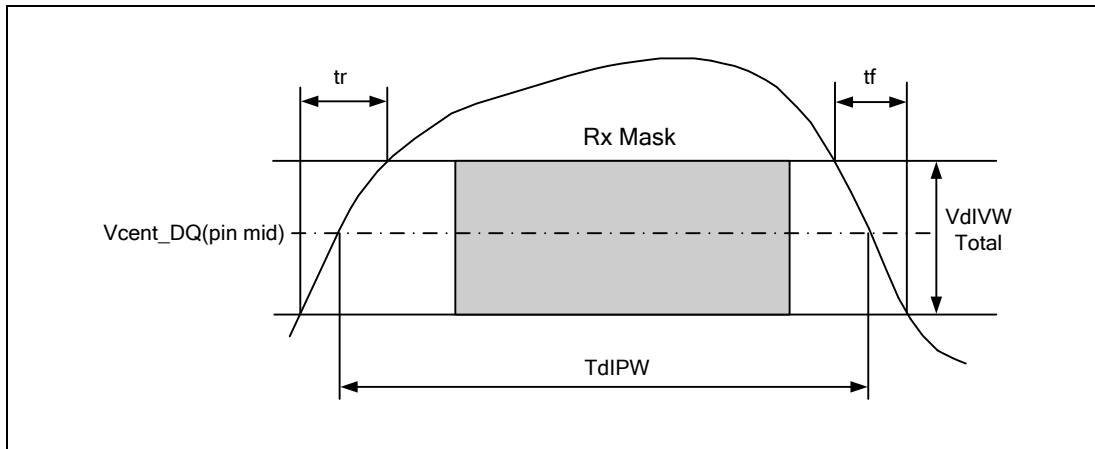
Figure 175 - DQ to DQS  $t_{DQS2DQ}$  and  $t_{DQ2DQ}$  Timings at the DRAM pins referenced from the internal latch



Figure 176 provides the DQ TdIPW and SRIN\_dIVW definition.

Figure 177 provides the DQ VIH<sub>L</sub>\_AC definition.

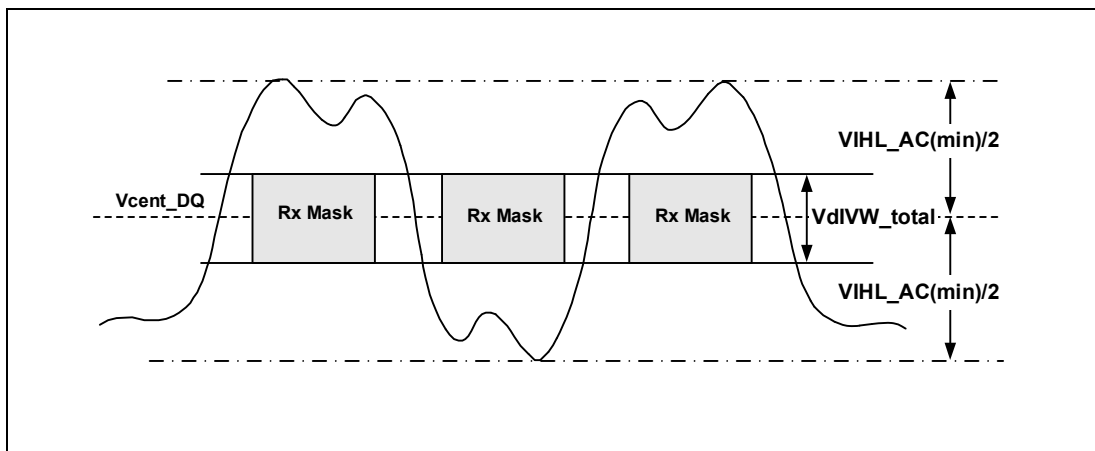
Table 124 shows DRAM DQs In Receive Mode.



**Note:**

1.  $SRIN\_dIVW = VdIVW\_Total / (tr \text{ or } tf)$ , signal must be monotonic within tr and tf range.

**Figure 176 - DQ TdIPW and SRIN\_dIVW definition (for each input pulse)**



**Figure 177 - DQ VIH<sub>L</sub>\_AC definition (for each input pulse)**



Table 124 - DRAM DQs In Receive Mode

| Parameter                                           | Symbol       | Min/<br>Max | Data Rate |           |      |      |      | Unit    | Notes    |
|-----------------------------------------------------|--------------|-------------|-----------|-----------|------|------|------|---------|----------|
|                                                     |              |             | 1600/1867 | 2133/2400 | 3200 | 3733 | 4267 |         |          |
| Rx Mask voltage - peak-to-peak total                | VdIVW_total  | Min         | -         |           |      |      |      | mV      | 1,2,3,4  |
|                                                     |              | Max         | 140       | 140       | 140  | 130  | 120  |         |          |
| Rx timing window total<br>(At VdIVW voltage levels) | TdIVW_total  | Min         | -         |           |      |      |      | UI*     | 1,2,4,13 |
|                                                     |              | Max         | 0.22      | 0.22      | 0.25 | 0.25 | 0.25 |         |          |
| DQ AC input pulse amplitude<br>peak-to-peak         | VIHL_AC      | Min         | 180       | 180       | 180  | 180  | 170  | mV      | 1,5,12   |
|                                                     |              | Max         | -         |           |      |      |      |         |          |
| Input pulse width<br>(At Vcent_DQ)                  | TdIPW DQ     | Min         | 0.45      |           |      |      |      | UI*     | 1,6,13   |
|                                                     |              | Max         |           |           |      |      |      |         |          |
| DQ to DQS offset                                    | tDQS2DQ      | Min         | 200       |           |      |      |      | pS      | 1,7      |
|                                                     |              | Max         | 800       |           |      |      |      |         |          |
| DQ to DQ offset                                     | tDQ2DQ       | Min         | -         |           |      |      |      | pS      | 1,8      |
|                                                     |              | Max         | 30        |           |      |      |      |         |          |
| DQ to DQS offset temperature<br>variation           | tDQS2DQ_temp | Min         | -         |           |      |      |      | pS/°C   | 1,9      |
|                                                     |              | Max         | 0.6       |           |      |      |      |         |          |
| DQ to DQS offset voltage<br>variation               | tDQS2DQ_volt | Min         | -         |           |      |      |      | pS/50mV | 1,10     |
|                                                     |              | Max         | 33        |           |      |      |      |         |          |
| Input Slew Rate over<br>VdIVW_total                 | SRIN_dIVW    | Min         | 1         |           |      |      |      | V/nS    | 1,11     |
|                                                     |              | Max         | 7         |           |      |      |      |         |          |

**Notes:**

1. The Rx voltage and absolute timing requirements apply for all DQ operating frequencies at or below 1600 for all speed bins. For example TdIVW\_total(pS) = 137.5pS at or below 1600 operating frequencies.
2. Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20 MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
3. Rx mask voltage VdIVW total(max) must be centered around Vcent\_DQ(pin\_mid).
4. Vcent\_DQ must be within the adjustment range of the DQ internal VREF.
5. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent\_DQ(pin\_mid) such that VIHL\_AC/2 min must be met both above and below Vcent\_DQ.
6. DQ only minimum input pulse width defined at the Vcent\_DQ(pin\_mid).
7. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
8. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
9. TDQS2DQ max delay variation as a function of temperature.
10. TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies > 20MHz and max voltage of 45mV pk-pk from DC-20MHz at a fixed temperature on the package. For tester measurement VDDQ = VDD2 is assumed.
11. Input slew rate over VdIVW Mask centered at Vcent\_DQ(pin\_mid).
12. VIHL\_AC does not have to be met when no transitions are occurring.
13. UI=tCK(avg)min/2.



## 9. SINGLE-ENDED MODE FOR CLOCK AND STROBE

W66CP6RB / W66DP2RQ LPDDR4/LPDDR4X SDRAM supports the function of single-ended mode for Clock and Strobe independently to reduce power consumption at low frequency operation. The clock frequency applied by this function is equal or less than 800MHz and each ODT state (CK/CA, DQS/DQ) is required to be unterminated.

This function support is indicated in MR0 OP[5].

The entering and exiting single-ended mode for Clock and Strobe is controlled by MR51 OP[3:1] setting.

The single-ended mode for Strobe affects to the following commands.

- Write-1
- Mask Write-1\*\*
- Read-1
- Mode Register Read-1\*
- MPC Write FIFO\*\*
- MPC Read FIFO\*
- MPC Read DQ calibration: regardless of the setting of Read Preamble Training Mode: MR13 OP[1]\*

\*: Read equivalent operations

\*\*: Write equivalent operations

### 9.1 Combination of Mode Register setting and ODT termination

Single-ended mode for Clock and Strobe MR setting: MR51 OP[3:1] can be independently. It means that the all setting i.e. OP[3:1] = 000, 001, 010 .... 110,111 is available. And ODT behavior for each MR51 OP[3:1] setting, to refer the following table.

**Table 125 - ODT status for Single-ended mode for Clock and Strobe**

| Function           | MR# / Operand | Data                          | SDRAM ODT                                   |
|--------------------|---------------|-------------------------------|---------------------------------------------|
| Single ended RDQS  | MR51 OP[1]    | 0 <sub>b</sub> : Differential | Don't Care                                  |
|                    |               | 1 <sub>b</sub> : Single-ended | Don't Care                                  |
| Single ended WDQS  | MR51 OP[2]    | 0 <sub>b</sub> : Differential | DQ/DQS ODT Supports both enable and disable |
|                    |               | 1 <sub>b</sub> : Single-ended | DQ/DQS ODT Supports disable only            |
| Single ended Clock | MR51 OP[3]    | 0 <sub>b</sub> : Differential | CK ODT Supports both enable and disable     |
|                    |               | 1 <sub>b</sub> : Single-ended | CK ODT Supports disable only                |

### 9.2 Restriction of Single-ended mode

The following restriction applies under Single-ended mode

MR51 OP[1] = 1<sub>b</sub>: Single ended RDQS is enabled.

- The output level of DQS\_c is always “LOW or Hi-Z” during read or equivalent operations

MR51 OP[2] = 1<sub>b</sub>: Single ended WDQS is enabled.

- DQS\_c should be Valid (LOW or High) for WRITE or equivalent operations.
- DQS\_t will be referenced to VREFDQ.
- The VREFDQ lower limit: MR14 OP[5:0] range is 000000<sub>b</sub> thru 110010<sub>b</sub>: for MR14 OP[6] = 0<sub>b</sub> or 1<sub>b</sub>.
- MR51 OP[2] has been set 1<sub>b</sub> (Enable) for either physical register. DQS\_c input level is required to “High” during tDQSCKE and tCAENT period at CBT operation.

MR51 OP[3] = 1<sub>b</sub>: Single ended Clock is enabled.

- CK\_c should be Valid (LOW or High).
- CK\_t will be referenced to VREFCA.
- The VREFCA lower limit: MR12 OP[5:0] range is 000000<sub>b</sub> thru 110010<sub>b</sub>: for MR12 OP[6] = 0<sub>b</sub> or 1<sub>b</sub>.
- MR51 OP[3] has been set 1<sub>b</sub> (Enable) for either or both physical register. Additional timing period is needed after MRW command of changing the FSP status. VRCG status change to high current mode also is the same situation as FSP change.



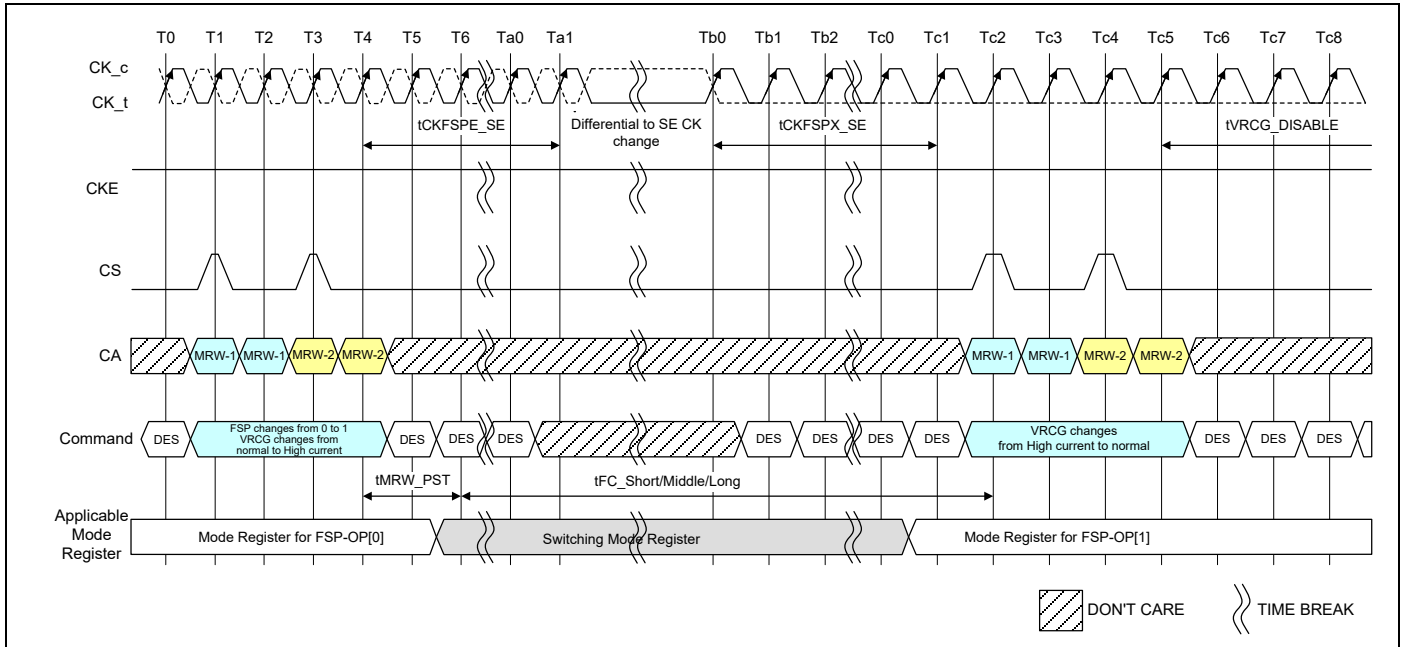
### 9.3 Switching sequence between Differential and Single-ended

Switching only Read DQS functionality from differential to single ended and vice versa, Single Ended Read DQS Enable: MR51 OP[1] can be written by Mode Register Write command regardless FSP OP setting.

Switching the Write DQS and CK functionality from differential to single ended and vice versa is done only via frequency set point switching. Therefore the setting of FSP-OP: MR13 OP[7] and MR13 OP[6] need to be different at setting MR51 OP[3:2].

To support operation with Single-ended Clock and Strobe enabled, MR51 supports two physical registers and are included in the configuration changes supported with set points 0 and 1 during FSP switching.

The frequency set point update timing for Differential/Single-ended mode switching is shown below. When changing the frequency set point via MR13 OP[7], the VRCG setting: MR13 OP[3] have to be changed into VREF fast response (high current) mode at the same time. After frequency change time ( $t_{FC}$ ) is satisfied. VRCG can be changed into normal operation mode via MR13 OP[3].

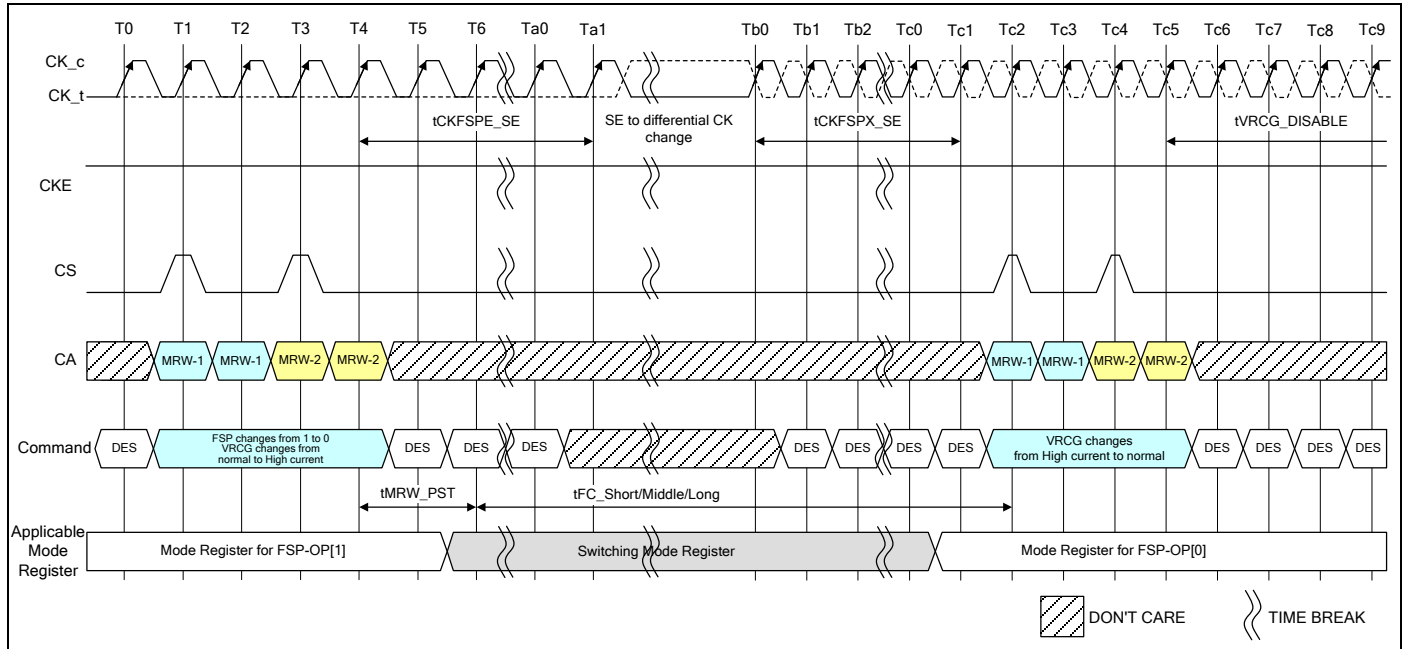


#### Notes:

1. The definition that is Clock frequency change during CKE HIGH should be followed at the frequency change operation. For more information, refer to section 7.4.45 Input Clock Stop and Frequency Change.
2. Clock input level after Tb0 is an example. The stable high to the clock input is also allowed.
3. Mode Register Setting  
 FSP-OP MR13 OP[7] = 0<sub>b</sub>  
 Single ended Clock MR51 OP[3] = 0<sub>b</sub> (Disabled)  
 FSP-OP MR13 OP[7] = 1<sub>b</sub>  
 Single ended Clock: MR51 OP[3] = 1<sub>b</sub> (Enabled)

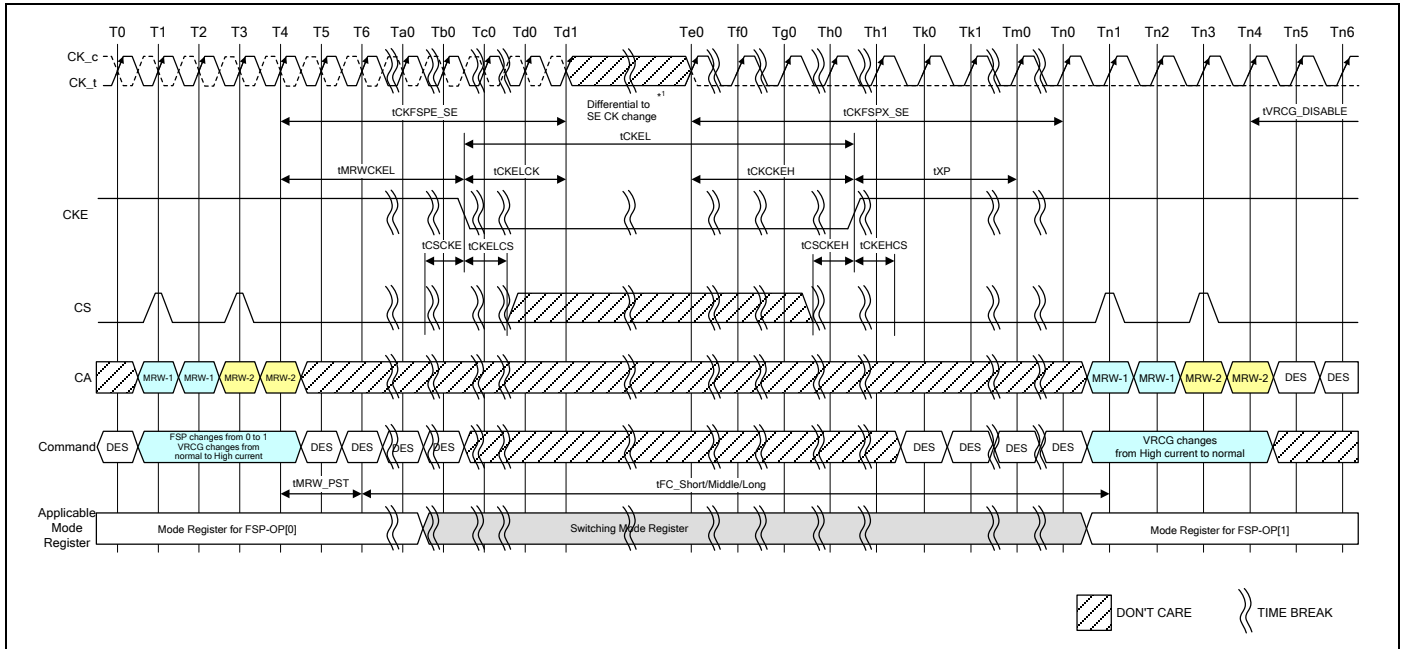
**Figure 178 - Differential to SE CK and Write DQS -FSP Switching Timing CKE=High**



**Notes:**

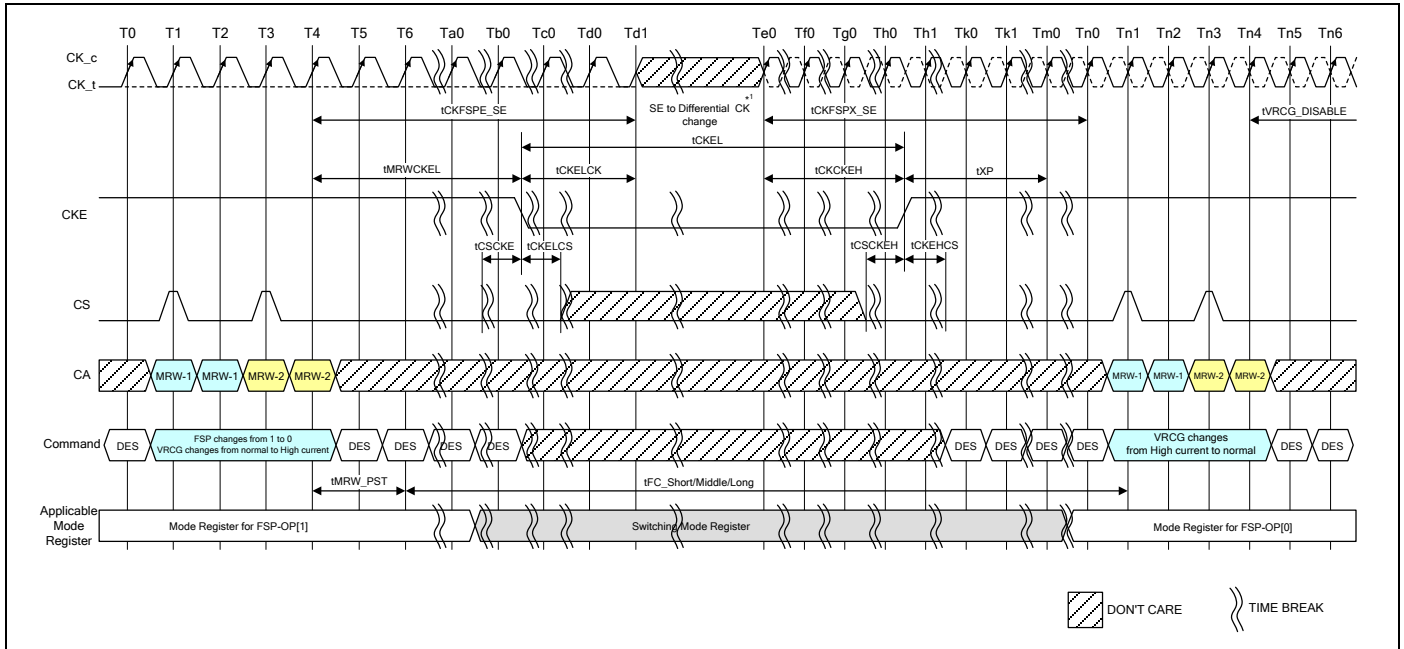
1. The definition that is Clock frequency change during CKE HIGH should be followed at the frequency change operation. For more information, refer to section **7.4.45** Input Clock Stop and Frequency Change.
2. Clock input level after Ta1 is an example. The stable high to the clock input is also allowed.
3. Mode Register Setting  
 FSP-OP MR13 OP[7] = 0<sub>b</sub>  
 Single ended Clock MR51 OP[3] = 0<sub>b</sub> (Disabled)  
 FSP-OP MR13 OP[7] = 1<sub>b</sub>  
 Single ended Clock: MR51 OP[3] = 1<sub>b</sub> (Enabled)

**Figure 179 - SE to Differential CK and Write DQS -FSP Switching Timing CKE=High**

**Notes:**

1. The input clock frequency can be changed, stopped, or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of  $t_{CKCKEH}$  of stable clock prior to power-down exit and that the clock frequency is between the minimum and maximum frequency for the speed grade in use.
2. Clock input level after  $T_{e0}$  is an example. The stable high to the clock input is also allowed.
3. The CKE is able to move to LOW without satisfying  $t_{VRCG}$  enable period.
4. Mode Register Setting  
 FSP-OP MR13 OP[7] =  $0_b$   
 Single ended Clock MR51 OP[3] =  $0_b$  (Disabled)  
 FSP-OP MR13 OP[7] =  $1_b$   
 Single ended Clock: MR51 OP[3] =  $1_b$  (Enabled)

**Figure 180 - Differential to SE CK and Write DQS -FSP Switching Timing CKE=Low**



#### Notes:

1. The input clock frequency can be changed, stopped, or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of  $t_{CKCKEH}$  of stable clock prior to power-down exit and that the clock frequency is between the minimum and maximum frequency for the speed grade in use.
2. Clock input level after Td1 is an example. The stable high to the clock input is also allowed.
3. The CKE is able to move to LOW without satisfying  $t_{VRCG}$  enable period.
4. Mode Register Setting  
 FSP-OP MR13 OP[7] = 0<sub>b</sub>  
 Single ended Clock MR51 OP[3] = 0<sub>b</sub> (Disabled)  
 FSP-OP MR13 OP[7] = 1<sub>b</sub>  
 Single ended Clock: MR51 OP[3] = 1<sub>b</sub> (Enabled)

**Figure 181 - SE to Differential CK and Write DQS -FSP Switching Timing CKE=Low**



#### 9.4 VRCG Enable timing

The VRCG Enable timing when MR51 OP[3]: Single ended Clock has been set 1<sub>b</sub> (Enable) for either or both physical register is shown in Figure 182.

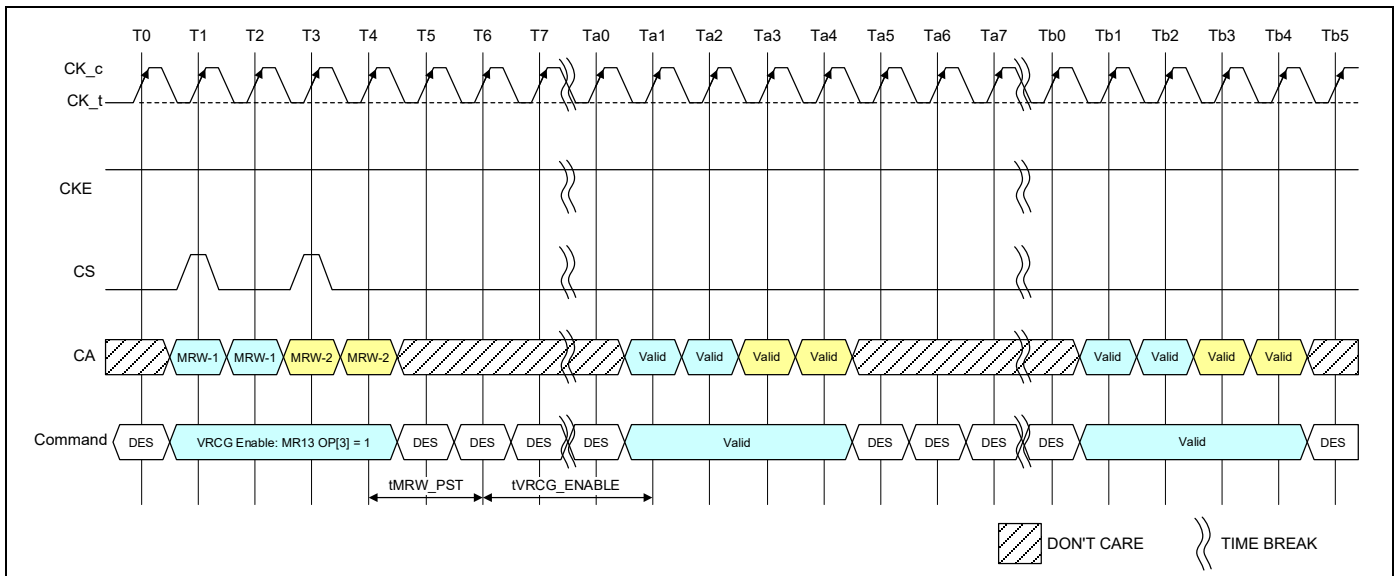
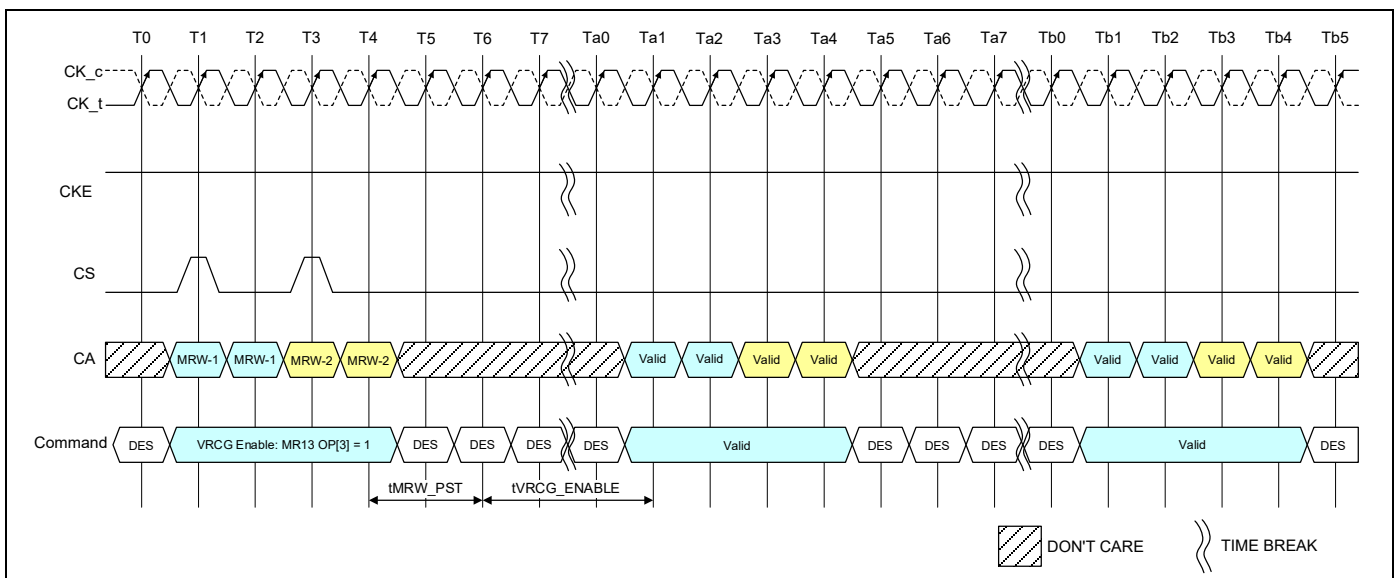


Figure 182 - VRCG status change to high current mode: Single-ended Clock Case



**Note:**

1. When Single-ended Clock is enabled on inactive mode register: MR51 OP[3].

Figure 183 - VRCG status change to high current mode: Differential Clock Case

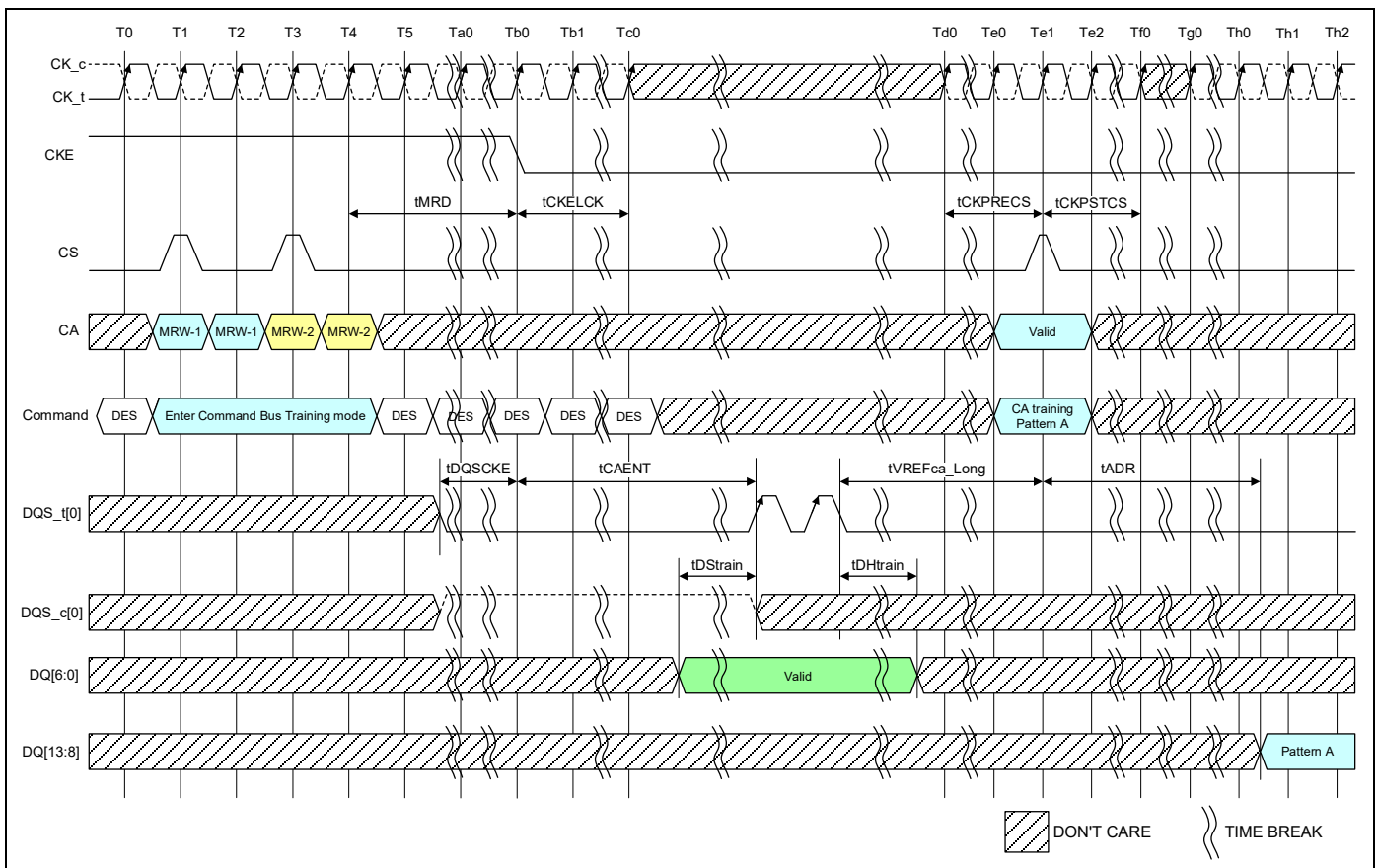


Table 126 - SE from/to Differential FSP and additional period for MRW AC timing

| Parameter                                                                                            | Symbol     | Min/Max | Data Rate                      | Unit | Note |
|------------------------------------------------------------------------------------------------------|------------|---------|--------------------------------|------|------|
|                                                                                                      |            |         | Equal to or less than 1600Mbps |      |      |
| Frequency Set Point Parameters for Switching Single-ended from/to Differential Clock/Strobe          |            |         |                                |      |      |
| Valid Clock Requirement after entering FSP when changing between SE/Differential modes               | tCKFSPE_SE | Min     | Max(15nS, 8nCK)                | -    |      |
| Valid Clock Requirement before first valid command after an FSP change between SE/Differential modes | tCKFSPX_SE | Min     | Max(15nS, 8nCK)                | -    |      |
| Additional period for after MRW command                                                              |            |         |                                |      |      |
| Post Clock for MRW                                                                                   | tMRW_PST   | Min     | 2                              | nCK  |      |

### 9.5 Command bus training procedure

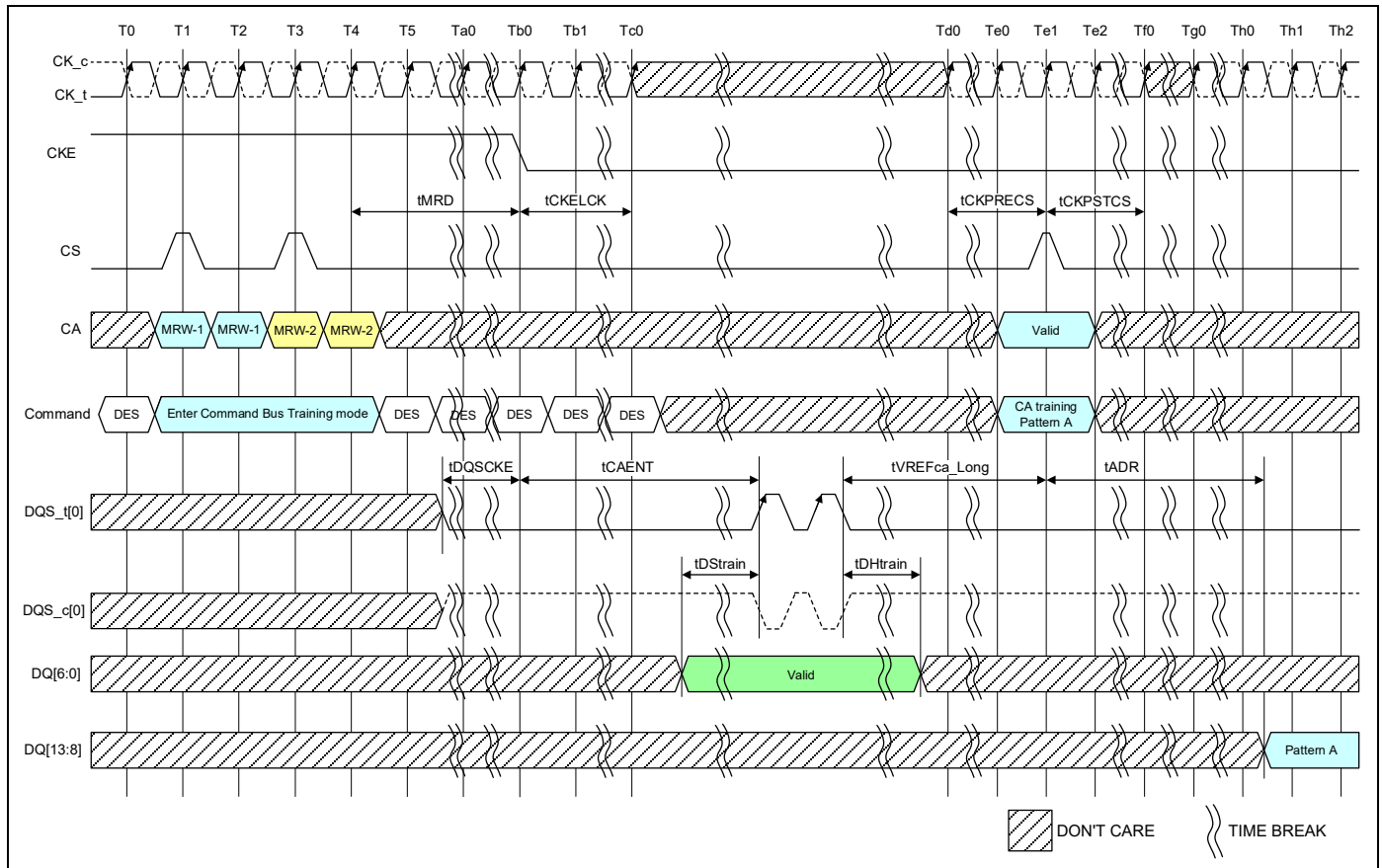
DQS\_c input level is required to “High” during tDQSCKE and CAENT period when the MR51 OP[2]: Single ended WDQS has been set 1<sub>b</sub> (Enable) for either physical register. This restriction is to prevent capturing unexpected DQS edge when SOC mode is moving from Diff. DQS mode to SE DQS mode and vice versa. The command bus training timing is shown below.



#### Note:

1. The status of following pins is don't care from T0 to Th2: DQ[7], DQ[15:14], DMI[1:0], DQS\_t[1] and DQS\_c[1].

Figure 184 - Write DQS mode changes from Differential to Single-ended for x16 device

**Note:**

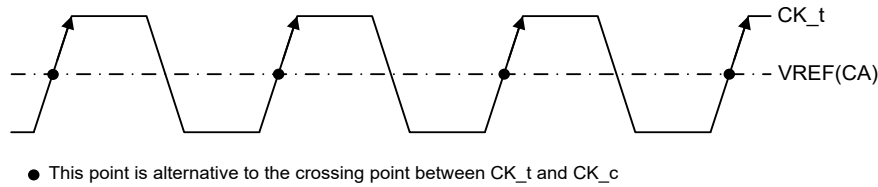
1. The status of following pins is don't care from T0 to Th2: DQ[7], DQ[15:14], DMI[1:0], DQS\_t[1] and DQS\_c[1].

**Figure 185 - Write DQS mode changes from Single-ended to Differential for x16 device**



## 9.6 Reference level for Single-ended mode

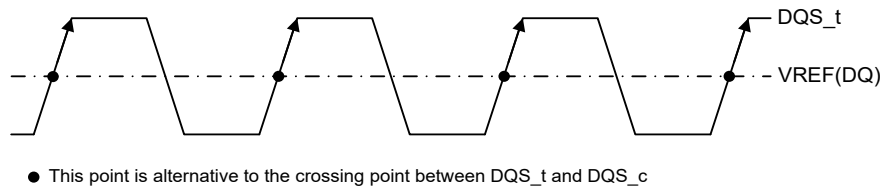
When Single-ended mode is enabled for Clock and Strobe, each reference level is as follows. CK<sub>t</sub> is referenced to VREF(CA) as the same as the command and the chip select and DQS<sub>t</sub> is referenced to VREF(DQ) as the same as DQ and DMI.



### Notes:

1. VREF(CA) is calculated value based on VDD2 and MR12.
2. VREF(CA) must be set in following Opcode.  
MR12 OP[6] = 0, MR12 OP[5:0] = 000000<sub>b</sub> through 110010<sub>b</sub>  
MR12 OP[6] = 1, MR12 OP[5:0] = 000000<sub>b</sub> through 110010<sub>b</sub>

**Figure 186 - Reference point of CK<sub>t</sub>**



### Notes:

1. VREF(DQ) is calculated value based on VDDQ and MR14.
2. VREF(DQ) must be set in following Opcode.  
MR14 OP[6] = 0, MR14 OP[5:0] = 000000<sub>b</sub> through 110010<sub>b</sub>  
MR14 OP[6] = 1, MR14 OP[5:0] = 000000<sub>b</sub> through 110010<sub>b</sub>

**Figure 187 - Reference point of DQS<sub>t</sub>**



## 9.7 AC parameters for Single Ended (SE)

The AC timing is shown in below Table is applied under conditions of Single ended mode.

**Table 127 - Delta CK and DQS Specification**

| Parameter                                           | Symbol                                                 | Min/Max | Data Rate Equal to or less than 1600Mbps | Unit     | Notes |
|-----------------------------------------------------|--------------------------------------------------------|---------|------------------------------------------|----------|-------|
| CK single-ended input voltage                       | V <sub>inse_CK_High</sub> - V <sub>inse_CK_low</sub>   | Min     | 210                                      | mV       | 1     |
| Rx timing window                                    | tCIVW                                                  | Max     | 0.35                                     | UI       | 1, 5  |
| Average High pulse width                            | tCH(avg)                                               | Min     | 0.46                                     | tCK(avg) | 1     |
|                                                     |                                                        | Max     | 0.54                                     | tCK(avg) | 1     |
| Average Low pulse width                             | tCL(avg)                                               | Min     | 0.46                                     | tCK(avg) | 1     |
|                                                     |                                                        | Max     | 0.54                                     | tCK(avg) | 1     |
| Absolute High clock pulse width                     | tCH(abs)                                               | Min     | 0.43                                     | tCK(avg) | 1     |
|                                                     |                                                        | Max     | 0.57                                     | tCK(avg) | 1     |
| Absolute Low clock pulse width                      | tCL(abs)                                               | Min     | 0.43                                     | tCK(avg) | 1     |
|                                                     |                                                        | Max     | 0.57                                     | tCK(avg) | 1     |
| Input Slew Rate for Clock                           | SRIN_CK                                                | Min     | 1                                        | V/nS     | 1     |
|                                                     |                                                        | Max     | 7                                        | V/nS     | 1     |
| DQS single-ended input voltage                      | V <sub>inse_DQS_High</sub> - V <sub>inse_DQS_low</sub> | Min     | 210                                      | mV       | 2     |
| Input Slew Rate for DQS                             | SRIN_DQS                                               | Min     | 1                                        | V/nS     | 2     |
|                                                     |                                                        | Max     | 7                                        | V/nS     | 2     |
| Rx timing window total                              | tDIVW                                                  | Max     | 0.35                                     | UI       | 2, 6  |
| DQS Single-ended output high time (DBI-Disabled)    | tQSH                                                   | Min     | tCH-0.10                                 | tCK(avg) | 1, 3  |
| DQS Single-ended output low time (DBI-Disabled)     | tQSL                                                   | Min     | tCL-0.10                                 | tCK(avg) | 1, 3  |
| DQ output window time total, per pin (DBI-Disabled) | tQW                                                    | Min     | 0.65                                     | UI       | 6     |
| Write leveling setup time                           | tWLS                                                   | Min     | 250                                      | pS       | 4     |
| Write leveling hold time                            | tWLH                                                   | Min     | 250                                      | pS       | 4     |
| DQS falling edge to CK setup time                   | tDSS                                                   | Min     | 0.3                                      | tCK(avg) | 4     |
| DQS falling edge hold time from CK                  | tDSH                                                   | Min     | 0.3                                      | tCK(avg) | 4     |

### Notes:

1. This spec is applied when MR51 OP[3]=1<sub>b</sub> (single ended CK enabled).
2. This spec is applied when MR51 OP[2]=1<sub>b</sub> (single ended Write DQS enabled).
3. This spec is applied when MR51 OP[1]=1<sub>b</sub> (single ended Read DQS enabled).
4. This spec is applied when MR51 OP[3]=1<sub>b</sub> and MR51 OP[2]=0<sub>b</sub> or MR51 OP[3]=0<sub>b</sub> and MR51 OP[2]=1<sub>b</sub>.
5. UI=tCK.
6. UI=tCK/2.





## 10. LPDDR4X SPECIFIC REQUIREMENT

This section defines LPDDR4X mode specific requirement to enable 0.6V VDDQ operation of LPDDR4X device. While the LPDDR4/LPDDR4X combo SDRAM operate as LPDDR4X mode, many specifications are different to the LPDDR4 mode such as the power-up initialization default values of Mode Registers settings, DC/AC spec values, ODT\_CA termination control... etc. Those differences can be refer to the words in blue color of this section.

### 10.1 Mode Register Definition – LPDDR4X

The table listed below shows the Mode Registers for LPDDR4X SDRAM. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

**Table 128 - Mode Register Assignment in LPDDR4X mode**

| MR#   | OP[7]                                                   | OP[6]          | OP[5]               | OP[4]   | OP[3]              | OP[2]             | OP[1]             | OP[0]        |
|-------|---------------------------------------------------------|----------------|---------------------|---------|--------------------|-------------------|-------------------|--------------|
| 0     | CATR                                                    | RFU            | Single Ended Mode   | RZQI    |                    | RFU               | Latency Mode      | Refresh Mode |
| 1     | RPST                                                    | nWR (for AP)   |                     |         | RD-PRE             | WR-PRE            | BL                |              |
| 2     | WR Lev                                                  | WLS            | WL                  |         |                    | RL                |                   |              |
| 3     | DBI-WR                                                  | DBI-RD         | PDDS                |         |                    | PPRP              | WR PST            | PU-CAL       |
| 4     | TUF                                                     | Thermal Offset |                     | PPRE    | SR Abort           | Refresh Rate      |                   |              |
| 5     | LPDDR4X Manufacturer ID                                 |                |                     |         |                    |                   |                   |              |
| 6     | Revision ID-1                                           |                |                     |         |                    |                   |                   |              |
| 7     | Revision ID-2                                           |                |                     |         |                    |                   |                   |              |
| 8     | IO Width                                                |                | Density             |         |                    |                   | Type              |              |
| 9     | Vendor Specific Test Register                           |                |                     |         |                    |                   |                   |              |
| 10    | RFU                                                     |                |                     |         |                    |                   |                   | ZQ-Reset     |
| 11    | Reserved                                                | CA ODT         |                     |         | Reserved           | DQ ODT            |                   |              |
| 12    | RFU                                                     | VR-CA          | VREF(CA)            |         |                    |                   |                   |              |
| 13    | FSP-OP                                                  | FSP-WR         | DMD                 | RRO     | VRCG               | VRO               | RPT               | CBT          |
| 14    | RFU                                                     | VR(dq)         | VREF(DQ)            |         |                    |                   |                   |              |
| 15    | Lower-Byte Invert Register for Calibration              |                |                     |         |                    |                   |                   |              |
| 16    | PASR Bank Mask                                          |                |                     |         |                    |                   |                   |              |
| 17    | PASR Segment Mask                                       |                |                     |         |                    |                   |                   |              |
| 18    | DQS Oscillator Count - LSB                              |                |                     |         |                    |                   |                   |              |
| 19    | DQS Oscillator Count - MSB                              |                |                     |         |                    |                   |                   |              |
| 20    | Upper-Byte Invert Register for DQ Calibration           |                |                     |         |                    |                   |                   |              |
| 21    | RFU                                                     |                | Low Speed CA Buffer | RFU     |                    |                   |                   |              |
| 22    | RFU                                                     |                | ODTD-CA             | ODTE-CS | ODTE-CK            | SOC ODT           |                   |              |
| 23    | DQS interval timer run time setting                     |                |                     |         |                    |                   |                   |              |
| 24    | TRR Mode                                                | TRR Mode BAn   |                     |         | Unlimited MAC      | MAC Value         |                   |              |
| 25    | PPR Resource                                            |                |                     |         |                    |                   |                   |              |
| 26~29 | RFU                                                     |                |                     |         |                    |                   |                   |              |
| 30    | Reserved for testing – SDRAM will ignore                |                |                     |         |                    |                   |                   |              |
| 31    | RFU                                                     |                |                     |         |                    |                   |                   |              |
| 32    | DQ Calibration Pattern “A” (default = 5A <sub>H</sub> ) |                |                     |         |                    |                   |                   |              |
| 33~38 | RFU                                                     |                |                     |         |                    |                   |                   |              |
| 39    | Reserved for testing – SDRAM will ignore                |                |                     |         |                    |                   |                   |              |
| 40    | DQ Calibration Pattern “B” (default = 3C <sub>H</sub> ) |                |                     |         |                    |                   |                   |              |
| 41~50 | RFU                                                     |                |                     |         |                    |                   |                   |              |
| 51    | RFU                                                     |                |                     |         | Single Ended Clock | Single Ended WDQS | Single Ended RDQS | RFU          |



### 10.1.1 MR0 Register Information (MA[5:0] = 00H)

| OP[7] | OP[6] | OP[5]             | OP[4] | OP[3] | OP[2] | OP[1]        | OP[0]        |
|-------|-------|-------------------|-------|-------|-------|--------------|--------------|
| CATR  | RFU   | Single Ended Mode | RZQI  |       | RFU   | Latency Mode | Refresh Mode |

| Function                             | Type      | Operand | Data                                                                                                                                                                                                                                                                                                                  | Notes      |
|--------------------------------------|-----------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| Refresh Mode                         | Read-only | OP[0]   | <b>0<sub>b</sub></b> : Both legacy and modified refresh mode supported (default)<br><b>1<sub>b</sub></b> : Only modified refresh mode supported                                                                                                                                                                       |            |
| Latency Mode                         |           | OP[1]   | <b>0<sub>b</sub></b> : Device supports normal latency<br><b>1<sub>b</sub></b> : Reserved                                                                                                                                                                                                                              | 5          |
| RZQI<br>(Built-in Self-Test for RZQ) |           | OP[4:3] | <b>00<sub>b</sub></b> : RZQ Self-Test not support.<br><b>01<sub>b</sub></b> : ZQ-pin may connect to VSSQ or float<br><b>10<sub>b</sub></b> : ZQ-pin may short to VDDQ<br><b>11<sub>b</sub></b> : ZQ-pin Self-Test completed, no error condition detected (ZQ-pin may not connect to VSSQ or float, nor short to VDDQ) | 1, 2, 3, 4 |
| Single Ended Mode                    |           | OP[5]   | <b>1<sub>b</sub></b> : Supports for Single Ended Mode                                                                                                                                                                                                                                                                 | 6          |
| CATR<br>(CA Terminating Rank)        |           | OP[7]   | <b>0<sub>b</sub></b> : CA for this rank is not terminated<br><b>1<sub>b</sub></b> : CA for this rank is terminated                                                                                                                                                                                                    | 7          |

#### Notes:

- RZQI MR value, if supported, will be valid after the following sequence:
  - Completion of MPC ZQCAL Start command to either channel.
  - Completion of MPC ZQCAL Latch command to either channel then tZQLAT is satisfied.  
RZQI value will be lost after Reset.
- If the ZQ-pin is connected to VSSQ to set default calibration, OP[4:3] shall be set to 01<sub>b</sub>. If the ZQ-pin is not connected to VSSQ, either OP[4:3] = 01<sub>b</sub> or OP[4:3] = 10<sub>b</sub> might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
- In the case of possible assembly error, the LPDDR4X SDRAM device will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.
- If ZQ Self-Test returns OP[4:3] = 11<sub>b</sub>, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240Ω ± 1%).
- Byte mode is not supported.
- OP[5] set to 1<sub>b</sub> support for Single Ended Mode, Single Ended Write DQS, Read DQS and CK can be enabled in MR51.
- CATR can indicate the CA for the rank is terminated or not.

10.1.2 MR3 Register Information (MA[5:0] = 03<sub>H</sub>)

| OP[7]  | OP[6]  | OP[5] | OP[4] | OP[3] | OP[2] | OP[1]  | OP[0]  |
|--------|--------|-------|-------|-------|-------|--------|--------|
| DBI-WR | DBI-RD | PDDS  |       |       | PPRP  | WR PST | PU-CAL |

| Function                              | Type       | Operand | Data                                                                                                                                                                                                                                    | Notes   |
|---------------------------------------|------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| PU-Cal<br>(Pull-up Calibration Point) | Write only | OP[0]   | 0 <sub>b</sub> : VDDQ*0.6<br>1 <sub>b</sub> : VDDQ*0.5 (default)                                                                                                                                                                        | 1, 4    |
| WR PST<br>(WR Post-Amble Length)      |            | OP[1]   | 0 <sub>b</sub> : WR Post-amble = 0.5*tCK (default)<br>1 <sub>b</sub> : WR Post-amble = 1.5*tCK                                                                                                                                          | 2, 3, 5 |
| Post Package Repair Protection        |            | OP[2]   | 0 <sub>b</sub> : PPR protection disabled (default)<br>1 <sub>b</sub> : PPR protection enabled                                                                                                                                           | 6       |
| PDDS<br>(Pull-Down Drive strength)    |            | OP[5:3] | 000 <sub>b</sub> : RFU<br>001 <sub>b</sub> : RZQ/1<br>010 <sub>b</sub> : RZQ/2<br>011 <sub>b</sub> : RZQ/3<br>100 <sub>b</sub> : RZQ/4<br>101 <sub>b</sub> : RZQ/5<br>110 <sub>b</sub> : RZQ/6 (default)<br>111 <sub>b</sub> : Reserved | 1, 2, 3 |
| DBI-RD<br>(DBI-Read Enable)           |            | OP[6]   | 0 <sub>b</sub> : Disabled (default)<br>1 <sub>b</sub> : Enabled                                                                                                                                                                         | 2, 3    |
| DBI-WR<br>(DBI-Write Enable)          |            | OP[7]   | 0 <sub>b</sub> : Disabled (default)<br>1 <sub>b</sub> : Enabled                                                                                                                                                                         | 2, 3    |

**Notes:**

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.
5. 1.5\*tCK apply > 1.6GHz clock.
6. If MR3 OP[2] is set to 1<sub>b</sub> then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0<sub>b</sub> by a power on reset. MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].



### 10.1.3 MR12 Register Information (MA[5:0] = 0C<sub>H</sub>)

| OP[7] | OP[6] | OP[5]    | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|-------|----------|-------|-------|-------|-------|-------|
| RFU   | VR-CA | VREF(CA) |       |       |       |       |       |

| Function                       | Type       | Operand | Data                                                                                                                  | Notes         |
|--------------------------------|------------|---------|-----------------------------------------------------------------------------------------------------------------------|---------------|
| VREF(CA)<br>(VREF(CA) Setting) | Read/Write | OP[5:0] | <b>000000<sub>b</sub>:</b><br>-- Thru --<br><b>110010<sub>b</sub>: See table below</b><br><b>All Others: Reserved</b> | 1, 2, 3, 5, 6 |
| VR-CA<br>(VREF(CA) Range)      |            | OP[6]   | <b>0<sub>b</sub>:</b> VREF(CA) Range[0] enabled<br><b>1<sub>b</sub>:</b> VREF(CA) Range[1] enabled (default)          | 1, 2, 4, 5, 6 |

#### Notes:

1. This register controls the VREF(CA) levels. Refer to Table 129 - VREF Settings for Range[0] and Range[1] for actual voltage of VREF(CA).
2. A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See section 7.4.23 on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(CA) level for FSP[0] when MR13 OP[6] = 0<sub>b</sub>, or sets the internal VREF(CA) level for FSP[1] when MR13 OP[6] = 1<sub>b</sub>. The time required for VREF(CA) to reach the set level depends on the step size from the current level to the new level. See section 7.4.26 on VREF(CA) training for more information.
4. A write to OP[6] switches the LPDDR4X SDRAM between two internal VREF(CA) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(CA) register. The value, once set, will be retained until over written, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.



Table 129 - VREF Settings for Range[0] and Range[1]

| Function               | Operand | Range[0] Values (% of VDDQ) |                             | Range[1] Values (% of VDDQ) |                                       | Notes   |
|------------------------|---------|-----------------------------|-----------------------------|-----------------------------|---------------------------------------|---------|
| VREF Settings for MR12 | OP[5:0] | 000000 <sub>b</sub> : 15.0% | 011010 <sub>b</sub> : 30.5% | 000000 <sub>b</sub> : 32.9% | 011010 <sub>b</sub> : 48.5%           | 1, 2, 3 |
|                        |         | 000001 <sub>b</sub> : 15.6% | 011011 <sub>b</sub> : 31.1% | 000001 <sub>b</sub> : 33.5% | 011011 <sub>b</sub> : 49.1%           |         |
|                        |         | 000010 <sub>b</sub> : 16.2% | 011100 <sub>b</sub> : 31.7% | 000010 <sub>b</sub> : 34.1% | 011100 <sub>b</sub> : 49.7%           |         |
|                        |         | 000011 <sub>b</sub> : 16.8% | 011101 <sub>b</sub> : 32.3% | 000011 <sub>b</sub> : 34.7% | 011101 <sub>b</sub> : 50.3% (Default) |         |
|                        |         | 000100 <sub>b</sub> : 17.4% | 011110 <sub>b</sub> : 32.9% | 000100 <sub>b</sub> : 35.3% | 011110 <sub>b</sub> : 50.9%           |         |
|                        |         | 000101 <sub>b</sub> : 18.0% | 011111 <sub>b</sub> : 33.5% | 000101 <sub>b</sub> : 35.9% | 011111 <sub>b</sub> : 51.5%           |         |
|                        |         | 000110 <sub>b</sub> : 18.6% | 100000 <sub>b</sub> : 34.1% | 000110 <sub>b</sub> : 36.5% | 100000 <sub>b</sub> : 52.1%           |         |
|                        |         | 000111 <sub>b</sub> : 19.2% | 100001 <sub>b</sub> : 34.7% | 000111 <sub>b</sub> : 37.1% | 100001 <sub>b</sub> : 52.7%           |         |
|                        |         | 001000 <sub>b</sub> : 19.8% | 100010 <sub>b</sub> : 35.3% | 001000 <sub>b</sub> : 37.7% | 100010 <sub>b</sub> : 53.3%           |         |
|                        |         | 001001 <sub>b</sub> : 20.4% | 100011 <sub>b</sub> : 35.9% | 001001 <sub>b</sub> : 38.3% | 100011 <sub>b</sub> : 53.9%           |         |
|                        |         | 001010 <sub>b</sub> : 21.0% | 100100 <sub>b</sub> : 36.5% | 001010 <sub>b</sub> : 38.9% | 100100 <sub>b</sub> : 54.5%           |         |
|                        |         | 001011 <sub>b</sub> : 21.6% | 100101 <sub>b</sub> : 37.1% | 001011 <sub>b</sub> : 39.5% | 100101 <sub>b</sub> : 55.1%           |         |
|                        |         | 001100 <sub>b</sub> : 22.2% | 100110 <sub>b</sub> : 37.7% | 001100 <sub>b</sub> : 40.1% | 100110 <sub>b</sub> : 55.7%           |         |
|                        |         | 001101 <sub>b</sub> : 22.8% | 100111 <sub>b</sub> : 38.3% | 001101 <sub>b</sub> : 40.7% | 100111 <sub>b</sub> : 56.3%           |         |
|                        |         | 001110 <sub>b</sub> : 23.4% | 101000 <sub>b</sub> : 38.9% | 001110 <sub>b</sub> : 41.3% | 101000 <sub>b</sub> : 56.9%           |         |
|                        |         | 001111 <sub>b</sub> : 24.0% | 101001 <sub>b</sub> : 39.5% | 001111 <sub>b</sub> : 41.9% | 101001 <sub>b</sub> : 57.5%           |         |
|                        |         | 010000 <sub>b</sub> : 24.6% | 101010 <sub>b</sub> : 40.1% | 010000 <sub>b</sub> : 42.5% | 101010 <sub>b</sub> : 58.1%           |         |
|                        |         | 010001 <sub>b</sub> : 25.1% | 101011 <sub>b</sub> : 40.7% | 010001 <sub>b</sub> : 43.1% | 101011 <sub>b</sub> : 58.7%           |         |
|                        |         | 010010 <sub>b</sub> : 25.7% | 101100 <sub>b</sub> : 41.3% | 010010 <sub>b</sub> : 43.7% | 101100 <sub>b</sub> : 59.3%           |         |
|                        |         | 010011 <sub>b</sub> : 26.3% | 101101 <sub>b</sub> : 41.9% | 010011 <sub>b</sub> : 44.3% | 101101 <sub>b</sub> : 59.9%           |         |
|                        |         | 010100 <sub>b</sub> : 26.9% | 101110 <sub>b</sub> : 42.5% | 010100 <sub>b</sub> : 44.9% | 101110 <sub>b</sub> : 60.5%           |         |
|                        |         | 010101 <sub>b</sub> : 27.5% | 101111 <sub>b</sub> : 43.1% | 010101 <sub>b</sub> : 45.5% | 101111 <sub>b</sub> : 61.1%           |         |
|                        |         | 010110 <sub>b</sub> : 28.1% | 110000 <sub>b</sub> : 43.7% | 010110 <sub>b</sub> : 46.1% | 110000 <sub>b</sub> : 61.7%           |         |
|                        |         | 010111 <sub>b</sub> : 28.7% | 110001 <sub>b</sub> : 44.3% | 010111 <sub>b</sub> : 46.7% | 110001 <sub>b</sub> : 62.3%           |         |
|                        |         | 011000 <sub>b</sub> : 29.3% | 110010 <sub>b</sub> : 44.9% | 011000 <sub>b</sub> : 47.3% | 110010 <sub>b</sub> : 62.9%           |         |
|                        |         | 011001 <sub>b</sub> : 29.9% | All Others: Reserved        | 011001 <sub>b</sub> : 47.9% | All Others: Reserved                  |         |

**Notes:**

1. These values may be used for MR12 OP[5:0] to set the VREF(CA) levels in the LPDDR4X mode.
2. The range may be selected in the MR12 register by setting OP[6] appropriately.
3. The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high frequency setting which may use different terminations values.



#### 10.1.4 MR14 Register Information (MA[5:0] = 0E<sub>H</sub>)

| OP[7] | OP[6]  | OP[5]    | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|--------|----------|-------|-------|-------|-------|-------|
| RFU   | VR(DQ) | VREF(DQ) |       |       |       |       |       |

| Function                       | Type       | Operand | Data                                                                                                                  | Notes         |
|--------------------------------|------------|---------|-----------------------------------------------------------------------------------------------------------------------|---------------|
| VREF(DQ)<br>(VREF(DQ) Setting) | Read/Write | OP[5:0] | <b>000000<sub>b</sub>:</b><br>-- Thru --<br><b>110010<sub>b</sub>: See table below</b><br><b>All Others: Reserved</b> | 1, 2, 3, 5, 6 |
| VR(DQ)<br>(VREF(DQ) Range)     |            | OP[6]   | <b>0<sub>b</sub>:</b> VREF(DQ) Range[0] enabled<br><b>1<sub>b</sub>:</b> VREF(DQ) Range[1] enabled (default)          | 1, 2, 4, 5, 6 |

##### Notes:

1. This register controls the VREF(DQ) levels for Frequency-Set-Point[1:0]. Values from either VR(DQ)[0] or VR(DQ)[1] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See section 7.4.23 on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(DQ) level for FSP[0] when MR13 OP[6]=0<sub>b</sub>, or sets FSP[1] when MR13 OP[6]=1<sub>b</sub>. The time required for VREF(DQ) to reach the set level depends on the step size from the current level to the new level. See section 7.4.27 on VREF(DQ) training for more information.
4. A write to OP[6] switches the LPDDR4X SDRAM between two internal VREF(DQ) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(DQ) register. The value, once set, will be retained until over written, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.



Table 130 - VREF Settings for Range[0] and Range[1]

| Function               | Operand | Range[0] Values (% of VDDQ) |                             | Range[1] Values (% of VDDQ) |                                       | Notes   |
|------------------------|---------|-----------------------------|-----------------------------|-----------------------------|---------------------------------------|---------|
| VREF Settings for MR14 | OP[5:0] | 000000 <sub>b</sub> : 15.0% | 011010 <sub>b</sub> : 30.5% | 000000 <sub>b</sub> : 32.9% | 011010 <sub>b</sub> : 48.5%           | 1, 2, 3 |
|                        |         | 000001 <sub>b</sub> : 15.6% | 011011 <sub>b</sub> : 31.1% | 000001 <sub>b</sub> : 33.5% | 011011 <sub>b</sub> : 49.1%           |         |
|                        |         | 000010 <sub>b</sub> : 16.2% | 011100 <sub>b</sub> : 31.7% | 000010 <sub>b</sub> : 34.1% | 011100 <sub>b</sub> : 49.7%           |         |
|                        |         | 000011 <sub>b</sub> : 16.8% | 011101 <sub>b</sub> : 32.3% | 000011 <sub>b</sub> : 34.7% | 011101 <sub>b</sub> : 50.3% (Default) |         |
|                        |         | 000100 <sub>b</sub> : 17.4% | 011110 <sub>b</sub> : 32.9% | 000100 <sub>b</sub> : 35.3% | 011110 <sub>b</sub> : 50.9%           |         |
|                        |         | 000101 <sub>b</sub> : 18.0% | 011111 <sub>b</sub> : 33.5% | 000101 <sub>b</sub> : 35.9% | 011111 <sub>b</sub> : 51.5%           |         |
|                        |         | 000110 <sub>b</sub> : 18.6% | 100000 <sub>b</sub> : 34.1% | 000110 <sub>b</sub> : 36.5% | 100000 <sub>b</sub> : 52.1%           |         |
|                        |         | 000111 <sub>b</sub> : 19.2% | 100001 <sub>b</sub> : 34.7% | 000111 <sub>b</sub> : 37.1% | 100001 <sub>b</sub> : 52.7%           |         |
|                        |         | 001000 <sub>b</sub> : 19.8% | 100010 <sub>b</sub> : 35.3% | 001000 <sub>b</sub> : 37.7% | 100010 <sub>b</sub> : 53.3%           |         |
|                        |         | 001001 <sub>b</sub> : 20.4% | 100011 <sub>b</sub> : 35.9% | 001001 <sub>b</sub> : 38.3% | 100011 <sub>b</sub> : 53.9%           |         |
|                        |         | 001010 <sub>b</sub> : 21.0% | 100100 <sub>b</sub> : 36.5% | 001010 <sub>b</sub> : 38.9% | 100100 <sub>b</sub> : 54.5%           |         |
|                        |         | 001011 <sub>b</sub> : 21.6% | 100101 <sub>b</sub> : 37.1% | 001011 <sub>b</sub> : 39.5% | 100101 <sub>b</sub> : 55.1%           |         |
|                        |         | 001100 <sub>b</sub> : 22.2% | 100110 <sub>b</sub> : 37.7% | 001100 <sub>b</sub> : 40.1% | 100110 <sub>b</sub> : 55.7%           |         |
|                        |         | 001101 <sub>b</sub> : 22.8% | 100111 <sub>b</sub> : 38.3% | 001101 <sub>b</sub> : 40.7% | 100111 <sub>b</sub> : 56.3%           |         |
|                        |         | 001110 <sub>b</sub> : 23.4% | 101000 <sub>b</sub> : 38.9% | 001110 <sub>b</sub> : 41.3% | 101000 <sub>b</sub> : 56.9%           |         |
|                        |         | 001111 <sub>b</sub> : 24.0% | 101001 <sub>b</sub> : 39.5% | 001111 <sub>b</sub> : 41.9% | 101001 <sub>b</sub> : 57.5%           |         |
|                        |         | 010000 <sub>b</sub> : 24.6% | 101010 <sub>b</sub> : 40.1% | 010000 <sub>b</sub> : 42.5% | 101010 <sub>b</sub> : 58.1%           |         |
|                        |         | 010001 <sub>b</sub> : 25.1% | 101011 <sub>b</sub> : 40.7% | 010001 <sub>b</sub> : 43.1% | 101011 <sub>b</sub> : 58.7%           |         |
|                        |         | 010010 <sub>b</sub> : 25.7% | 101100 <sub>b</sub> : 41.3% | 010010 <sub>b</sub> : 43.7% | 101100 <sub>b</sub> : 59.3%           |         |
|                        |         | 010011 <sub>b</sub> : 26.3% | 101101 <sub>b</sub> : 41.9% | 010011 <sub>b</sub> : 44.3% | 101101 <sub>b</sub> : 59.9%           |         |
|                        |         | 010100 <sub>b</sub> : 26.9% | 101110 <sub>b</sub> : 42.5% | 010100 <sub>b</sub> : 44.9% | 101110 <sub>b</sub> : 60.5%           |         |
|                        |         | 010101 <sub>b</sub> : 27.5% | 101111 <sub>b</sub> : 43.1% | 010101 <sub>b</sub> : 45.5% | 101111 <sub>b</sub> : 61.1%           |         |
|                        |         | 010110 <sub>b</sub> : 28.1% | 110000 <sub>b</sub> : 43.7% | 010110 <sub>b</sub> : 46.1% | 110000 <sub>b</sub> : 61.7%           |         |
|                        |         | 010111 <sub>b</sub> : 28.7% | 110001 <sub>b</sub> : 44.3% | 010111 <sub>b</sub> : 46.7% | 110001 <sub>b</sub> : 62.3%           |         |
|                        |         | 011000 <sub>b</sub> : 29.3% | 110010 <sub>b</sub> : 44.9% | 011000 <sub>b</sub> : 47.3% | 110010 <sub>b</sub> : 62.9%           |         |
|                        |         | 011001 <sub>b</sub> : 29.9% | All Others: Reserved        | 011001 <sub>b</sub> : 47.9% | All Others: Reserved                  |         |

**Notes:**

1. These values may be used for MR14 OP[5:0] to set the VREF(DQ) levels in the LPDDR4X mode.
2. The range may be selected in the MR14 register by setting OP[6] appropriately.
3. The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high frequency setting which may use different terminations values.



### 10.1.5 MR22 Register Information (MA[5:0] = 16H)

| OP[7] | OP[6] | OP[5]   | OP[4]   | OP[3]   | OP[2]   | OP[1] | OP[0] |
|-------|-------|---------|---------|---------|---------|-------|-------|
| RFU   |       | ODTD-CA | ODTE-CS | ODTE-CK | SOC ODT |       |       |

| Function                                              | Type       | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Notes   |
|-------------------------------------------------------|------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| SoC ODT<br>(Controller ODT Value for VOH calibration) | Write-only | OP[2:0] | <b>000<sub>b</sub></b> : Disable (Default)<br><b>001<sub>b</sub></b> : RZQ/1 (illegal if MR3 OP[0] = 0 <sub>b</sub> )<br><b>010<sub>b</sub></b> : RZQ/2<br><b>011<sub>b</sub></b> : RZQ/3 (illegal if MR3 OP[0] = 0 <sub>b</sub> )<br><b>100<sub>b</sub></b> : RZQ/4<br><b>101<sub>b</sub></b> : RZQ/5 (illegal if MR3 OP[0] = 0 <sub>b</sub> )<br><b>110<sub>b</sub></b> : RZQ/6 (illegal if MR3 OP[0] = 0 <sub>b</sub> )<br><b>111<sub>b</sub></b> : RFU | 1, 2, 3 |
| ODTE-CK<br>(CK ODT enabled for nonterminating rank)   |            | OP[3]   | ODT bond PAD is ignored<br><b>0<sub>b</sub></b> : ODT-CK Enabled (default)<br><b>1<sub>b</sub></b> : ODT-CK Disabled                                                                                                                                                                                                                                                                                                                                       | 2, 3, 4 |
| ODTE-CS<br>(CS ODT enable for nonterminating rank)    |            | OP[4]   | ODT bond PAD is ignored<br><b>0<sub>b</sub></b> : ODT-CS Enabled (default)<br><b>1<sub>b</sub></b> : ODT-CS Disabled                                                                                                                                                                                                                                                                                                                                       | 2, 3, 4 |
| ODTD-CA<br>(CA ODT termination disable)               |            | OP[5]   | ODT bond PAD is ignored<br><b>0<sub>b</sub></b> : ODT-CA Enabled (default)<br><b>1<sub>b</sub></b> : ODT-CA Disabled                                                                                                                                                                                                                                                                                                                                       | 2, 3, 4 |

#### Notes:

- All values are "typical".
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
- The ODT\_CA pin is ignored by LPDDR4X devices. The ODT\_CA pin shall be connected to either VDD2 or VSS. CA/ CS/ CK ODT is fully controlled through MR11 and MR22. Before enabling CA termination via MR11, all ranks should have appropriate MR22 termination settings programmed.





## 10.2 Pull Up/Pull Down Driver Characteristics and Calibration - LPDDR4X

Table 131 - Pull-down Driver Characteristics, with ZQ Calibration

| RONPD,nom | Resistor | Min | Nom | Max | Unit  |
|-----------|----------|-----|-----|-----|-------|
| 40 Ohm    | RON40PD  | 0.9 | 1   | 1.1 | RZQ/6 |
| 48 Ohm    | RON48PD  | 0.9 | 1   | 1.1 | RZQ/5 |
| 60 Ohm    | RON60PD  | 0.9 | 1   | 1.1 | RZQ/4 |
| 80 Ohm    | RON80PD  | 0.9 | 1   | 1.1 | RZQ/3 |
| 120 Ohm   | RON120PD | 0.9 | 1   | 1.1 | RZQ/2 |
| 240 Ohm   | RON240PD | 0.9 | 1   | 1.1 | RZQ/1 |

**Note:**

1. All value are after ZQ Calibration. Without ZQ Calibration RONPD values are  $\pm 30\%$ .

Table 132 - **Terminated** Pull-Up Characteristics, with ZQ Calibration

| VOHPU,nom | VOH,nom(mV) | Min | Nom | Max | Unit    |
|-----------|-------------|-----|-----|-----|---------|
| VDDQ*0.5  | 300         | 0.9 | 1   | 1.1 | VOH,nom |
| VDDQ*0.6  | 360         | 0.9 | 1   | 1.1 | VOH,nom |

**Notes:**

1. All values are after ZQ Calibration. Without ZQ Calibration VOH(nom) values are  $\pm 30\%$ .
2. VOH,nom (mV) values are based on a nominal VDDQ = 0.6V.

Table 133 - **Terminated** Valid Calibration Points

| VOHPU,nom | SOC ODT Value |       |       |       |       |       |
|-----------|---------------|-------|-------|-------|-------|-------|
|           | 240           | 120   | 80    | 60    | 48    | 40    |
| VDDQ*0.5  | VALID         | VALID | VALID | VALID | VALID | VALID |
| VDDQ*0.6  | DNU           | VALID | DNU   | VALID | DNU   | DNU   |

**Notes:**

1. Once the output is calibrated for a given VOH(nom) calibration point, the ODT value may be changed without recalibration.
2. If the VOH(nom) calibration point is changed, then re-calibration is required.
3. DNU = Do Not Use.

## 10.3 ODT Mode Register and ODT Characteristics - LPDDR4X

The characteristics are provided in Figure 188 and Table 134.

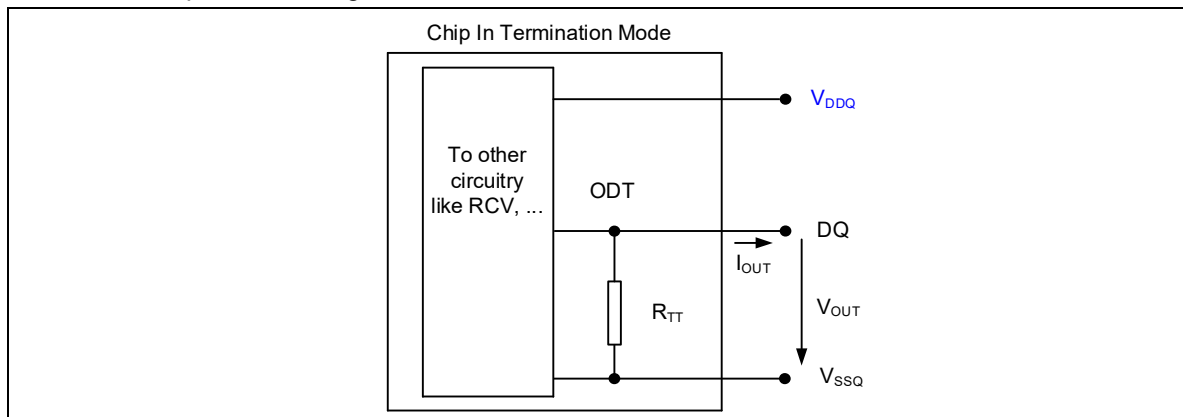


Figure 188 - On Die Termination for CA

$$R_{TT} = \frac{V_{out}}{|I_{out}|}$$



Table 134 - ODT DC Electrical Characteristics for Command/Address Bus

(Assuming RZQ = 240 Ω ±1% over the entire operating temperature range after a proper ZQ calibration)

| MR11[6:4]                       | RTT   | Vout                  | Min | Nom | Max | Unit  | Notes   |
|---------------------------------|-------|-----------------------|-----|-----|-----|-------|---------|
| 001                             | 240 Ω | $VOLdc = 0.2 * VDDQ$  | 0.8 | 1.0 | 1.1 | RZQ   | 1, 2    |
|                                 |       | $VOMdc = 0.5 * VDDQ$  | 0.9 | 1.0 | 1.1 | RZQ   | 1, 2    |
|                                 |       | $VOHdc = 0.75 * VDDQ$ | 0.9 | 1.0 | 1.3 | RZQ   | 1, 2    |
| 010                             | 120 Ω | $VOLdc = 0.2 * VDDQ$  | 0.8 | 1.0 | 1.1 | RZQ/2 | 1, 2    |
|                                 |       | $VOMdc = 0.5 * VDDQ$  | 0.9 | 1.0 | 1.1 | RZQ/2 | 1, 2    |
|                                 |       | $VOHdc = 0.75 * VDDQ$ | 0.9 | 1.0 | 1.3 | RZQ/2 | 1, 2    |
| 011                             | 80 Ω  | $VOLdc = 0.2 * VDDQ$  | 0.8 | 1.0 | 1.1 | RZQ/3 | 1, 2    |
|                                 |       | $VOMdc = 0.5 * VDDQ$  | 0.9 | 1.0 | 1.1 | RZQ/3 | 1, 2    |
|                                 |       | $VOHdc = 0.75 * VDDQ$ | 0.9 | 1.0 | 1.3 | RZQ/3 | 1, 2    |
| 100                             | 60 Ω  | $VOLdc = 0.2 * VDDQ$  | 0.8 | 1.0 | 1.1 | RZQ/4 | 1, 2    |
|                                 |       | $VOMdc = 0.5 * VDDQ$  | 0.9 | 1.0 | 1.1 | RZQ/4 | 1, 2    |
|                                 |       | $VOHdc = 0.75 * VDDQ$ | 0.9 | 1.0 | 1.3 | RZQ/4 | 1, 2    |
| 101                             | 48 Ω  | $VOLdc = 0.2 * VDDQ$  | 0.8 | 1.0 | 1.1 | RZQ/5 | 1, 2    |
|                                 |       | $VOMdc = 0.5 * VDDQ$  | 0.9 | 1.0 | 1.1 | RZQ/5 | 1, 2    |
|                                 |       | $VOHdc = 0.75 * VDDQ$ | 0.9 | 1.0 | 1.3 | RZQ/5 | 1, 2    |
| 110                             | 40 Ω  | $VOLdc = 0.2 * VDDQ$  | 0.8 | 1.0 | 1.1 | RZQ/6 | 1, 2    |
|                                 |       | $VOMdc = 0.5 * VDDQ$  | 0.9 | 1.0 | 1.1 | RZQ/6 | 1, 2    |
|                                 |       | $VOHdc = 0.75 * VDDQ$ | 0.9 | 1.0 | 1.3 | RZQ/6 | 1, 2    |
| Mismatch CA-CA within clk group |       | $0.50 * VDDQ$         | -   |     | 2   | %     | 1, 2, 3 |

**Notes:**

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see section 10.5 on voltage and temperature sensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at  $0.5 * VDDQ$ . Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at  $0.75 * VDDQ$  and  $0.2 * VDDQ$ .
3. CA to CA mismatch within clock group (CA, CS) variation for a given component including CK\_t and CK\_c (characterized).

$$\text{CA - CA Mismatch} = \frac{\text{RODT(max)} - \text{RODT(min)}}{\text{RODT(avg)}}$$



#### 10.4 On Die Termination for DQ, DQS and DMI - LPDDR4X

On-Die Termination effective resistance  $R_{TT}$  is defined by MR11 OP[2:0].

ODT is applied to the DQ, DMI, DQS\_t and DQS\_c pins.

A functional representation of the on-die termination is shown in Figure 189.

Electrical characteristics are provided in Table 135.

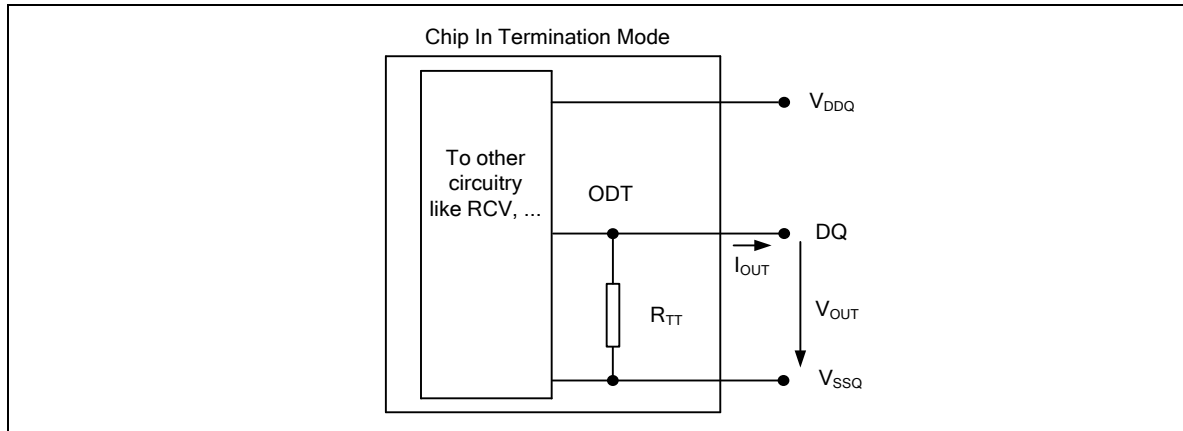


Figure 189 - On Die Termination

$$R_{TT} = \frac{V_{out}}{|I_{out}|}$$



Table 135 - ODT DC Electrical Characteristics for DQ Bus

(Assuming RZQ = 240 Ω ±1% over the entire operating temperature range after a proper ZQ calibration)

| MR11[2:0]                  | R <sub>TT</sub> | Vout               | Min | Nom | Max | Unit  | Notes   |
|----------------------------|-----------------|--------------------|-----|-----|-----|-------|---------|
| 001                        | 240 Ω           | VOLdc= 0.2 * VDDQ  | 0.8 | 1.0 | 1.1 | RZQ   | 1, 2    |
|                            |                 | VOMdc= 0.5 * VDDQ  | 0.9 | 1.0 | 1.1 | RZQ   | 1, 2    |
|                            |                 | VOHdc= 0.75 * VDDQ | 0.9 | 1.0 | 1.3 | RZQ   | 1, 2    |
| 010                        | 120 Ω           | VOLdc= 0.2 * VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/2 | 1, 2    |
|                            |                 | VOMdc= 0.5 * VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/2 | 1, 2    |
|                            |                 | VOHdc= 0.75 * VDDQ | 0.9 | 1.0 | 1.3 | RZQ/2 | 1, 2    |
| 011                        | 80 Ω            | VOLdc= 0.2 * VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/3 | 1, 2    |
|                            |                 | VOMdc= 0.5 * VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/3 | 1, 2    |
|                            |                 | VOHdc= 0.75 * VDDQ | 0.9 | 1.0 | 1.3 | RZQ/3 | 1, 2    |
| 100                        | 60 Ω            | VOLdc= 0.2 * VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/4 | 1, 2    |
|                            |                 | VOMdc= 0.5 * VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/4 | 1, 2    |
|                            |                 | VOHdc= 0.75 * VDDQ | 0.9 | 1.0 | 1.3 | RZQ/4 | 1, 2    |
| 101                        | 48 Ω            | VOLdc= 0.2 * VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/5 | 1, 2    |
|                            |                 | VOMdc= 0.5 * VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/5 | 1, 2    |
|                            |                 | VOHdc= 0.75 * VDDQ | 0.9 | 1.0 | 1.3 | RZQ/5 | 1, 2    |
| 110                        | 40 Ω            | VOLdc= 0.2 * VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/6 | 1, 2    |
|                            |                 | VOMdc= 0.5 * VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/6 | 1, 2    |
|                            |                 | VOHdc= 0.75 * VDDQ | 0.9 | 1.0 | 1.3 | RZQ/6 | 1, 2    |
| Mismatch DQ-DQ within byte |                 | 0.5 * VDDQ         | -   |     | 2   | %     | 1, 2, 3 |

**Notes:**

- The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see section 10.5 on voltage and temperature sensitivity.
- Pull-down ODT resistors are recommended to be calibrated at 0.75\*V<sub>DDQ</sub> and 0.2\*V<sub>DDQ</sub>. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.75\*V<sub>DDQ</sub> and 0.1\*V<sub>DDQ</sub>.
- DQ to DQ mismatch within byte variation for a given component including DQS<sub>t</sub> and DQS<sub>c</sub> (characterized).

$$\text{DQ - DQ Mismatch} = \frac{\text{RODT(max)} - \text{RODT(min)}}{\text{RODT(avg)}}$$



### 10.5 Output Driver and Termination Resistor Temperature and Voltage Sensitivity - LPDDR4X

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 136 and Table 137.

**Table 136 - Output Driver and Termination Resistor Sensitivity Definition**

| Resistor             | Definition Point | Min                                                        | Max                                                         | Unit | Notes   |
|----------------------|------------------|------------------------------------------------------------|-------------------------------------------------------------|------|---------|
| R <sub>ONPD</sub>    | 0.5 x VDDQ       | 90-(dR <sub>ondT</sub> x  ΔT )-(dR <sub>ondV</sub> x  ΔV ) | 110+(dR <sub>ondT</sub> x  ΔT )+(dR <sub>ondV</sub> x  ΔV ) | %    | 1, 2    |
| VOH <sub>PU</sub>    | 0.5 x VDDQ       | 90-(dVOHdT x  ΔT )-(dVOHdV x  ΔV )                         | 110+(dVOHdT x  ΔT )+(dVOHdV x  ΔV )                         | %    | 1, 2, 5 |
| R <sub>TT(I/O)</sub> | 0.5 x VDDQ       | 90-(dR <sub>ondT</sub> x  ΔT )-(dR <sub>ondV</sub> x  ΔV ) | 110+(dR <sub>ondT</sub> x  ΔT )+(dR <sub>ondV</sub> x  ΔV ) | %    | 1, 2, 3 |
| R <sub>TT(In)</sub>  | 0.5 x VDDQ       | 90-(dR <sub>ondT</sub> x  ΔT )-(dR <sub>ondV</sub> x  ΔV ) | 110+(dR <sub>ondT</sub> x  ΔT )+(dR <sub>ondV</sub> x  ΔV ) | %    | 1, 2, 4 |

**Notes:**

1.  $\Delta T = T - T(@ \text{Calibration})$ ,  $\Delta V = V - V(@ \text{Calibration})$ .
2. dR<sub>ondT</sub>, dR<sub>ondV</sub>, dVOHdT, dVOHdV, dR<sub>TTdV</sub>, and dR<sub>TTdT</sub> are not subject to production test but are verified by design and characterization.
3. This parameter applies to Input/Output pin such as DQS, DQ and DMI.
4. This parameter applies to Input pin such as CK, CA and CS.
5. Refer to **10.2** Pull Up/Pull Down Driver Characteristics for VOH<sub>PU</sub>.

**Table 137 - Output Driver and Termination Resistor Temperature and Voltage Sensitivity**

| Symbol             | Parameter                               | Min  | Max  | Unit |
|--------------------|-----------------------------------------|------|------|------|
| dR <sub>ondT</sub> | R <sub>ON</sub> Temperature Sensitivity | 0.00 | 0.75 | %/°C |
| dR <sub>ondV</sub> | R <sub>ON</sub> Voltage Sensitivity     | 0.00 | 0.20 | %/mV |
| dVOHdT             | VOH Temperature Sensitivity             | 0.00 | 0.75 | %/°C |
| dVOHdV             | VOH Voltage Sensitivity                 | 0.00 | 0.35 | %/mV |
| dR <sub>TTdT</sub> | R <sub>TT</sub> Temperature Sensitivity | 0.00 | 0.75 | %/°C |
| dR <sub>TTdV</sub> | R <sub>TT</sub> Voltage Sensitivity     | 0.00 | 0.20 | %/mV |



## 10.6 AC & DC Operating Conditions for LPDDR4X

### 10.6.1 Recommended DC Operating Conditions

| DRAM                             | Symbol | Min  | Typ  | Max  | Unit | Notes      |
|----------------------------------|--------|------|------|------|------|------------|
| Core 1 Power                     | VDD1   | 1.70 | 1.80 | 1.95 | V    | 1, 2       |
| Core 2 Power/ Input Buffer Power | VDD2   | 1.06 | 1.10 | 1.17 | V    | 1, 2, 3    |
| I/O Buffer Power                 | VDDQ   | 0.57 | 0.6  | 0.65 | V    | 2, 3, 4, 5 |

#### Notes:

- VDD1 uses significantly less power than VDD2.
- The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
- The voltage noise tolerance from DC to 20 MHz exceeding a pk-pk tolerance of 45 mV at the DRAM ball is not included in the TdIVW.
- VDDQ(max) may be extended to 0.67 V as an option in case the operating clock frequency is equal or less than 800 MHz.
- Pull up, pull down and ZQ calibration tolerance spec is valid only in normal VDDQ tolerance range (0.57 V - 0.65 V).

### 10.6.2 Single Ended Output Slew Rate

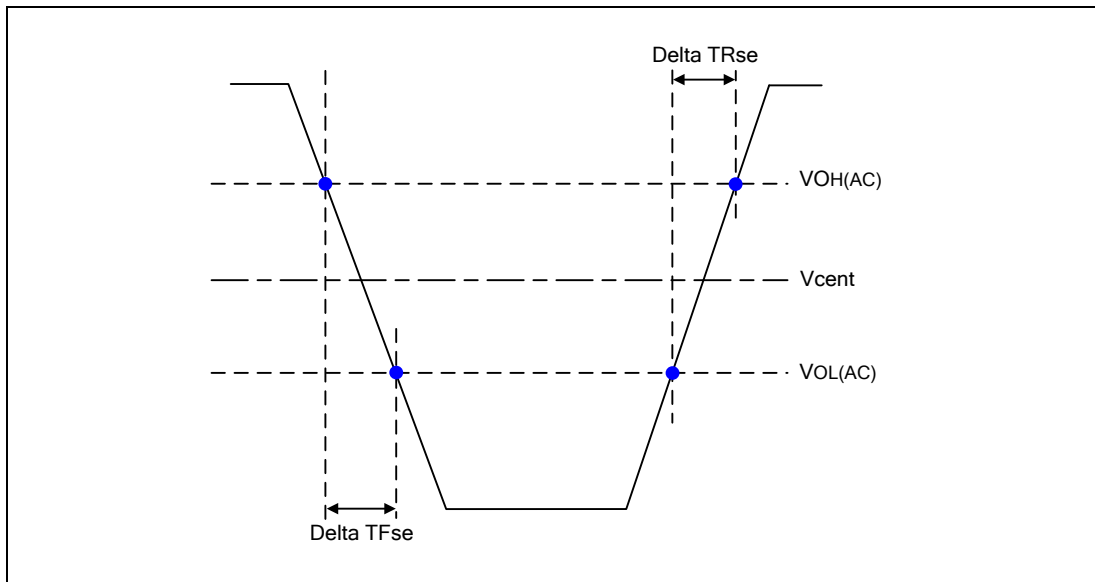


Figure 190 - Single Ended Output Slew Rate Definition

Table 138 - Output Slew Rate (Single-ended) for 0.6V VDDQ

| Parameter                                      | Symbol | Value             |                   | Units |
|------------------------------------------------|--------|-------------------|-------------------|-------|
|                                                |        | Min* <sup>1</sup> | Max* <sup>2</sup> |       |
| Single-ended Output Slew Rate (VOH = VDDQ*0.5) | SRQse  | 3.0               | 9                 | V/nS  |
| Output slew-rate matching Ratio (Rise to Fall) | -      | 0.8               | 1.2               | -     |

#### Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

#### Notes:

- Measured with output reference load.
- The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
- The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.2\*VOH(DC) and VOH(AC)=0.8\*VOH(DC).
- Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.



## 10.7 Differential Output Slew Rate

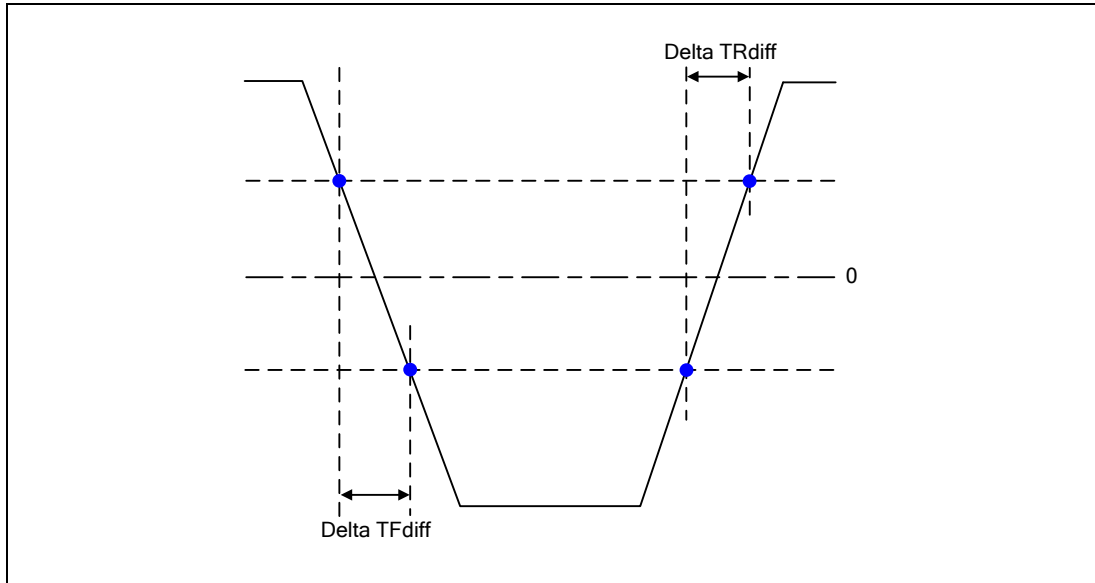


Figure 191 - Differential Output Slew Rate Definition

Table 139 - Differential Output Slew Rate for 0.6V VDDQ

| Parameter                                                  | Symbol  | Value |     | Units |
|------------------------------------------------------------|---------|-------|-----|-------|
|                                                            |         | Min   | Max |       |
| Differential Output Slew Rate ( $V_{OH} = V_{DDQ} * 0.5$ ) | SRQdiff | 6     | 18  | V/nS  |

### Description:

**SR:** Slew Rate

**Q:** Query Output (like in DQ, which stands for Data-in, Query-Output)

**diff:** Differential Signals

### Notes:

1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between  $V_{OL}(AC) = -0.8 * V_{OH}(DC)$  and  $V_{OH}(AC) = 0.8 * V_{OH}(DC)$ .
3. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.



## 10.8 VREF Specifications - LPDDR4X

### 10.8.1 CA Internal VREF Specifications for LPDDR4X

Table 140 contains the CA internal VREF specifications that will be characterized at the component level for compliance.

**Table 140 - CA Internal VREF Specifications**

| Parameter                       | Symbol           | Min    | Typ   | Max   | Unit | Notes   |
|---------------------------------|------------------|--------|-------|-------|------|---------|
| VREF Max operating point Range0 | VREF_max_R0      | -      | -     | 44.9% | VDDQ | 1, 11   |
| VREF Min operating point Range0 | VREF_min_R0      | 15%    | -     | -     | VDDQ | 1, 11   |
| VREF Max operating point Range1 | VREF_max_R1      | -      | -     | 62.9% | VDDQ | 1, 11   |
| VREF Min operating point Range1 | VREF_min_R1      | 32.9%  | -     | -     | VDDQ | 1, 11   |
| VREF Step size                  | VREF Step        | 0.50%  | 0.60% | 0.70% | VDDQ | 2       |
| VREF Set Tolerance              | VREF_set_tol     | -11    | 0     | 11    | mV   | 3, 4, 6 |
|                                 |                  | -1.1   | 0     | 1.1   | mV   | 3, 5, 7 |
| VREF Step Time                  | VREF_time-Short  | -      | -     | 100   | nS   | 8       |
|                                 | VREF_time_Middle | -      | -     | 200   | nS   | 12      |
|                                 | VREF_time-Long   | -      | -     | 250   | nS   | 9       |
|                                 | VREF_time_weak   | -      | -     | 1     | mS   | 13, 14  |
| VREF Valid tolerance            | VREF_val_tol     | -0.10% | 0.00% | 0.10% | VDDQ | 10      |

#### Notes:

- VREF DC voltage referenced to VDD2\_DC.
- VREF step size increment/decrement range. VREF at DC level.
- $VREF_{new} = VREF_{old} + n \cdot VREF_{step}$ ; n= number of steps; if increment use "+"; If decrement use "-".
- The minimum value of VREF setting tolerance =  $VREF_{new} - 11 \text{ mV}$ . The maximum value of VREF setting tolerance =  $VREF_{new} + 11 \text{ mV}$ . For  $n > 4$ .
- The minimum value of VREF setting tolerance =  $VREF_{new} - 1.1 \text{ mV}$ . The maximum value of VREF setting tolerance =  $VREF_{new} + 1.1 \text{ mV}$ . For  $n \leq 4$ .
- Measured by recording the min and max values of the VREF output over the range, drawing a straight line between those points and comparing all other VREF output settings to that line.
- Measured by recording the min and max values of the VREF output across 4 consecutive steps ( $n=4$ ), drawing a straight line between those points and comparing all other VREF output settings to that line.
- Time from MRS command to increment or decrement one step size for VREF.
- Time from MRS command to increment or decrement VREFmin to VREFmax or VREFmax to VREFmin change across the VREFCA Range in VREF voltage.
- Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VREF valid is to qualify the step times which will be characterized at the component level.
- DRAM range 0 or 1 set by MR12 OP[6].
- Time from MRS command to increment or decrement more than one step size up to a full range of VREF voltage within the same VREFCA range.
- Applies when VRCG high current mode is not enabled, specified by MR13 OP[3] = 0.
- VREF\_time\_weak covers all VREF(CA) Range and Value change conditions are applied to VREF\_time\_Short/Middle/Long.





### 10.8.2 DQ Internal VREF Specifications for LPDDR4X

Table 141 contains the DQ internal VREF specifications that will be characterized at the component level for compliance.

**Table 141 - DQ Internal VREF Specifications**

| Parameter                       | Symbol           | Min    | Typ   | Max   | Unit | Notes   |
|---------------------------------|------------------|--------|-------|-------|------|---------|
| VREF Max operating point Range0 | VREF_max_R0      | -      | -     | 44.9% | VDDQ | 1, 11   |
| VREF Min operating point Range0 | VREF_min_R0      | 15%    | -     | -     | VDDQ | 1, 11   |
| VREF Max operating point Range1 | VREF_max_R1      | -      | -     | 62.9% | VDDQ | 1, 11   |
| VREF Min operating point Range1 | VREF_min_R1      | 32.9%  | -     | -     | VDDQ | 1, 11   |
| VREF Step size                  | VREF Step        | 0.50%  | 0.60% | 0.70% | VDDQ | 2       |
| VREF Set Tolerance              | VREF_set_tol     | -11    | 0     | 11    | mV   | 3, 4, 6 |
|                                 |                  | -1.1   | 0     | 1.1   | mV   | 3, 5, 7 |
| VREF Step Time                  | VREF_time-Short  | -      | -     | 100   | nS   | 8       |
|                                 | VREF_time_Middle | -      | -     | 200   | nS   | 12      |
|                                 | VREF_time-Long   | -      | -     | 250   | nS   | 9       |
|                                 | VREF_time_weak   | -      | -     | 1     | mS   | 13, 14  |
| VREF Valid tolerance            | VREF_val_tol     | -0.10% | 0.00% | 0.10% | VDDQ | 10      |

**Notes:**

- VREF DC voltage referenced to VDDQ\_DC.
- VREF step size increment/decrement range. VREF at DC level.
- $VREF\_new = VREF\_old + n \cdot VREF\_step$ ; n= number of steps; if increment use "+"; If decrement use "-".
- The minimum value of VREF setting tolerance =  $VREF\_new - 11mV$ . The maximum value of VREF setting tolerance =  $VREF\_new + 11mV$ . For  $n > 4$ .
- The minimum value of VREF setting tolerance =  $VREF\_new - 1.1mV$ . The maximum value of VREF setting tolerance =  $VREF\_new + 1.1mV$ . For  $n \leq 4$ .
- Measured by recording the min and max values of the VREF output over the range, drawing a straight line between those points and comparing all other VREF output settings to that line.
- Measured by recording the min and max values of the VREF output across 4 consecutive steps( $n=4$ ), drawing a straight line between those points and comparing all other VREF output settings to that line.
- Time from MRS command to increment or decrement one step size for VREF.
- Time from MRS command to increment or decrement VREFmin to VREFmax or VREFmax to VREFmin change across the VREFDQ Range in VREF voltage.
- Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VREF valid is to qualify the step times which will be characterized at the component level.
- DRAM range 0 or 1 set by MR14 OP[6].
- Time from MRS command to increment or decrement more than one step size up to a full range of VREF voltage within the same VREFDQ range.
- Applies when VRCG high current mode is not enabled, specified by MR13 OP[3] = 0.
- VREF\_time\_weak covers all VREF(DQ) Range and Value change conditions are applied to VREF\_time\_Short/Middle/Long.



### 10.9 Power-up, Initialization, and Power-Off Procedure – LPDDR4X

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as the table below.

**Table 142 - MRS defaults settings – LPDDR4X**

| Item             | MRS          | Default Setting | Description                     |
|------------------|--------------|-----------------|---------------------------------|
| FSP-OP/WR        | MR13 OP[7:6] | 00B             | FSP-OP/WR[0] are enabled        |
| WLS              | MR2 OP[6]    | 0B              | Write Latency Set A is selected |
| WL               | MR2 OP[5:3]  | 000B            | WL = 4                          |
| RL               | MR2 OP[2:0]  | 000B            | RL = 6, nRTP=8                  |
| nWR              | MR1 OP[6:4]  | 000B            | nWR = 6                         |
| DBI-WR/RD        | MR3 OP[7:6]  | 00B             | Write & Read DBI are disabled   |
| CA ODT           | MR11 OP[6:4] | 000B            | CA ODT is disabled              |
| DQ ODT           | MR11 OP[2:0] | 000B            | DQ ODT is disabled              |
| VREF(CA) Setting | MR12 OP[6]   | 1B              | VREF(CA) Range[1] enabled       |
| VREF(CA) Value   | MR12 OP[5:0] | 011101B         | Range1: 50.3% of VDDQ           |
| VREF(DQ) Setting | MR14 OP[6]   | 1B              | VREF(DQ) Range[1] enabled       |
| VREF(DQ) Value   | MR14 OP[5:0] | 011101B         | Range1: 50.3% of VDDQ           |



## 10.10 On Die Termination for Command/Address Bus - LPDDR4X

ODT (On-Die Termination) is a feature of the LPDDR4X SDRAM that allows the SDRAM to turn on/off termination resistance for CK<sub>t</sub>, CK<sub>c</sub>, CS and CA[5:0] signals without the ODT control pin.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via Mode Register setting.

A simple functional representation of the DRAM ODT feature is shown in Figure 192.

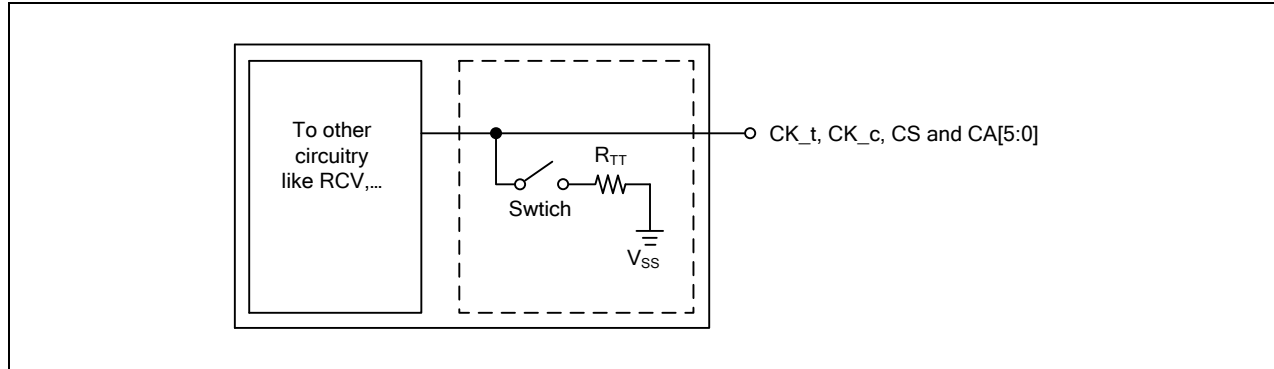


Figure 192 - Functional Representation of CA ODT

### 10.10.1 ODT Mode Register and ODT State Table

ODT termination values are set and enabled via MR11. The CA bus (CK<sub>t</sub>, CK<sub>c</sub>, CS, CA[5:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA is ODT disabled.

ODT is applied on the CA bus to the CK<sub>t</sub>, CK<sub>c</sub>, CS and CA[5:0] signals. Generally, only one termination load will be present even if multiple devices are sharing the command signals. In contrast to LPDDR4 where the ODT<sub>CA</sub> input is used in combination with mode registers, LPDDR4X uses mode registers exclusively to enable CA termination. Before enabling CA termination via MR11, all ranks should have appropriate MR22 termination settings programmed. In a multi rank system, the terminating rank should be trained first, followed by the non-terminating rank(s).

Table 143 - Command Bus ODT State – LPDDR4X

| ODTE-CA<br>MR11[6:4]   | ODTD-CA<br>MR22[5]  | ODTF-CK<br>MR22[3]  | ODTF-CS<br>MR22[4]  | ODT State<br>for CA | ODT State<br>for CK <sub>t</sub> /CK <sub>c</sub> | ODT State<br>for CS |
|------------------------|---------------------|---------------------|---------------------|---------------------|---------------------------------------------------|---------------------|
| Disabled* <sup>1</sup> | Valid* <sup>2</sup> | Valid* <sup>2</sup> | Valid* <sup>2</sup> | Off                 | Off                                               | Off                 |
| Valid* <sup>2</sup>    | 0                   | 0                   | 0                   | On                  | On                                                | On                  |
| Valid* <sup>2</sup>    | 0                   | 0                   | 1                   | On                  | On                                                | Off                 |
| Valid* <sup>2</sup>    | 0                   | 1                   | 0                   | On                  | Off                                               | On                  |
| Valid* <sup>2</sup>    | 0                   | 1                   | 1                   | On                  | Off                                               | Off                 |
| Valid* <sup>2</sup>    | 1                   | 0                   | 0                   | Off                 | On                                                | On                  |
| Valid* <sup>2</sup>    | 1                   | 0                   | 1                   | Off                 | On                                                | Off                 |
| Valid* <sup>2</sup>    | 1                   | 1                   | 0                   | Off                 | Off                                               | On                  |
| Valid* <sup>2</sup>    | 1                   | 1                   | 1                   | Off                 | Off                                               | Off                 |

**Notes:**

1. Default Value.
2. "Valid" means "0 or 1".



## 10.11 Core Timing - LPDDR4X

Table 144 - Core Timing for LPDDR4X

| Parameter                                    | Symbol | Min/Max | Data Rate       |      |      |      |      |      |      |      | Unit |
|----------------------------------------------|--------|---------|-----------------|------|------|------|------|------|------|------|------|
| Core Parameters                              |        |         | 533             | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4267 |      |
| Active bank-A to active bank-B* <sup>1</sup> | tRRD   | MIN     | max(10nS, 4nCK) |      |      |      |      |      |      |      | nS   |
| Four-bank ACTIVATE window                    | tFAW   | MIN     | 40              |      |      |      |      |      |      |      | nS   |

### Notes:

1. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
2. Devices supporting 4267 Mbps specification shall support these timings at lower data rates.

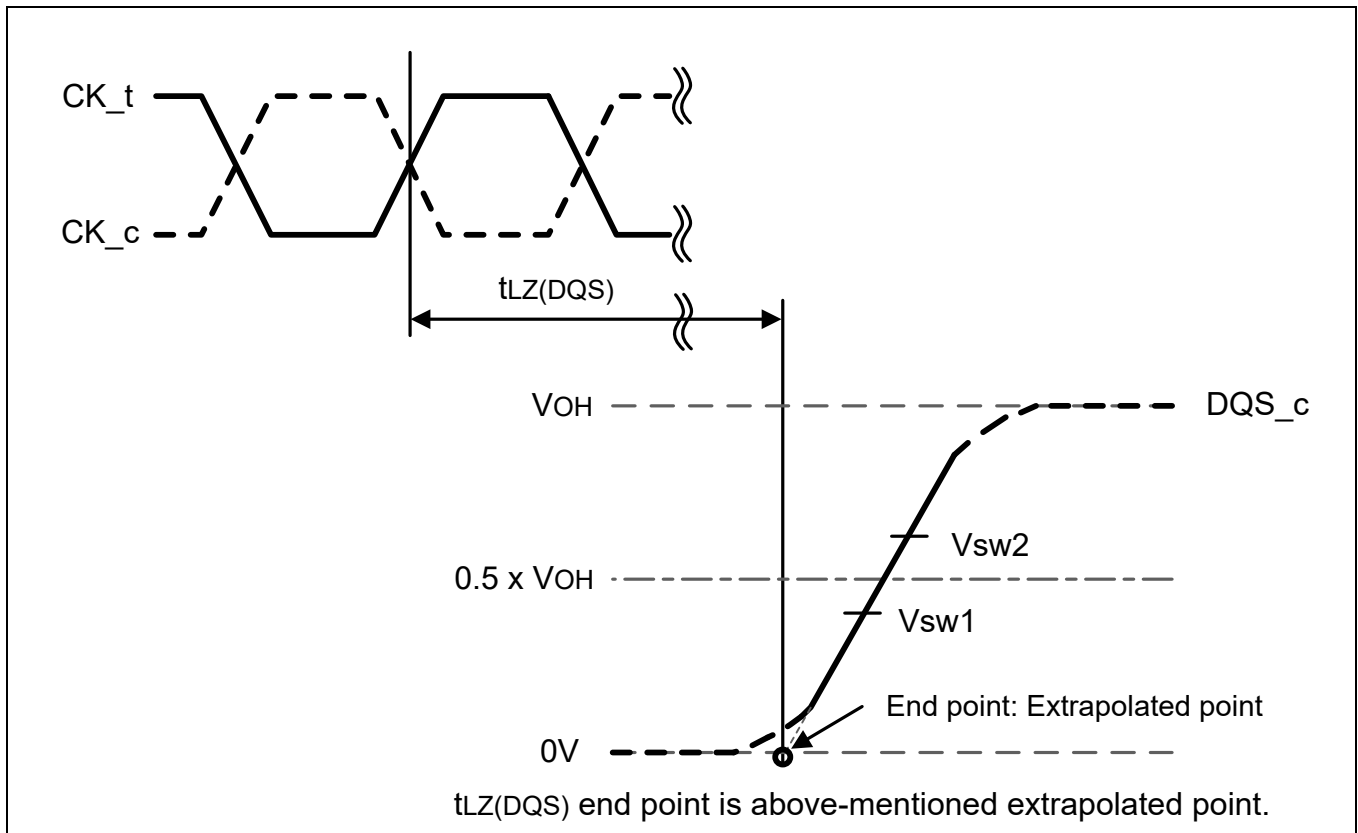
## 10.12 Burst READ Operation - LPDDR4X ATE Condition

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ).

This section shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single ended.

### 10.12.1 tLZ(DQS) and tHZ(DQS) Calculation for ATE (Automatic Test Equipment) – LPDDR4X

CK\_t - CK\_c crossing at 2nd CAS-2 of Read Command



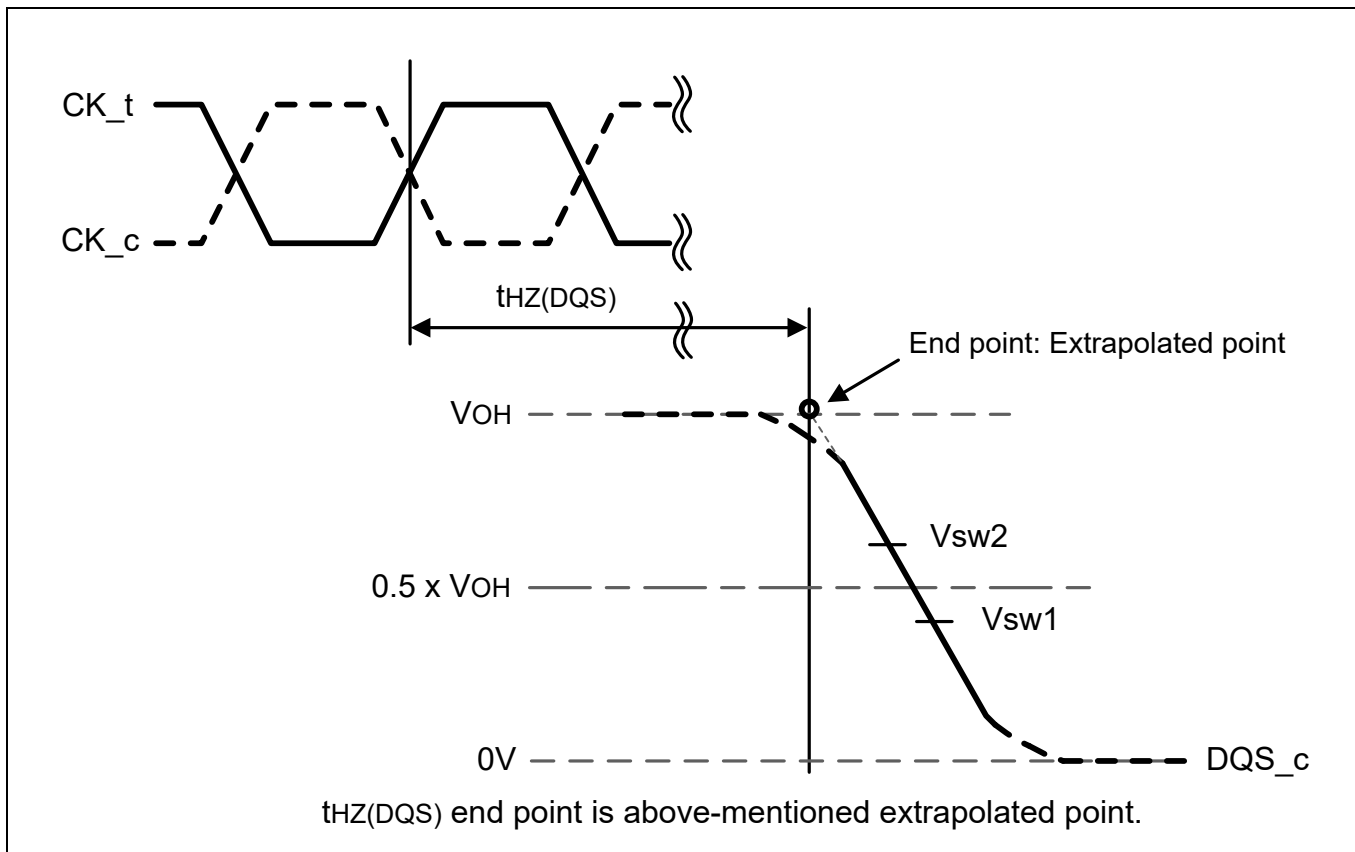
### Notes:

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH =  $VDDQ \times 0.5$ .
2. Termination condition for DQS\_t and DQS\_C = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual VOH value for tHZ and tLZ measurements.

Figure 193 - tLZ(DQS) method for calculating transitions and end point



CK\_t - CK\_c crossing at 2nd CAS-2 of Read Command



**Notes:**

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH =  $V_{DDQ} \times 0.5$ .
2. Termination condition for DQS\_t and DQS\_C = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.  
Use the actual VOH value for tHZ and tLZ measurements.

**Figure 194 - tHZ(DQS) method for calculating transitions and end point**

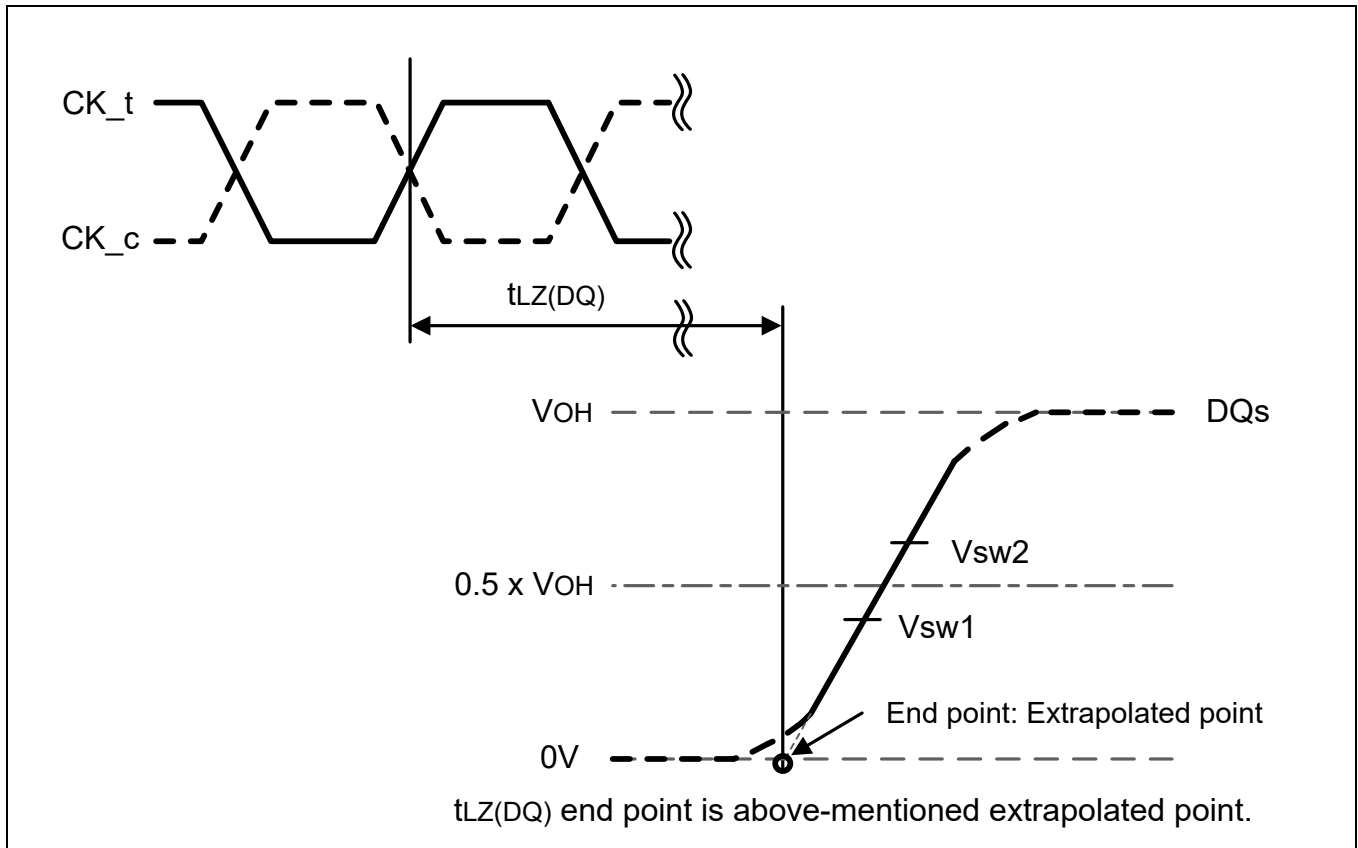
**Table 145 - Reference Voltage for tLZ(DQS), tHZ(DQS) Timing Measurements**

| Measured Parameter                        | Measured Parameter Symbol | Vsw1[V]   | Vsw2[V]   | Note |
|-------------------------------------------|---------------------------|-----------|-----------|------|
| DQS_c low-impedance time from CK_t, CK_c  | tLZ(DQS)                  | 0.4 x VOH | 0.6 x VOH |      |
| DQS_c high impedance time from CK_t, CK_c | tHZ(DQS)                  | 0.4 x VOH | 0.6 x VOH |      |



### 10.12.2 tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment) – LPDDR4X

CK\_t - CK\_c crossing at 2nd CAS-2 of Read Command



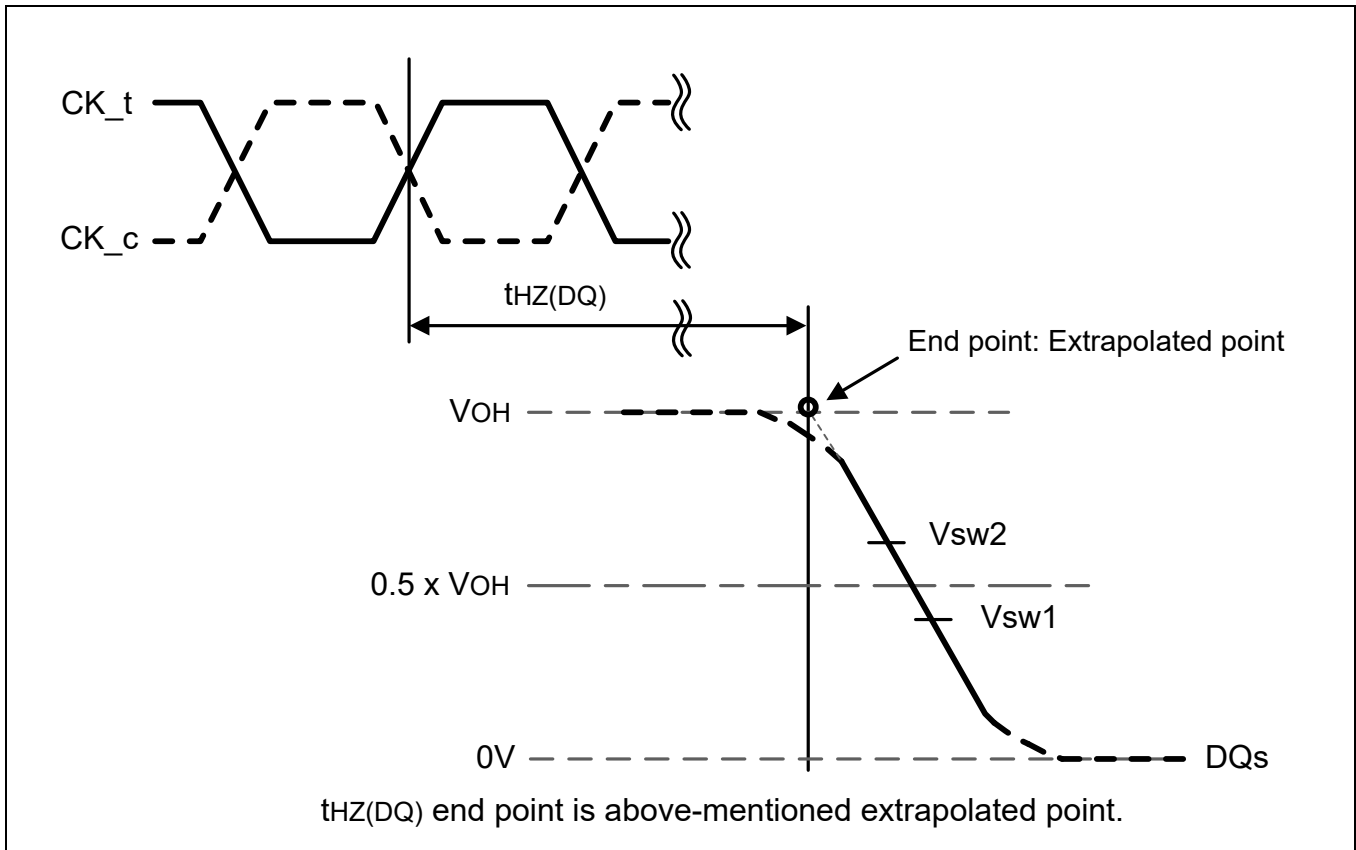
#### Notes:

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm,  $V_{OH} = V_{DDQ} \times 0.5$ .
2. Termination condition for DQ and DMI = 50ohm to VSSQ.
3. The  $V_{OH}$  level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.  
Use the actual  $V_{OH}$  value for tHZ and tLZ measurements.

**Figure 195 - tLZ(DQ) method for calculating transitions and end point**



CK\_t - CK\_c crossing at 2nd CAS-2 of Read Command



**Notes:**

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH =  $V_{DDQ} \times 0.5$ .
2. Termination condition for DQ and DMI = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.  
Use the actual VOH value for tHZ and tLZ measurements.

**Figure 196 - tHZ(DQ) method for calculating transitions and end point**

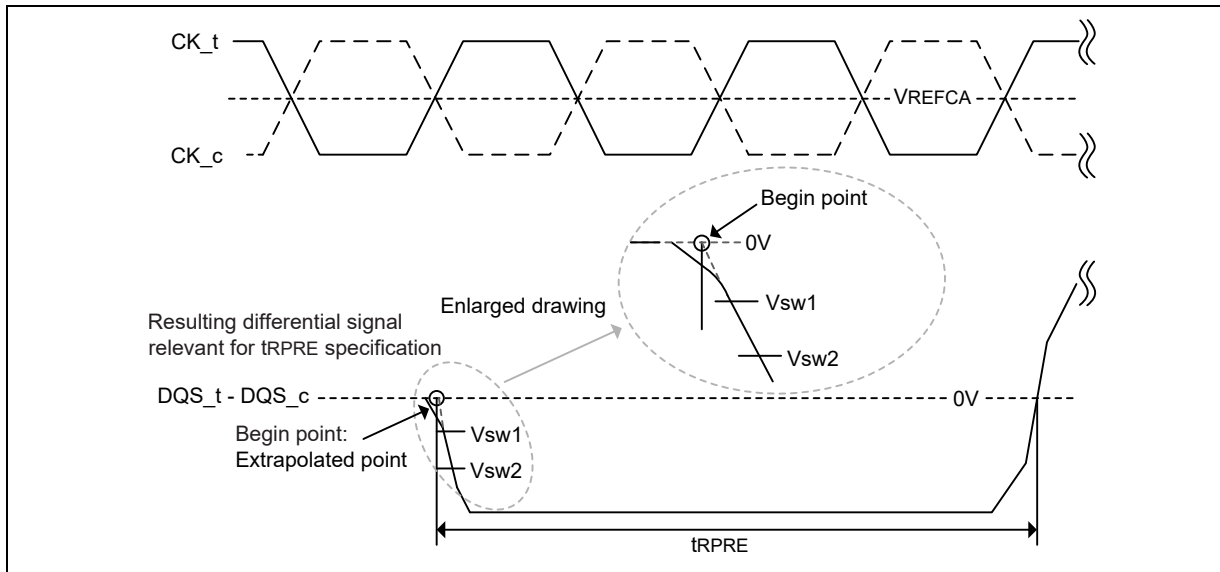
**Table 146 - Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements**

| Measured Parameter                     | Measured Parameter Symbol | Vsw1[V]   | Vsw2[V]   | Note |
|----------------------------------------|---------------------------|-----------|-----------|------|
| DQ low-impedance time from CK_t, CK_c  | tLZ(DQ)                   | 0.4 x VOH | 0.6 x VOH |      |
| DQ high impedance time from CK_t, CK_c | tHZ(DQ)                   | 0.4 x VOH | 0.6 x VOH |      |



### 10.12.3 tRPRE Calculation for ATE (Automatic Test Equipment) – LPDDR4X

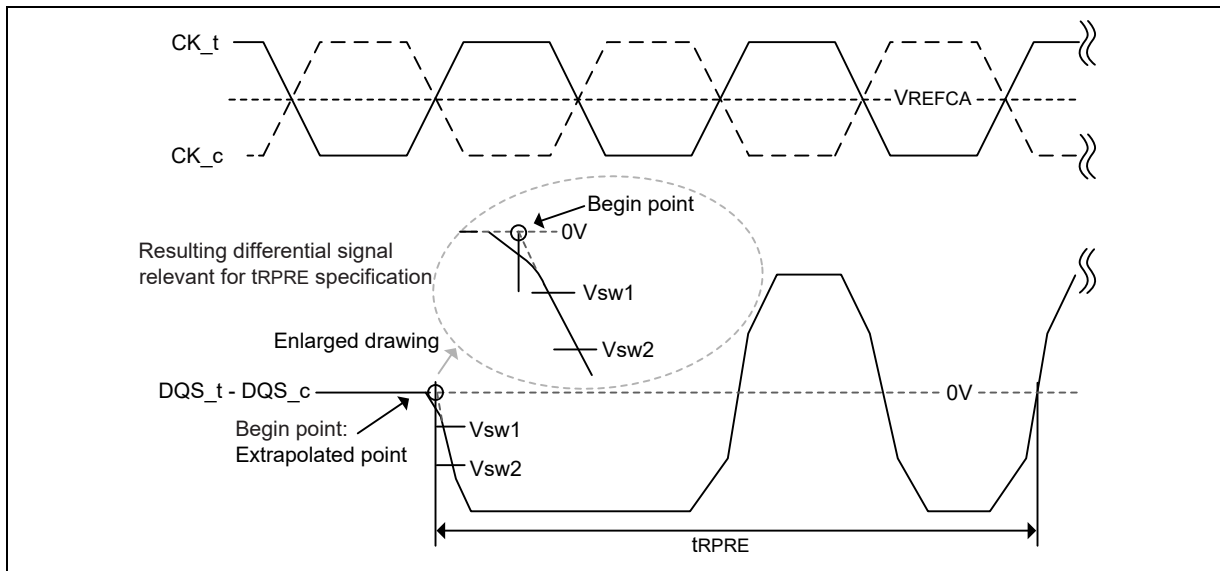
The method for calculating differential pulse widths for tRPRE is shown in Figure 197 and Figure 198, and Table 147.



**Notes:**

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH =  $V_{DDQ} \times 0.5$ .
2. Termination condition for DQS\_t, DQS\_c, DQ and DMI = 50ohm to VSSQ.
3. Preamble = Static.

**Figure 197 - Method for calculating tRPRE transitions and endpoints**



**Notes:**

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH =  $V_{DDQ} \times 0.5$ .
2. Termination condition for DQS\_t, DQS\_c, DQ and DMI = 50ohm to VSSQ.
3. Preamble = Toggle.

**Figure 198 - Method for calculating tRPRE transitions and endpoints**

**Table 147 - Reference Voltage for tRPRE Timing Measurements**

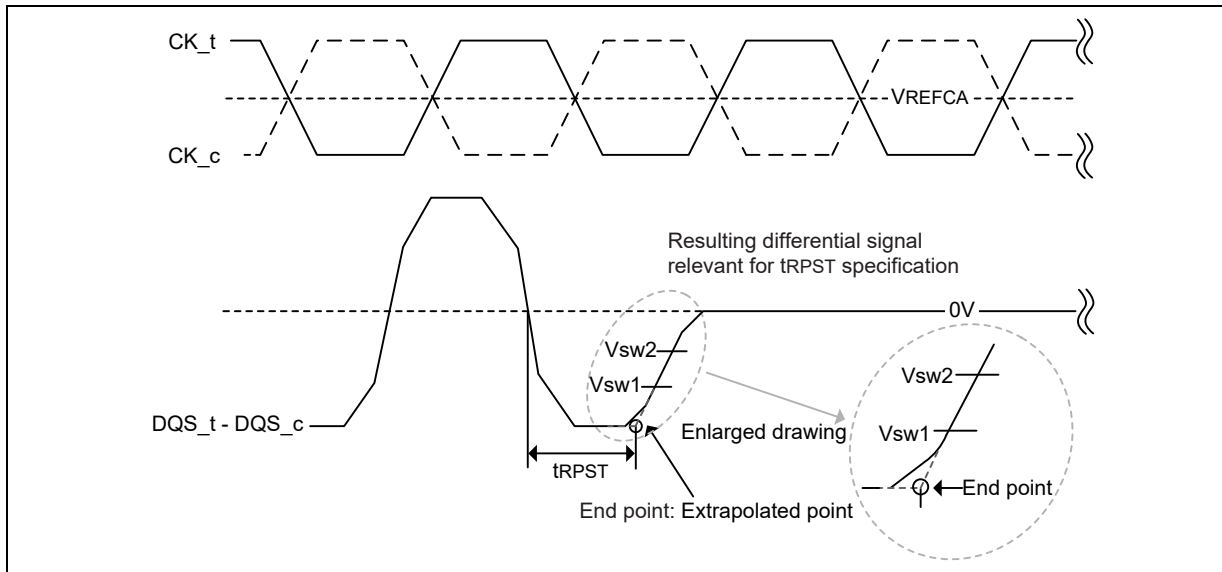
| Measured Parameter                      | Measured Parameter Symbol | Vsw1[V]             | Vsw2[V]             | Note |
|-----------------------------------------|---------------------------|---------------------|---------------------|------|
| DQS_t, DQS_c differential Read Preamble | tRPRE                     | $-(0.3 \times VOH)$ | $-(0.7 \times VOH)$ |      |





#### 10.12.4 tRPST Calculation for ATE (Automatic Test Equipment) – LPDDR4X

The method for calculating differential pulse widths for tRPST is shown in Figure 199 and Table 148.



##### Notes:

1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH =  $V_{DDQ} \times 0.5$ .
2. Termination condition for DQS\_t, DQS\_c, DQ and DMI = 50ohm to VSSQ.
3. Read Postamble: 0.5tCK.
4. The method for calculating differential pulse widths for 1.5 tCK Postamble is same as 0.5 tCK Postamble.

**Figure 199 - Method for calculating tRPST transitions and endpoints**

**Table 148 - Reference Voltage for tRPST Timing Measurements**

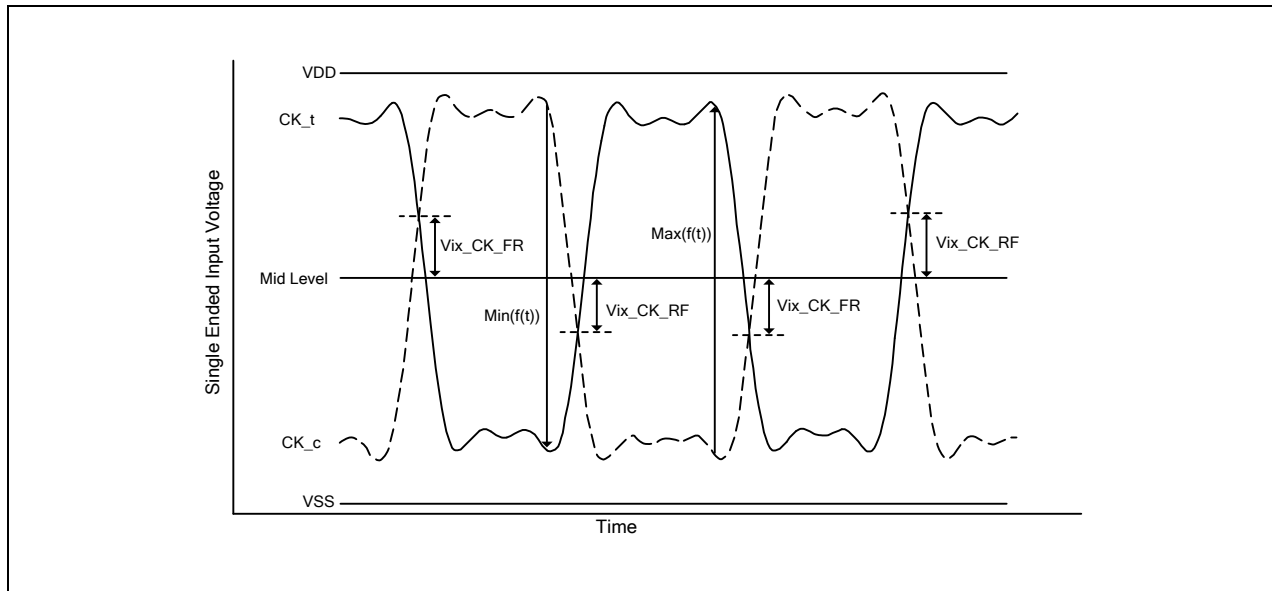
| Measured Parameter                       | Measured Parameter Symbol | Vsw1[V]                | Vsw2[V]                | Note |
|------------------------------------------|---------------------------|------------------------|------------------------|------|
| DQS_t, DQS_c differential Read Postamble | tRPST                     | $-(0.7 \times V_{OH})$ | $-(0.3 \times V_{OH})$ |      |



### 10.13 Differential Input Cross Point Voltage – LPDDR4X

#### 10.13.1 Differential Input Cross Point Voltage

The cross point voltage of differential input signals (CK<sub>t</sub>, CK<sub>c</sub>) are shown in Figure 200 and must meet the requirements in Table 149. The differential input cross point voltage V<sub>IX</sub> is measured from the actual cross point of true and complement signals to the mid level.



**Note:** 1. The base level of V<sub>ix\_CK\_FR/RF</sub> is V<sub>REFCA</sub> that is LPDDR4X SDRAM internal setting value by V<sub>REF</sub> Training.

**Figure 200 - Vix Definition (Clock)**

**Table 149 - Cross point voltage for differential input signals (Clock) – LPDDR4X**

| Parameter                                          | Symbol       | Data Rate |     |                |     |           |     | Unit | Note             |
|----------------------------------------------------|--------------|-----------|-----|----------------|-----|-----------|-----|------|------------------|
|                                                    |              | 1600/1867 |     | 2133/2400/3200 |     | 3733/4267 |     |      |                  |
|                                                    |              | Min       | Max | Min            | Max | Min       | Max |      |                  |
| Clock Differential input cross point voltage ratio | Vix_CK_ratio | -         | 25  | -              | 25  | -         | 25  | %    | 1, 2, 3, 4, 5, 6 |

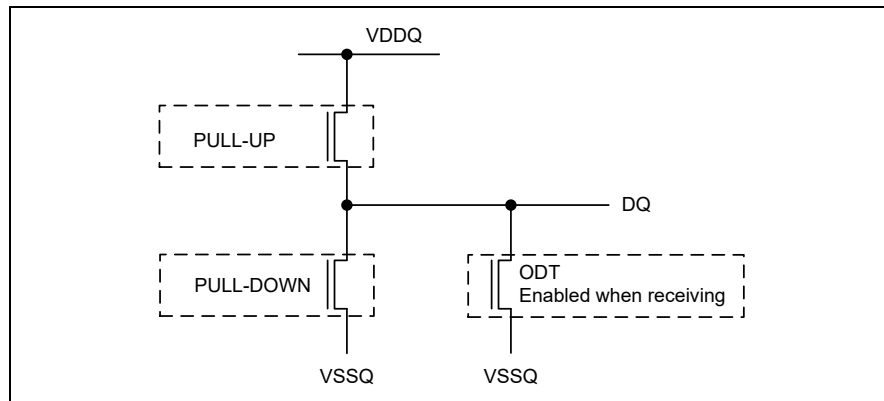
**Notes:**

- The requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.
- V<sub>ix\_CK\_Ratio</sub> is defined by this equation:  $V_{ix\_CK\_Ratio} = V_{ix\_CK\_FR} / |\text{Min}(f(t))|$ .
- V<sub>ix\_CK\_Ratio</sub> is defined by this equation:  $V_{ix\_CK\_Ratio} = V_{ix\_CK\_RF} / \text{Max}(f(t))$ .
- V<sub>ix\_CK\_FR</sub> is defined as delta between cross point (CK<sub>t</sub> fall, CK<sub>c</sub> rise) to Min(f(t))/2.
- V<sub>ix\_CK\_RF</sub> is defined as delta between cross point (CK<sub>t</sub> rise, CK<sub>c</sub> fall) to Max(f(t))/2.
- In LPDDR4X un-terminated case, CK mid-level is calculated as:  
High level = VDDQ, Low level = VSS, Mid-level = VDDQ/2.



### 10.14 LVSTL (Low Voltage Swing Terminated Logic) IO System for 0.6V VDDQ

LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in Figure 201.

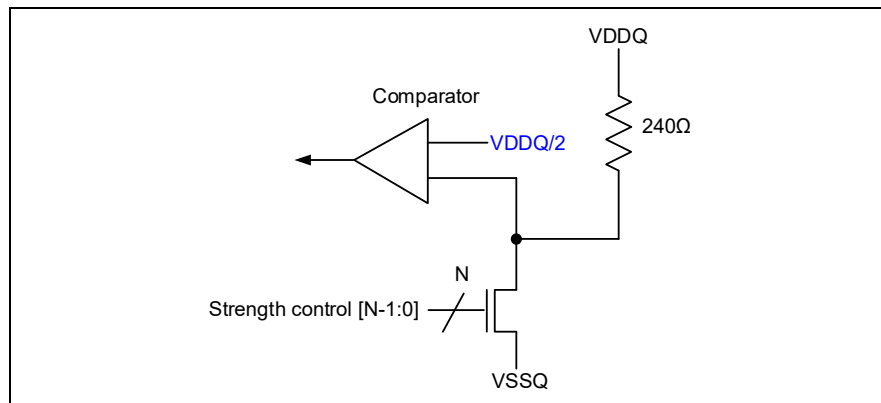


**Figure 201 - LVSTL I/O Cell**

To ensure that the target impedance is achieved the LVSTL I/O cell is designed to be calibrated as below procedure.

1. First calibrate the pull-down device against a 240  $\Omega$  resistor to VDDQ via the ZQ pin.

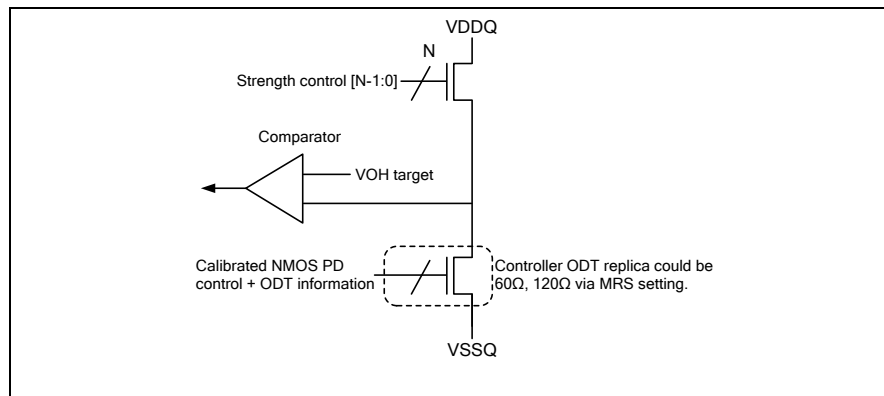
- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is less than  $V_{DDQ}/2$
- NMOS pull-down device is calibrated to 240  $\Omega$



**Figure 202 - Pull-down calibration for LPDDR4X**

2. Then calibrate the pull-up device against the calibrated pull-down device.

- Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS)
- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is greater than VOH target
- NMOS pull-up device is now calibrated to VOH target



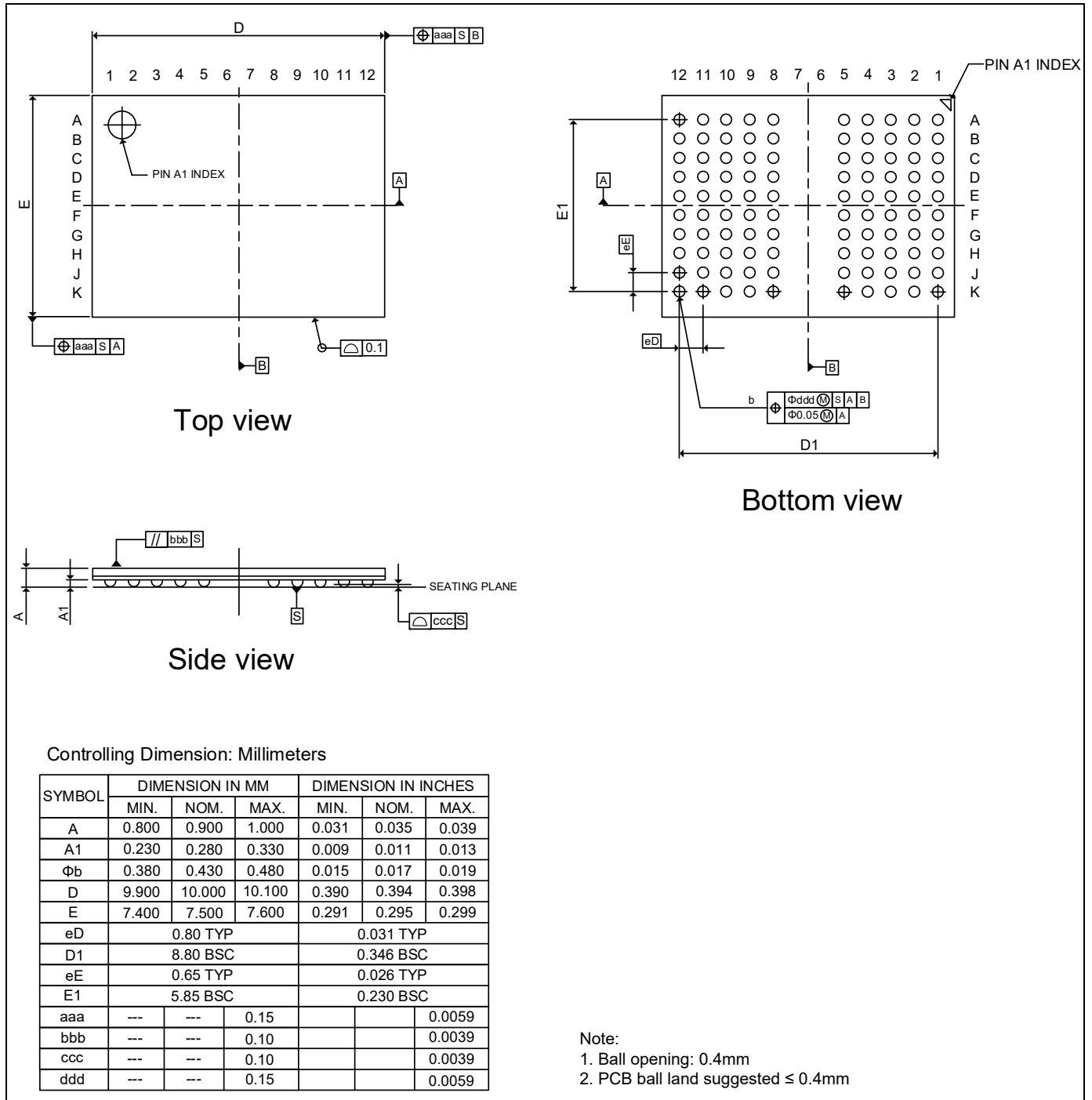
**Figure 203 - Pull-up calibration**



## 11. PACKAGE DIMENSIONS

### 11.1 VFBGA 100 Ball

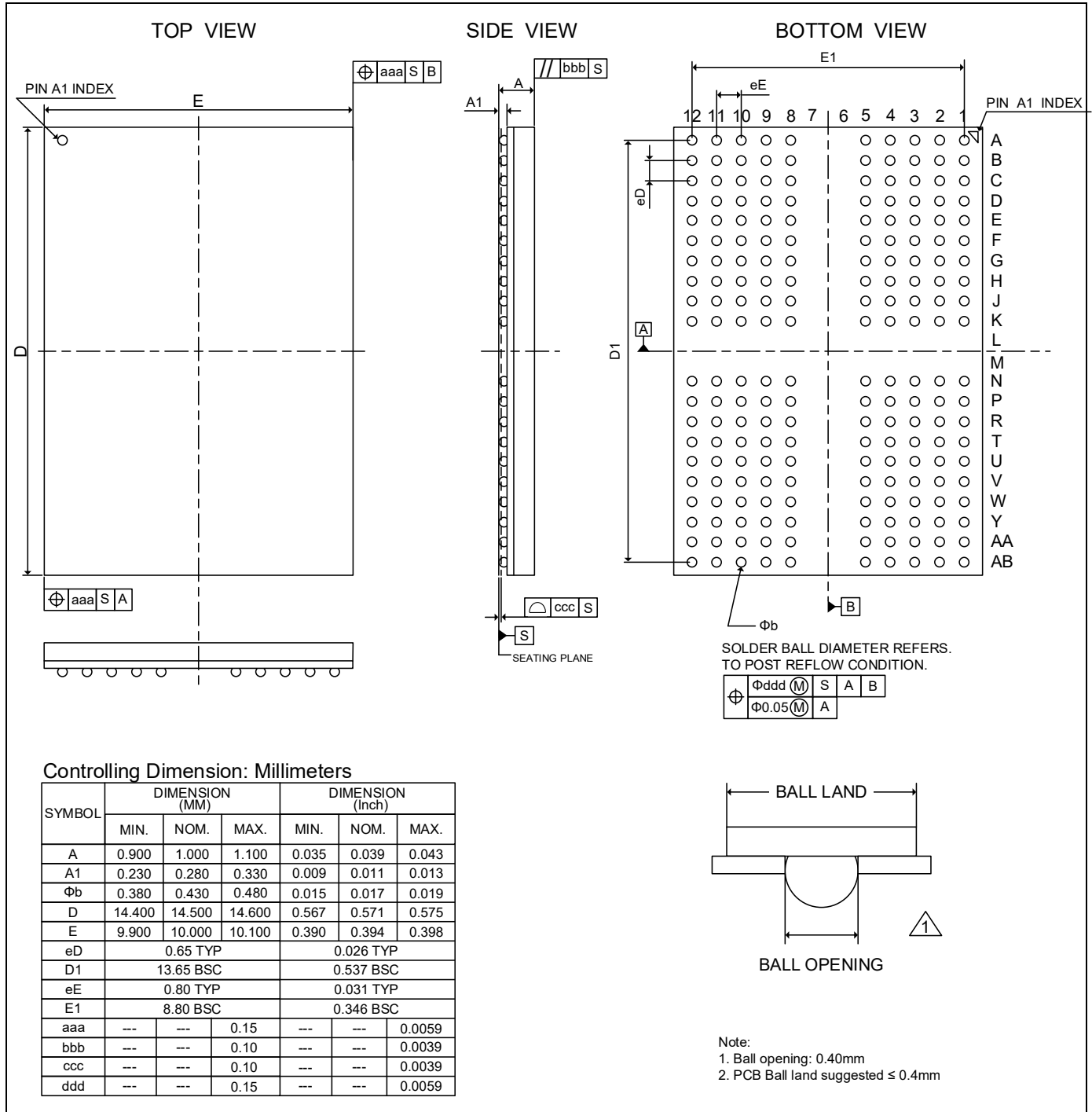
Package Outline VFBGA 100 Ball (10x7.5 mm<sup>2</sup>, Ø=0.4mm)





## 11.2 TFBGA 200 Ball

Package Outline TFBGA 200 Ball (10x14.5 mm<sup>2</sup>, Ball pitch: 0.8 x 0.65mm)



**12. REVISION HISTORY**

| VERSION | DATE          | PAGE | DESCRIPTION              |
|---------|---------------|------|--------------------------|
| A01-001 | Dec. 30, 2024 | All  | Initial formal datasheet |

*Please note that all data and specifications are subject to change without notice.  
All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.*

*Publication Release Date: Dec. 30, 2024  
Revision: A01-001*