ULTRALOW-POWER 100-mA LOW DROPOUT LINEAR REGULATORS

Check for Samples: TPS76901-EP

FEATURES

- **100-mA Low-Dropout Regulator**
- **Available in Adjustable Versions**
- **Only 335-µA Quiescent Current With 100 mA at 150°C**
- **1-µA Quiescent Current in Standby Mode**
- **Dropout Voltage Typically 71 mV at 100 mA**
- **Over Current Limitation**

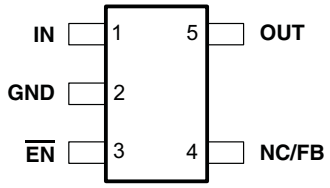
APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/150°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments' high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

DBV PACKAGE
(TOP VIEW)



(1) Custom temperature ranges available

DESCRIPTION

The TPS76901 low-dropout (LDO) voltage regulator offers the benefits of low dropout voltage, ultralow-power operation, and miniaturized packaging. This regulator features low dropout voltages and ultralow quiescent current compared to conventional LDO regulators. The TPS76901 is ideal for micropower operations and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual PNP pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low, and is directly proportional to the load current. Since the PMOS pass element is a voltage-driven device, the quiescent current is ultralow (28 µA maximum) and is stable over the entire range of output load current (0 mA to 100 mA). Intended for use in portable systems such as laptops and cellular phones, the ultralow-dropout voltage feature and ultralow-power operation result in a significant increase in system battery operating life.

The TPS76901 also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 µA, typical at T_J = 25°C. The TPS76901 is a variable version programmable over the range of 1.2 V to 4.5 V.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

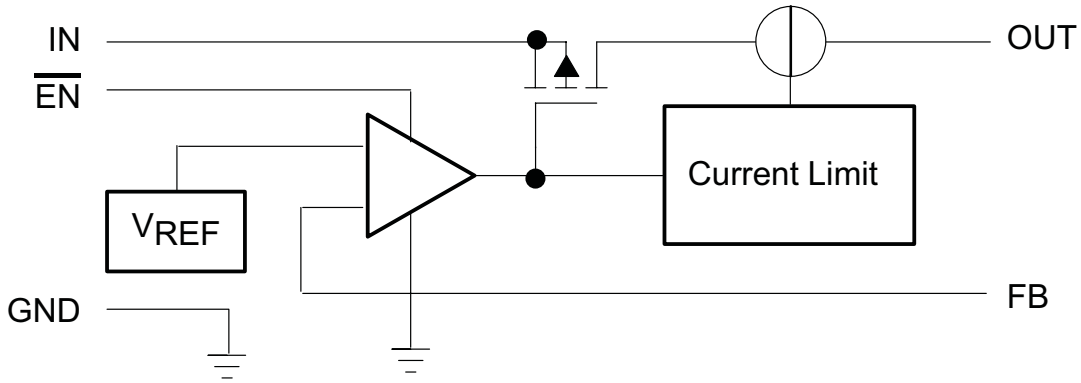
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 150°C	DBV	TPS76901SDBVTEP	PCFS

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{REF}	Input voltage range(2)	–0.3 to 13.5	V
	Voltage range at $\overline{EN}$	–0.3 to V_I + 0.3	V
	Voltage on OUT, FB	7	V
	Peak output current	Internally limited	
	ESD rating, HBM	2	kV
	Continuous total power dissipation	See Dissipation Ratings Table	
T_J	Operating virtual junction temperature range	–55 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL CHARACTERISTICS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C
Low K(1)	DBV	65.8 °C/W	259 °C/W	3.9 mW/°C
High K(2)	DBV	65.8 °C/W	180 °C/W	5.6 mW/°C

(1) The JEDEC Low K (1s) board design used to derive this data was a 3-inch x 3-inch, two layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC High K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input votlage(1)	5		10	V
V_O	Ouput voltage range	1.2		4.5	V
I_O	Continuous output current(2)	0		100	mA
T_J	Operating junction temperature	–55		150	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following formula:
$V_I(min) = V_O(max) + V_{DO}(max\ load)$.
(2) Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage (10 µA to 100 mA load)(1)	12. V ≤ V_O ≤ 4.5 V	T_J = 25°C		V_O		V
			T_J = –55°C to 150°C	0.97V_O		1.03V_O	
I_Q	Quiescent Current (GND current)(1) (2)	$\overline{EN}$ = 0 V, 0 mA < I_O < 100 mA	T_J = 25°C		17		µA
		$\overline{EN}$ = 4 V, I_O = 100 mA	T_J = –55°C to 150°C			28	
	Load regulation	$\overline{EN}$ = 0 V, I_O = 0 to 100 mA	T_J = 25°C		12		mV
			T_J = 150°C		13.5		
	Output voltage line regulation ($\Delta V_O/V_O$)(2)	5 V ≤ V_I ≤ 10 V(1)	T_J = 25°C		0.04		%
			T_J = –55°C to 150°C			0.1	
V_N	Output noise voltage	BW = 300 Hz to 50 kHz, C_O = 10 µF	T_J = 25°C		190		µVms
	Output current limit	V_O = 0 V(1)	T_J = 25°C		350		mA
			T_J = –55°C to 150°C			750	
I_{STDBY}	Standby current	$\overline{EN}$ = V_I, 5 V ≤ V_I ≤ 10 V	T_J = 25°C		1		µA
			T_J = –55°C to 150°C			2.4	
I_{FB}	FB input current	FB = 1.18 V	T_J = –55°C to 150°C	–1		1	µA
V_{IH}	High level enable input voltage	5 V ≤ V_I ≤ 10 V	T_J = 25°C	1.7			V
V_{IL}	Low level enable input voltage	5 V ≤ V_I ≤ 10 V	T_J = 25°C			0.9	V
			T_J = 150°C		0.75		
PSRR	Power supply ripple rejection	f = 1 kHz, CO = 10 µF(1)	T_J = 25°C		60		dB
I_{IN}	Input current	$\overline{EN}$ = 0 V	T_J = –55°C to 150°C	–1	0	1	µA
		$\overline{EN}$ = V_I		–1		1	

(1) Minimum IN operating voltage is 5V. Maximum IN voltage 10 V, minimum output current 10 µA, maximum output current 100 mA.
(2) Line Regulation (%) = (ΔV_{OUT}) / (ΔV_{IN}) x 100

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
IN	1	I	Input
GND	2	-	Ground
$\overline{EN}$	3	I	Enable
FB	4	I	Feedback
OUT	5	O	Output

TYPICAL CHARACTERISTICS

V_{OUT} VS TEMPERATURE (V_{IN} = 5 V , Load = 100 mA)

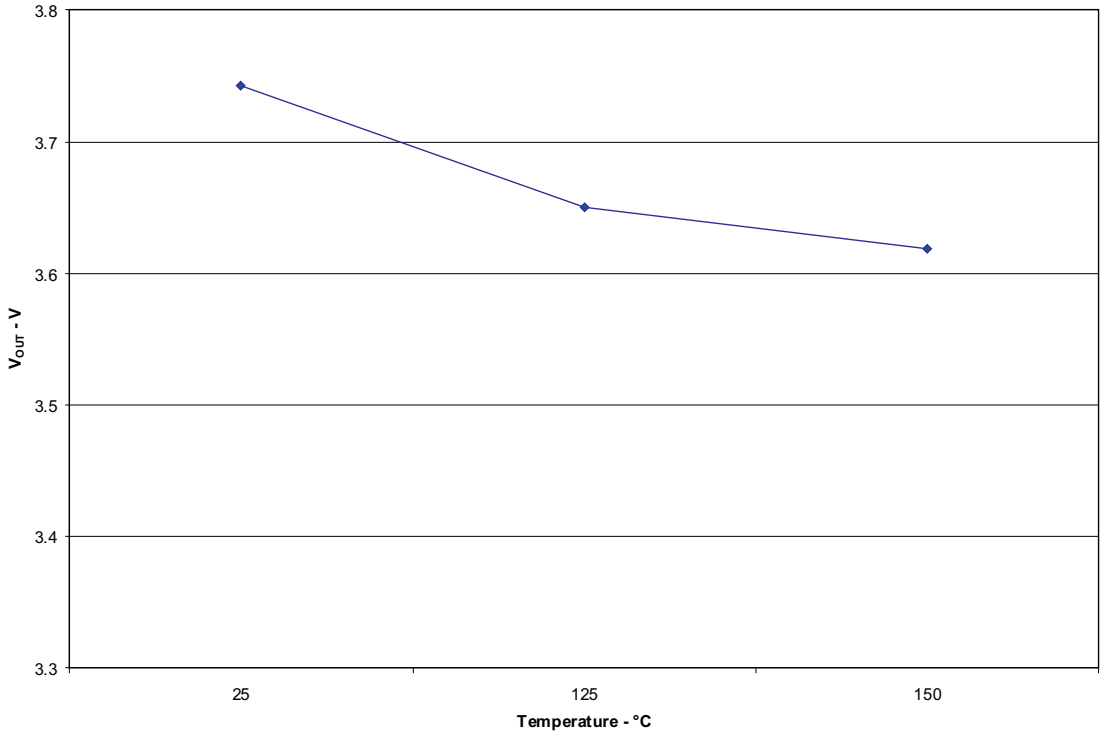


Figure 1.

TYPICAL CHARACTERISTICS (continued)

OUTPUT IMPEDANCE vs FREQUENCY

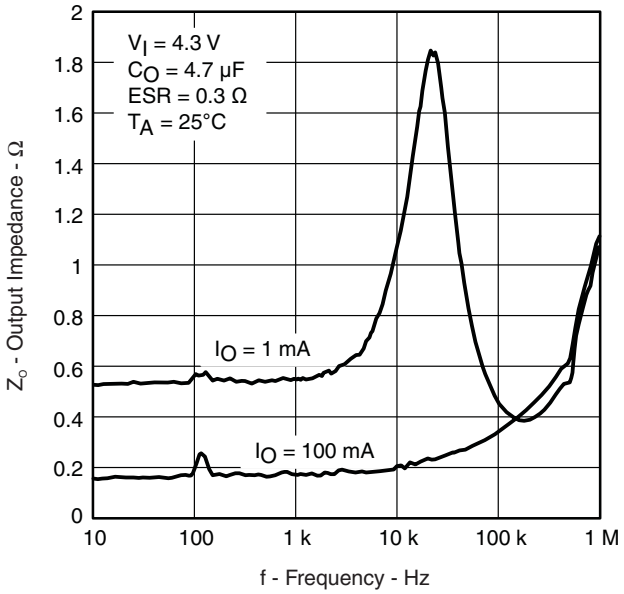


Figure 2.

LDO STARTUP TIME

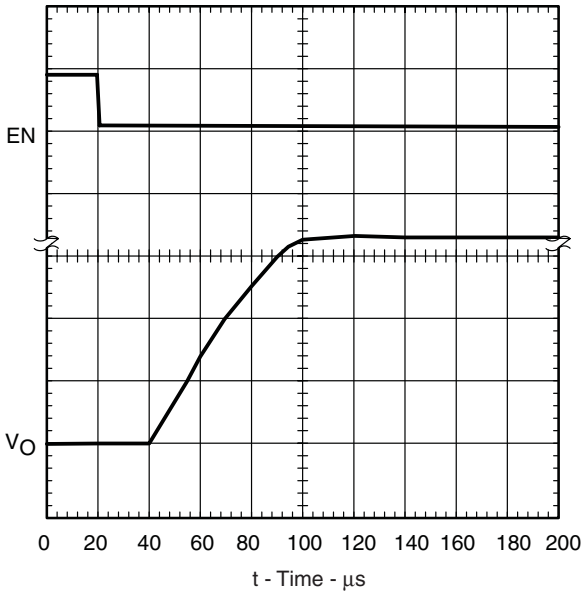


Figure 3.

TYPICAL CHARACTERISTICS (continued)

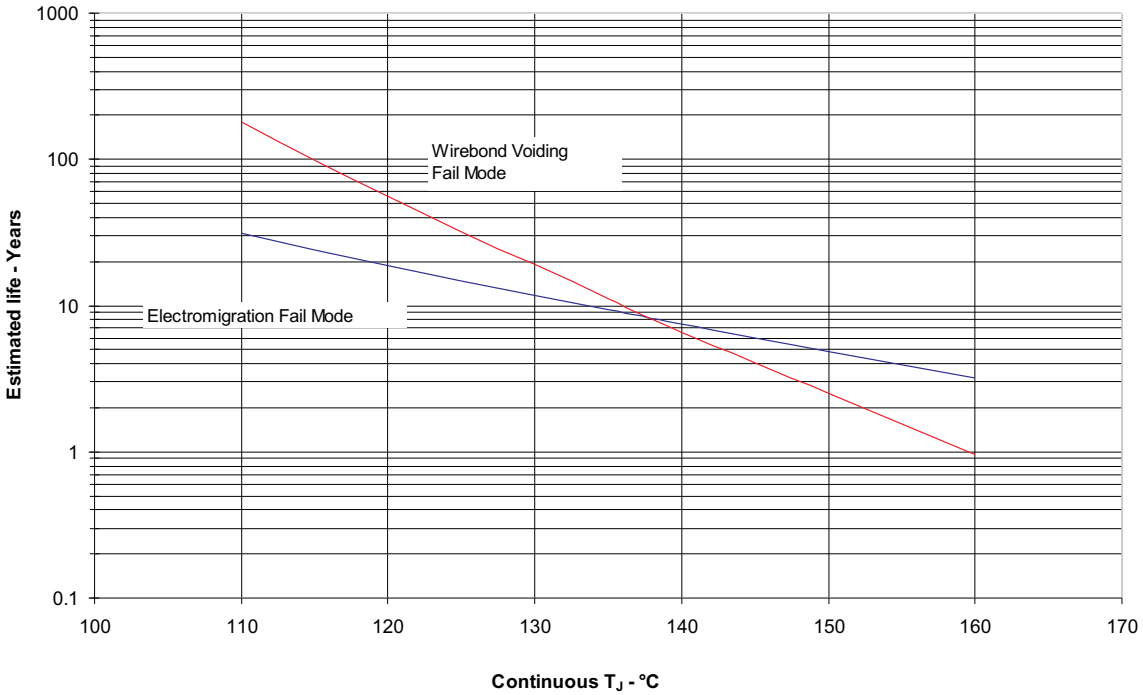


Figure 4. TPS76901SDBVTEP Operating Life Derating Chart

Note:

1. See datasheet for absolute maximum and minimum recommended operating conditions.
2. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

APPLICATION INFORMATION(1)

The TPS76901 low-dropout (LDO) regulator has been optimized for use in battery-operated equipment. It features extremely low dropout voltages, low quiescent current (17 µA nominally), and enables inputs to reduce supply currents to 1 µA when the regulators are turned off.

DEVICE OPERATION

The TPS76901 uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS pass element is a voltage-controlled device and, unlike a PNP transistor, it does not require increased drive current as output current increases. Supply current in the TPS76901 is essentially constant from no load to maximum load.

Current limiting prevents damage by excessive output current. The device switches into a constant-current mode at approximately 350 mA; further load reduces the output voltage instead of increasing the output current. The PMOS pass element includes a back gate diode that conducts reverse current when the input voltage level drops below the output voltage level.

A voltage of 1.7 V or greater on the EN input will disable the TPS76901 internal circuitry, reducing the supply current to 1 µA. A voltage of less than 0.9 V on the EN input will enable the TPS76901 and will enable normal operation to resume. The EN input does not include any deliberate hysteresis, and it exhibits an actual switching threshold of approximately 1.5 V.

A typical application circuit is shown in Figure 5.

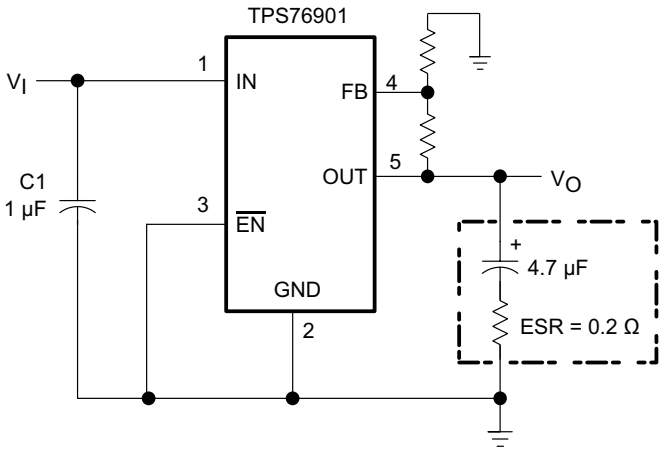


Figure 5. Typical Application Circuit

EXTERNAL CAPACITOR REQUIREMENTS

Although not required, a 0.047-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS76901, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS76901 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 µF. The ESR (equivalent series resistance) of the capacitor should be between 0.2 Ω and 10 Ω. to ensure stability. Capacitor values larger than 4.7 µF are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7 µF are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7-µF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may thus require the addition of a low value series resistor to ensure stability.

(1) Application information is provided for commercial temperature as a reference and not for high temperature.

Table 1. CAPACITOR SELECTION

PART NO.	MANUFACTURER	VALUE	MAX ESR(1)	SIZE (H x L x W)(1)
T494B475K016AS	KEMET	4.7 µF	1.5 Ω	1.9 x 3.5 x 2.8
195D106x0016x2T	SPRAGUE	10 µF	1.5 Ω	1.3 x 7.0 x 2.7
695D106x003562T	SPRAGUE	10 µF	1.3 Ω	2.5 x 7.6 x 2.5
TPSC475K035R0600	AVX	4.7 µF	0.6 Ω	2.6 x 6.0 x 3.2

(1) Size is in mm. ESR is maximum resistance in Ohms at 100 kHz and T_A = 25°C. Contact manufacturer for minimum ESR values.

OUTPUT VOLTAGE PROGRAMMING

The output voltage of the TPS76901 adjustable regulator is programmed using an external resistor divider as shown in Figure 6. The output voltage is calculated using:

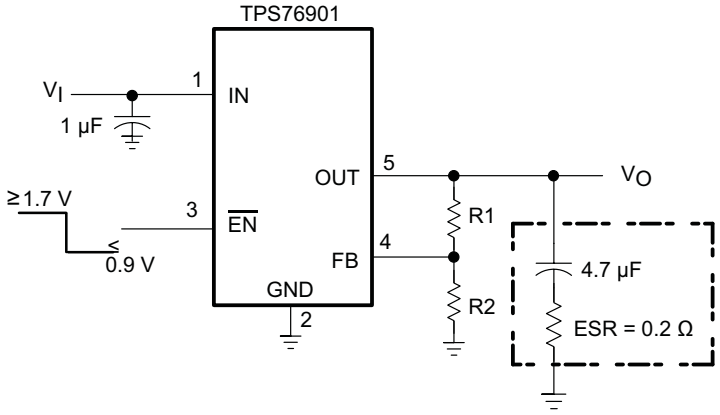
$$V_O = V_{REF} \bullet \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where:

V_{REF} = 1.127 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 7-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{REF}} - 1\right) \bullet R2 \quad (2)$$



Note:

1. The above calculations hold good for room temperature values only.

Figure 6. Adjustable LDO Reulator Programming

REGULATOR PROTECTION

The TPS76901 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS76901 features internal current limiting protection. During normal operation, the TPS76901 limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the over current condition ends.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76901SDBVTEP	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	PCFS	Samples
V62/10607-01XE	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	PCFS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

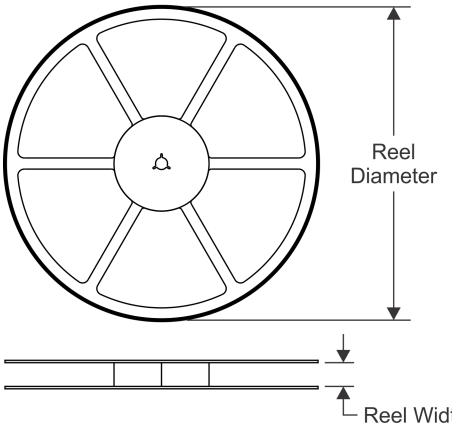
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS76901-EP :

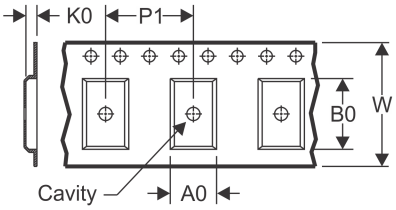
NOTE: Qualified Version Definitions:

TAPE AND REEL INFORMATION

REEL DIMENSIONS

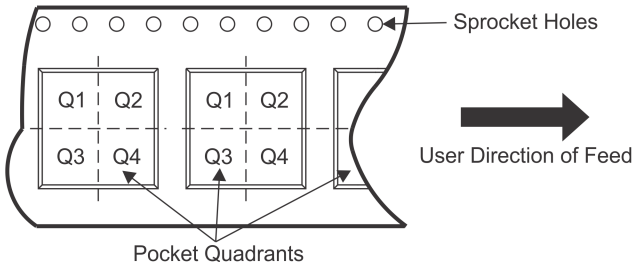


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

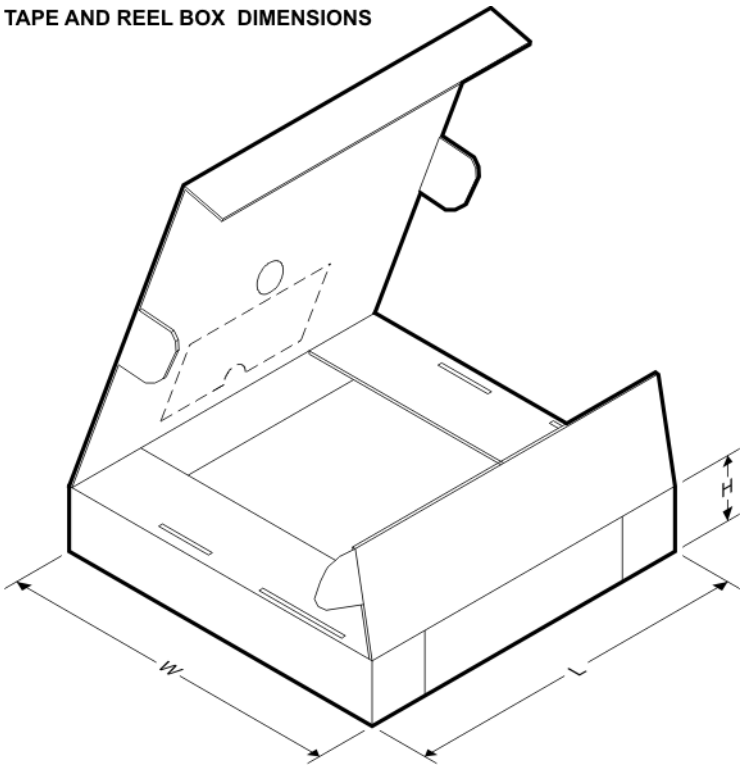
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76901SDBVTEP	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

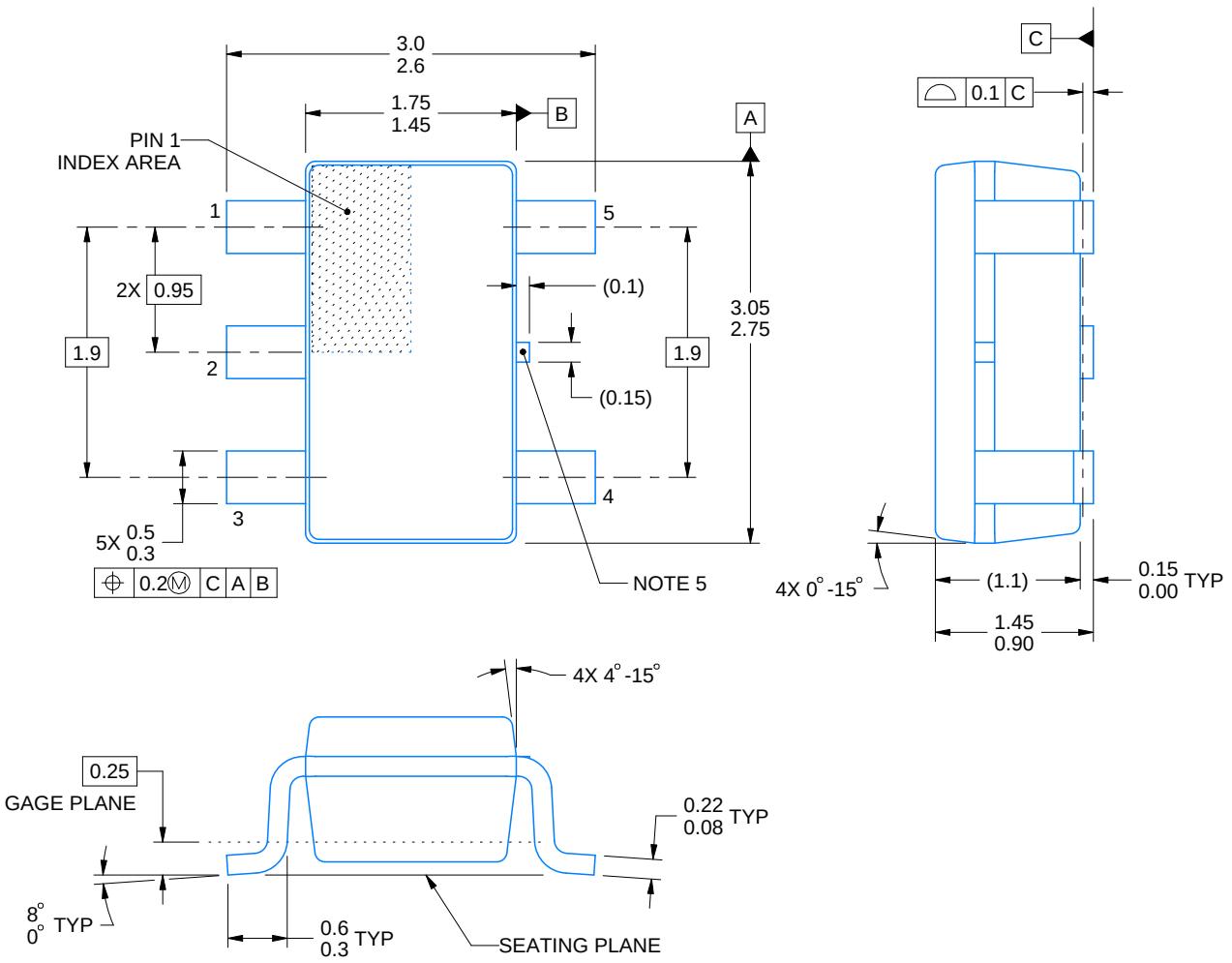
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76901SDBVTEP	SOT-23	DBV	5	250	182.0	182.0	20.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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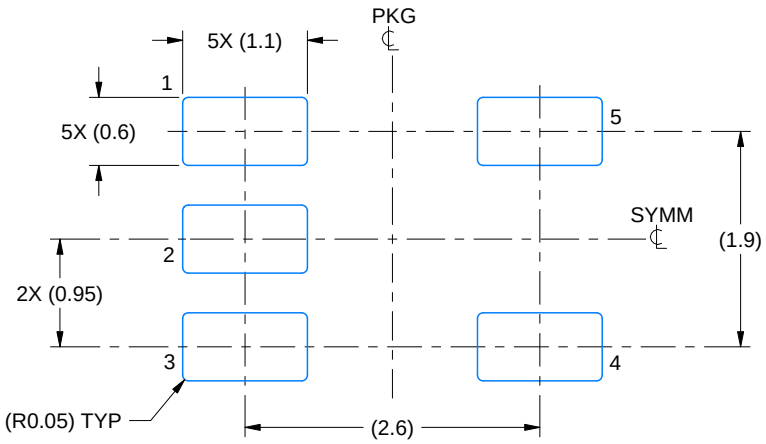
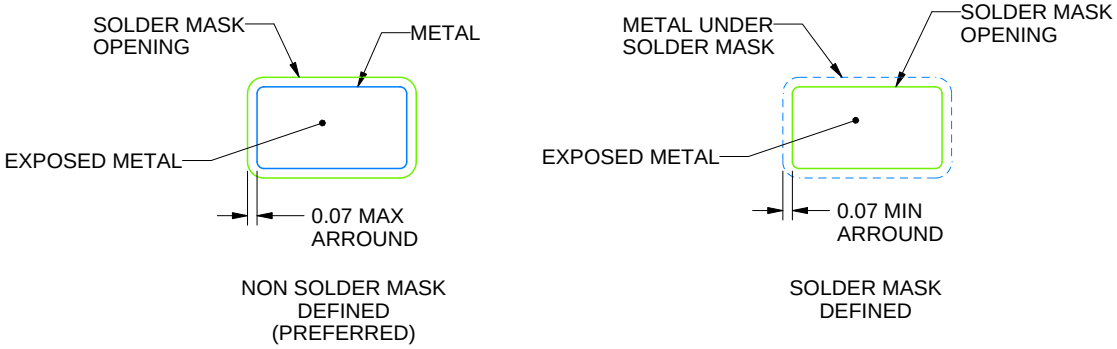
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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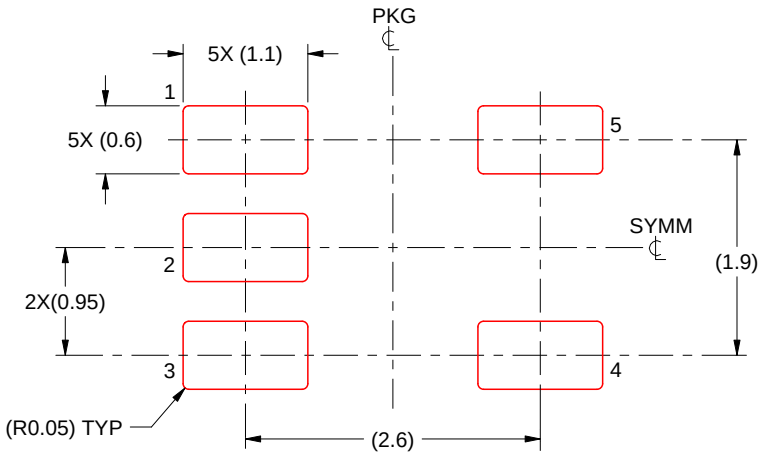
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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