

Features

- Very high speed
 - 55 ns
- Wide voltage range
 - 2.2 V to 3.6 V
- Ultra-low standby power
 - Typical standby current: 8 μA
 - Maximum standby current: 48 μA
- Ultra-low active power
 - Typical active current: 15 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2 , and $\overline{OE}$ features
- Automatic Power Down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 48-ball FBGA package

Functional Description

CY62187EV30 is a high-performance CMOS static RAM organized as 4M words by 16 bits. This device features an advanced circuit design to provide ultra-low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular phones.

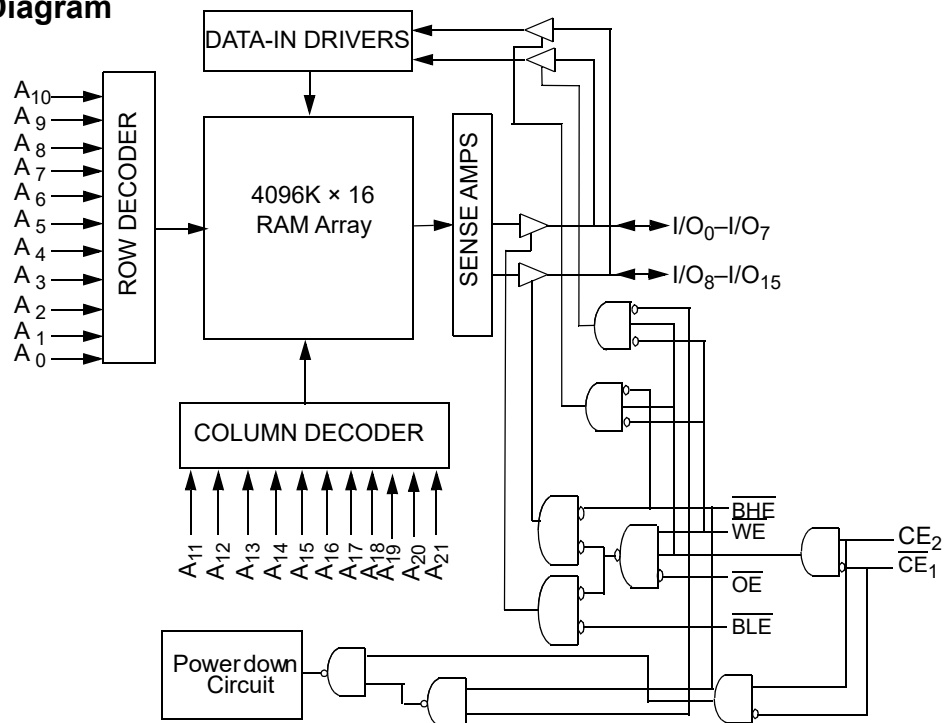
The device also has an Automatic Power Down feature that significantly reduces power consumption by 99 percent when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a High-Z state when: deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation (CE_1 LOW, CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{21}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{21}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. If $\overline{BLE}$ is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7 . If $\overline{BHE}$ is LOW, then data from the memory appears on I/O_8 to I/O_{15} . See the [Truth Table on page 12](#) for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

Logic Block Diagram

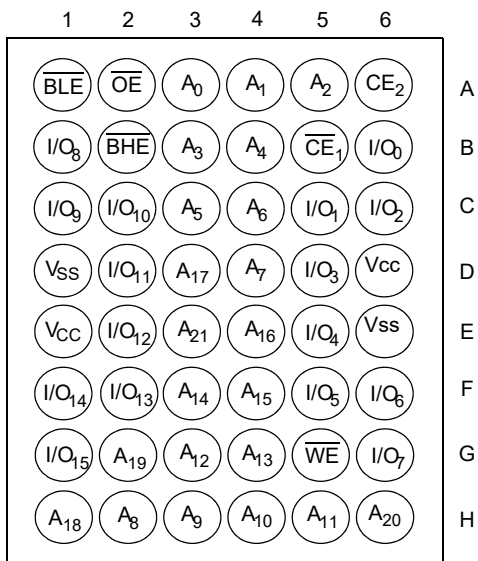


Contents

Pin Configuration	4	Ordering Information	13
Product Portfolio	4	Ordering Code Definitions	13
Maximum Ratings	5	Package Diagram	14
Operating Range	5	Acronyms	15
Electrical Characteristics	5	Document Conventions	15
Capacitance	6	Units of Measure	15
Thermal Resistance	6	Document History Page	16
AC Test Loads and Waveforms	6	Sales, Solutions, and Legal Information	20
Data Retention Characteristics	7	Worldwide Sales and Design Support	20
Data Retention Waveform	7	Products	20
Switching Characteristics	8	PSoC® Solutions	20
Switching Waveforms	9	Cypress Developer Community	20
Truth Table	12	Technical Support	20

Pin Configuration

Figure 1. 48-ball FBGA pinout



Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
					f = 1 MHz		f = f _{Max}			
	Min	Typ ^[1]	Max		Typ ^[1]	Max	Typ ^[1]	Max	Typ ^[1]	Max
CY62187EV30LL	2.2	3.0	3.6	55	15	38	45	55	8	48

Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature -65 °C to +150 °C

Ambient Temperature
with Power Applied -55 °C to +125 °C

Supply Voltage
to Ground Potential -0.3 V to $V_{CC(max)}$ + 0.3 V

DC Voltage Applied to Outputs
in High Z State ^[2, 3] -0.3 V to $V_{CC(max)}$ + 0.3 V

DC Input Voltage ^[2, 3] -0.3 V to $V_{CC(max)}$ + 0.3 V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage
(per MIL-STD-883, Method 3015) > 2001 V

Latch-up Current > 140 mA

Operating Range

Device	Range	Ambient Temperature	$V_{CC}^{[4]}$
CY62187EV30LL	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	55 ns			Unit
			Min	Typ ^[5]	Max	
V_{OH}	Output HIGH voltage	$2.2\text{ V} \leq V_{CC} \leq 2.7\text{ V}$ $I_{OH} = -0.1\text{ mA}$	2.0	—	—	V
		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ $I_{OH} = -1.0\text{ mA}$	2.4	—	—	V
V_{OL}	Output LOW voltage	$2.2\text{ V} \leq V_{CC} \leq 2.7\text{ V}$ $I_{OL} = 0.1\text{ mA}$	—	—	0.4	V
		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ $I_{OL} = 2.1\text{ mA}$	—	—	0.4	V
V_{IH}	Input HIGH voltage	$2.2\text{ V} \leq V_{CC} \leq 2.7\text{ V}$	1.8	—	$V_{CC} + 0.3$	V
		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	2.2	—	$V_{CC} + 0.3$	V
V_{IL}	Input LOW voltage	$2.2\text{ V} \leq V_{CC} \leq 2.7\text{ V}$	-0.3	—	0.6	V
		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	-0.3	—	0.8 ^[6]	V
I_{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	—	+1	μA
I_{OZ}	Output leakage current	$GND \leq V_O \leq V_{CC}$, output disabled	-1	—	+1	μA
I_{CC}	V_{CC} operating supply current	$f = f_{Max} = 1/t_{RC}$ $V_{CC} = V_{CC(max)}$	—	45	55	mA
		$f = 1\text{ MHz}$ $I_{OUT} = 0\text{ mA}$ CMOS levels	—	15	38	mA
$I_{SB2}^{[7]}$	Automatic CE power down current — CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or (BHE and BLE) $\geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$, $f = 0$, $V_{CC} = 3.7\text{ V}$	—	8	48	μA

Notes

- $V_{IL(min)}$ = -2.0V for pulse durations less than 20 ns.
- $V_{IH(max)}$ = $V_{CC} + 0.75\text{ V}$ for pulse durations less than 20 ns.
- Full device AC operation assumes a 100-μs ramp time from 0 to $V_{CC(min)}$ and 200-μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25\text{ °C}$.
- Under DC conditions, the device meets a V_{IL} of 0.8 V. However, in dynamic conditions, the input LOW Voltage applied to the device must not be higher than 0.7 V.
- Chip Enables ($\overline{CE}_1$ and CE_2), Address Pins A_{20} , A_{21} and Byte Enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

Parameter ^[8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC}(\text{typ})$	25	pF
C_{OUT}	Output capacitance		35	pF

Thermal Resistance

Parameter ^[8]	Description	Test Conditions	FBGA	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	73.0	$^{\circ}\text{C/W}$
θ_{JC}	Thermal resistance (junction to case)		10.9	$^{\circ}\text{C/W}$

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

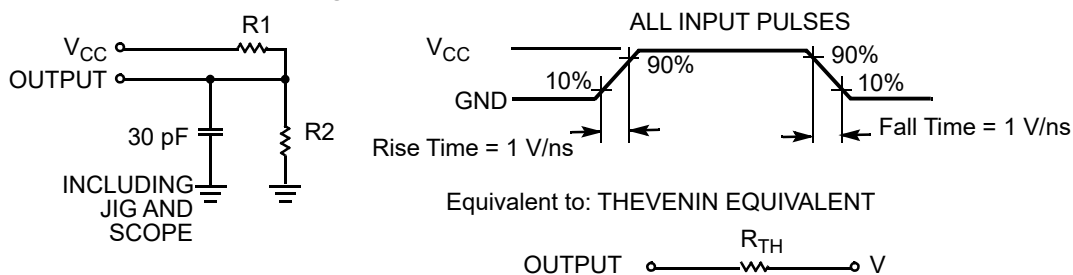


Table 1. AC Test Loads

Parameter	2.5 V	3.3 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note

8. Tested initially and after any design or process changes that may affect these parameters.

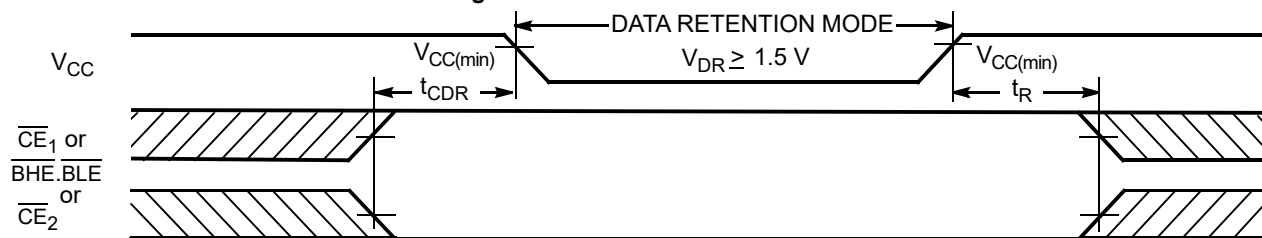
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[9]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
$I_{CCDR}^{[10]}$	Data retention current	$V_{CC} = 1.5\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	48	μA
$t_{CDR}^{[11]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[12]}$	Operation recovery time		55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform^[13]



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25\text{ }^\circ\text{C}$.
10. Chip Enables ($\overline{CE}_1$ and CE_2), Address Pins A_{20} , A_{21} and Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2}/I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.
13. $\overline{BHE.BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. The chip is deselected by either disabling the Chip Enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter ^[14]	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	55	–	ns
t _{AA}	Address to data valid	–	55	ns
t _{OHA}	Data hold from address change	4	–	ns
t _{ACE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to data valid	–	55	ns
t _{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t _{LZOE}	$\overline{OE}$ LOW to low Z ^[15]	5	–	ns
t _{HZOE}	$\overline{OE}$ HIGH to High-Z ^[15, 16]	–	20	ns
t _{LZCE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to low Z ^[15]	10	–	ns
t _{HZCE}	$\overline{CE}_1$ HIGH and CE ₂ LOW to High-Z ^[15, 16]	–	20	ns
t _{PU}	$\overline{CE}_1$ LOW and CE ₂ HIGH to power up	0	–	ns
t _{PD}	$\overline{CE}_1$ HIGH and CE ₂ LOW to power down	–	55	ns
t _{DBE}	BLE/BHE LOW to data valid	–	55	ns
t _{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to low Z ^[15]	10	–	ns
t _{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High-Z ^[15, 16]	–	20	ns
Write Cycle ^[17, 18]				
t _{WC}	Write cycle time	55	–	ns
t _{SCE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to write end	45	–	ns
t _{AW}	Address setup to write end	45	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	$\overline{WE}$ pulse width	40	–	ns
t _{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	45	–	ns
t _{SD}	Data setup to write end	25	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{HZWE}	$\overline{WE}$ LOW to High-Z ^[15, 16]	–	20	ns
t _{LZWE}	$\overline{WE}$ HIGH to low Z ^[15]	10	–	ns

Notes

14. Test conditions for all parameters other than High-Z parameters assume signal transition time of 1 V/ns, timing reference levels of V_{TH} , input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in [Figure 2 on page 6](#).
15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
16. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter the High-Z state.
17. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
18. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [19, 20]

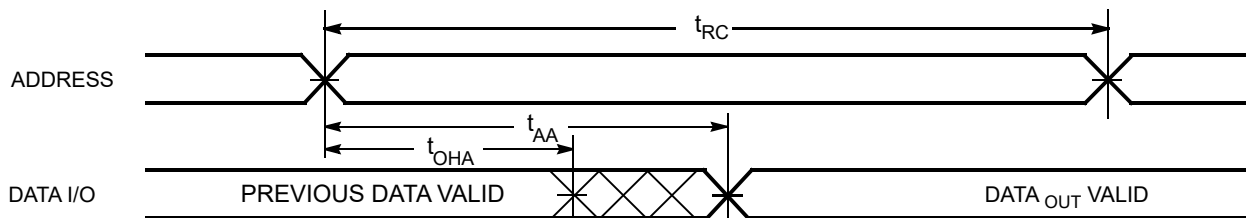
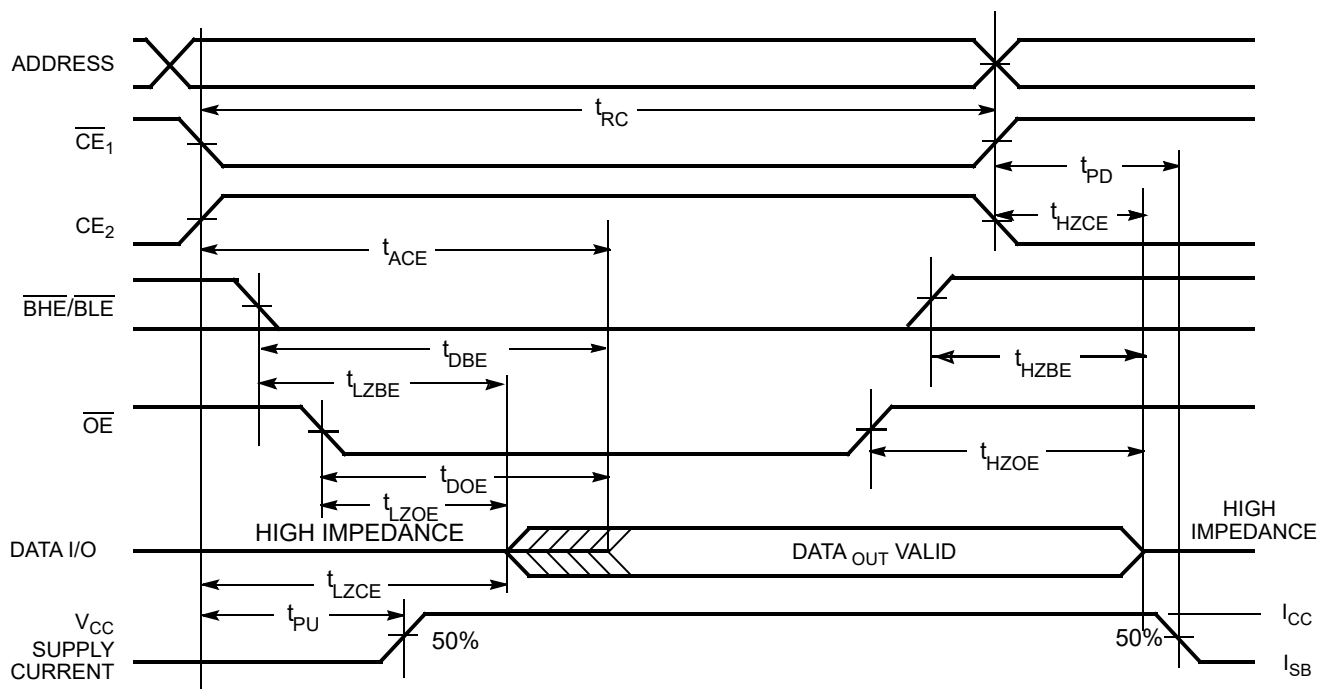


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [20, 21]



Notes

19. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.

20. $\overline{WE}$ is HIGH for read cycle.

21. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [22, 23, 24, 25]

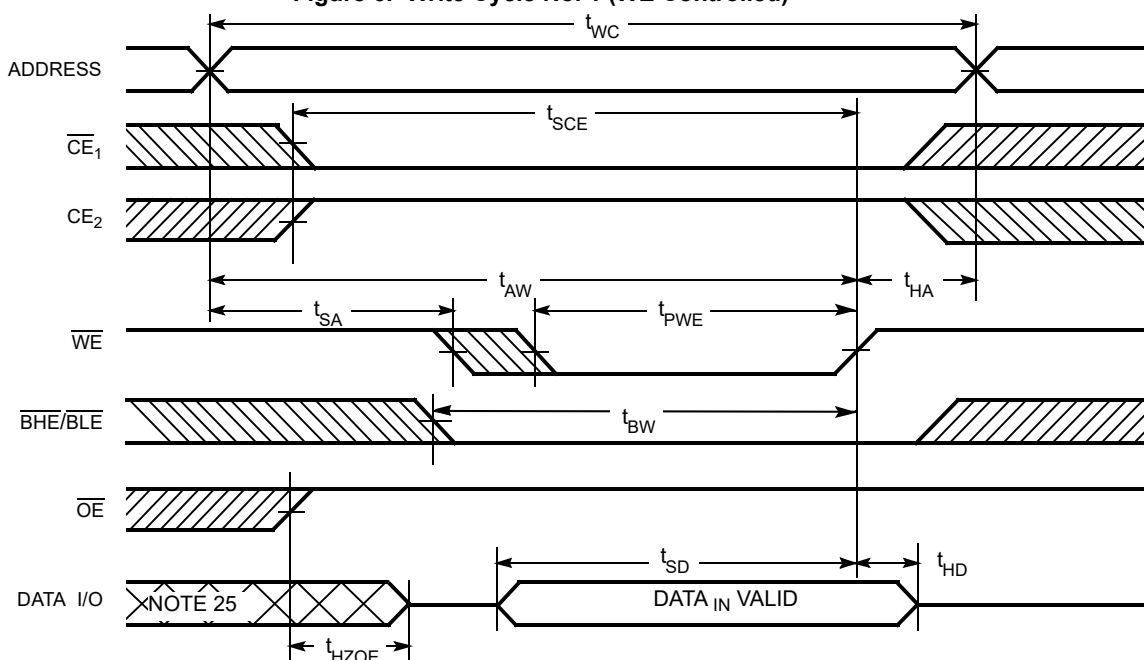
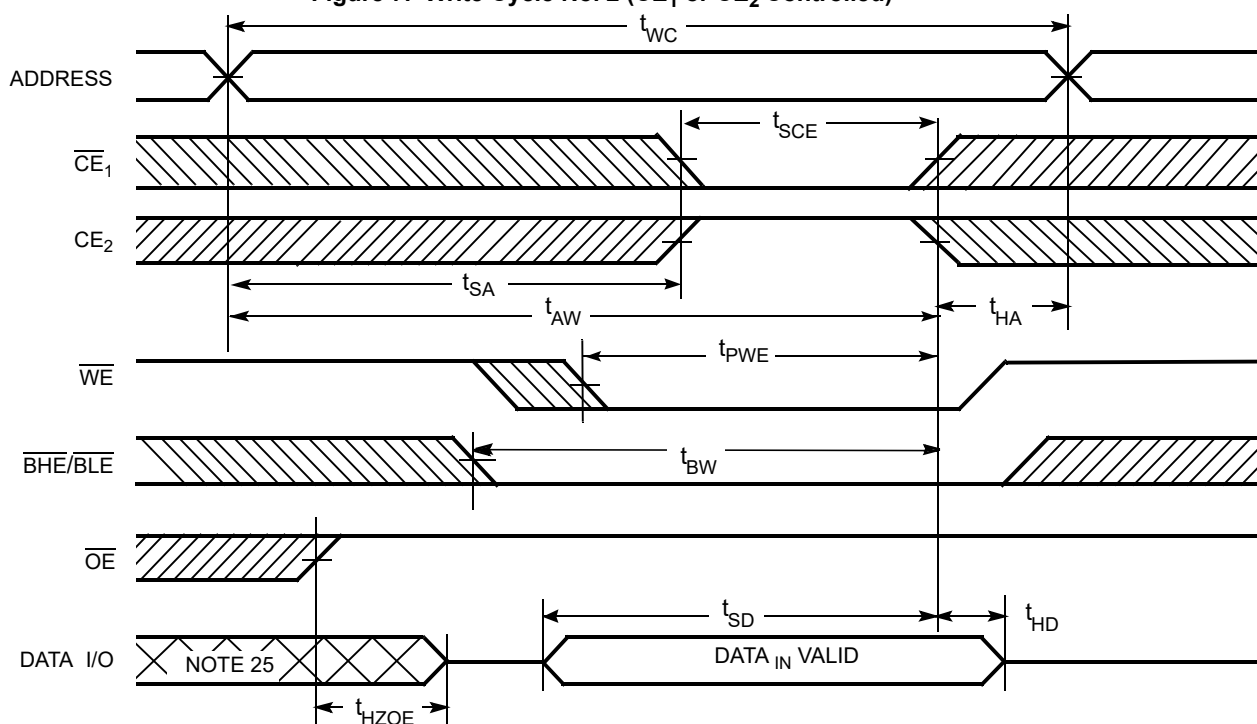


Figure 7. Write Cycle No. 2 ($\overline{CE_1}$ or $\overline{CE_2}$ Controlled) [22, 23, 24, 25]



Notes

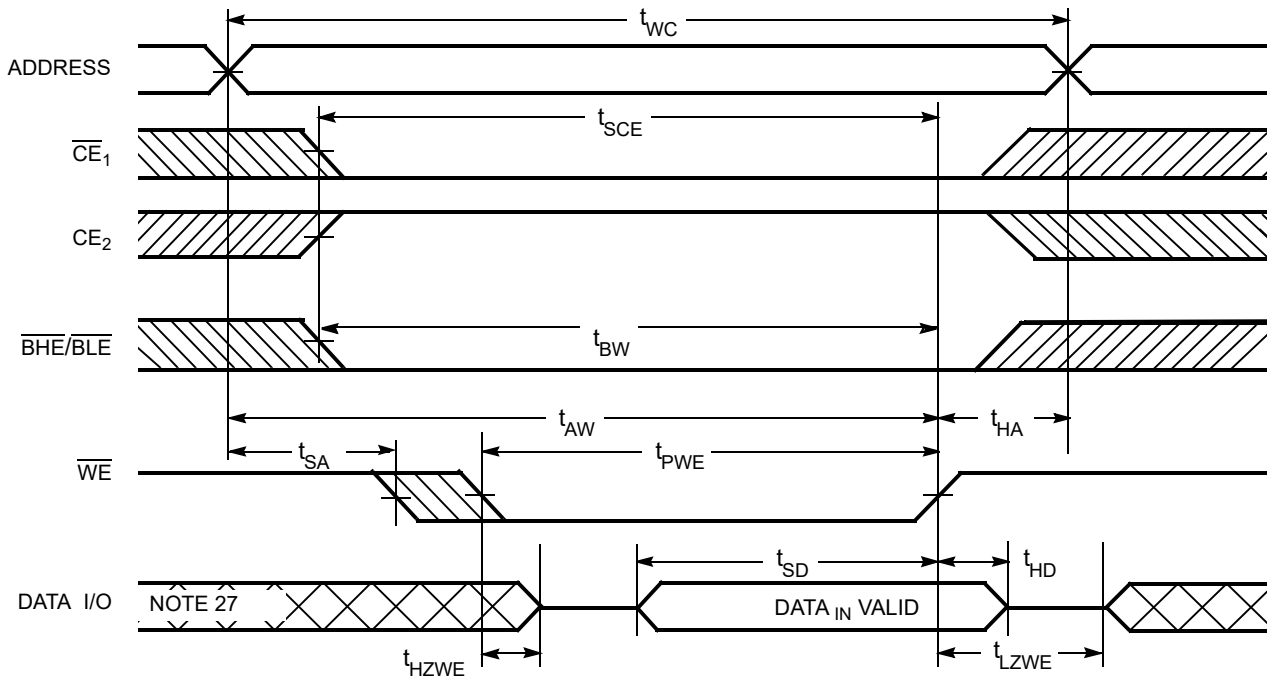
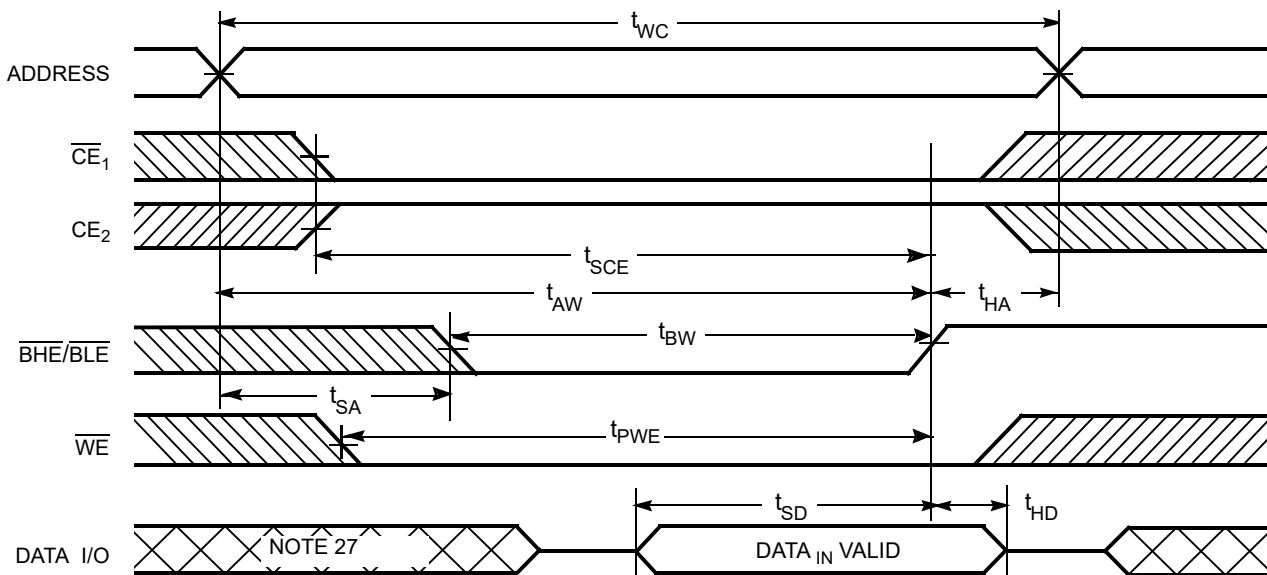
22. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $\overline{CE_2} = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

23. Data I/O is High-Z if $\overline{OE} = V_{IH}$.

24. If $\overline{CE_1}$ goes HIGH and $\overline{CE_2}$ goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in the High-Z state.

25. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [26, 27, 28]

Figure 9. Write Cycle No. 4 ($\overline{BHE/BLE}$ Controlled, $\overline{OE}$ LOW) [26, 27]

Notes

26. If $\overline{CE}_1$ goes HIGH and $\overline{CE}_2$ goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in the High-Z state.

27. During this period the I/Os are in output state and input signals should not be applied.

28. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE} .

Truth Table

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs Outputs	Mode	Power
H	X ^[29]	X	X	X ^[29]	X ^[29]	High-Z	Deselect/Power Down	Standby (I_{SB})
X ^[29]	L	X	X	X ^[29]	X ^[29]	High-Z	Deselect/Power Down	Standby (I_{SB})
X ^[29]	X ^[29]	X	X	H	H	High-Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	High-Z (I/O_8 – I/O_{15}); Data Out (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (I/O_8 – I/O_{15}); High-Z (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	High-Z (I/O_8 – I/O_{15}); Data In (I/O_0 – I/O_7)	Write	Active (I_{CC})
L	H	L	X	L	H	Data In (I/O_8 – I/O_{15}); High-Z (I/O_0 – I/O_7)	Write	Active (I_{CC})
L	H	H	H	L	H	High-Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High-Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High-Z	Output Disabled	Active (I_{CC})

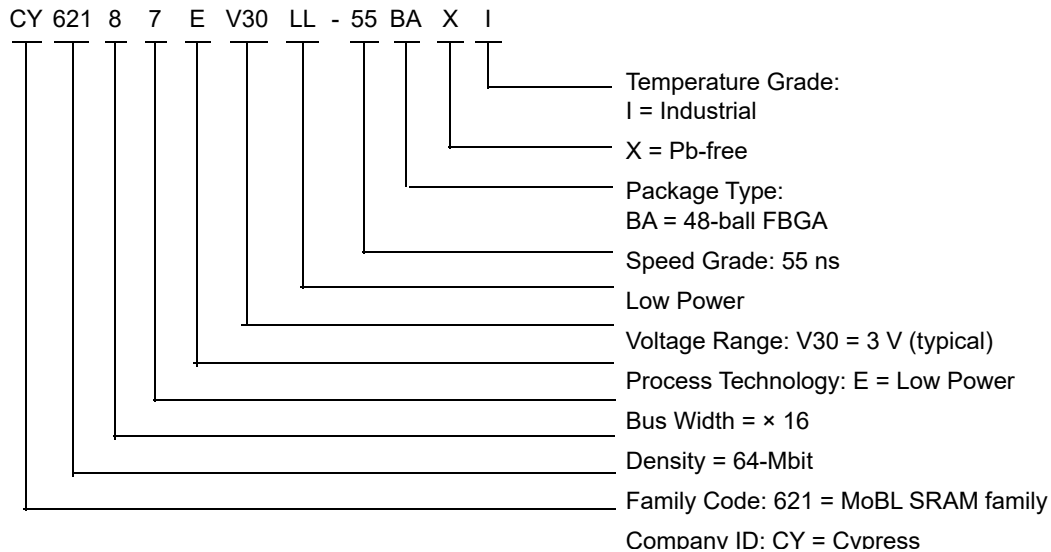
Note

29. The 'X' (Don't care) state for the Chip Enables and Byte Enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

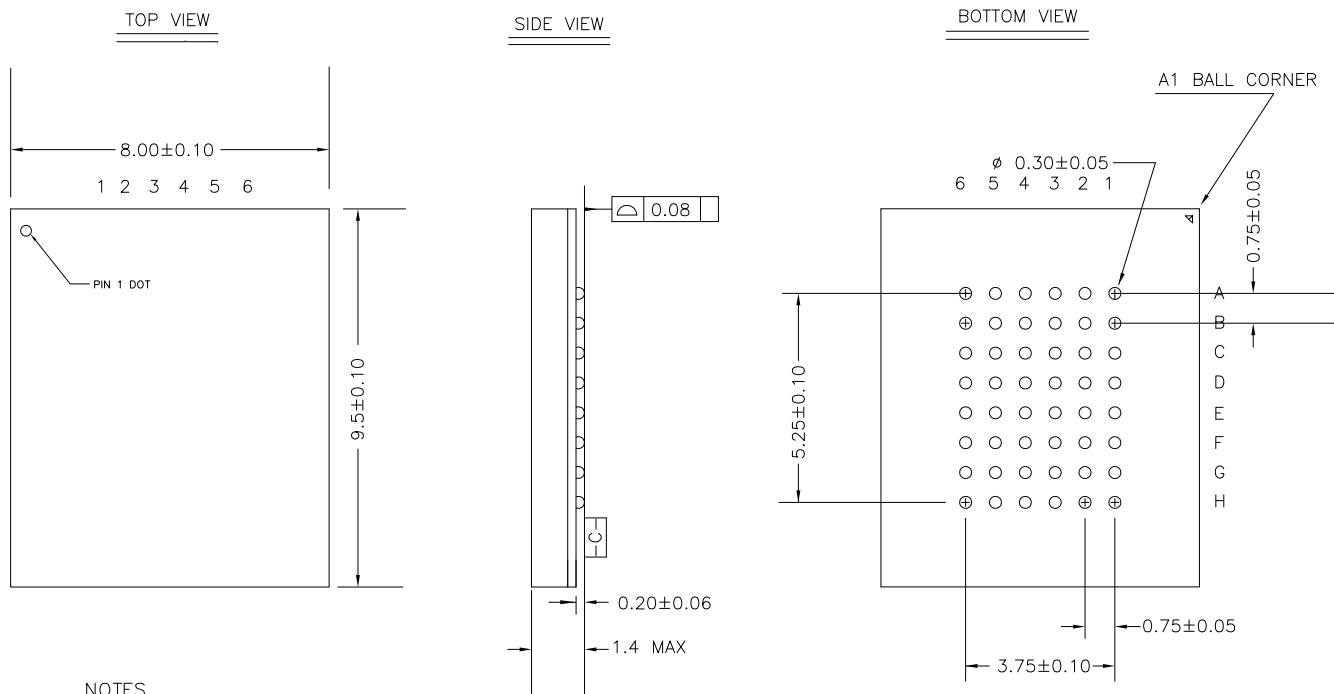
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62187EV30LL-55BAXI	001-50044	48-ball FBGA (8 × 9.5 × 1.4 mm) Pb-free	Industrial

Ordering Code Definitions



Package Diagram

Figure 10. 48-ball FBGA (8 × 9.5 × 1.4 mm) BK48L Package Outline, 001-50044



NOTES

1. REFERENCE JEDEC # MO-205
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-50044 *D

Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohms
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62187EV30 MoBL®, 64-Mbit (4M × 16) Static RAM Document Number: 001-48998			
Revision	ECN	Submission Date	Description of Change
**	2595932	10/24/2008	New data sheet.
*A	2644442	01/23/2009	Updated Package Diagram : Removed spec 001-49341 Rev. **. Added spec 001-50044 Rev. **.
*B	2672650	03/12/2009	Added 55 ns speed bin related information in all instances across the document. Updated Product Portfolio : Changed maximum value in V_{CC} range from 3.6 V to 3.7 V. Changed typical value of “Operating I_{CC} ” from 2.5 mA to 3.5 mA at $f = 1$ MHz corresponding to 70 ns speed bin. Changed maximum value of “Operating I_{CC} ” from 4 mA to 6 mA at $f = 1$ MHz corresponding to 70 ns speed bin. Changed typical value of “Operating I_{CC} ” from 33 mA to 28 mA at $f = f_{MAX}$ corresponding to 70 ns speed bin. Changed maximum value of “Operating I_{CC} ” from 40 mA to 45 mA at $f = f_{MAX}$ corresponding to 70 ns speed bin. Updated Electrical Characteristics : Changed typical value of I_{CC} parameter from 33 mA to 28 mA at $f = f_{MAX}$ corresponding to 70 ns speed bin. Changed maximum value of I_{CC} parameter from 40 mA to 45 mA at $f = f_{MAX}$ corresponding to 70 ns speed bin. Changed typical value of I_{CC} parameter from 2.5 mA to 3.5 mA at $f = 1$ MHz corresponding to 70 ns speed bin. Changed maximum value of I_{CC} parameter from 4 mA to 6 mA at $f = 1$ MHz corresponding to 70 ns speed bin. Updated Note 7. Updated Switching Characteristics : Changed minimum value of t_{PWE} parameter from 45 ns to 50 ns corresponding to 70 ns speed bin. Changed minimum value of t_{SD} parameter from 30 ns to 35 ns corresponding to 70 ns speed bin. Updated Package Diagram : Changed 48-ball FBGA package dimensions from “8 × 9.5 × 1.6 mm” to “8 × 9.5 × 1.4 mm”. spec 001-50044 – Changed revision from ** to *A.
*C	2737164	07/13/2009	Changed status from Preliminary to Final. Updated Product Portfolio : Changed typical value of “Operating I_{CC} ” from 3.5 mA to 4 mA at $f = 1$ MHz corresponding to 55 ns and 70 ns speed bins. Changed typical value of “Operating I_{CC} ” from 35 mA to 45 mA at $f = f_{max}$ corresponding to 55 ns speed bin. Changed typical value of “Operating I_{CC} ” from 28 mA to 35 mA at $f = f_{max}$ corresponding to 70 ns speed bin.

Document History Page (continued)

Document Title: CY62187EV30 MoBL®, 64-Mbit (4M × 16) Static RAM Document Number: 001-48998			
Revision	ECN	Submission Date	Description of Change
*C (cont.)	2737164	07/13/2009	Updated Electrical Characteristics: Updated details in "Test Conditions" column of V_{OH}, V_{OL}, V_{IH}, V_{IL} parameters (Included V_{CC} range). Changed maximum value of V_{IL} parameter from 0.8 V to 0.7 V corresponding to Test Condition "$V_{CC} = 2.7$ V to 3.7 V". Changed typical value of I_{CC} parameter from 35 mA to 45 mA at $f = f_{max}$ corresponding to 55 ns speed bin. Changed typical value of I_{CC} parameter from 28 mA to 35 mA at $f = f_{max}$ corresponding to 70 ns speed bin. Changed typical value of I_{CC} parameter from 3.5 mA to 4 mA at $f = 1$ MHz corresponding to 55 ns and 70 ns speed bins. Updated Capacitance: Changed maximum value of C_{IN} parameter from 20 pF to 25 pF. Changed maximum value of C_{OUT} parameter from 20 pF to 35 pF. Updated Thermal Resistance: Replaced TBD with values for 48-ball FBGA package. Updated AC Test Loads and Waveforms: Updated Table 1: Included V_{CC} range for V_{TH} parameter. Updated Switching Characteristics: Changed minimum value of t_{LZBE} parameter from 5 ns to 10 ns. Updated Truth Table: Added Note 29 and referred the same note in "X" in "$\overline{CE_1}$" and "$\overline{CE_2}$" columns.
*D	2765892	09/18/2009	Removed 70 ns speed bin related information in all instances across the document. Updated Product Portfolio: Changed maximum value of "Operating I_{CC}" from 6 mA to 9 mA at $f = 1$ MHz corresponding to 55 ns speed bin. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 4 mA to 7.5 mA at $f = 1$ MHz corresponding to 55 ns speed bin. Changed maximum value of I_{CC} parameter from 6 mA to 9 mA at $f = 1$ MHz corresponding to 55 ns speed bin. Completing Sunset Review.
*E	3177000	02/18/2011	Updated Features: Changed value of "Typical Active Current" from 4 mA to 7.5 mA. Updated Pin Configuration: Fixed typo in Figure 1 (Renamed "48-Ball VFBGA" as "48-ball FBGA"). Updated Product Portfolio: Changed typical value of "Operating I_{CC}" from 4 mA to 7.5 mA at $f = 1$ MHz corresponding to 55 ns speed bin. Updated Electrical Characteristics: Updated details in "Test Conditions" column of I_{SB2} parameter (Included $\overline{BHE}$ and $\overline{BLE}$ to reflect Byte power down feature). Updated AC Test Loads and Waveforms: Updated Table 1. Updated Data Retention Characteristics: Updated details in "Test Conditions" column of I_{CCDR} parameter (Included $\overline{BHE}$ and $\overline{BLE}$ to reflect Byte power down feature). Changed minimum value of t_R parameter from t_{RC} to 55 ns. Added Ordering Code Definitions under Ordering Information. Updated Package Diagram: spec 001-50044 – Changed revision from *A to *C.
*E (cont.)	3177000	02/18/2011	Added Acronyms and Units of Measure. Changed all instances of IO to I/O. Updated to new template.

Document History Page (continued)

Document Title: CY62187EV30 MoBL®, 64-Mbit (4M × 16) Static RAM Document Number: 001-48998			
Revision	ECN	Submission Date	Description of Change
*F	3282088	06/14/2011	Updated Functional Description : Removed the note "For best practice recommendations, refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com website" and its reference. Updated Electrical Characteristics : Changed maximum value of V_{IL} parameter corresponding to Test Condition " $2.7\text{ V} \leq V_{CC} \leq 3.7\text{ V}$ " from 0.7 V to 0.8 V. Added Note 6 and referred the same note in maximum value of V_{IL} parameter. Updated to new template.
*G	3785005	10/18/2012	Minor text edits. Updated Package Diagram : spec 001-50044 – Changed revision from *C to *D. Completing Sunset Review.
*H	4101127	08/21/2013	Updated Switching Characteristics : Added Note 14 and referred the same note in "Parameter" column. Updated to new template. Completing Sunset Review.
*I	4114808	09/12/2013	Updated Electrical Characteristics : Updated Note 7. Updated Data Retention Characteristics : Updated Note 10.
*J	4576478	11/21/2014	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Switching Characteristics : Added Note 18 and referred the same note in "Write Cycle". Updated Switching Waveforms : Added Note 28 and referred the same note in Figure 8 .
*K	4990839	10/27/2015	Updated Thermal Resistance : Replaced "2-layer" with "four-layer" in "Test Conditions" column. Changed value of θ_{JA} parameter corresponding to FBGA package from 59.06 °C/W to 42.35 °C/W. Changed value of θ_{JC} parameter corresponding to FBGA package from 14.08 °C/W to 6.25 °C/W. Updated to new template. Completing Sunset Review.
*L	5962070	11/09/2017	Updated logo and Copyright.
*M	6315678	09/27/2018	Updated Maximum Ratings : Changed value of Latch-up current from "> 200 mA" to "> 140 mA". Updated Operating Range : Replaced "2.2 V to 3.7 V" with "2.2 V to 3.6 V" under " V_{CC} " column. Updated Electrical Characteristics : Changed typical value of I_{CC} parameter from 7.5 mA to 15 mA corresponding to Test Condition " $f = 1\text{ MHz}$ ". Changed maximum value of I_{CC} parameter from 9 mA to 18 mA corresponding to Test Condition " $f = 1\text{ MHz}$ ".
*M (cont.)	6315678	09/27/2018	Updated Thermal Resistance : Changed value of θ_{JA} parameter corresponding to FBGA package from 42.35 °C/W to 76.7 °C/W. Changed value of θ_{JC} parameter corresponding to FBGA package from 6.25 °C/W to 10.9 °C/W. Updated Switching Characteristics : Changed minimum value of t_{OHA} parameter from 6 ns to 4 ns. Updated to new template.

Document History Page *(continued)*

Document Title: CY62187EV30 MoBL®, 64-Mbit (4M × 16) Static RAM Document Number: 001-48998			
Revision	ECN	Submission Date	Description of Change
*N	6713141	10/24/2019	Updated product portfolio In Electrical Characteristics , updated I _{CC} @ 1 MHz maximum and I _{SB2}

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2008-2019. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.