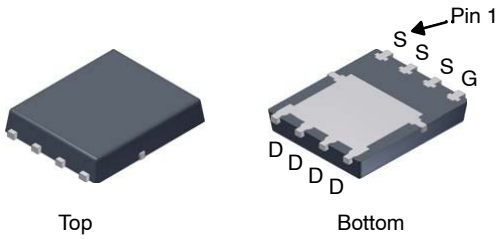
# MOSFET - Shielded Gate N-Channel, POWERTRENCH®

## 60 V, 22 A, 8.2 mΩ

# FDMS86520L, FDMS86520L-NC

| $V_{DS}$ | $R_{DS(on)}$ MAX | $I_D$ Max |
|---|---|---|
| 60 V | 11.7 mΩ @ $V_{GS}$ = 4.5 V | 11.5 A |
| | 8.2 mΩ @ $V_{GS}$ = 6 V | 13.5 A |




Top Bottom

**PQFN8 5X6, 1.27P**
**Power 56**
**CASE 483AE**

### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

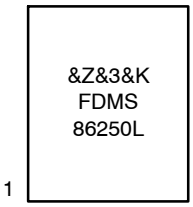
### Features

- Max $R_{DS(on)}$ = 8.2 mΩ at $V_{GS}$ = 10 V, $I_D$ = 13.5 A
- Max $R_{DS(on)}$ = 11.7 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 11.5 A
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- MSL1 Robust Package Design
- 100% UIL Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

### Applications

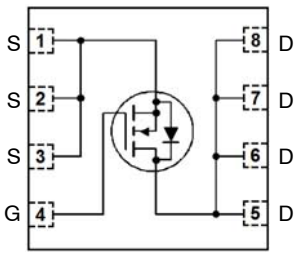
- Primary Switch in Isolated DC-DC
- Synchronous Rectifier
- Load Switch

### MARKING DIAGRAM




&Z = Assembly Plant Code
& = 3-Digit Date Code
&K = 2-Digits Lot Run Code
FDMS86520L = Specific Device Code

### PIN CONNECTIONS




### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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**MAXIMUM RATINGS** ($T_A$ = 25 °C unless otherwise noted)

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | 60 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±20 | V |
| $I_D$ | Drain Current | Continuous, $T_C$ = 25 °C | 22 | A |
| | | Continuous, $T_A$ = 25 °C (Note 1a) | 13.5 | |
| | | Pulsed (Note 3) | 60 | |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 3) | | 91 | mJ |
| $P_D$ | Power Dissipation | $T_C$ = 25 °C | 69 | W |
| | | $T_A$ = 25 °C (Note 1a) | 2.5 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL CHARACTERISTICS**

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 1.8 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1a) | 50 | |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25 °C unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 60 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | 29 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 48 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate-to-Source Leakage Current, Forward | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| $V_{GS(th)}$ | Gate-to-Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1 | 1.8 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate-to-Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | −7 | | mV/°C |
| $R_{DS(on)}$ | Static Drain-to-Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 13.5 A | | 6.7 | 8.2 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 11.5 A | | 9.1 | 11.7 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 13.5 A, $T_J$ = 125 °C | | 9.6 | 11.8 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 13.5 A | | 51 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V, f = 1 MHz | | 3470 | 4615 | pF |
| $C_{oss}$ | Output Capacitance | | | 625 | 835 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 25 | 45 | pF |
| $R_g$ | Gate Resistance | | | 0.6 | | Ω |



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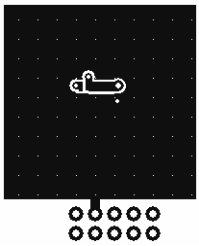
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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25 °C unless otherwise noted) (continued)

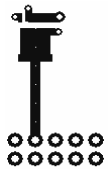
| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 30 V, $I_D$ = 13.5 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 15 | 27 | ns |
| $t_r$ | Rise Time | | | 5.6 | 11 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 32 | 52 | ns |
| $t_f$ | Fall Time | | | 3.4 | 10 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V, $V_{DD}$ = 30 V, $I_D$ = 13.5 A | | 45 | 63 | nC |
| | Total Gate Charge | $V_{GS}$ = 0 V to 4.5 V, $V_{DD}$ = 30 V, $I_D$ = 13.5 A | | 21 | 30 | nC |
| $Q_{gs}$ | Gate-to-Source Charge | $V_{DD}$ = 30 V, $I_D$ = 13.5 A | | 9.5 | | nC |
| $Q_{gd}$ | Gate-to-Drain “Miller” Charge | | | 4.7 | | nC |
| **DRAIN-SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.1 A (Note 2) | | 0.72 | 1.2 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 13.5 A (Note 2) | | 0.83 | 1.3 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 13.5 A, di/dt = 100 A/μs | | 37 | 60 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 21 | 34 | nC |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 13.5 A, di/dt = 300 A/μs | | 30 | 48 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 37 | 59 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 50 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting $T_J$ = 25 °C, L = 1 mH, $I_{AS}$ = 13.5 A, $V_{DD}$ = 54 V, $V_{GS}$ = 10 V. 100% test at L = 0.1 mH, $I_{AS}$ = 29 A.



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## TYPICAL CHARACTERISTICS ($T_J$ = 25 °C unless otherwise noted)

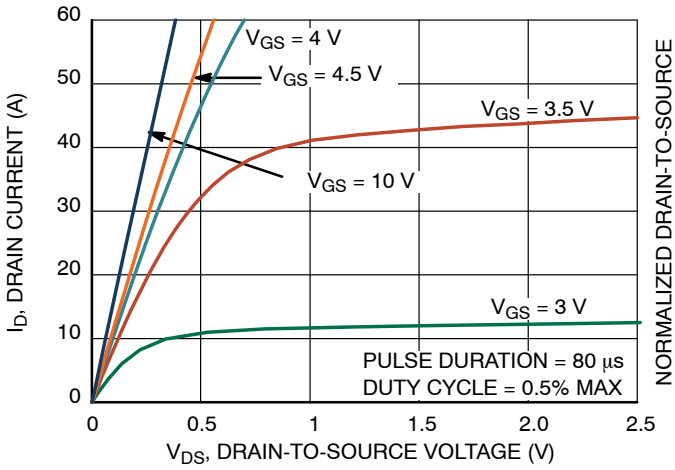



**Figure 1. On Region Characteristics**

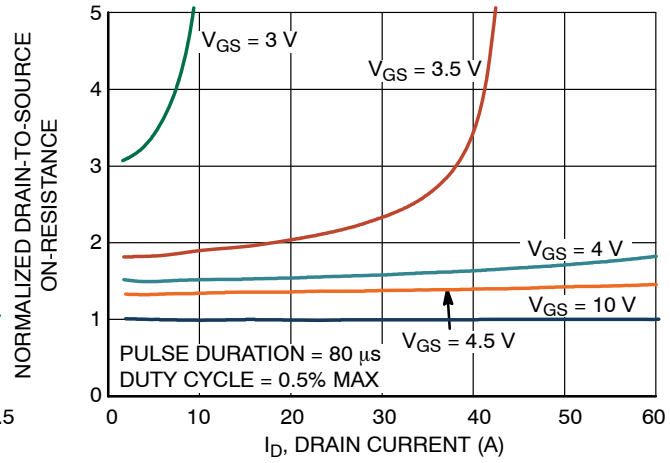



**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**

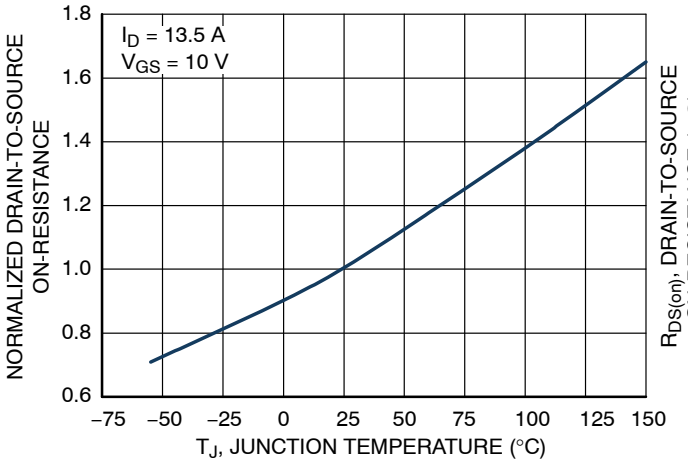



**Figure 3. Normalized On Resistance vs. Junction Temperature**

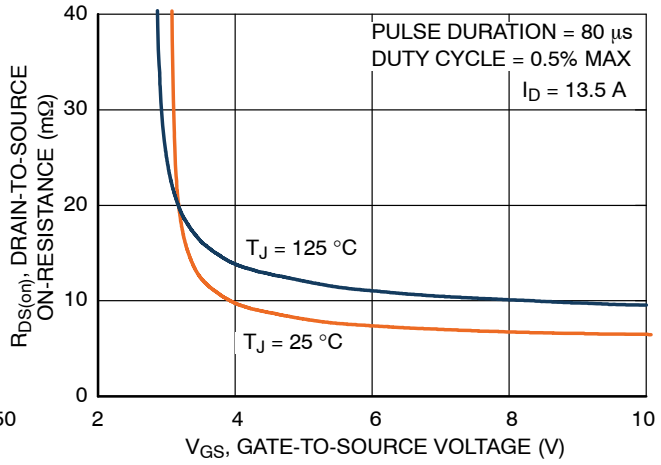



**Figure 4. On-Resistance vs. Gate-to-Source Voltage**

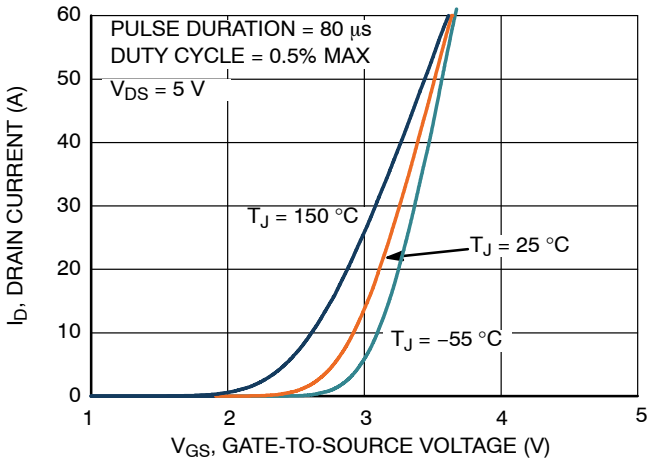



**Figure 5. Transfer Characteristics**

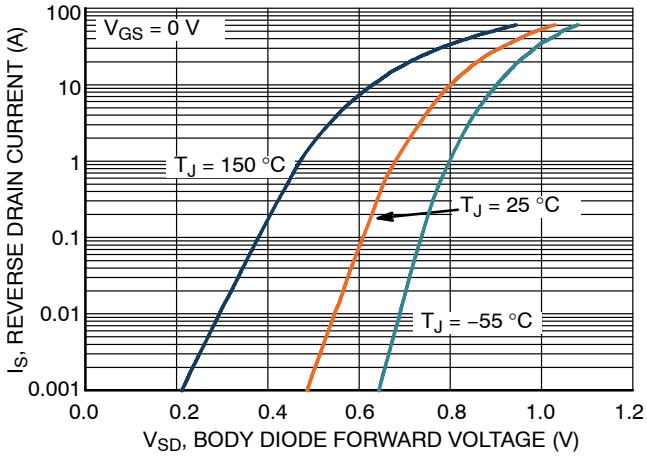



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**



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## TYPICAL CHARACTERISTICS ($T_J$ = 25 °C unless otherwise noted) (continued)

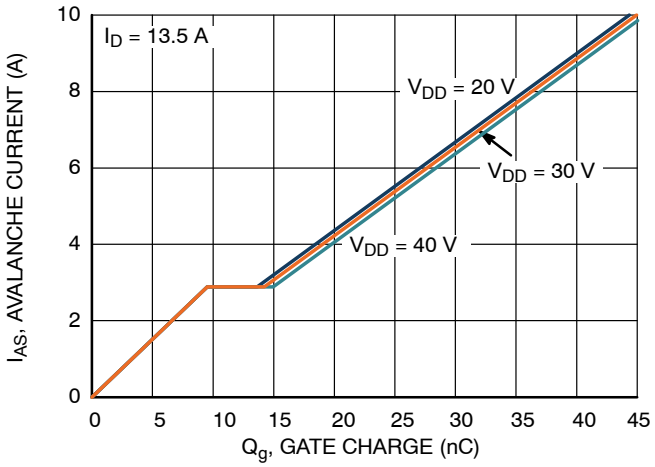



**Figure 7. Gate Charge Characteristics**

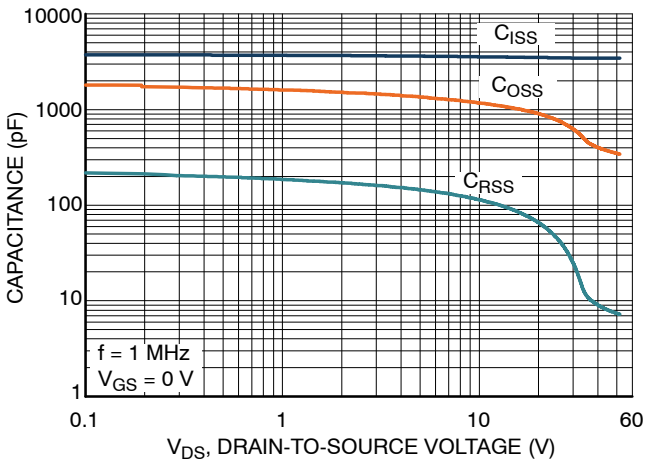



**Figure 8. Capacitance vs. Drain to Source Voltage**

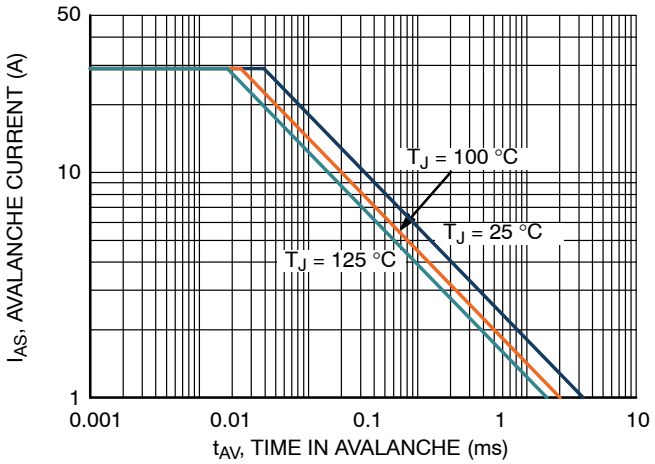



**Figure 9. Unclamped Inductive Switching Capability**

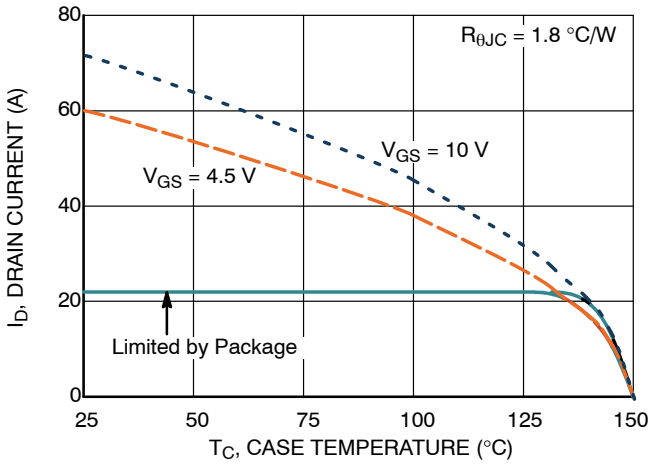



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

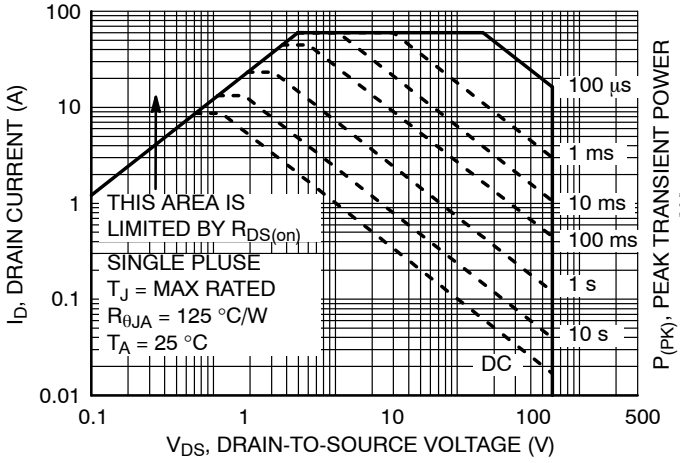



**Figure 11. Forward Bias Safe Operating Area**

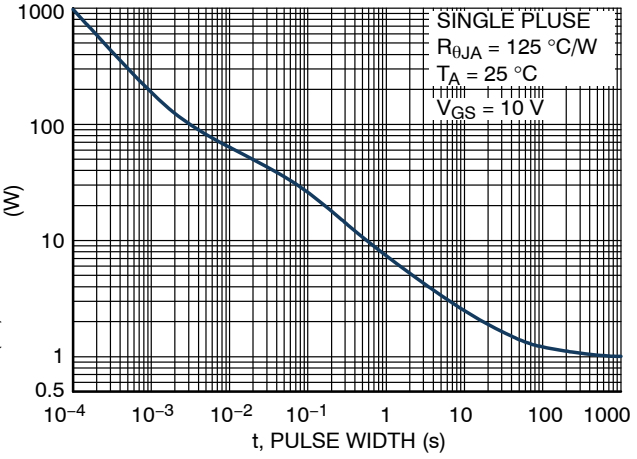



**Figure 12. Single Pulse Maximum Power Dissipation**



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## TYPICAL CHARACTERISTICS ($T_J$ = 25 °C unless otherwise noted) (continued)

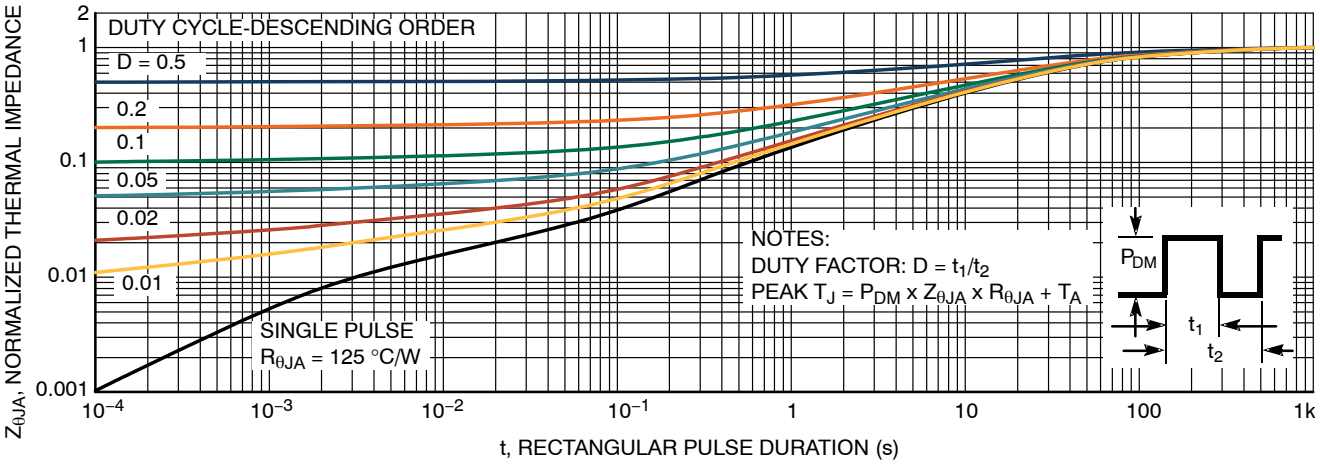



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## PACKAGE MARKING AND ORDERING INFORMATION

| Device | Device Marking | Package Type | Reel Size | Tape Width | Shipping† |
|---|---|---|---|---|---|
| FDMS86520L | FDMS86520L | PQFN8 5X6, 1.27P Power 56 | 13” | 12 mm | 3000 / Tape & Reel |
| FDMS86520L-NC | | | | | |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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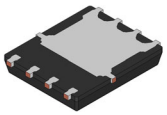
| Revision | Description of Changes | Date |
|---|---|---|
| 4 | Converted the document to **onsemi** format. Added new OPN. | 5/13/2026 |
| 5 | Device FDMS86520L-NC added to the front page title block. | 8/28/2026 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



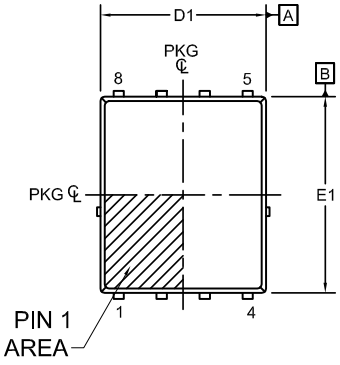
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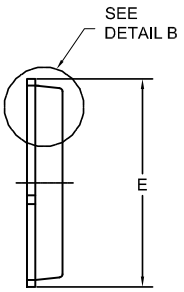


**PQFN8 5X6, 1.27P**
CASE 483AE
ISSUE C

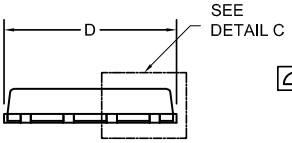
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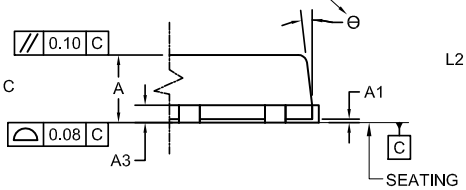

TOP VIEW



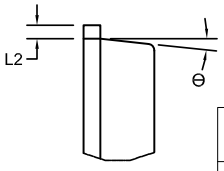

OPTIONAL DRAFT
ANGLE MAY APPEAR
ON FOUR SIDES
OF THE PACKAGE




SIDE VIEW




DETAIL C
SCALE: 2:1

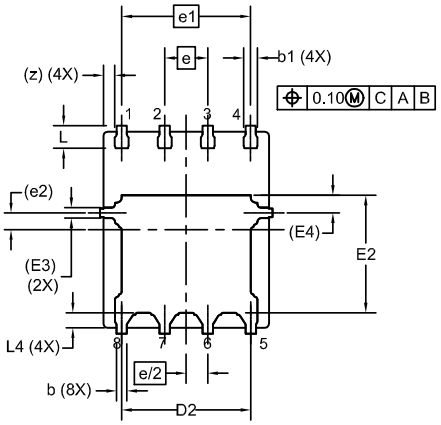



DETAIL B
SCALE: 2:1

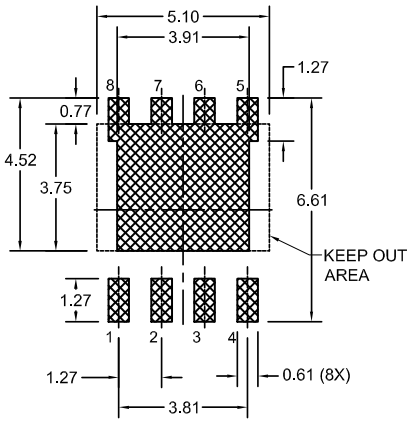
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | - | 0.05 |
| b | 0.21 | 0.31 | 0.41 |
| b1 | 0.31 | 0.41 | 0.51 |
| A3 | 0.15 | 0.25 | 0.35 |
| D | 4.90 | 5.00 | 5.20 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.61 | 3.82 | 3.96 |
| E | 5.90 | 6.15 | 6.25 |
| E1 | 5.70 | 5.80 | 5.90 |
| E2 | 3.38 | 3.48 | 3.78 |
| E3 | 0.30 REF | | |
| E4 | 0.52 REF | | |
| e | 1.27 BSC | | |
| e/2 | 0.635 BSC | | |
| e1 | 3.81 BSC | | |
| e2 | 0.50 REF | | |
| L | 0.51 | 0.66 | 0.76 |
| L2 | 0.05 | 0.18 | 0.30 |
| L4 | 0.34 | 0.44 | 0.54 |
| z | 0.34 REF | | |
| Θ | 0° | - | 12° |




BOTTOM VIEW




LAND PATTERN
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**Technical Library:** www.onsemi.com/design/resources/technical−documentation
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