

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ max	I_D $T_A = +25^\circ C$
30V	15m Ω @ $V_{GS} = 10V$	8.4A
	18m Ω @ $V_{GS} = 4.5V$	7.7A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

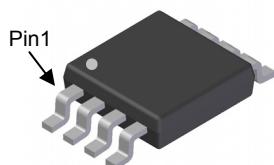
- DC-DC Converters
- Power Management Functions
- Backlighting

Features and Benefits

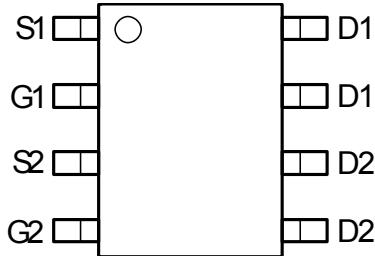
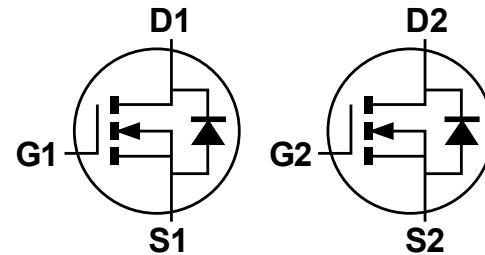
- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Tin Finish annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 **63**
- Weight: 0.074 grams (approximate)



Top View

Top View
Pin Configuration

Equivalent Circuit

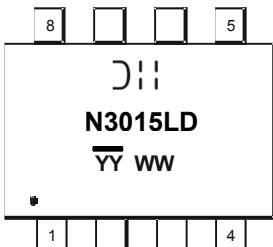
Ordering Information (Note 4)

Part Number	Case	Packaging
DMN3015LSD-13	SO-8	2,500/Tape & Reel

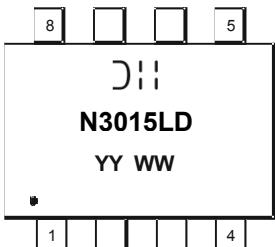
Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

DII = Manufacturer's Marking

N3015LD = Product Type Marking Code

YYWW = Date Code Marking

YY or YY = Year (ex: 14 = 2014)

WW = Week (01 - 53)

YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)

YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	8.4 6.8	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	11.0 9.0	A
Maximum Body Diode Forward Current (Note 6)			I_S	2.5	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	80	A
Avalanche Current (Notes 7) $L = 0.1\text{mH}$			I_{AS}	22	A
Avalanche Energy (Notes 7) $L = 0.1\text{mH}$			E_{AS}	25	mJ

 Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$		P_D	1.2	W
	$T_A = +70^\circ\text{C}$			0.8	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state		$R_{\theta JA}$	102	$^\circ\text{C/W}$
	$t < 10\text{s}$			62	
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$		P_D	1.6	W
	$T_A = +70^\circ\text{C}$			1.0	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state		$R_{\theta JA}$	78	$^\circ\text{C/W}$
	$t < 10\text{s}$			47	
Thermal Resistance, Junction to Case (Note 6)			$R_{\theta JC}$	14.5	
Operating and Storage Temperature Range			T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

 Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(\text{TH})}$	1.3	—	2.5	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	—	8	15	$\text{m}\Omega$	$V_{GS} = 10\text{V}, I_D = 12\text{A}$
		—	12	18		$V_{GS} = 4.5\text{V}, I_D = 10\text{A}$
Diode Forward Voltage	V_{SD}	—	0.7	1.0	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1415	—	pF	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	119	—		
Reverse Transfer Capacitance	C_{rss}	—	82	—		
Gate Resistance	R_G	—	2.6	3.2	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	11.3	—	nC	$V_{DS} = 15\text{V}, I_D = 12\text{A}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	25.1	—		
Gate-Source Charge	Q_{gs}	—	3.5	—		
Gate-Drain Charge	Q_{gd}	—	3.6	—		
Turn-On Delay Time	$t_{D(\text{on})}$	—	4.8	—	nS	$V_{DD} = 15\text{V}, V_{GS} = 10\text{V}, R_L = 1.25\Omega, R_G = 3\Omega$
Turn-On Rise Time	t_r	—	16.5	—		
Turn-Off Delay Time	$t_{D(\text{off})}$	—	26.1	—		
Turn-Off Fall Time	t_f	—	5.6	—		
Body Diode Reverse Recovery Time	t_{rr}	—	8.5	—	nS	$I_S = 12\text{A}, dI/dt = 500\text{A}/\mu\text{s}$
Body Diode Reverse Recovery Charge	Q_{rr}	—	7.0	—	nC	$I_S = 12\text{A}, dI/dt = 500\text{A}/\mu\text{s}$

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

7. UIS in production with $L = 0.1\text{mH}$, starting $T_A = +25^\circ\text{C}$.

8. Short duration pulse test used to minimize self-heating effect.

9. Guaranteed by design. Not subject to product testing.

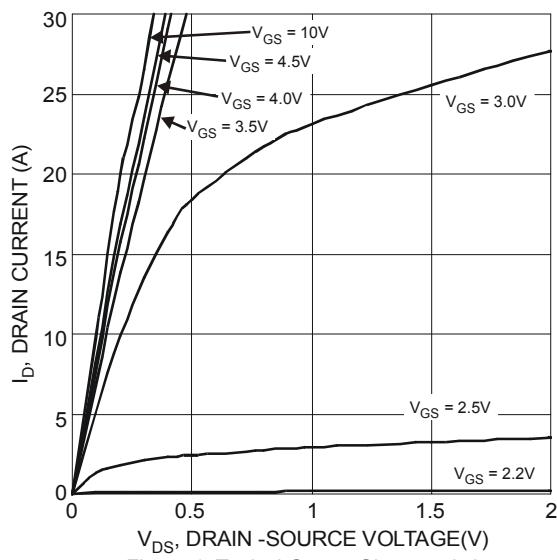


Figure 1 Typical Output Characteristics

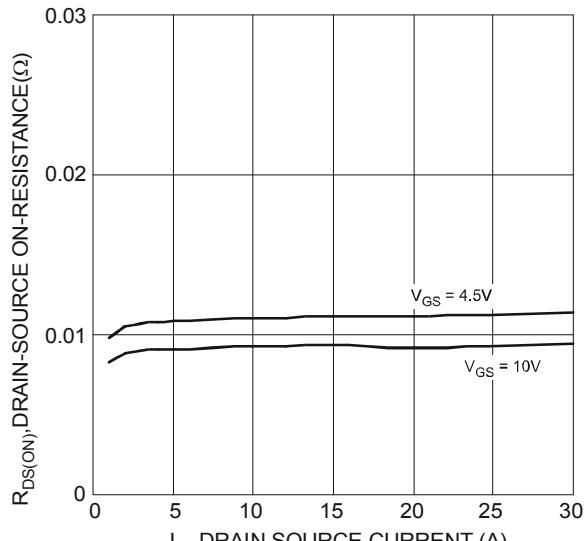


Figure 3 Typical On-Resistance vs.
Drain Current and Gate Voltage

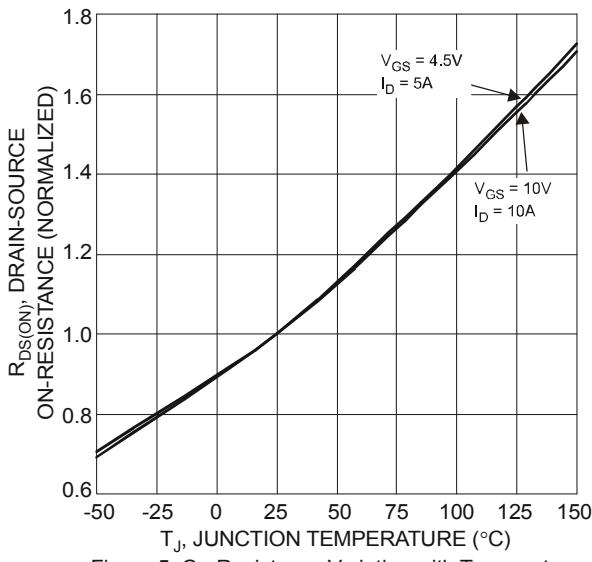


Figure 5 On-Resistance Variation with Temperature

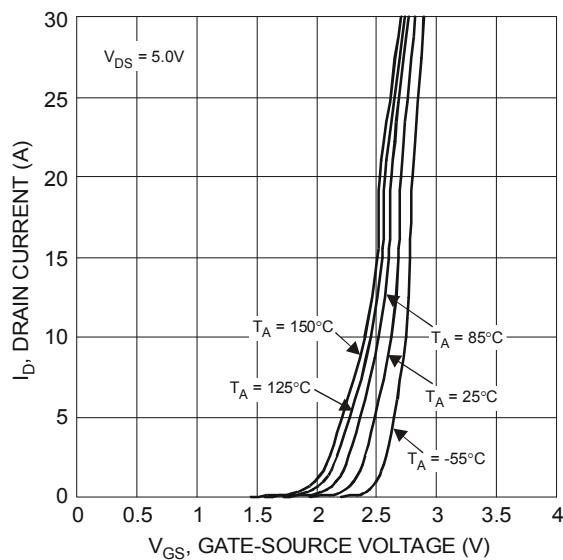


Figure 2 Typical Transfer Characteristics

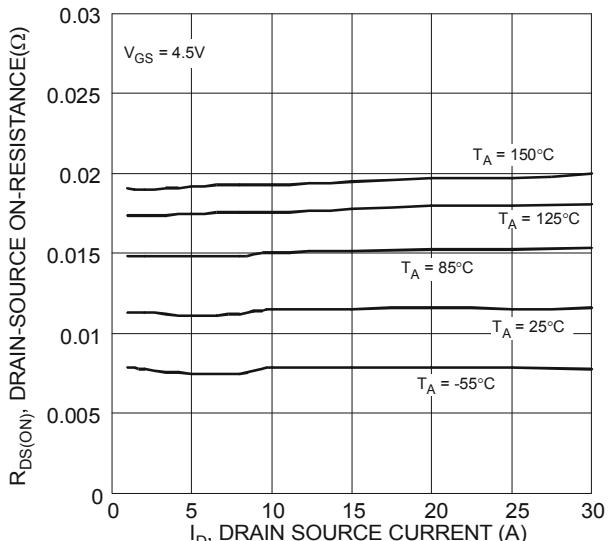


Figure 4 Typical On-Resistance vs.
Drain Current and Temperature

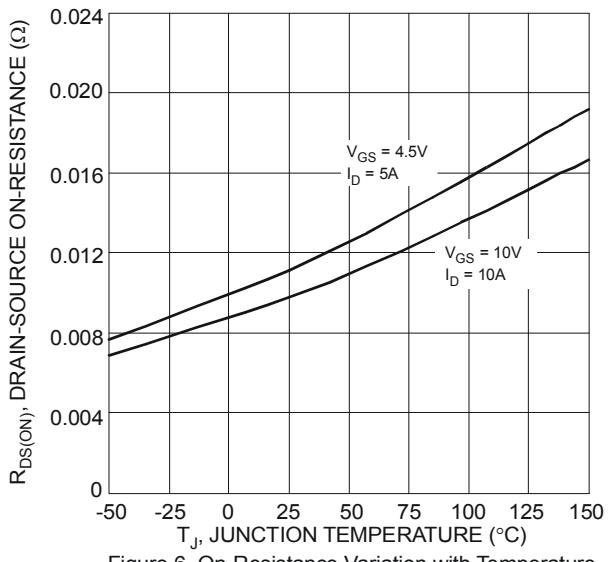


Figure 6 On-Resistance Variation with Temperature

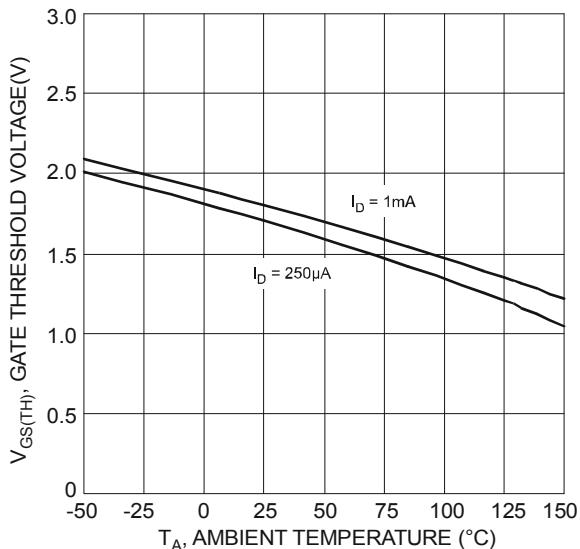


Figure 7 Gate Threshold Variation vs. Ambient Temperature

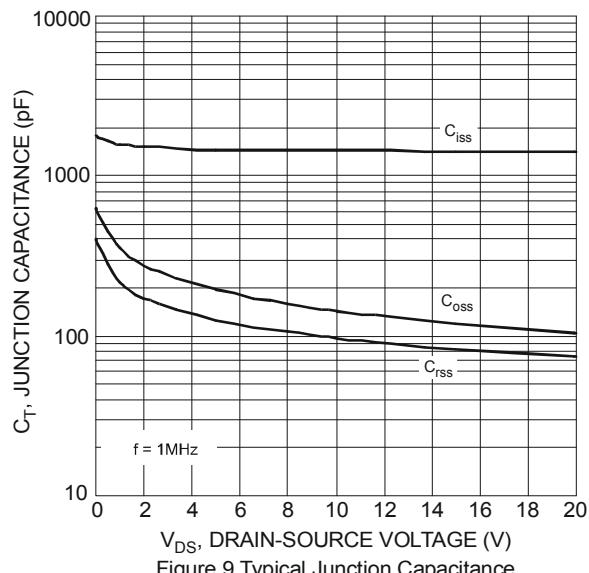


Figure 9 Typical Junction Capacitance

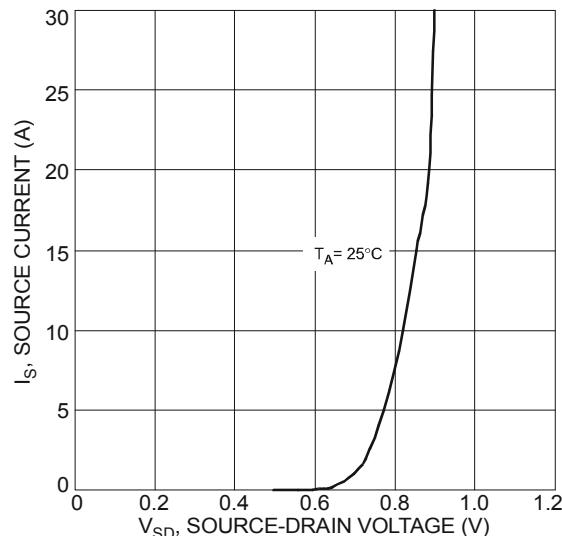


Figure 8 Diode Forward Voltage vs. Current

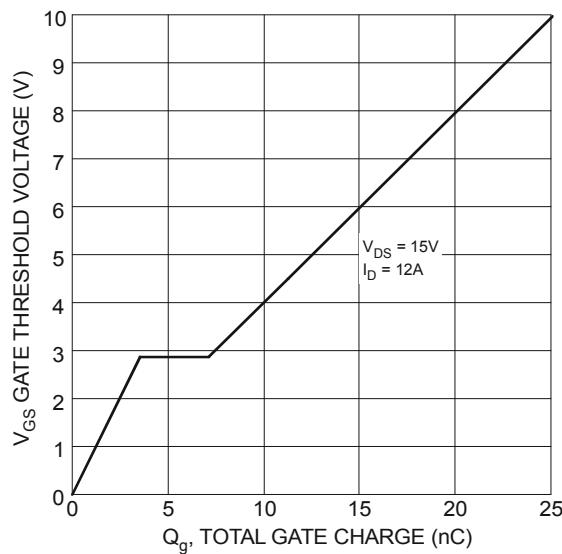


Figure 10 Gate Charge

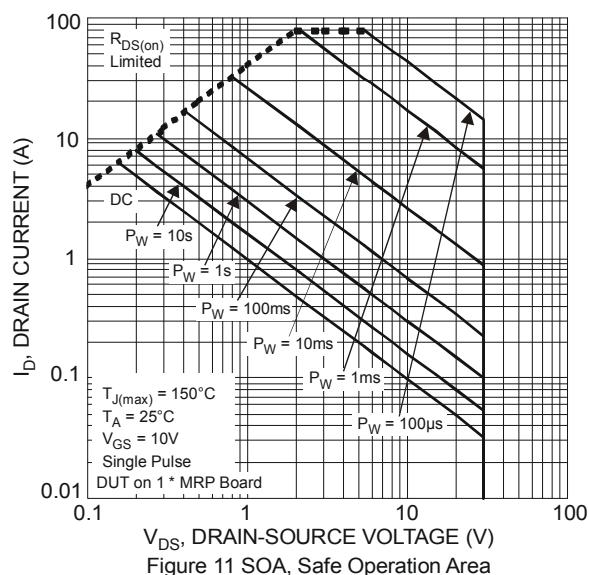
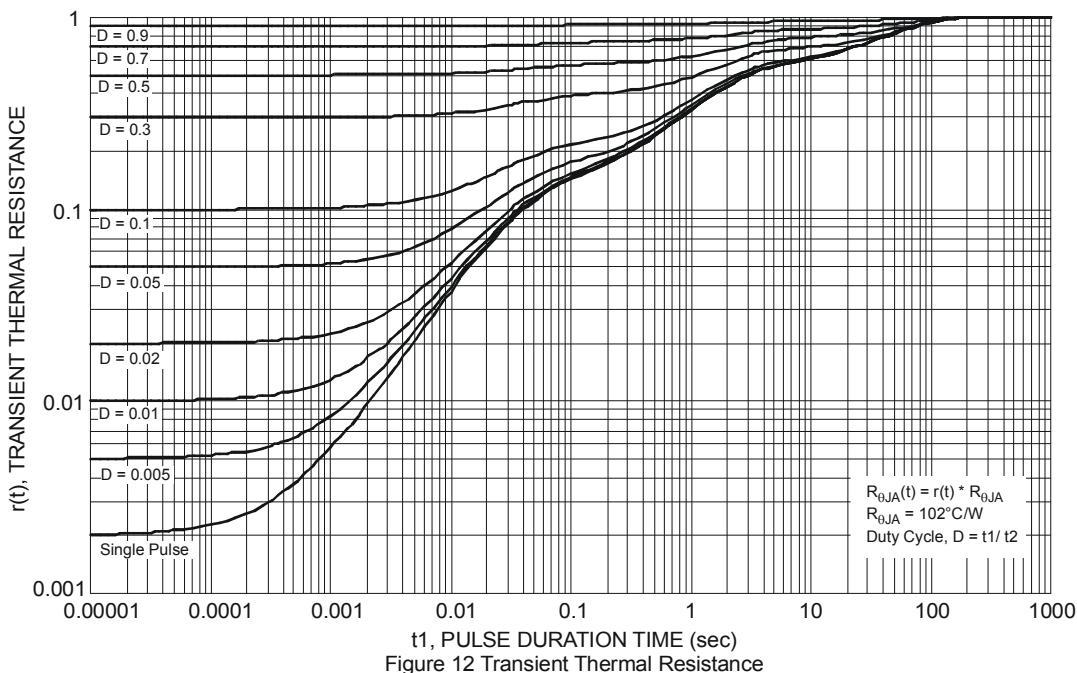
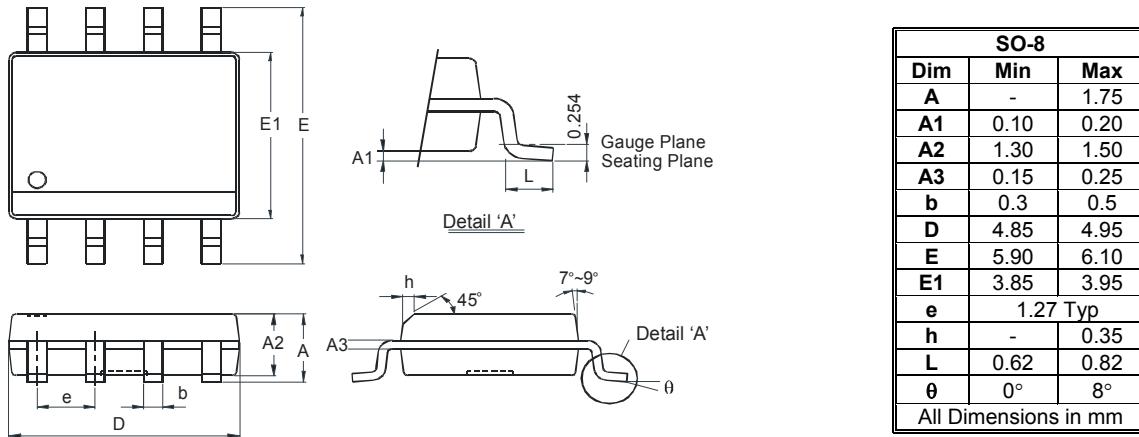


Figure 11 SOA, Safe Operation Area



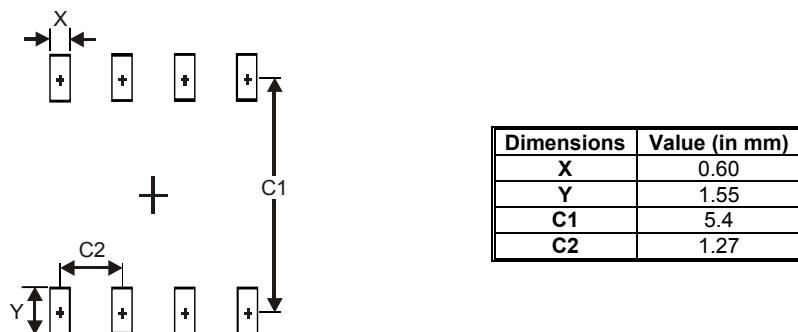
Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for latest version.



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