REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor CAGE number 75569 to the drawing. Add vendor CAGE number 6Y440 to device types 03LX, 03XX, 04LX, and 04XX. Removed Vendor CAGE number OBK02 from drawing as approved source of supply. Editorial changes throughout.	89-10-16	M. A. Frye
B	Drawing updated to reflect current requirements. Editorial changes throughout. - gap	00-10-23	Raymond Monnin
C	Boilerplate update and part of five year review. tcr	07-02-23	Joseph Rodenbeck

THE FRONT PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
James E. Jamison

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-10-22

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 256K X 1 SRAM, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
C	A	**67268**	**5962-88725**

SHEET 1 OF 14

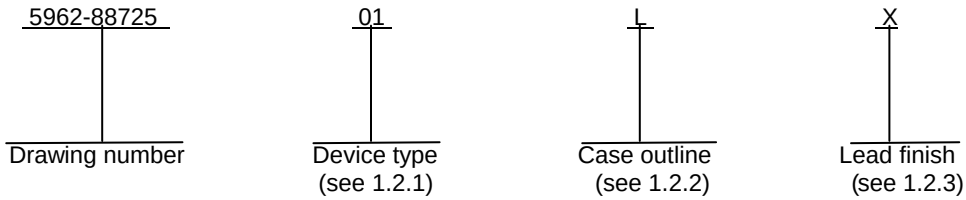
DSCC FORM 2233
APR 97

5962-E271-07

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	5C2561	256K x 1 CMOS SRAM	35 ns
02	5C2561	256K x 1 CMOS SRAM	45 ns
03	5C2561	256K x 1 CMOS SRAM	55 ns
04	5C2561	256K x 1 CMOS SRAM	70 ns
05	5C2561	256K x 1 CMOS SRAM	25 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line package
X	CQCC3-N28	28	Rectangular leadless chip carrier
Y	CDFP4-F28	28	Flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Voltage on any input relative to V_{SS}	-0.5 V dc to +7.0 V dc
Voltage applied to Q	-0.5 V dc to +6.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C 1/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage (V_{SS})	0 V
Input high voltage range (V_{IH})	+2.2 V dc to +6.0 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc 2/
Case operating temperature range (T_C)	-55°C to +125°C

1/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
2/ V_{IL} minimum = -3.0 V dc for pulse width less than 20 ns.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V V_{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Operating supply current 1/	I_{CC1}	$t_{AVAV} = t_{AVAV}$ (minimum), V_{CC} = 5.5 V, $\overline{CE}$ = V_{IL}, All other inputs at V_{IL}	1, 2, 3	01-04		120	mA
				05		135	
Standby power supply current TTL 1/	I_{CC2}	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = 5.5 V, f = 0 MHz	1, 2, 3	All		25	mA
Standby power supply current CMOS 1/	I_{CC3}	$\overline{CE} \ge (V_{CC}$ -0.2 V), f = 0 MHz, V_{CC} = 5.5 V, all other inputs < 0.2 V or > (V_{CC} -0.2 V)	1, 2, 3	All		20	mA
Input leakage current, any input	I_{ILK}	V_{CC} = 5.5 V, V_{IN} = 0 V to 5.5 V	1, 2, 3	All		±10	µA
Off-state output leakage current	I_{OLK}	V_{CC} = 5.5 V, V_{IN} = 0 V to 5.5 V	1, 2, 3	All		±10	µA
Output high voltage	V_{OH}	I_{OUT} = -4.0 mA, V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	I_{OUT} = 8.0 mA, V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All		0.4	V
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1.0 MHz, T_C = 25°C, See 4.3.1c	4	All		10.0	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, f = 1.0 MHz, T_C = 25°C, See 4.3.1c	4	All		12.0	pF
Chip enable access time	t_{ELQV}	See figure 3 2/	9, 10, 11	01		35	ns
				02		45	
				03		55	
				04		70	
				05		25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V V_{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle time	t_{AVAV}	See figure 3 2/, 3/	9, 10, 11	01	35		ns
				02	45		
				03	55		
				04	70		
				05	25		
Address access time	t_{AVQV}	See figure 3 2/, 4/	9, 10, 11	01		35	ns
				02		45	
				03		55	
				04		70	
				05		25	
Output hold after address change	t_{AVQX}	See figure 3 2/,	9, 10, 11	All	3.0		ns
Chip enable to output active	t_{ELQX}	See figure 3 2/, 5/, 6/	9, 10, 11	All	3.0		ns
Chip disable to output inactive	t_{EHQZ}	See figure 3 2/, 5/, 6/	9, 10, 11	01, 02, 05	0	20	ns
				03	0	25	
				04	0	30	
Chip enable to power up	t_{ELPU}	See figure 3 2/, 5/	9, 10, 11	All	0		ns
Chip enable to power down	t_{EHPD}	See figure 3 2/, 5/	9, 10, 11	01		35	ns
				02		45	
				03		55	
				04		70	
				05		25	
Write cycle time	t_{AVAV}	See figure 4 2/	9, 10, 11	01	35		ns
				02	45		
				03	55		
				04	70		
				05	25		
Write pulse width	t_{WLWH}	See figure 4 2/	9, 10, 11	01	30		ns
				02	40		
				03	50		
				04	55		
				05	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V V_{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip enable to end of write	t_{ELEH}	See figure 4 2/	9, 10, 11	01	30		ns
				02	40		
				03	50		
				04	55		
				05	20		
Data setup to end of write	t_{DVWH}	See figure 4 2/	9, 10, 11	01, 02	20		ns
				03, 04	25		
				05	16		
Data hold after end of write	t_{WHDX}	See figure 4 2/	9, 10, 11	All	2.0		ns
Address setup to end of write	t_{AVWH}	See figure 4 2/	9, 10, 11	01	30		ns
				02	40		
				03	50		
				04	55		
				05	20		
Address setup to beginning of write	t_{AVWL}	See figure 4 2/ (write cycle number 1)	9, 10, 11	All	0		ns
	t_{AVEL}	See figure 4 2/ (write cycle number 2)	9, 10, 11	All	2.0		ns
Address hold after end of write	t_{WHAV}	See figure 4 2/	9, 10, 11	All	5.0		ns
Write enable to output disable	t_{WLQZ}	See figure 4 2/, 5/, 6/	9, 10, 11	01, 05	0	15	ns
				02	0	20	
				03	0	25	
				04	0	30	
Output active after end of write	t_{WHQX}	See figure 4 2/, 5/, 6/, 7/	9, 10, 11	All	0		ns

1/ I_{CC} is dependent upon output loading and cycle rate. The specified values apply with output(s) unloaded.
2/ AC measurements assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading of 30 pF load capacitance. Output timing reference is 1.5 V. See figure 5.
3/ For read cycles 1 and 2, $\overline{WE}$ is high for entire cycle.
4/ Device is continuously selected, $\overline{CE}$ low.
5/ Parameter, if not tested, shall be guaranteed to the limits specified in table I.
6/ Measured ±500 mV from steady-state output voltage. Load capacitance is 5.0 pF.
7/ If $\overline{WE}$ is low when $\overline{CE}$ goes low, the output remains in the high impedance state.

Device types	01 through 05		
Case outlines	L	X	Y
Terminal number	Terminal symbol		
1	A	A	A
2	A	A	A
3	A	A	A
4	A	NC	A
5	A	A	A
6	A	A	A
7	A	A	NC
8	A	A	NC
9	A	A	A
10	Q	A	A
11	$\overline{WE}$	Q	A
12	V_{SS}	NC	Q
13	$\overline{CE}$	$\overline{WE}$	$\overline{WE}$
14	D	V_{SS}	V_{SS}
15	A	$\overline{CE}$	$\overline{CE}$
16	A	D	D
17	A	A	A
18	A	NC	A
19	A	A	A
20	A	A	A
21	A	A	NC
22	A	A	NC
23	A	A	A
24	V_{CC}	A	A
25	---	A	A
26	---	NC	A
27	---	A	A
28	---	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

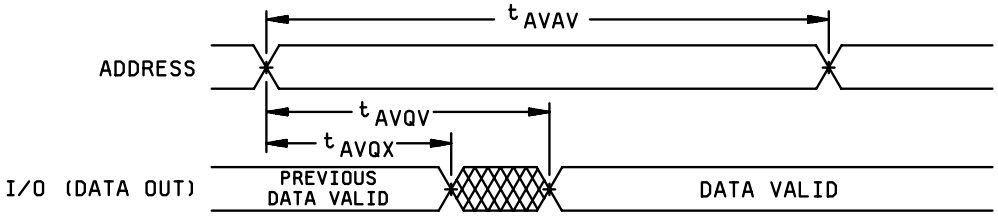
Device types 01 through 05

$\overline{CE}$	$\overline{WE}$	Mode	I/O	Power
H	X	Not selected	High Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

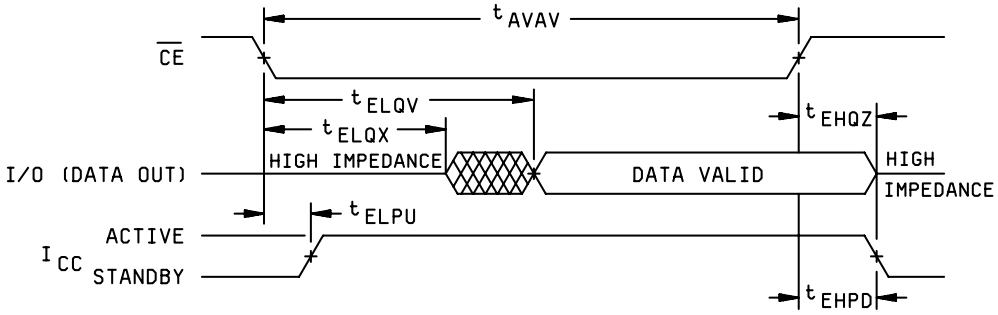
H = Logic “1” state
L = Logic “0” state
X = Don’t care

FIGURE 2. Truth table.

READ CYCLE NO. 1 ($\overline{WE}$ HIGH, $\overline{CE}$ LOW) (See notes 1, 2, and 3)



READ CYCLE NO. 2 ($\overline{WE}$ HIGH) (See notes 1 and 2)

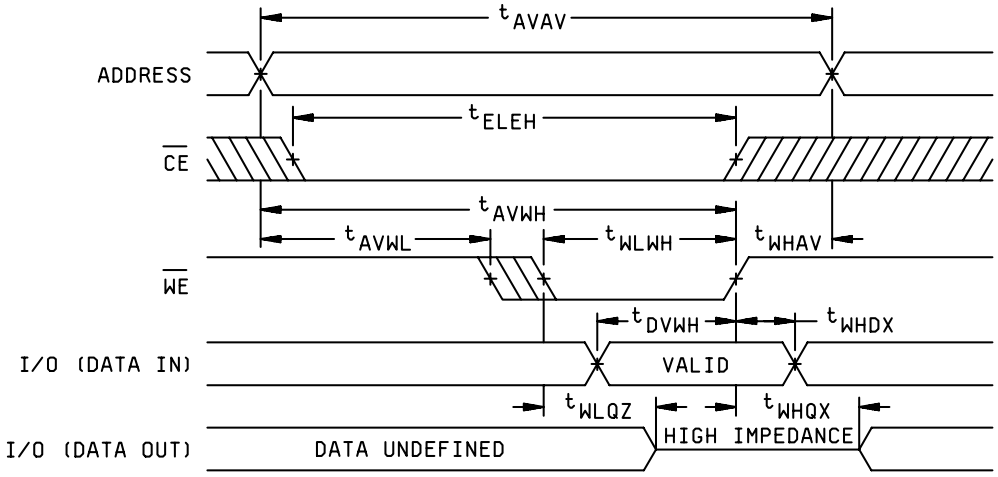


NOTES:

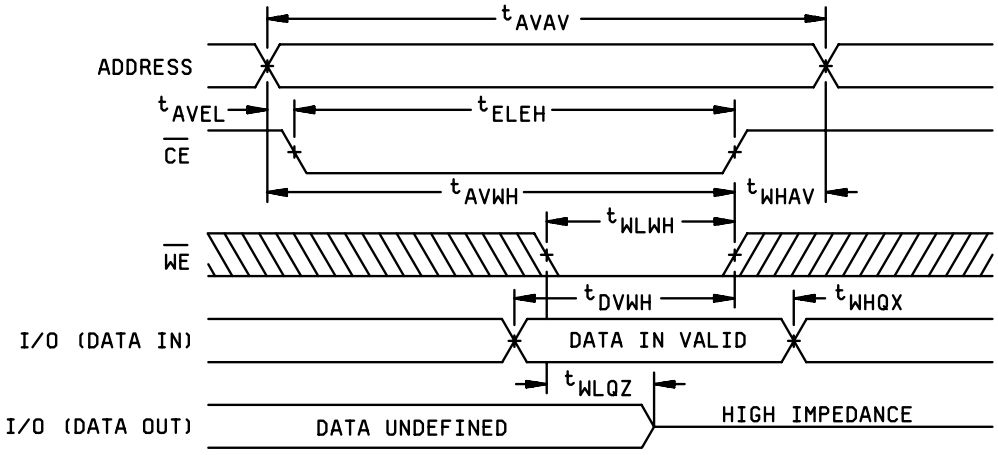
1. $\overline{WE}$ is high for entire cycle.
2. $\overline{CE}$ and $\overline{WE}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in monotonic fashion.
3. Device is continuously selected, $\overline{CE}$ low.

FIGURE 3. Read cycle timing diagrams.

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (See notes 1 and 2)



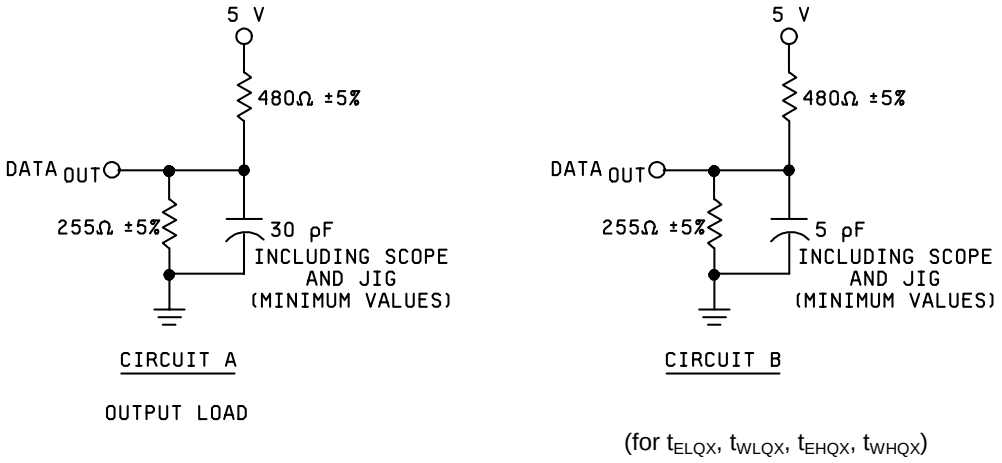
WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED) (See notes 1 and 2)



NOTES:

1. $\overline{CE}$ and $\overline{WE}$ must transition between V_{IH} (min) to V_{IL} (max) to V_{IH} (min) in monotonic fashion.
2. $\overline{CE}$ and $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.

FIGURE 4. Write cycle timing diagram.



OUTPUT LOAD

(for t_{ELQX}, t_{WLQX}, t_{EHQX}, t_{WHQX})

AC test conditions	
Input pulse levels	GND to 3.0 V
Input rise fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 5. Output load circuits.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* PDA applies to subgroup 1 and 7.
** See 4.3.1c.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-02-23

Approved sources of supply for SMD 5962-88725 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8872501LA	0EU86	MT5C2561C-35
	0C7V7	CY7C197-35DMB
	3/	EDI81256C35QB
	3/	P4C1257-35CMB
	3/	IDT71257S35CB
	3/	HM1-65797K/883
5962-8872501XA	0EU86	MT5C2561EC-35
	0C7V7	CY7C197-35LMB
	3/	EDI81256C35LB
	3/	P4C1257-35LMB
5962-8872501YA	0C7V7	CY7C197-35FMB
	3/	EDI81256C35FB
5962-8872502LA	0EU86	MT5C2561C-45
	0C7V7	CY7C197-45DMB
	3/	EDI81256C45LB
	3/	P4C1257-45LMB
	3/	IDT71257S45CB
	3/	HM1-65797M/883
5962-8872502XA	0EU86	MT5C2561EC-45
	0C7V7	CY7C197-45LMB
	3/	EDI81256C45LB
	3/	P4C1257-45LMB
5962-8872502YA	0C7V7	CY7C197-45FMB
	3/	EDI81256C45FB
5962-8872503LA	0EU86	MT5C2561C-55
	0C7V7	CY7C197-55DMB
	3/	EDI81256C55QB
	3/	P4C1257-55CMB
	3/	IDT71257S55CB
	3/	HM1-65797N/883
5962-8872503XA	0EU86	MT5C2561EC-55
	0C7V7	CY7C197-55LMB
	3/	EDI81256C55LB
	3/	P4C1257-55LMB

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8872503YA	0C7V7	CY7C197-55FMB
	3/	EDI81256C55FB
5962-8872504LA	0EU86	MT5C2561C-70
	0C7V7	CY7C197-70DMB
	3/	EDI81256C70QB
	3/	P4C1257-70CMB
	3/	IDT71257S70CB
	3/	HM1-65797N/883
5962-8872504XA	0EU86	MT5C2561EC-70
	0C7V7	CY7C197-70LMB
	3/	EDI81256C70LB
	3/	P4C1257-70LMB
5962-8872504YA	0C7V7	CY7C197-70FMB
	3/	EDI81256C70FB
5962-8872505LA	0EU86	MT5C2561C-25
	0C7V7	CY7C197-25DMB
	3/	IDT71257S25CB
	3/	P4C1257-25CMB
	3/	HM1-65797H/883
5962-8872505XA	0EU86	MT5C2561EC-25
	0C7V7	CY7C197-25LMB
	3/	P4C1257-25LMB
5962-8872505YA	0C7V7	CY7C197-25FMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0EU86	Austin Semiconductor International L.P. 8701 Cross Park Drive Austin, TX 78754-4566
0C7V7	QP Semiconductor 2945 Oakmead Village Ct. Santa Clara, CA 95051-0812