Spansion® Analog and Microcontroller Products

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There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal document improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

Spansion continues to support existing part numbers beginning with “MB”. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

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FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13753-3E

16-bit Microcontrollers

CMOS

F²MC-16LX MB90990 Series

MB90F997JBS/F997MBS/ MB90V950AJAS/V950AMAS

■ DESCRIPTION

The MB90990-series, loaded 1 channel FULL-CAN interface and Flash ROM, is general-purpose FUJITSU 16-bit microcontroller designing for automotive and industrial applications. Its main feature is the on-board CAN Interfaces, which conform to Ver 2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal FULL-CAN approach. With the new 0.18 µm CMOS technology, Fujitsu now offers on-chip Flash ROM program memory up to 128 Kbytes.

The power supply (1.8 V) is supplied to the MCU core from an internal regulator circuit. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 31.25 ns instruction execution time from an external 4 MHz clock. Also, the main clock can be monitored using the clock supervisor function.

The unit features a 4-channel input capture unit 1 channel 16-bit free-run timer, 2-channel LIN-UART,1 channel UART, and 16-channel 8/10-bit A/D converter as the peripheral resource.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

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FUJITSU

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■ FEATURES

- **Clock**
  - Built-in PLL clock frequency multiplication circuit
  - Selection of machine clocks (PLL clocks) is allowed among frequency division by 2 on oscillation clock and multiplication of 1 to 8 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 32 MHz)
  - Minimum execution time of instruction : 31.25 ns (when operating with 4-MHz oscillation clock and 8-time multiplied PLL clock)
- **Clock supervisor (only for devices with J-suffix)**
  - Main clock is monitored
  - Internal CR oscillation clock (100 kHz typical) can be used as sub clock
- **16 Mbytes CPU memory space**
  24-bit internal addressing
- **Instruction system best suited to controller**
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - Enhanced multiply-divide instructions with sign and RETI instructions
  - Enhanced high-precision computing with 32-bit accumulator
- **Instruction system compatible with high-level language (C language) and multitask**
  - Employing system stack pointer
  - Enhanced various pointer indirect instructions
  - Barrel shift instructions
- **Increased processing speed**
  4-byte instruction queue
- **Powerful interrupt function**
  - Powerful 8-level, 34-condition interrupt feature
  - 8 channels external interrupts are supported
- **CPU-independent automatic data transfer function**
  Expanded intelligent I/O service function (EI^{2}OS) : up to 16 channels
- **Low power consumption (standby) mode**
  Sleep mode (a mode that halts CPU operating clock)
- **Timebase timer mode**
  - Main timer mode (timebase timer mode that is transferred from main clock mode)
  - PLL timer mode (timebase timer mode that is transferred from PLL clock mode)
  - Watch mode (a mode that operates sub clock and watch timer only)
  - Stop mode (a mode that stops oscillation clock and sub clock)
  - CPU blocking operation mode
- **Process**
  CMOS technology
- **I/O port**
  General purpose input/output port (CMOS output) :36 ports

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- **Timer**
  - Timebase timer, watch timer, watchdog timer : 1 channel
  - 8/16-bit PPG timer : 8-bit × 6 channels or 16-bit × 3 channels
  - 16-bit reload timer : 2 channels
  - 16- bit input/output timer
    - 16-bit free-run timer : 1 channel (FRT0 : ICU 0/1/2/3)
    - 16- bit input capture : (ICU) : 4 channels
- **FULL-CAN interface : 1 channel**
  - Compliant with CAN specifications Version 2.0 A and B
  - 16 message buffers are built in
  - CAN wake-up function
- **UART (LIN/SCI) : LIN-UART × 2 channels, UART × 1 channel**
  - Equipped with full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transmission is available
- **DTP/External interrupt : up to 8 channels, CAN wakeup : up to 1 channel**
  Module for activation of expanded intelligent I/O service (EI^{2}OS) and generation of external interrupt by external input
- **Delay interrupt generator module**
  Generates interrupt request for task switching
- **8/10-bit A/D converter : 16 channels**
  - Resolution is selectable between 8-bit and 10-bit
  - Activation by external trigger input is allowed
  - Conversion time : 3 µs (at 32-MHz machine clock, including sampling time)
- **Program patch function**
  Address matching detection for 6 address pointers
- **Low voltage/CPU operation detection reset (devices with J-suffix)**
  - Detects low voltage (Set the voltage 2.8 V to 4.2 V.) and resets automatically
  - Resets automatically when program is runaway and counter is not cleared within interval time
    (Set in the programming approx.16.4 ms to approx.524 ms for external 4 MHz operation.)
- **Clock calibration unit (products with J-suffix)**
  Capable of improving precision of CR oscillation circuit by calculating calibration value from measurement and performing trimming.
- **Capable of changing input voltage for port**
  Automotive/CMOS-Schmitt input level (initial level is Automotive in single-chip mode)
- **Flash memory security function**
  Protects the content of Flash memory
- **8-bit D/A converter : 1 channel**

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■ PRODUCT LINEUP

Part number / Parameter	MB90V950AMAS	MB90V950AJAS	MB90F997JBS	MB90F997MBS
Type	Evaluation product		Flash memory product	
CPU	F²MC-16LX CPU			
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, ×8, 1/2 when PLL stops) Minimum instruction execution time : 31.25 ns (Oscillation clock 4 MHz PLL ×8)			
ROM	External		Main 128 Kbytes Satellite 32 Kbytes	
RAM	30 Kbytes		8 Kbytes	
Emulator-specific power supply*1	Yes		—	
FPGA data*2	Rev 050617		—	
Adaptor board*2	MB2147-20 Rev.04C or later		—	
Clock supervisor	No	Yes	Yes	No
Clock calibration unit	No	Yes	Yes	No
Low-voltage/CPU operation detection reset	No	Yes (Corresponds to CPU operation detection reset only)	Yes	No
Technology	0.35 µm CMOS with built-in power supply regulator		0.18 µm CMOS with built-in power supply regulator + Flash memory with charge pump for programming voltage	
Operation voltage range	5 V ± 10 %		3.0 V to 5.5 V : When normal operating	
Operation ambient temperature	—		–40 °C to +105 °C	
Package	PGA-299		LQFP-48	
UART	7 channels		LIN-UART × 2 channels, UART × 1 channel	
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device (Supported by LIN-UART only)			
I²C (400 kbps)	2 channels		—	
A/D converter	24 channels		16 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 µs include sample time (per one channel)			
16-bit Reload timer	4 channels		2 channels	
	Operation clock frequency : fsys/2¹, fsys/2³, fsys/2⁵ (fsys = Machine clock frequency) Supports External Event Count function			

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Part number / Parameter	MB90V950AMAS	MB90V950AJAS	MB90F997JBS	MB90F997MBS
16-bit I/O timer	2 channels		1 channel	
	Generates an interrupt signal on overflow Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock freq.) I/O Timer 0 (clock input FRCK0) corresponds to ICU0/1/2/3, OCU 0/1/2/3 I/O Timer 1 (clock input FRCK1) corresponds to ICU4/5/6/7, OCU 4/5/6/7			
16-bit Output compare	8 channels		—	
	Generates an interrupt signal when one of the 16-bit I/O timer matches the output compare register A pair of compare registers can be used to generate an output signal.			
16-bit Input capture	8 channels		4 channels	
	Rising edge, falling edge or rising & falling edge sensitive Signals an interrupt upon external event			
8/16-bit PPG	8 channels (16-bit) /16 channels (8-bit) Sixteen 8-bit reload counters Sixteen 8-bit reload registers for L pulse width Sixteen 8-bit reload registers for H pulse width		3 channels (16-bit) /6 channels (8-bit) Six 8-bit reload counters Six 8-bit reload registers for L pulse width Six 8-bit reload registers for H pulse width	
	Supports 8-bit and 16-bit operation modes A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operating clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
CAN Interface	3 channels		1 channel	
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission in response to Remote Frames Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps			
External interrupt (8 channels)	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, expanded intelligent I/O services (EI^{2}OS)			
D/A Converter	2 channels		1 channel	
Sub clock	No	Yes	Yes	No

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Part number / Parameter	MB90V950AMAS	MB90V950AJAS	MB90F997JBS	MB90F997MBS
I/O Ports	Virtually all external pins can be used as general purpose I/O port All ports are push-pull outputs Bit-wise settable as input/output or peripheral signal Can be configured 8 as CMOS schmitt trigger/ automotive inputs (in blocks of 8 pins) TTL input level settable for external bus (32-pin only for external bus)			
Flash memory (Flash memory product only)	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Boot block configuration Erase can be performed on each block Flash Security			

*1: It is setting of Jumper switch (TOOL VCC) when emulator (MB2147-01) is used. Please refer to the Emulator hardware manual for the details.

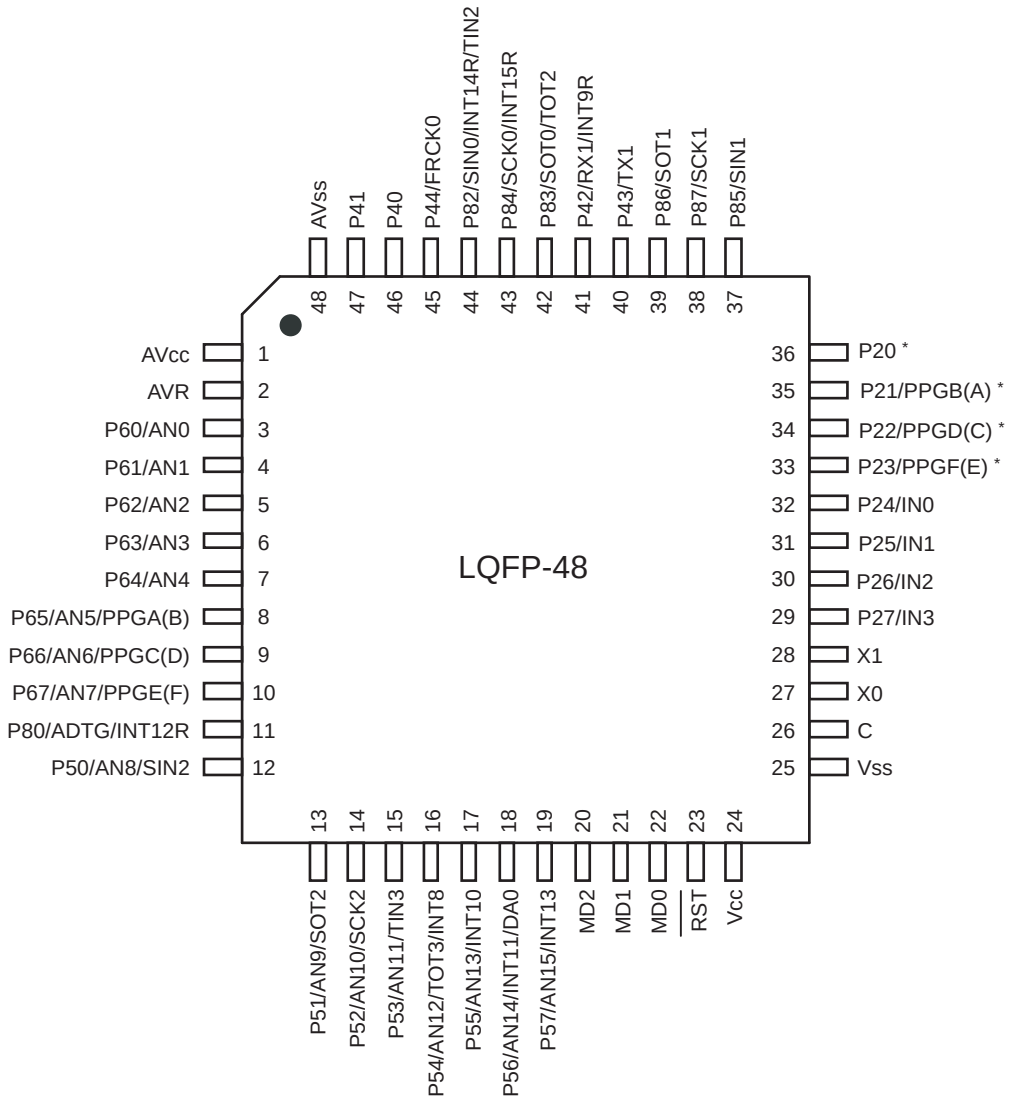
*2: Customers considering the use of other FPGA data and the adaptor boards should consult with sales representatives.

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■ PIN ASSIGNMENT

• MB90F997MBS, MB90F997JBS

(TOP VIEW)



(FPT-48P-M26)

* : High current output port

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■ PIN DESCRIPTION

Pin No.	Pin name	I/O circuit type*	Function
1	AV_{CC}	I	V_{CC} power input pin for analog circuit.
2	AVR	—	Power (Vref+) input pin for A/D converter. It should be below V_{CC}.
3 to 7	P60 to P64	H	General-purpose I/O ports.
	AN0 to AN4		Analog input pins for A/D converter.
8 to 10	P65 to P67	H	General-purpose I/O ports.
	AN5 to AN7		Analog input pins for A/D converter.
	PPGA (B) , PPGC (D) , PPGE (F)		Output pins for PPG.
11	P80	F	General-purpose I/O port.
	ADTG		Trigger input pin for A/D converter.
	INT12R		External interrupt request input pin for INT12R.
12	P50	L	General-purpose I/O port.
	AN8		Analog input pin for A/D converter.
	SIN2		Serial data input pin for UART2.
13	P51	H	General-purpose I/O port.
	AN9		Analog input pin for A/D converter.
	SOT2		Serial data output pin for UART2.
14	P52	H	General-purpose I/O port.
	AN10		Analog input pin for A/D converter.
	SCK2		Clock I/O pin for UART2.
15	P53	H	General-purpose I/O port.
	AN11		Analog input pin for A/D converter.
	TIN3		Event input pin for reload timer 3.
16	P54	H	General-purpose I/O port.
	AN12		Analog input pin for A/D converter.
	TOT3		Output pin for reload timer 3.
	INT8		External interrupt request input pin for INT8.
17	P55	H	General-purpose I/O port.
	AN13		Analog input pin for A/D converter.
	INT10		External interrupt request input pin for INT10.

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Pin No.	Pin name	I/O circuit type*	Function
18	P56	M	General-purpose I/O port.
	AN14		Analog input pin for A/D converter.
	INT11		External interrupt request input pin for INT11.
	DA0		Analog output pin for D/A converter.
19	P57	H	General-purpose I/O port. (Different I/O circuit type from those in MB90V950AJAS, MB90V950AMAS).
	AN15		Analog input pin for A/D converter.
	INT13		External interrupt request input pin for INT13.
20	MD2	D	Input pin for operation mode specification.
21, 22	MD1, MD0	C	Input pins for operation mode specification.
23	$\overline{RST}$	E	Reset input pin.
24	V_{CC}	—	Power input pin (3.5 V to 5.5 V) .
25	V_{SS}	—	Power input pin (0 V) .
26	C	I	Power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 µF ceramic condenser.
27	X0	A	Oscillation input pin.
28	X1		Oscillation output pin.
29 to 32	P27 to P24	G	General-purpose I/O ports. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	IN3 to IN0		Event input pins for input capture 0 to 3.
33 to 35	P23 to P21	J	General-purpose I/O ports. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. High current output port. (Different I/O circuit type from those in MB90V950AJAS,MB90V950AMAS).
	PPGF (E) , PPGD (C) , PPGB(A)		Output pins for PPG.
36	P20	J	General-purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. High current output port. (Different I/O circuit type from those in MB90V950AJAS,MB90V950AMAS).
37	P85	K	General-purpose I/O port.
	SIN1		Serial data input pin for UART1.
38	P87	F	General-purpose I/O port.
	SCK1		Clock I/O pin for UART1.

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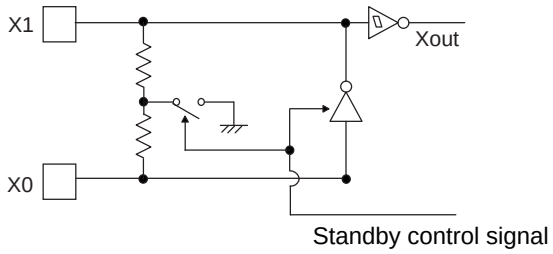
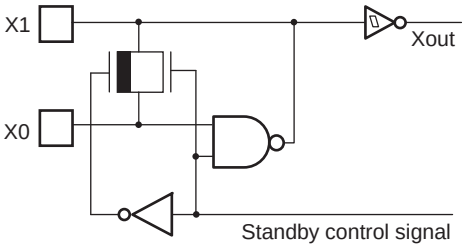
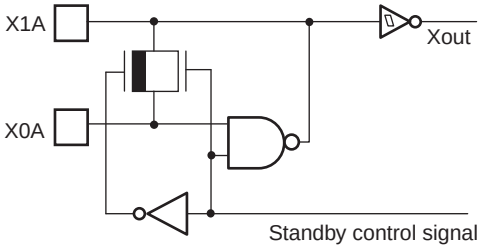
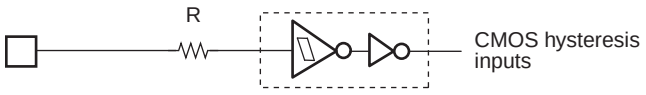
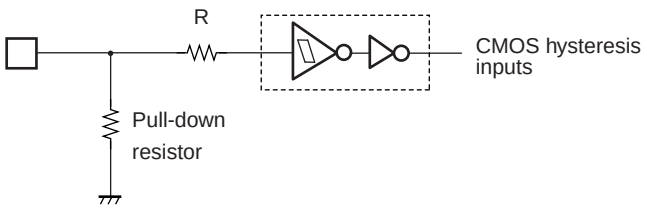
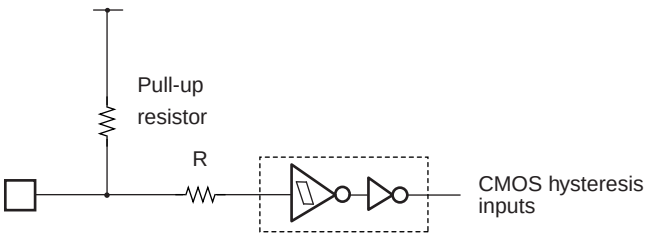
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Pin No.	Pin name	I/O circuit type*	Function
39	P86	F	General-purpose I/O port.
	SOT1		Serial data output pin for UART1.
40	P43	F	General-purpose I/O port.
	TX1		TX output pin for CAN1 interface.
41	P42	F	General-purpose I/O port.
	RX1		RX input pin for CAN1 interface.
	INT9R		External interrupt request input pin for INT9R.
42	P83	F	General-purpose I/O port.
	SOT0		Serial data output pin for UART0.
	TOT2		Output pin for reload timer 2.
43	P84	F	General-purpose I/O port.
	SCK0		Clock I/O pin for UART0.
	INT15R		External interrupt request input pin for INT15R.
44	P82	K	General-purpose I/O port.
	SIN0		Serial data input pin for UART0.
	INT14R		External interrupt request input pin for INT14R.
	TIN2		Event input pin for reload timer 2.
45	P44	F	General-purpose I/O port (Different I/O circuit type from those in MB90V950AJAS, MB90V950AMAS) .
	FRCK0		Free-run timer 0 clock input pin.
46, 47	P40, P41	F	General-purpose I/O ports.
48	AV_{SS}	I	V_{SS} power input pin for analog circuit.

* : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

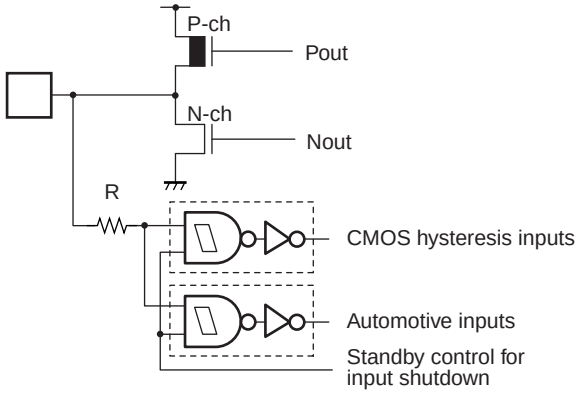
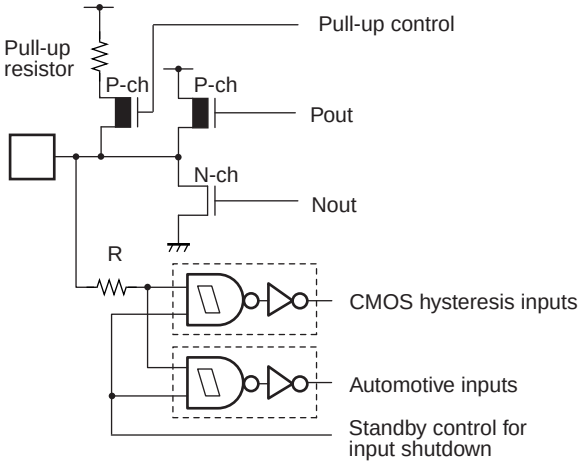
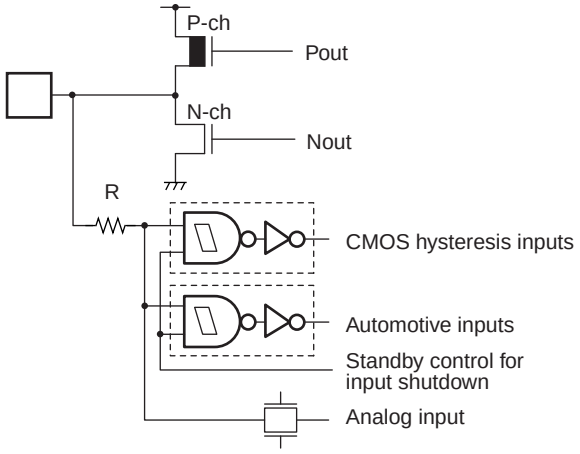
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■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation circuit : High-speed oscillation feedback resistor = approx. 1 MΩ (Flash memory product)
		Oscillation circuit : High-speed oscillation feedback resistor = approx. 1 MΩ (Evaluation product)
B		Oscillation circuit : Low-speed oscillation feedback resistor = approx. 10 MΩ
C		• Evaluation product : CMOS hysteresis input • Flash memory product CMOS input
D		• Evaluation product : CMOS hysteresis input • Flash memory product - CMOS input - No Pull-down
E		CMOS hysteresis input

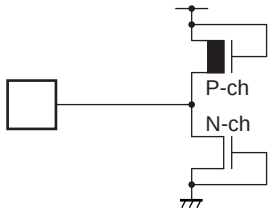
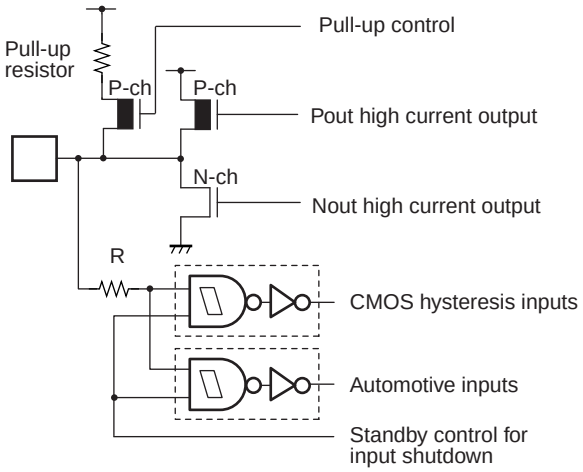
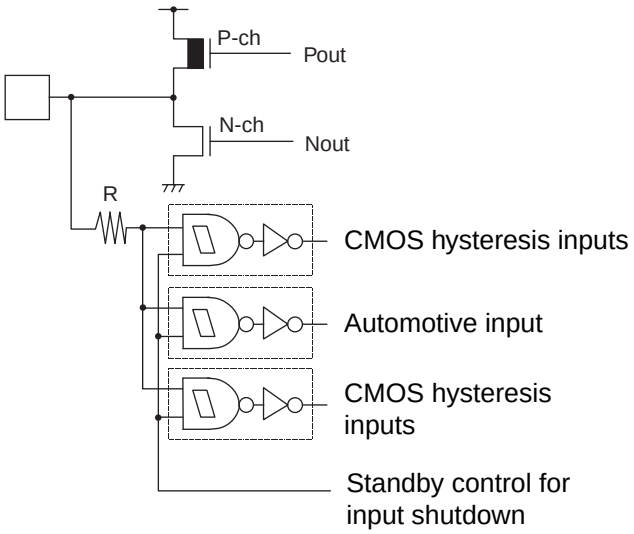
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Type	Circuit	Remarks
F		• CMOS level output (I_{OL} = 4 mA, I_{OH} = – 4 mA) • CMOS hysteresis inputs (V_{IH} 0.8Vcc V_{IL} 0.2Vcc) (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)
G		• CMOS level output (I_{OL} = 4 mA, I_{OH} = – 4 mA) • CMOS hysteresis inputs (V_{IH} 0.8Vcc V_{IL} 0.2Vcc) (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)
H		• CMOS level output (I_{OL} = 4 mA, I_{OH} = – 4 mA) • CMOS hysteresis inputs (V_{IH} 0.8Vcc V_{IL} 0.2Vcc) (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D analog input

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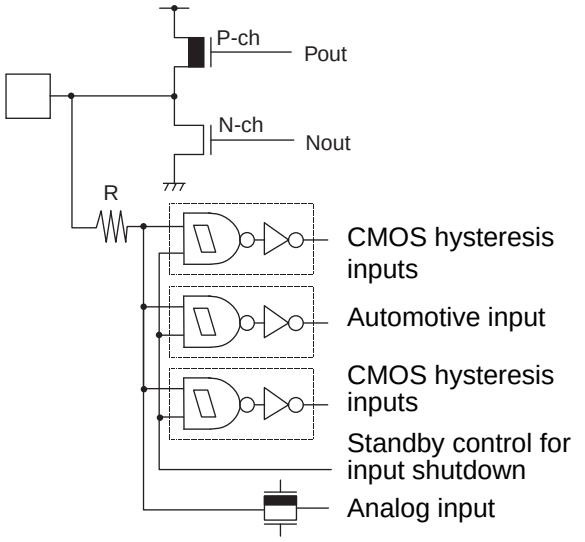
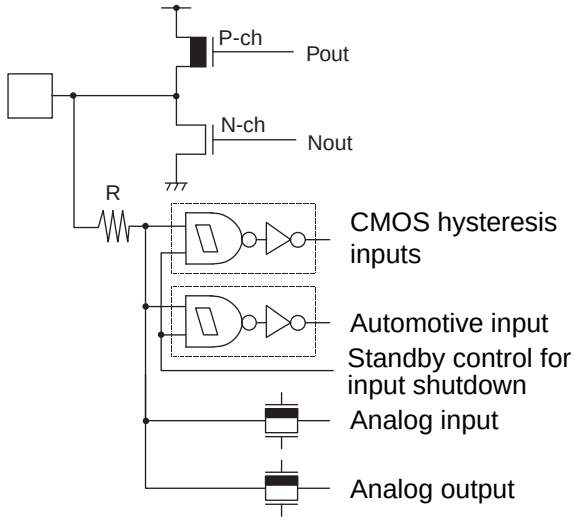
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Type	Circuit	Remarks
I		Protection circuit for power supply input
J		• CMOS level output (I_{OL} = 20 mA, I_{OH} = – 14 mA) (I_{OL} = 4 mA, I_{OH} = – 4 mA) • CMOS hysteresis inputs (V_{IH} 0.8Vcc V_{IL} 0.2Vcc) (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)
K		• CMOS level output (I_{OL} = 4 mA, I_{OH} = – 4 mA) • CMOS hysteresis inputs (V_{IH} 0.7Vcc V_{IL} 0.3Vcc) (With standby-time input shutdown function) • Automotive input (With standby-time input shutdown function) • CMOS hysteresis inputs (V_{IH} 0.8Vcc V_{IL} 0.2Vcc) (With the standby-time input shutdown function)

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Type	Circuit	Remarks
L		• CMOS level output (I_{OL} = 4 mA, I_{OH} = – 4 mA) • CMOS hysteresis inputs (V_{IH} 0.8Vcc V_{IL} 0.2Vcc) (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • CMOS hysteresis inputs (V_{IH} 0.7Vcc V_{IL} 0.3Vcc) (With the standby-time input shutdown function) • A/D analog input
M		• CMOS level output (I_{OL} = 4 mA, I_{OH} = – 4 mA) • CMOS hysteresis inputs (V_{IH} 0.8Vcc V_{IL} 0.2Vcc) (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D analog input • D/A analog output

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■ HANDLING DEVICES

• Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} pin or lower than V_{SS} pin is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pin and V_{SS} pin.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

Use meticulous care not to exceed the rating.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVR) exceed the digital power-supply voltage.

• Treatment of unused pins

Leaving unused input pins open may result in permanent damage of the device due to misbehavior or latch-up. Therefore, they must be pulled up or pulled down through resistors. In this case, those resistors should be more than 2 kΩ.

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

• Using external clock

The high-speed oscillator pins (X0, X1) can not be used for external clock inputs.

• Notes on during operation of PLL clock mode

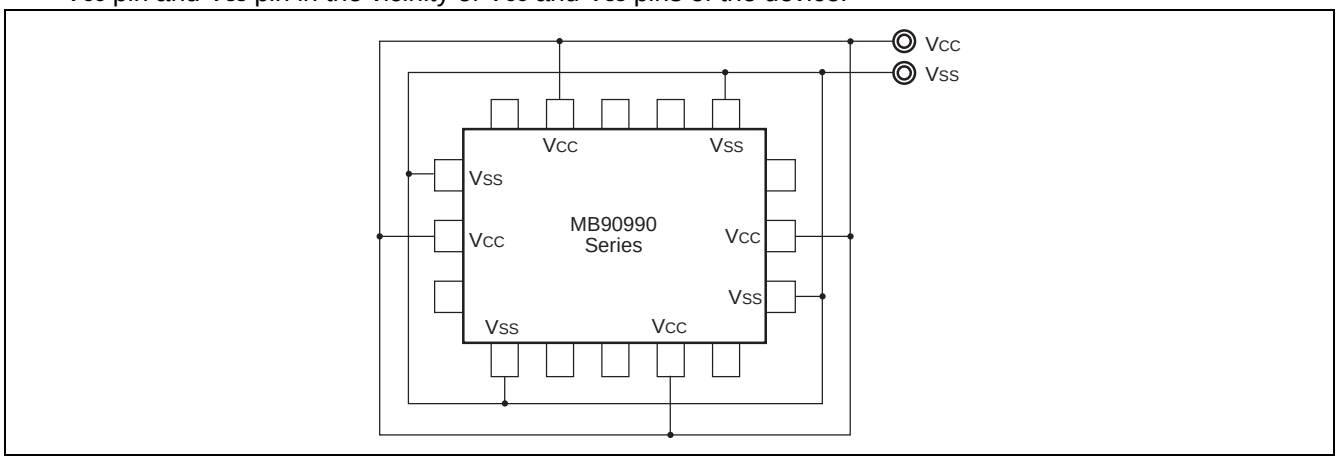
On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

• Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent malfunction such as latch-up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
- Connect V_{CC} and V_{SS} pins to the device from the current supply source at a low impedance.

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- As a measure against power supply noise, connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} pin and V_{SS} pin in the vicinity of V_{CC} and V_{SS} pins of the device.



• Pull-up/down resistors

The MB90990 series does not support internal pull-up/down resistors (Port 2 : built-in pull-up resistors) . Use external components where needed.

• Crystal oscillator circuit

Noises around X0 or X1 pins may be possible causes of malfunctions. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, that lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation. Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

• Turning-on sequence of power supply to A/D converter and analog inputs

Make sure to turn on the A/D converter power supply (AV_{CC} and AVR) and analog inputs (AN0 to AN15) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter power supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC}.

• Connection of unused pins of A/D converter if A/D converter is not used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVR = V_{SS}$.

• Notes on energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V) .

• Stabilization of power supply voltage

A sudden change in the power supply voltage may cause the device to malfunction even within the specified V_{CC} power supply voltage operating guarantee range. Therefore, the V_{CC} power supply voltage should be stabilized.

For reference, the power supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard V_{CC} power supply voltage and the coefficient of transient fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

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• **Initialization**

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

• **Notes on using CAN function**

To use CAN function, please set “1” to DIRECT bit of CAN direct mode register (CDMR) .
If DIRECT bit is set to “0” (initial value) , wait states will be performed when accessing CAN registers.

Note : Please refer to Hardware Manual of “MB90990 series for detail of CAN Direct Mode Register”.

• **Flash security function**

The security bit is located in the area of the Flash memory.
If protection code 01_H is written in the security bit, the Flash memory is in the protected state by security.
Therefore, please do not write 01_H in this address if you do not use the security function.
Please refer to following table for the address of the security bit.

	Flash memory size	Address for security bit
MB90F997	Embedded 1 Mbit Flash Memory	$FE0001_H$

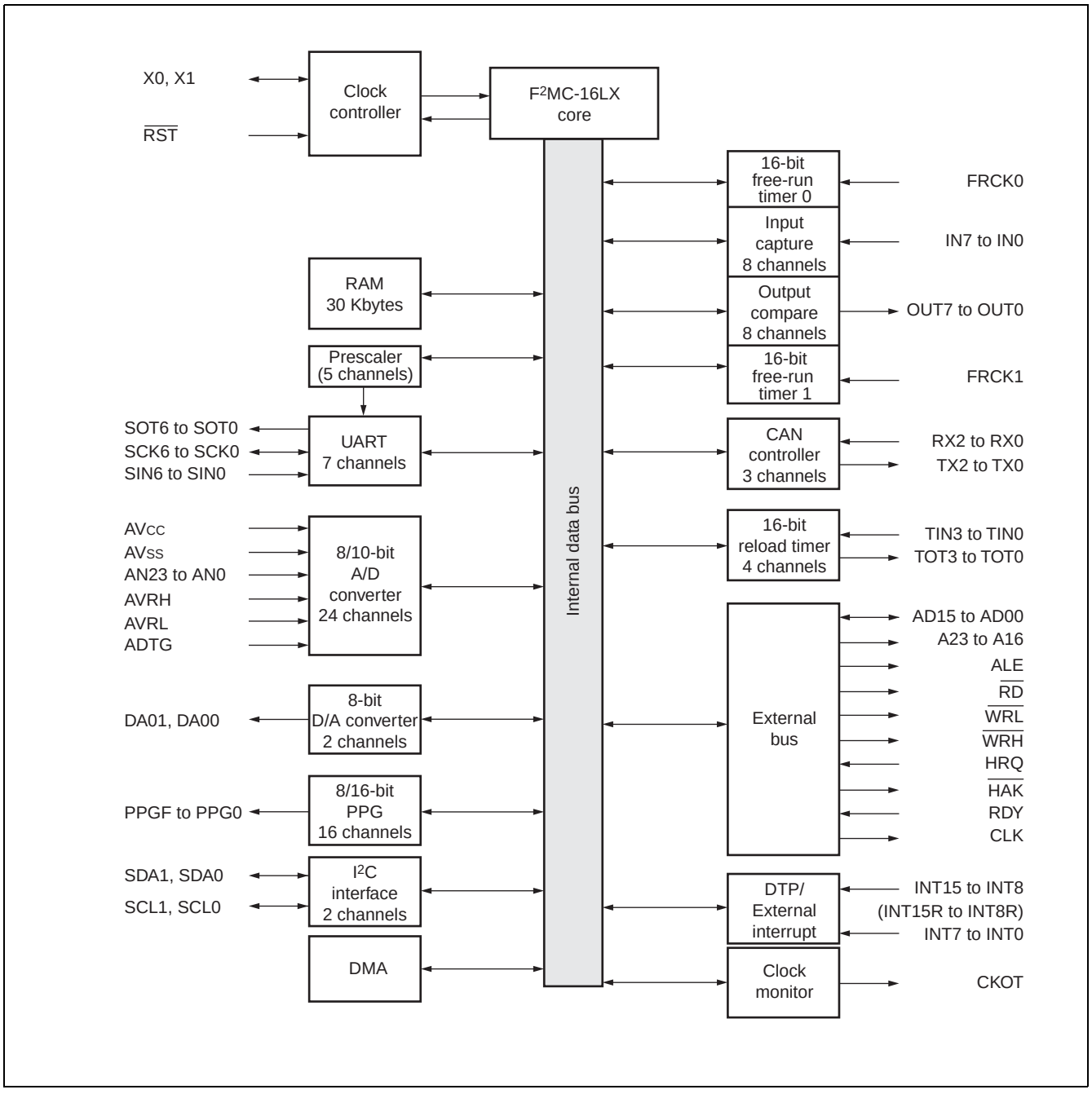
• **Correspondence with T_A = +105 °C or more**

If used exceeding T_A = +105 °C, please consult with us due to the restricted reliability.
It is ensured to write/erase data to the Flash memory between T_A = − 40 °C and +105 °C.

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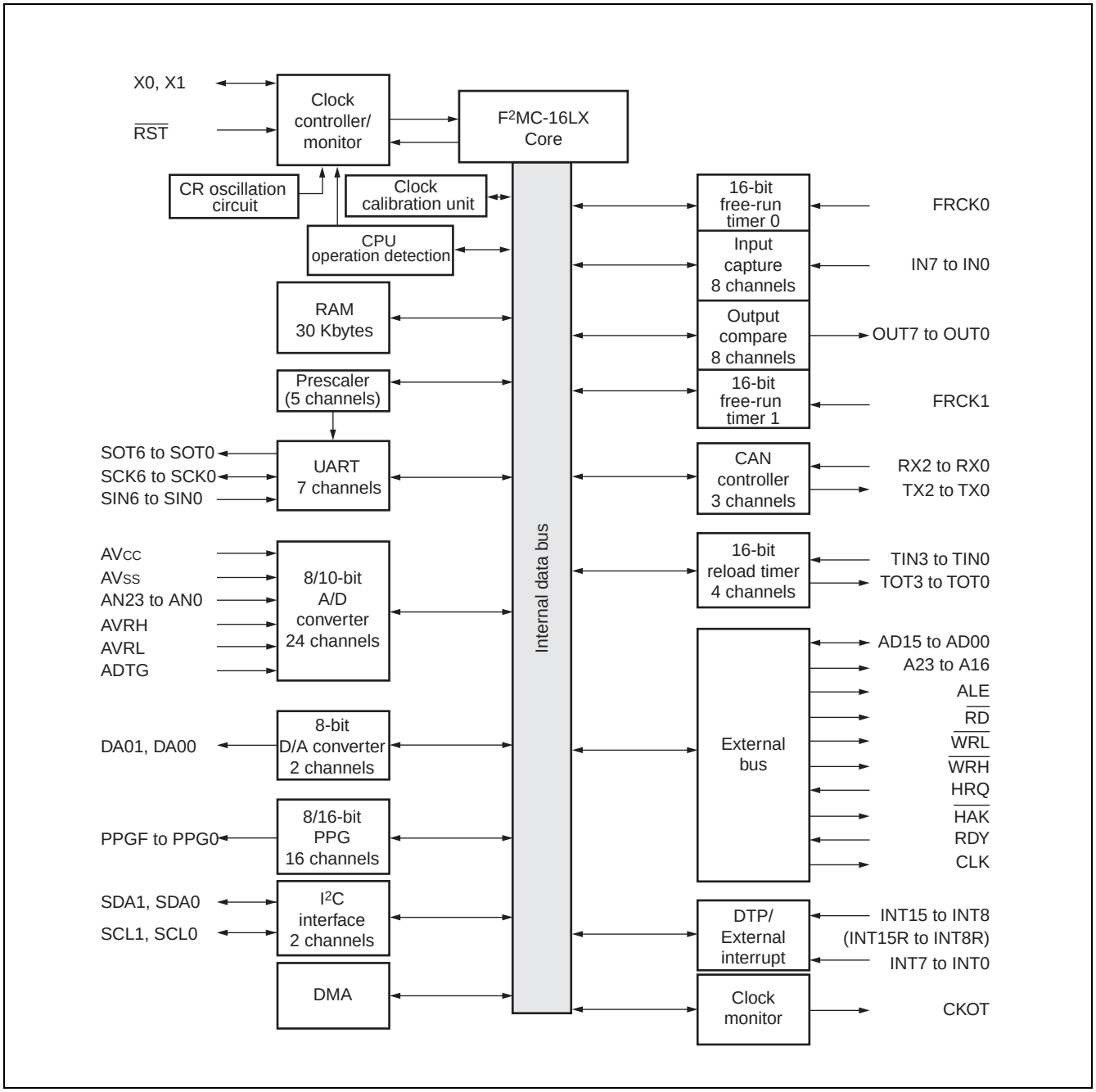
■ BLOCK DIAGRAMS

- MB90V950AMAS



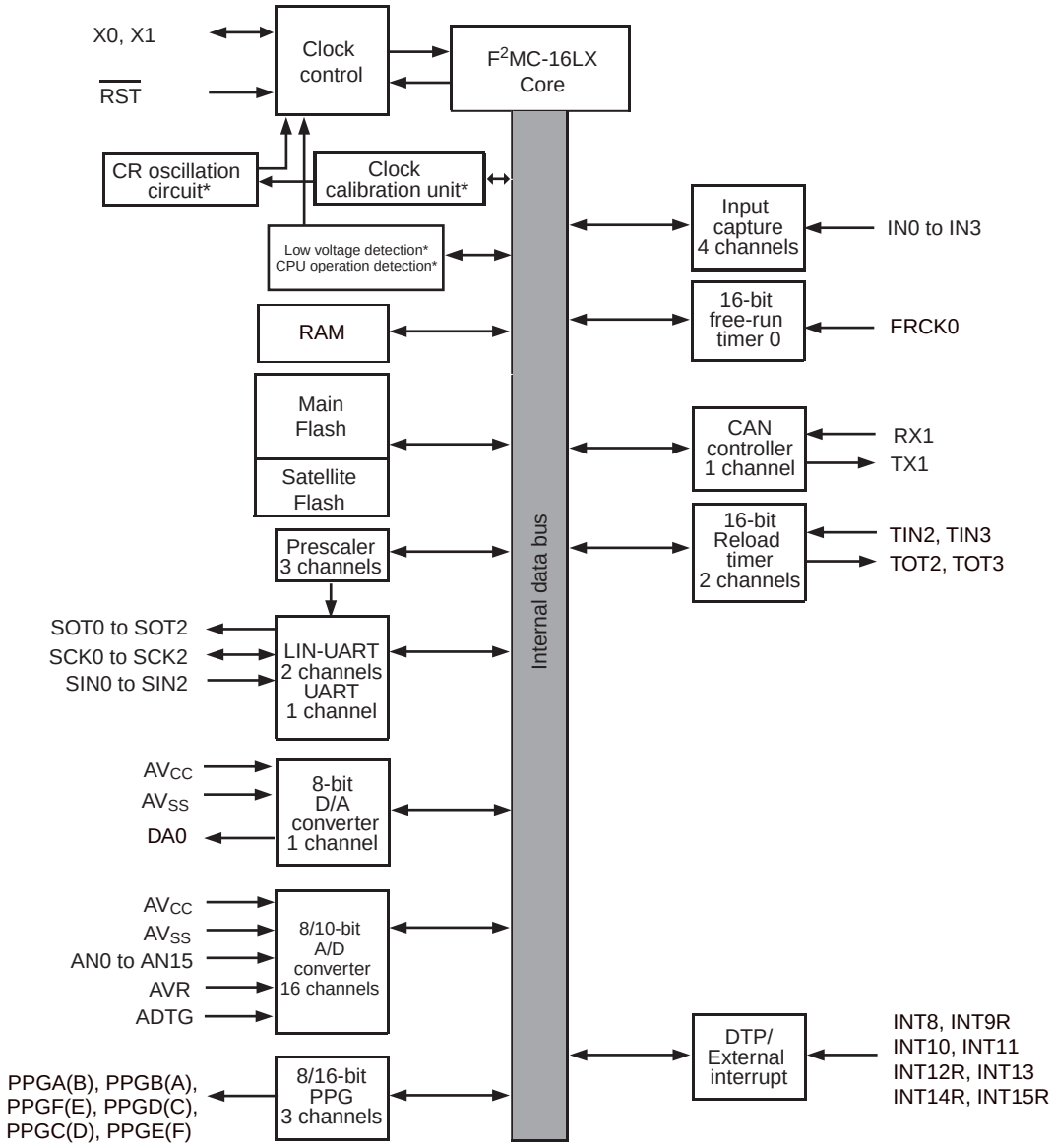
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• **MB90V950AJAS**



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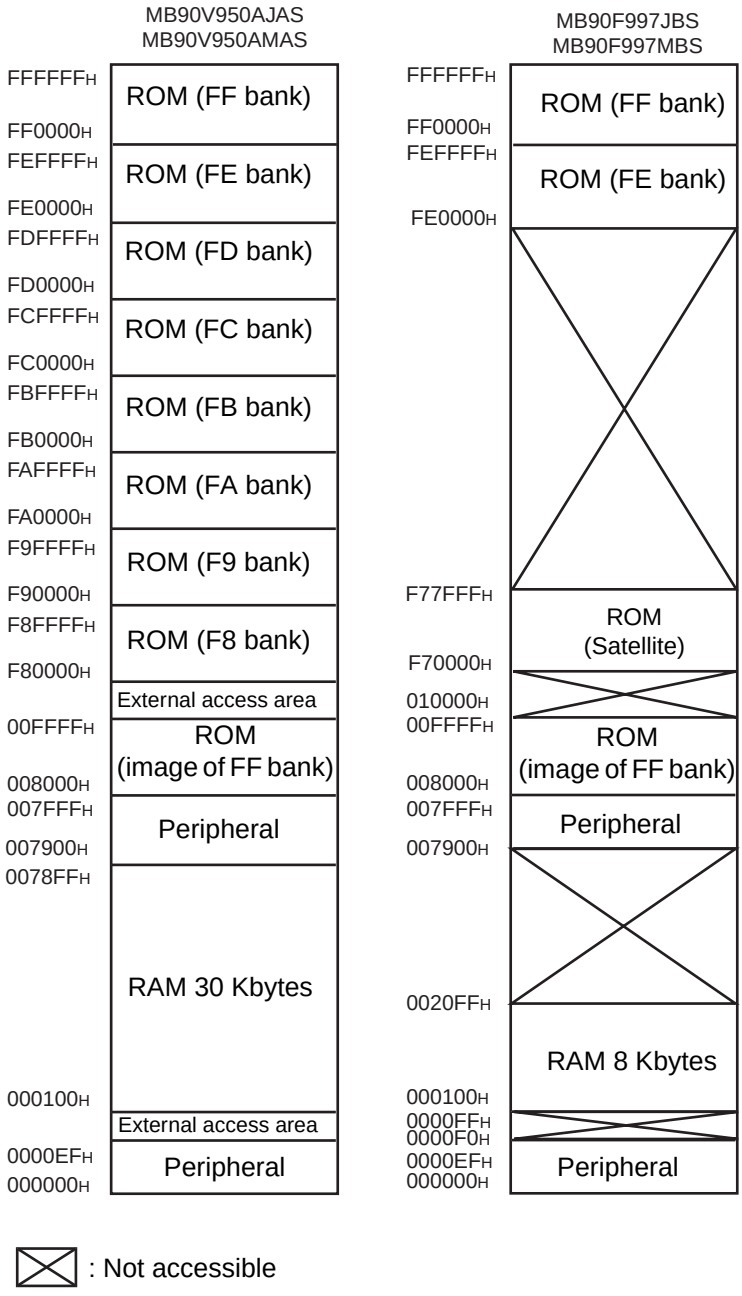
• **MB90F997JBS, MB90F997MBS**



* : Only for devices with J-suffix

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■ MEMORY MAP



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referred without using the far specification in the pointer declaration.
For example, an attempt to access 00C000H practically accesses the value at FFC000H in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

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■ I/O MAP

Address	Register	Abbreviation	Access	Resource name	Initial value
000000H, 000001H	Reserved				
000002H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXXB
000003H	Reserved				
000004H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXXB
000005H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXXB
000006H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXXB
000007H	Reserved				
000008H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXXB
000009H, 00000AH	Reserved				
00000BH	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111B
00000CH	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111B
00000DH	Reserved				
00000EH	Input Level Select Register	ILSR0	R/W	Ports	XXXXXXXXB
00000FH	Input Level Select Register	ILSR1	R/W		XXXX0XXXB
000010H, 000011H	Reserved				
000012H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000B
000013H	Reserved				
000014H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000B
000015H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000B
000016H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000B
000017H	Reserved				
000018H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000B
000019H	Reserved				
00001AH	Port A Direction Register	DDRA	W	Port A	00000111B
00001BH to 00001DH	Reserved				
00001EH	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000B
00001FH	Reserved				

(Continued)

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Address	Register	Abbreviation	Access	Resource name	Initial value
000020H	Serial Mode Register 0	SMR0	W, R/W	UART0	00000000B
000021H	Serial Control Register 0	SCR0	W, R/W		00000000B
000022H	Reception/Transmission Data Register 0	RDR0/ TDR0	R/W		00000000B/ 11111111B
000023H	Serial Status Register 0	SSR0	R, R/W		00001000B
000024H	Extended Communication Control Register 0	ECCR0	R, W, R/W		000000XXB
000025H	Extended Status/Control Register 0	ESCR0	R/W		00000X00B
000026H	Baud Rate Generator Register 00	BGR00	R/W, R		00000000B
000027H	Baud Rate Generator Register 01	BGR01	R/W, R		00000000B
000028H	Serial Mode Register 1	SMR1	W, R/W	UART1	00000000B
000029H	Serial Control Register 1	SCR1	W, R/W		00000000B
00002AH	Reception/Transmission Data Register 1	RDR1/ TDR1	R/W		00000000B/ 11111111B
00002BH	Serial Status Register 1	SSR1	R, R/W		00001000B
00002CH	Extended Communication Control Register 1	ECCR1	R, W, R/W		000000XXB
00002DH	Extended Status/Control Register 1	ESCR1	R/W		00000X00B
00002EH	Baud Rate Generator Register 10	BGR10	R/W, R		00000000B
00002FH	Baud Rate Generator Register 11	BGR11	R/W, R		00000000B
000030H to 00003AH	Reserved				
00003BH	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	11000000B
00003CH to 000043H	Reserved				
000044H	PPGA Operation Mode Control Register	PPGCA	W, R/W	16-bit PPG A/B	01000111B
000045H	PPGB Operation Mode Control Register	PPGCB	W, R/W		01000001B
000046H	PPGA/B Count Clock Select Register	PPGAB	R/W		00000010B
000047H	Reserved				
000048H	PPG C Operation Mode Control Register	PPGCC	W, R/W	16-bit PPG C/D	01000111B
000049H	PPG D Operation Mode Control Register	PPGCD	W, R/W		01000001B
00004AH	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		00000010B
00004BH	Reserved				

(Continued)

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Address	Register	Abbreviation	Access	Resource name	Initial value
00004C$_H$	PPG E Operation Mode Control Register	PPGCE	W, R/W	16-bit PPG E/F	01000111$_B$
00004D$_H$	PPG F Operation Mode Control Register	PPGCF	W, R/W		01000001$_B$
00004E$_H$	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		00000010$_B$
00004F$_H$	Reserved				
000050$_H$	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000$_B$
000051$_H$	Input Capture Edge 0/1	ICE01	R/W, R		111010XX$_B$
000052$_H$	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000$_B$
000053$_H$	Input Capture Edge 2/3	ICE23	R		111111XX$_B$
000054$_H$ to 000063$_H$	Reserved				
000064$_H$	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000$_B$
000065$_H$	Timer Control Status 2	TMCSR2	R/W		11110000$_B$
000066$_H$	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000$_B$
000067$_H$	Timer Control Status 3	TMCSR3	R/W		11110000$_B$
000068$_H$	A/D Control Status 0	ADCS0	R/W	A/D Converter	00011110$_B$
000069$_H$	A/D Control Status 1	ADCS1	R/W, W		00000001$_B$
00006A$_H$	A/D Data 0	ADCR0	R		00000000$_B$
00006B$_H$	A/D Data 1	ADCR1	R		11111100$_B$
00006C$_H$	A/D Converter Setting 0	ADSR0	R/W		00000000$_B$
00006D$_H$	A/D Converter Setting 1	ADSR1	R/W		00000000$_B$
00006E$_H$	Low Voltage/CPU Operation Detection Reset Control Register	LVRC	R/W, W	Low Voltage/CPU Operation Detection Reset	00111000$_B$
00006F$_H$	ROM Mirror Function Select	ROMM	W	ROM Mirror	11111101$_B$
000070$_H$ to 00007F$_H$	Reserved				
000080$_H$ to 00008F$_H$	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
000090$_H$ to 00009D$_H$	Reserved				
00009E$_H$	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	11000000$_B$

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Address	Register	Abbreviation	Access	Resource name	Initial value
00009F$_H$	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt Generation module	11111110$_B$
0000A0$_H$	Low-power Consumption Mode Control Register	LPMCR	W, R/W	Low-Power Consumption Control Circuit	00011000$_B$
0000A1$_H$	Clock Selection Register	CKSCR	R, R/W		11111100$_B$
0000A2$_H$ to 0000A7$_H$	Reserved				
0000A8$_H$	Watchdog Control Register	WDTC	R, W	Watchdog Timer	XXXXX111$_B$
0000A9$_H$	Timebase Timer Control Register	TBTC	W, R/W	Timebase Timer	11100100$_B$
0000AA$_H$	Watch Timer Control register	WTC	R, R/W	Watch Timer	1X001000$_B$
0000AB$_H$ to 0000AD$_H$	Reserved				
0000AE$_H$	Flash Control Status (Flash Devices only. Otherwise reserved)	FMCS	R, R/W	Flash Memory	000X0000$_B$
0000AF$_H$	Reserved				
0000B0$_H$	Interrupt Control Register 00	ICR00	W, R/W	Interrupt Control	00000111$_B$
0000B1$_H$	Interrupt Control Register 01	ICR01	W, R/W		00000111$_B$
0000B2$_H$	Interrupt Control Register 02	ICR02	W, R/W		00000111$_B$
0000B3$_H$	Interrupt Control Register 03	ICR03	W, R/W		00000111$_B$
0000B4$_H$	Interrupt Control Register 04	ICR04	W, R/W		00000111$_B$
0000B5$_H$	Interrupt Control Register 05	ICR05	W, R/W		00000111$_B$
0000B6$_H$	Interrupt Control Register 06	ICR06	W, R/W		00000111$_B$
0000B7$_H$	Interrupt Control Register 07	ICR07	W, R/W		00000111$_B$
0000B8$_H$	Interrupt Control Register 08	ICR08	W, R/W		00000111$_B$
0000B9$_H$	Interrupt Control Register 09	ICR09	W, R/W		00000111$_B$
0000BA$_H$	Interrupt Control Register 10	ICR10	W, R/W		00000111$_B$
0000BB$_H$	Interrupt Control Register 11	ICR11	W, R/W		00000111$_B$
0000BC$_H$	Interrupt Control Register 12	ICR12	W, R/W		00000111$_B$
0000BD$_H$	Interrupt Control Register 13	ICR13	W, R/W		00000111$_B$
0000BE$_H$	Interrupt Control Register 14	ICR14	W, R/W		00000111$_B$
0000BF$_H$	Interrupt Control Register 15	ICR15	W, R/W		00000111$_B$
0000C0$_H$	D/A Converter Data 0	DAT0	R/W	D/A Converter	XXXXXXXX$_B$

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Address	Register	Abbreviation	Access	Resource name	Initial value
0000C1H	Reserved				
0000C2H	D/A Control 0	DACR0	R/W	D/A Converter	00000000B
0000C3H to 0000C9H	Reserved				
0000CAH	External Interrupt Enable 1	ENIR1	R/W	DTP/ External Interrupt	00000000B
0000CBH	External Interrupt Source 1	EIRR1	R/W		XXXXXXXXB
0000CCH	Detection Level Setting 1	ELVR1	R/W		00000000B
0000CDH					00000000B
0000CEH	External Interrupt Source Select	EISSR	R/W		00000000B
0000CFH	PLL/Sub clock Control Register	PSCCR	W	PLL	11110000B
0000D0H to 0000D7H	Reserved				
0000D8H	Serial Mode Register 2	SMR2	W, R/W	UART2	00000000B
0000D9H	Serial Control Register 2	SCR2	W, R/W		00000000B
0000DAH	Reception/Transmission Data Register 2	RDR2/ TDR2	R/W		00000000B/ 11111111B
0000DBH	Serial Status Register 2	SSR2	R, R/W		00001000B
0000DCH	Extended Communication Control Register 2	ECCR2	R, W, R/W		000000XXB
0000DDH	Extended Status/Control Register 2	ESCR2	R/W		00000X00B
0000DEH	Baud Rate Generator Register 20	BGR20	R/W, R		00000000B
0000DFH	Baud Rate Generator Register 21	BGR21	R/W, R		00000000B
0000E0H to 0000FFH	Reserved				
007900H to 007913H	Reserved				
007914H	Reload Register LA	PRLLA	R/W	16-bit PPG A/B	XXXXXXXXB
007915H	Reload Register HA	PRLHA	R/W		XXXXXXXXB
007916H	Reload Register LB	PRLLB	R/W		XXXXXXXXB
007917H	Reload Register HB	PRLHB	R/W		XXXXXXXXB
007918H	Reload Register LC	PRLLC	R/W	16-bit PPG C/D	XXXXXXXXB
007919H	Reload Register HC	PRLHC	R/W		XXXXXXXXB
00791AH	Reload Register LD	PRLLD	R/W		XXXXXXXXB
00791BH	Reload Register HD	PRLHD	R/W		XXXXXXXXB

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Address	Register	Abbreviation	Access	Resource name	Initial value
00791C$_H$	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	XXXXXXXX$_B$
00791D$_H$	Reload Register HE	PRLHE	R/W		XXXXXXXX$_B$
00791E$_H$	Reload Register LF	PRLLF	R/W		XXXXXXXX$_B$
00791F$_H$	Reload Register HF	PRLHF	R/W		XXXXXXXX$_B$
007920$_H$	Input Capture 0	IPCP0	R	Input Capture 0/1*	00000000$_B$
007921$_H$	Input Capture 0	IPCP0	R		00000000$_B$
007922$_H$	Input Capture 1	IPCP1	R		00000000$_B$
007923$_H$	Input Capture 1	IPCP1	R		00000000$_B$
007924$_H$	Input Capture 2	IPCP2	R	Input Capture 2/3*	00000000$_B$
007925$_H$	Input Capture 2	IPCP2	R		00000000$_B$
007926$_H$	Input Capture 3	IPCP3	R		00000000$_B$
007927$_H$	Input Capture 3	IPCP3	R		00000000$_B$
007928$_H$ to 00793F$_H$	Reserved				
007940$_H$	Timer Data 0	TCDT0	R/W	I/O Timer 0	00000000$_B$
007941$_H$	Timer Data 0	TCDT0	R/W		00000000$_B$
007942$_H$	Timer Control Status 0	TCCSL0	R/W		00000000$_B$
007943$_H$	Timer Control Status 0	TCCSH0	R/W		01100000$_B$
007944$_H$ to 00794B$_H$	Reserved				
00794C$_H$	Timer 2/Reload 2	TMR2/ TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX$_B$
00794D$_H$			R/W		XXXXXXXX$_B$
00794E$_H$	Timer 3/Reload 3	TMR3/ TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX$_B$
00794F$_H$			R/W		XXXXXXXX$_B$
007950$_H$ to 00795F$_H$	Reserved				
007960$_H$	Clock Supervisor Control Register	CSVCR	R, R/W	Clock supervisor	00011100$_B$
007961$_H$ to 00796D$_H$	Reserved				
00796E$_H$	CAN Direct Mode Register	CDMR	R/W	CAN clock sync	11111110$_B$
00796F$_H$ to 0079A1$_H$	Reserved				

* : The initial value of the evaluation product is XXXXXXXX$_B$.

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Address	Register	Abbreviation	Access	Resource name	Initial value
0079A2H	Flash Write Control Register 0	FWR0	R/W	Flash	00000000B
0079A3H	Flash Write Control Register 1	FWR1	R/W		00000000B
0079A4H to 0079B1H	Reserved				
0079B2H	Low Voltage/CPU Operation Detection Setting Register	LVRS	R/W	Low Voltage/CPU Operation Detection Reset	10000000B
0079B3H to 0079B7H	Reserved				
0079B8H	Clock Calibration Unit Control Register	CUCR	R/W	Clock Calibration Unit	00000000B
0079B9H	CR Trimming Register	CRTR	R/W		11110111B
0079BAH	CR Oscillation Timer Deta Register	CUTDL	R/W		01010000B
0079BBH	CR Oscillation Timer Deta Register	CUTDL	R/W		11000011B
0079BCH	Main Oscillation Timer Deta Register 1	CUTR1L	R		00000000B
0079BDH	Main Oscillation Timer Deta Register 1	CUTR1H	R		00000000B
0079BEH	Main Oscillation Timer Deta Register 2	CUTR2L	R		00000000B
0079BFH	Main Oscillation Timer Deta Register 2	CUTR2H	R		00000000B
0079C0H to 0079DFH	Reserved				
0079E0H	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXXB
0079E1H	Detect Address Setting 0	PADR0	R/W		XXXXXXXXB
0079E2H	Detect Address Setting 0	PADR0	R/W		XXXXXXXXB
0079E3H	Detect Address Setting 1	PADR1	R/W		XXXXXXXXB
0079E4H	Detect Address Setting 1	PADR1	R/W		XXXXXXXXB
0079E5H	Detect Address Setting 1	PADR1	R/W		XXXXXXXXB
0079E6H	Detect Address Setting 2	PADR2	R/W		XXXXXXXXB
0079E7H	Detect Address Setting 2	PADR2	R/W		XXXXXXXXB
0079E8H	Detect Address Setting 2	PADR2	R/W		XXXXXXXXB
0079E9H to 0079EFH	Reserved				

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Address	Register	Abbrevia-tion	Access	Resource name	Initial value
0079F0H	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXXB
0079F1H	Detect Address Setting 3	PADR3	R/W		XXXXXXXXB
0079F2H	Detect Address Setting 3	PADR3	R/W		XXXXXXXXB
0079F3H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F4H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F5H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F6H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F7H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F8H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F9H to 007BFFH	Reserved				
007C00H to 007CFFH	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
007D00H to 007DFFH	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
007E00H to 007FFFH	Reserved				

Notes :
- Initial value of “X” represents undefined value.
- Do not write to reserved address in I/O map. A read access to reserved addresses results in reading “X”.

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■ CAN CONTROLLERS

- Conforms to CAN Specification Ver 2.0 A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 1 Mbps (when input clock is at 16 MHz)

List of Control Registers (1)

Address CAN1	Register	Abbreviation	Access	Initial Value
000080H	Message buffer valid register	BVALR	R/W	00000000 00000000B
000081H				
000082H	Transmit request register	TREQR	R/W	00000000 00000000B
000083H				
000084H	Transmit cancel register	TCANR	W	00000000 00000000B
000085H				
000086H	Transmission complete register	TCR	R/W	00000000 00000000B
000087H				
000088H	Receive complete register	RCR	R/W	00000000 00000000B
000089H				
00008AH	Remote request receiving register	RRTRR	R/W	00000000 00000000B
00008BH				
00008CH	Receive overrun register	ROVRR	R/W	00000000 00000000B
00008DH				
00008EH	Reception interrupt enable register	RIER	R/W	00000000 00000000B
00008FH				

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List of Control Registers (2)

Address CAN1	Register	Abbreviation	Access	Initial Value
007D00H	Control status register	CSR	R/W, W R/W, R	0XXXX0X1 00XXX000B
007D01H				
007D02H	Last event indicator register	LEIR	R/W	000X0000 XXXXXXXXB
007D03H				
007D04H	Receive and transmit error counter	RTEC	R	00000000 00000000B
007D05H				
007D06H	Bit timing register	BTR	R/W	11111111 X1111111B
007D07H				
007D08H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXXB
007D09H				
007D0AH	Transmit RTR register	TRTRR	R/W	00000000 00000000B
007D0BH				
007D0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXXB
007D0DH				
007D0EH	Transmit interrupt enable register	TIER	R/W	00000000 00000000B
007D0FH				
007D10H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXXB
007D11H				
007D12H				XXXXXXXX XXXXXXXXB
007D13H				
007D14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXXB
007D15H				
007D16H				XXXXXXXX XXXXXXXXB
007D17H				
007D18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXXB
007D19H				
007D1AH				XXXXXXXX XXXXXXXXB
007D1BH				

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List of Message Buffers (ID Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
007C00H to 007C1FH	General-purpose RAM	—	R/W	XXXXXXXXB to XXXXXXXXB
007C20H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXXB
007C21H				
007C22H				XXXXXXXX XXXXXXXXB
007C23H				
007C24H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXXB
007C25H				
007C26H				XXXXXXXX XXXXXXXXB
007C27H				
007C28H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXXB
007C29H				
007C2AH				XXXXXXXX XXXXXXXXB
007C2BH				
007C2CH	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXXB
007C2DH				
007C2EH				XXXXXXXX XXXXXXXXB
007C2FH				
007C30H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXXB
007C31H				
007C32H				XXXXXXXX XXXXXXXXB
007C33H				
007C34H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXXB
007C35H				
007C36H				XXXXXXXX XXXXXXXXB
007C37H				
007C38H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXXB
007C39H				
007C3AH				XXXXXXXX XXXXXXXXB
007C3BH				
007C3CH	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXXB
007C3DH				
007C3EH				XXXXXXXX XXXXXXXXB
007C3FH				

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Address CAN1	Register	Abbreviation	Access	Initial Value
007C40H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXXB
007C41H				
007C42H				XXXXXXXX XXXXXXXXB
007C43H				
007C44H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXXB
007C45H				
007C46H				XXXXXXXX XXXXXXXXB
007C47H				
007C48H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXXB
007C49H				
007C4AH				XXXXXXXX XXXXXXXXB
007C4BH				
007C4CH	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXXB
007C4DH				
007C4EH				XXXXXXXX XXXXXXXXB
007C4FH				
007C50H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXXB
007C51H				
007C52H				XXXXXXXX XXXXXXXXB
007C53H				
007C54H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXXB
007C55H				
007C56H				XXXXXXXX XXXXXXXXB
007C57H				
007C58H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXXB
007C59H				
007C5AH				XXXXXXXX XXXXXXXXB
007C5BH				
007C5CH	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXXB
007C5DH				
007C5EH				XXXXXXXX XXXXXXXXB
007C5FH				

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List of Message Buffers (DLC Registers and Data Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
007C60H	DLC register 0	DLCR0	R/W	XXXXXXXXB
007C61H				
007C62H	DLC register 1	DLCR1	R/W	XXXXXXXXB
007C63H				
007C64H	DLC register 2	DLCR2	R/W	XXXXXXXXB
007C65H				
007C66H	DLC register 3	DLCR3	R/W	XXXXXXXXB
007C67H				
007C68H	DLC register 4	DLCR4	R/W	XXXXXXXXB
007C69H				
007C6AH	DLC register 5	DLCR5	R/W	XXXXXXXXB
007C6BH				
007C6CH	DLC register 6	DLCR6	R/W	XXXXXXXXB
007C6DH				
007C6EH	DLC register 7	DLCR7	R/W	XXXXXXXXB
007C6FH				
007C70H	DLC register 8	DLCR8	R/W	XXXXXXXXB
007C71H				
007C72H	DLC register 9	DLCR9	R/W	XXXXXXXXB
007C73H				
007C74H	DLC register 10	DLCR10	R/W	XXXXXXXXB
007C75H				
007C76H	DLC register 11	DLCR11	R/W	XXXXXXXXB
007C77H				
007C78H	DLC register 12	DLCR12	R/W	XXXXXXXXB
007C79H				
007C7AH	DLC register 13	DLCR13	R/W	XXXXXXXXB
007C7BH				
007C7CH	DLC register 14	DLCR14	R/W	XXXXXXXXB
007C7DH				
007C7EH	DLC register 15	DLCR15	R/W	XXXXXXXXB
007C7FH				

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Address CAN1	Register	Abbreviation	Access	Initial Value
007C80H to 007C87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB
007C88H to 007C8FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
007C90H to 007C97H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
007C98H to 007C9FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
007CA0H to 007CA7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
007CA8H to 007CAFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
007CB0H to 007CB7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
007CB8H to 007CBFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
007CC0H to 007CC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
007CC8H to 007CCFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
007CD0H to 007CD7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
007CD8H to 007CDFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
007CE0H to 007CE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
007CE8H to 007CEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB

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Address CAN1	Register	Abbreviation	Access	Initial Value
007CF0H to 007CF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
007CF8H to 007CFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

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■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI²OS corresponding	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N	#08	FFFFDC$_H$	—	—
INT9 instruction	N	#09	FFFFD8$_H$	—	—
Exception	N	#10	FFFFD4$_H$	—	—
Reserved	N	#11	FFFFD0$_H$	ICR00	0000B0$_H$
Reserved	N	#12	FFFFCC$_H$		
CAN 1 reception	N	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 transmission/node status	N	#14	FFFFC4$_H$		
Reserved	N	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Clock calibration unit	N	#16	FFFFBC$_H$		
Reserved	N	#17	FFFFB8$_H$	ICR03	0000B3$_H$
Reserved	N	#18	FFFFB4$_H$		
16-bit reload timer 2	Y1	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit reload timer 3	Y1	#20	FFFFAC$_H$		
Reserved	N	#21	FFFFA8$_H$	ICR05	0000B5$_H$
Reserved	N	#22	FFFFA4$_H$		
PPG C/D	N	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG A/B/E/F	N	#24	FFFF9C$_H$		
Timebase timer	N	#25	FFFF98$_H$	ICR07	0000B7$_H$
External interrupt 8 to 11	Y1	#26	FFFF94$_H$		
Watch timer	N	#27	FFFF90$_H$	ICR08	0000B8$_H$
External interrupt 12 to 15	Y1	#28	FFFF8C$_H$		
A/D converter	Y1	#29	FFFF88$_H$	ICR09	0000B9$_H$
I/O timer 0	N	#30	FFFF84$_H$		
Reserved	N	#31	FFFF80$_H$	ICR10	0000BA$_H$
Reserved	N	#32	FFFF7C$_H$		
Input capture 0 to 3	Y1	#33	FFFF78$_H$	ICR11	0000BB$_H$
Reserved	N	#34	FFFF74$_H$		
UART 0 reception	Y2	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART 0 transmission	Y1	#36	FFFF6C$_H$		
UART 1 reception	Y2	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 1 transmission	Y1	#38	FFFF64$_H$		

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Interrupt cause	EI²OS corresponding	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
UART 2 reception	Y2	#39	FFFF60H	ICR14	0000BEH
UART 2 transmission	Y1	#40	FFFF5CH		
Flash memory	N	#41	FFFF58H	ICR15	0000BFH
Delayed interrupt generation module	N	#42	FFFF54H		

Y1 : Usable

Y2 : Usable, with EI²OS stop function

N : Unusable

Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
- When the peripheral resources sharing the ICR register use extended intelligent I/O service, only one can use extended intelligent I/O service at a time.
- When either of the 2 peripheral resources sharing the ICR register specifies extended intelligent I/O service, the other one cannot use interrupts.

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■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVR$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum clamp current	I_{CLAMP}	–2.0	+2.0	mA	*6
Total Maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	40	mA	*6
“L” level maximum output current	I_{OL1}	—	15	mA	*4
	I_{OL2}	—	40	mA	*5
“L” level average output current	I_{OLAV1}	—	4	mA	*4
	I_{OLAV2}	—	30	mA	*5
“L” level maximum overall output current	ΣI_{OL1}	—	125	mA	*4
	ΣI_{OL2}	—	160	mA	*5
“L” level average overall output current	ΣI_{OLAV1}	—	40	mA	*4
	ΣI_{OLAV2}				*5
	ΣI_{OLAV1}	—	40	mA	*4
	ΣI_{OLAV2}				*5
“H” level maximum output current	I_{OH1}	—	–15	mA	*4
	I_{OH2}	—	–40	mA	*5
“H” level average output current	I_{OHAV1}	—	–4	mA	*4
	I_{OHAV2}	—	–30	mA	*5
“H” level maximum overall output current	ΣI_{OH1}	—	–125	mA	*4
	ΣI_{OH2}	—	–160	mA	*5
“H” level average overall output current	ΣI_{OHAV1}	—	–40	mA	*4
	ΣI_{OHAV2}				*5
	ΣI_{OHAV1}	—	–40	mA	*4
	ΣI_{OHAV2}				*5
Power consumption	P_D	—	420	mW	
Operating temperature	T_A	–40	+105	°C	
		–40	+125	°C	*7
Storage temperature	T_{STG}	–55	+150	°C	

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*1 : This parameter is based on V_{SS} = AV_{SS} = 0 V.

*2 : Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3 : V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However, if the maximun current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

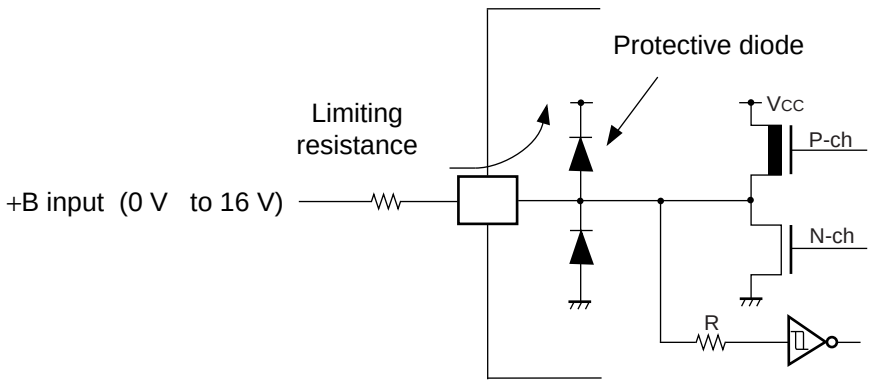
*4 : Applicable to pins : P24 to P27, P40 to P44, P50 to P57, P60 to P67, P80, P82 to P87

*5 : Applicable to pins : P20 to P23

*6 : Applicable to pins : P20 to P27, P40 to P44, P50 to P57, P60 to P67, P80, P82 to P87

- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied a connecting limit resistance between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is inputted when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Recommended circuit sample :

• Input/output equivalent circuits



*7 : If used exceeding T_A = +105 °C, please consult with us due to the restricted reliability.
It is ensured to write/erase data to the Flash memory between T_A = − 40 °C and +105 °C.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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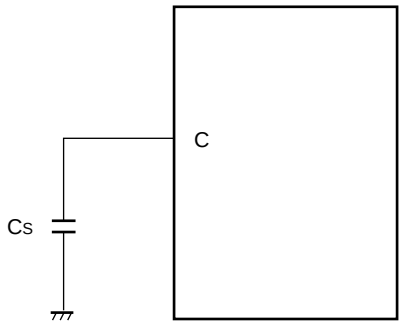
2. Recommended Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	3.0	5.0	5.5	V	Under normal operation
		2.6	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	–40	—	+105	°C	
		–40	—	+125	°C	*

* : For the restricted reliability, contact us if use the devices over Ta=+105 °C.
It is ensured to write/erase data to the Flash memory between T_A = – 40 °C and +105 °C.

• **C Pin Connection Diagram**



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

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3. DC Characteristics

Parameter	Sym-bol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “H” voltage	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if CMOS hysteresis input levels are selected
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if Automotive input levels are selected
	V_{IHS}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P50, P82, P85 inputs if CMOS input levels are selected
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	MD input pin
Input “L” voltage	V_{ILS}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Pin inputs if CMOS hysteresis input levels are selected
	V_{ILA}	—	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	Pin inputs if Automotive input levels are selected
	V_{ILS}	—	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	P50, P82, P85 inputs if CMOS input levels are selected
	V_{ILR}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	MD input pin
Output “H” voltage	V_{OH}	Other than P20 to P23	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
	V_{OHI}	P20 to P23	V_{CC} = 4.5 V, I_{OH} = –14.0 mA	V_{CC} – 0.5	—	—	V	
Output “L” voltage	V_{OL}	Other than P20 to P23	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OLI}	P20 to P23	V_{CC} = 4.5 V, I_{OL} = 20.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–1	—	+ 1	µA	
Pull-up resistance	R_{UP}	P20 to P27, $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Evaluation products only

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Parameter	Sym-bol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 32 MHz, At normal operation.	—	30	40	mA	
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	22.5	30	mA	
			V_{CC} = 5.0 V, Internal frequency : 2 MHz, At normal operation.	—	3	7	mA	
			V_{CC} = 5.0 V, Internal frequency : 32 MHz, At writing Flash memory.	—	50	65	mA	
			V_{CC} = 5.0 V, Internal frequency : 32 MHz, At erasing Flash memory.	—	50	65	mA	
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 32 MHz, At sleep mode.	—	13	23	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, At main timer mode	—	0.4	1.0	mA	MB90F997JBS
				—	0.3	0.9		MB90F997MBS
	$I_{CTSPLL8}$		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At PLL timer mode, External frequency = 4 MHz	—	4	7	mA	
	I_{CCL}		V_{CC} = 5.0 V, Internal frequency : 12.5 kHz At CR sub operation, T_A = +25°C	—	170	400	µA	MB90F997JBS
	I_{CCLS}		V_{CC} = 5.0 V, Internal frequency : 12.5 kHz At CR sub sleep, T_A = +25°C	—	130	250	µA	MB90F997JBS
	I_{CCT}		V_{CC} = 5.0 V, Internal frequency : 12.5 kHz At CR watch mode, T_A = +25°C	—	130	250	µA	MB90F997JBS
	I_{CCH}		V_{CC} = 5.0 V, At stop mode, T_A = +25°C	—	70	170	µA	MB90F997JBS
				—	25	100	µA	MB90F997MBS
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, V_{CC}, V_{SS}, C	—	—	5	15	pF	

* : The power supply current is measured with an external clock.

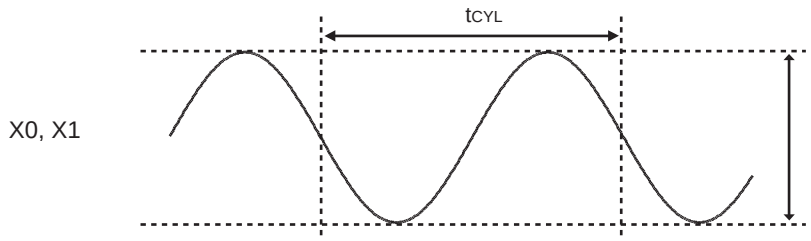
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4. AC Characteristics

(1) Clock Timing

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	1/2 when PLL stops, When using an oscillation circuit
			4	—	16	MHz	PLL × 1, When using an oscillation circuit
			4	—	16	MHz	PLL × 2, When using an oscillation circuit
			4	—	10	MHz	PLL × 3, When using an oscillation circuit
			4	—	8	MHz	PLL × 4, When using an oscillation circuit
			4	—	5	MHz	PLL × 6, When using an oscillation circuit
			4	—	4	MHz	PLL × 8, When using an oscillation circuit
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	32	MHz	When using main clock
		—	10.625	12.5	14.375	kHz	When using CR clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	31.25	—	666	ns	When using main clock
		—	69.565	80	94.118	µs	When using CR clock
Internal CR oscillation frequency	f_{CCR}	—	85	100	115	kHz	When trimming with clock calibration unit.

• **When using an oscillation circuit**

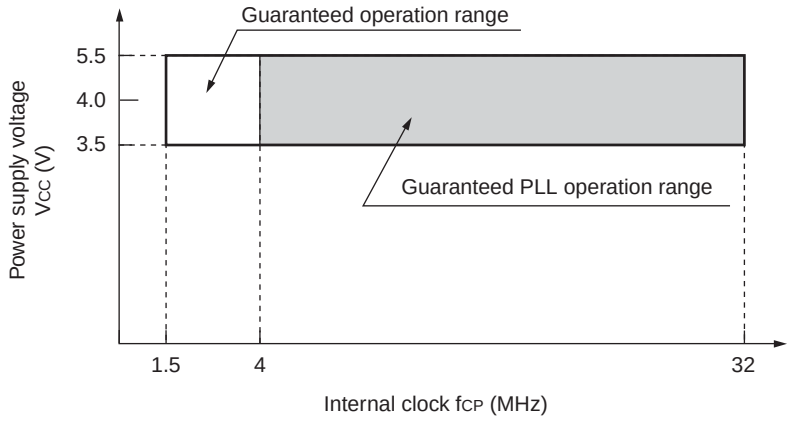


Amplitude:
It varies depending on the external resistance, power rating and the different kind of device.
Reference values: 1 V to 2.5 V

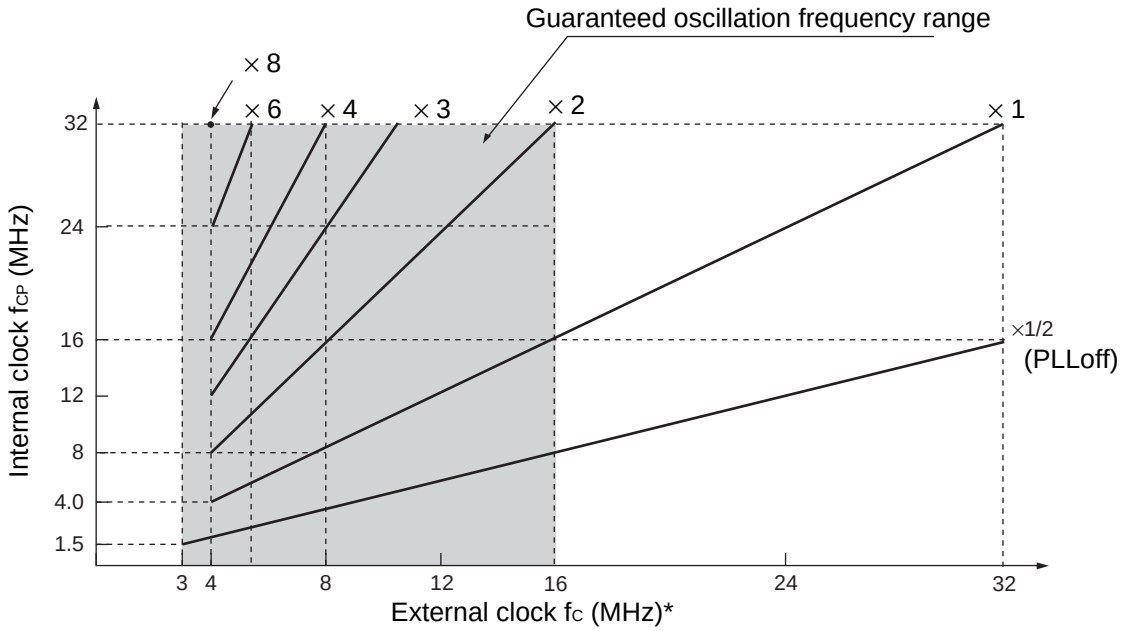
Note: The amplitude of MB90V950AJAS and MB90V950AMAS are the same as V_{CC}.

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• Guaranteed PLL Operation Range



Guaranteed operation range of MB90990 series



* : When using the oscillation circuit, the maximum oscillation clock frequency is 16 MHz.

Note: MB90F997JBS will be at a reset state under the power supply voltage of less than low-voltage detection voltage.

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(2) Reset Standby Input

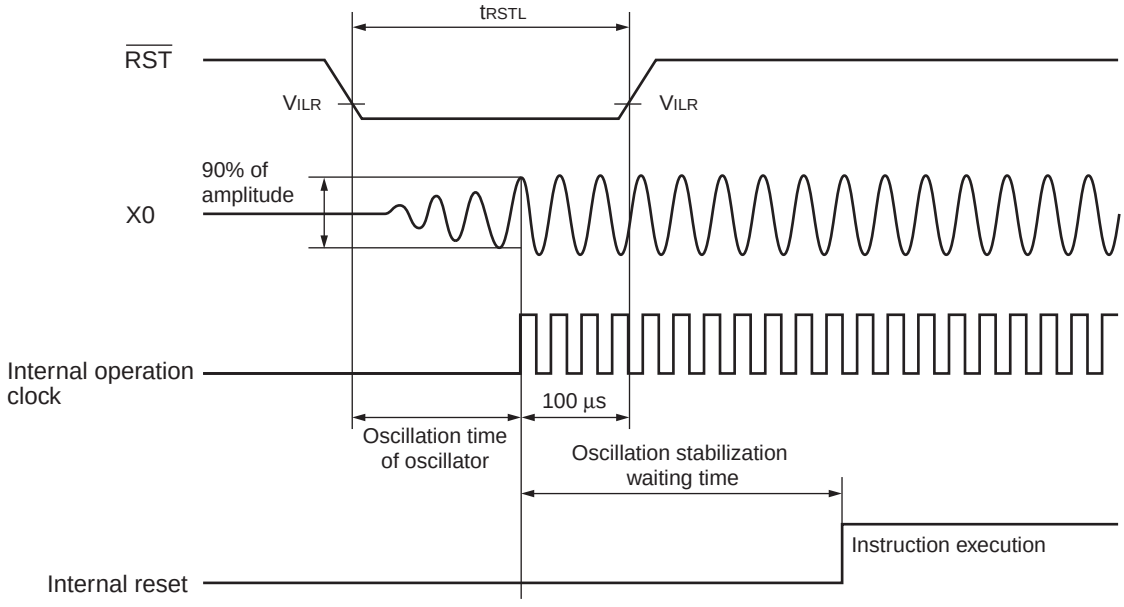
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 µs	—	µs	In stop mode, sub clock mode, sub sleep mode, and watch mode
			100	—	µs	In timebase timer mode

* : Oscillation time of oscillator is the time that the amplitude reaches 90%. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs and several ms. An External clock of oscillation time is 0 ms.

- **Under normal operation :**



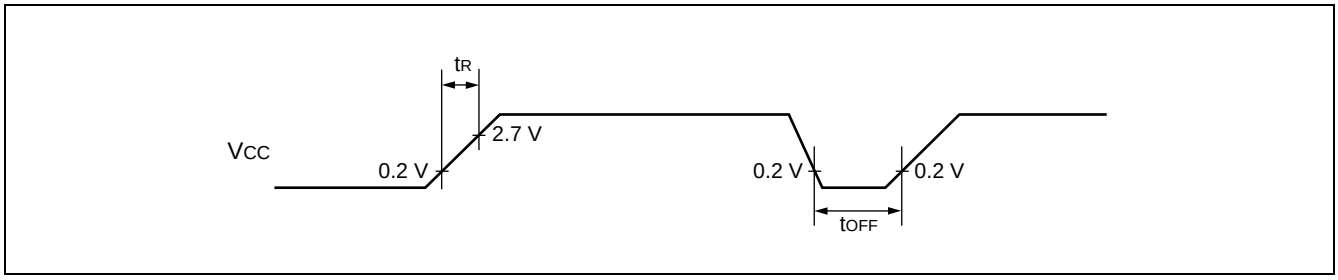
- **In stop mode, sub clock mode, sub sleep mode, and watch mode :**



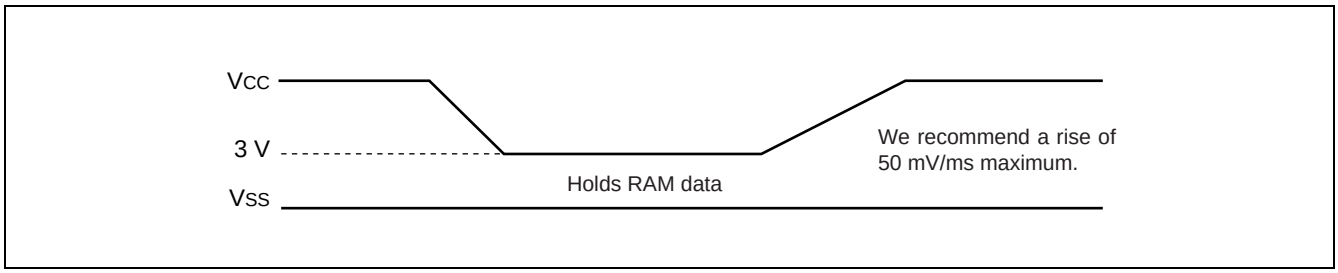
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(3) Power-on Reset

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Due to repetitive operation



Note : If you change the power supply voltage too rapidly, a power-on reset may occur. We recommend that you start up smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



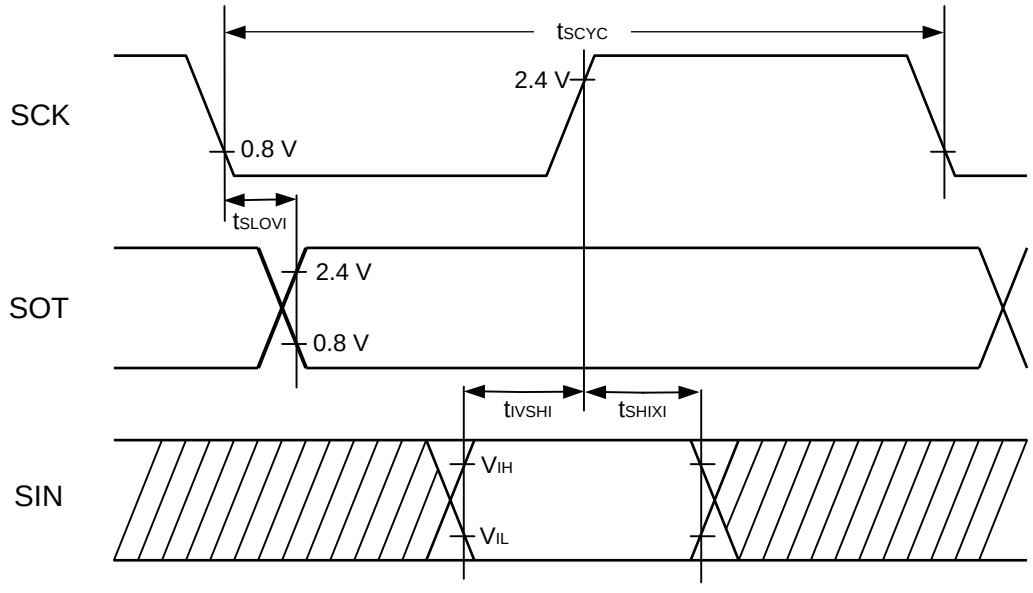
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(4) UART

ESCR : SCES = 0, ECCR : SCDE = 0

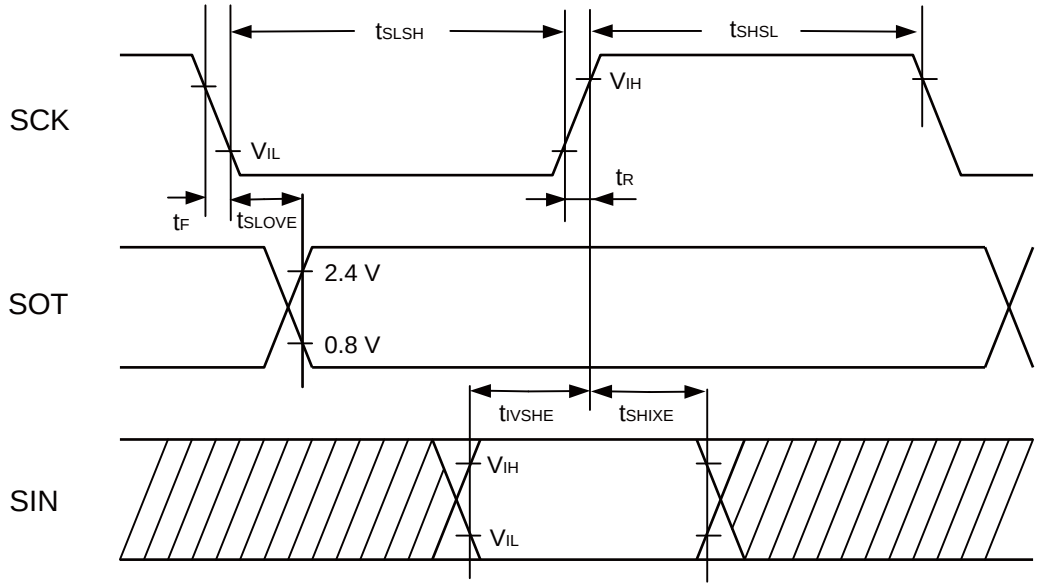
Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal shift clock operation C_L = 80pF + 1 TTL.	5 tcp*	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}		− 50	+ 50	ns
SIN → SCK ↑ setup time	t_{IVSHI}		tcp + 80	—	ns
SCK↑ → SIN hold time	t_{SHIXI}		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	External shift clock operation C_L = 80pF + 1 TTL.	3 tcp − tR	—	ns
Serial clock “H” pulse width	t_{SHSL}		tcp + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}		—	2 tcp + 60	ns
SIN → SCK ↑ setup time	t_{IVSHE}		30	—	ns
SCK↑ → SIN hold time	t_{SHIXE}		tcp + 30	—	ns
SCK fall time	t_F		—	10	ns
SCK rise time	t_R		—	10	ns

*: The tcp indicates machine clock



Internal Clock Shift Operation

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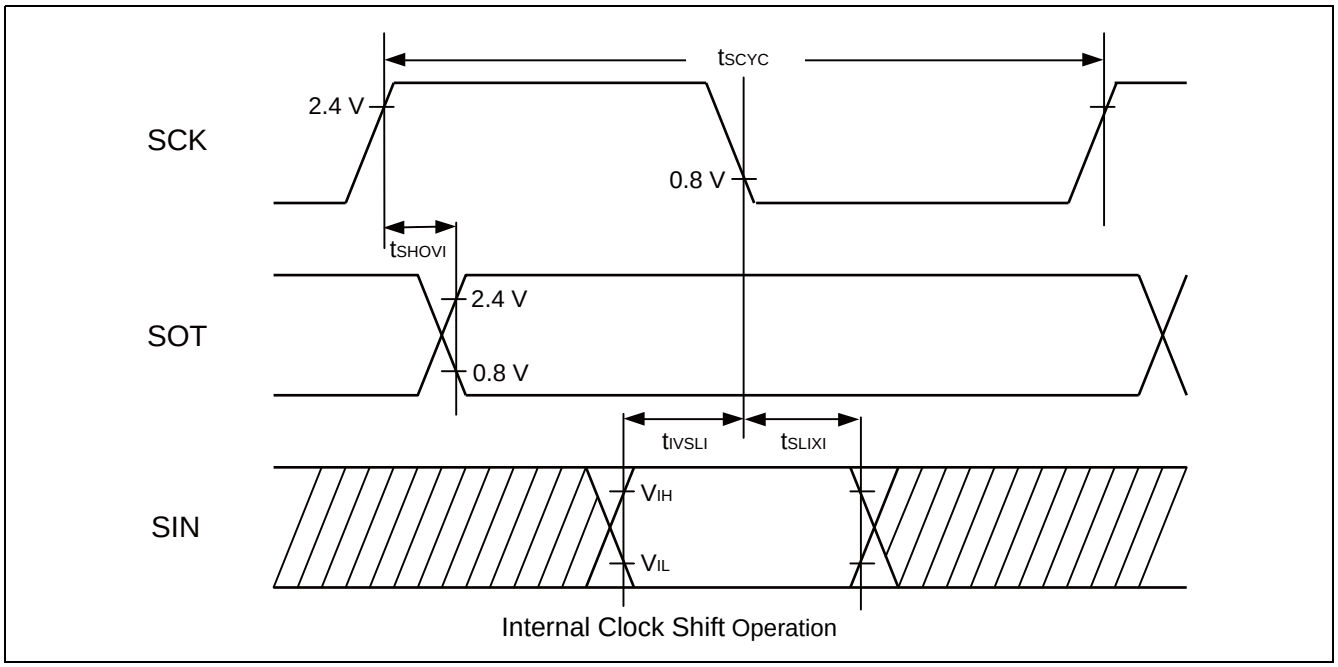
External Clock Shift Operation

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ESCR : SCES = 1, ECCR : SCDE = 0

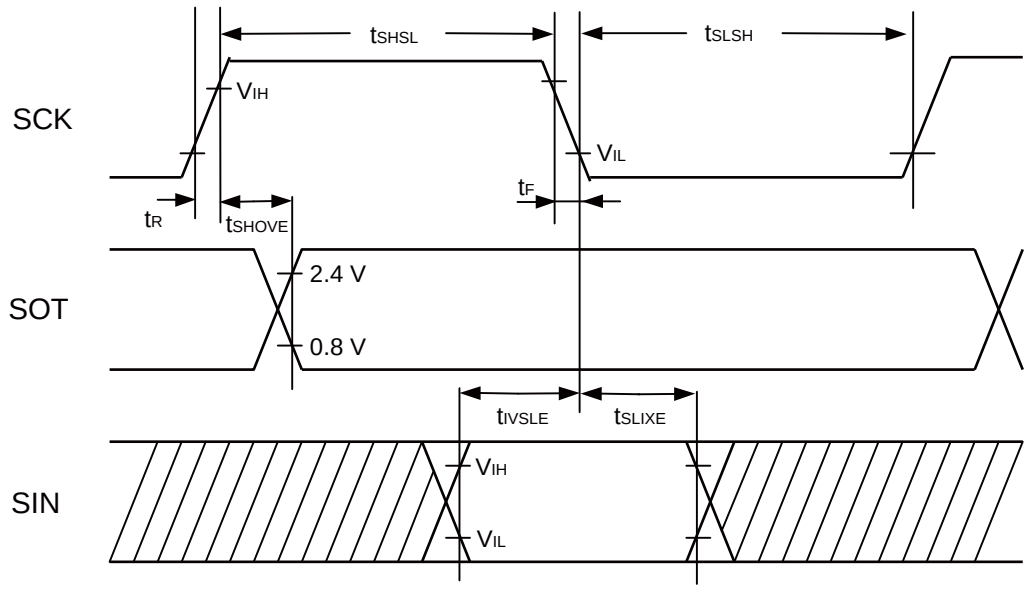
Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal shift clock operation C_L = 80pF + 1 TTL.	5 tcp*	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}		− 50	+ 50	ns
SIN → SCK ↓ setup time	t_{IVSLI}		tcp + 80	—	ns
SCK ↓ → SIN hold time	t_{SLIXI}		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	External shift clock operation C_L = 80pF + 1 TTL.	3 tcp − tR	—	ns
Serial clock “L” pulse width	t_{SLSH}		tcp + 10	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}		—	2 tcp + 60	ns
SIN → SCK ↓ setup time	t_{IVSLE}		30	—	ns
SCK ↓ → SIN hold time	t_{SLIXE}		tcp + 30	—	ns
SCK fall time	t_F		—	10	ns
SCK rise time	t_R		—	10	ns

*: The tcp indicates machine clock



Internal Clock Shift Operation

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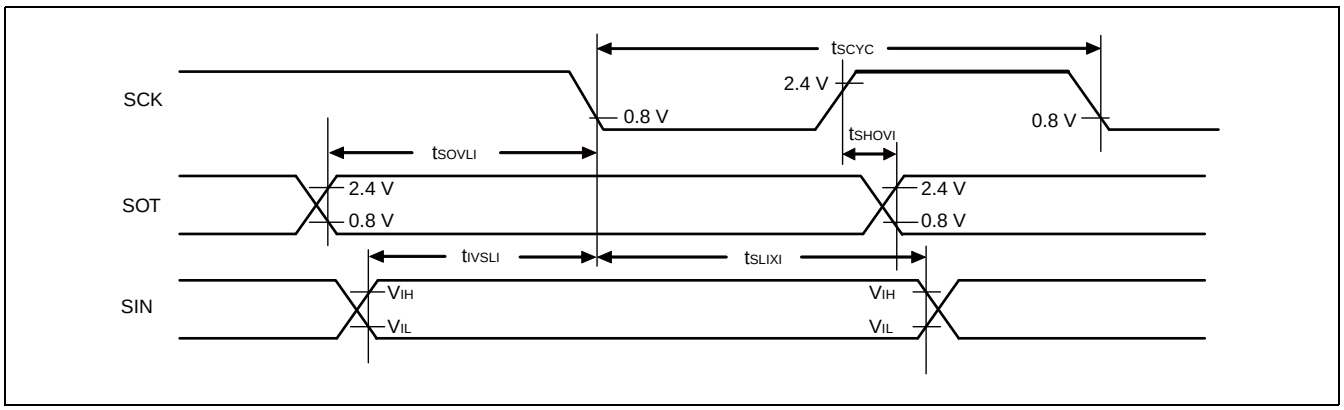
External Clock Shift Operation

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ESCR : SCES = 0, ECCR : SCDE = 1

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal shift clock operation C_L = 80pF + 1 TTL.	5 tcp*	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}		– 50	+ 50	ns
SIN → SCK ↓ setup time	t_{IVSLI}		tcp + 80	—	ns
SCK ↓ → SIN hold time	t_{SLIXI}		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}		3 tcp – 70	—	ns

*: The tcp indicates machine clock

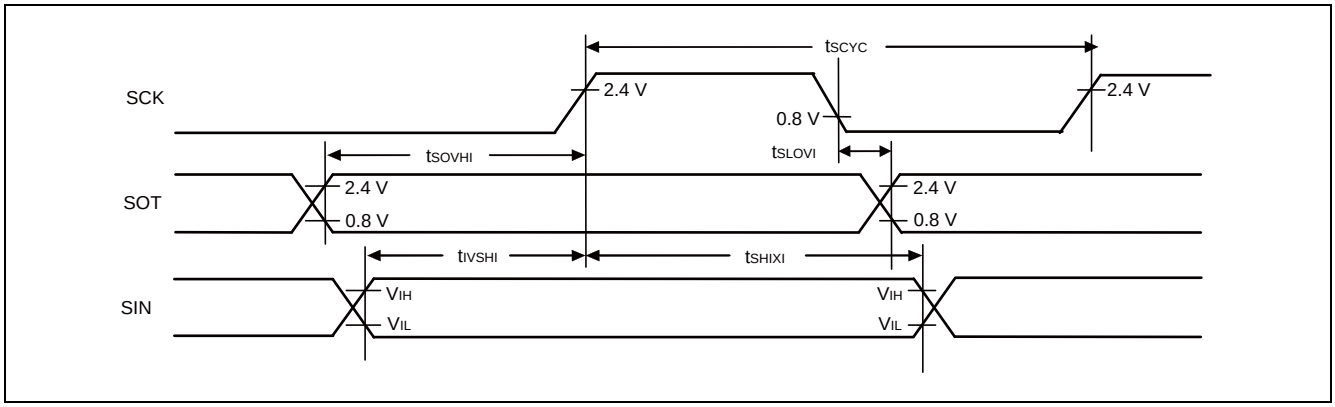


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ESCR : SCES = 1, ECCR : SCDE = 1

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal clock operation C_L = 80pF + 1 TTL.	5 tcp*	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}		– 50	+ 50	ns
SIN → SCK ↑ setup time	t_{IVSHI}		tcp + 80	—	ns
SCK ↑ → SIN hold time	t_{SHIXI}		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}		3 tcp – 70	—	ns

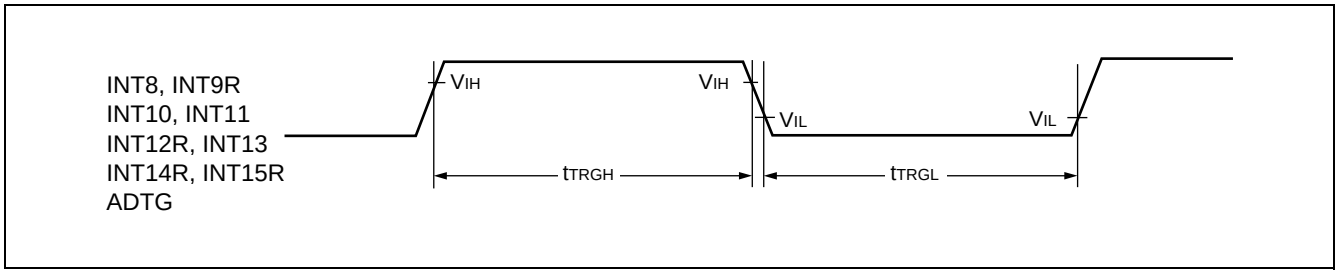
*: The tcp indicates machine clock



(5) Trigger Input Timing

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT8, INT9R INT10, INT11 INT12R, INT13 INT14R, INT15R ADTG	—	5 t_{CP}	—	ns

Note : t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

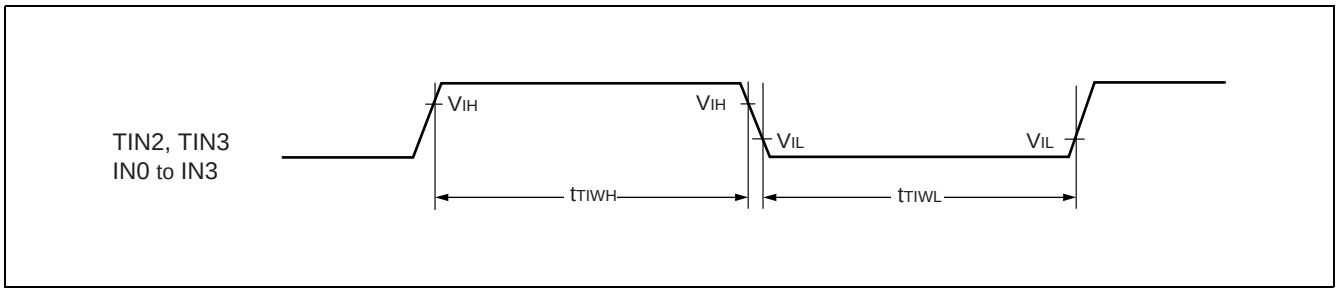


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(6) Timer Related Resource Input Timing

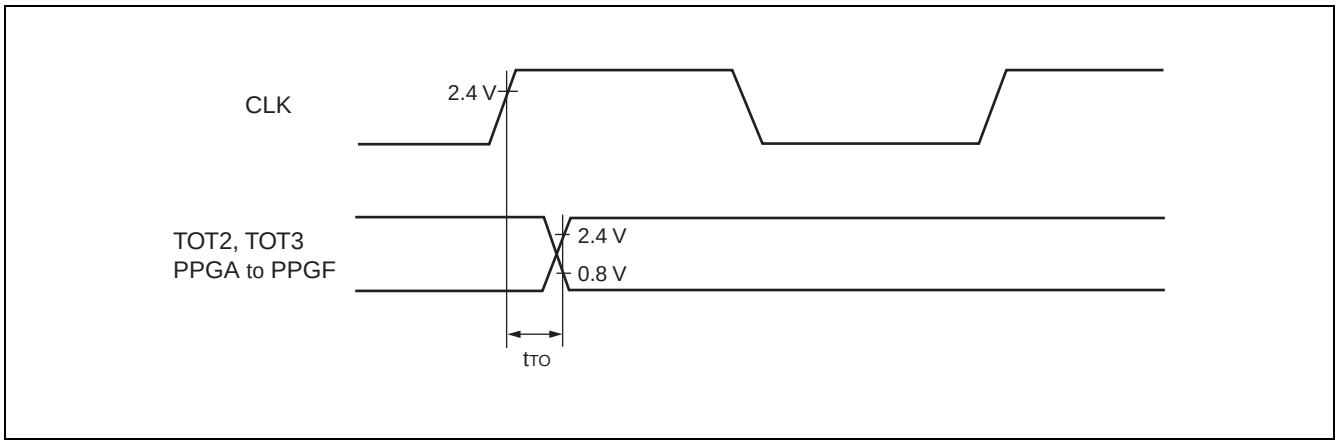
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH}	TIN2, TIN3 IN0 to IN3	—	4 t_{CP}	—	ns
	t_{TIWL}					

Note : t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.



(7) Timer Related Resource Output Timing

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT2, TOT3 PPGA to PPGF	—	30	—	ns

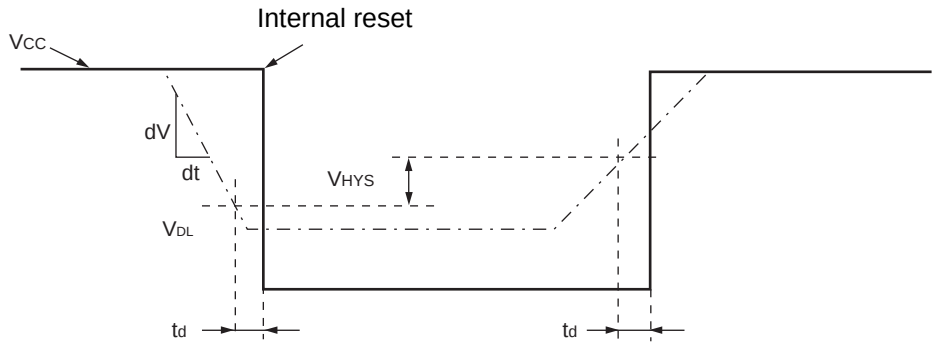


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(8) Low Voltage Detection

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Detection voltage initial value	V_{DL}	V_{CC}	—	3.8	4.0	4.2	V	During voltage drop
Hysteresis width	V_{HYS}	V_{CC}	—	169	173	177	mV	During voltage rise
Power supply voltage change rate	dV/dt	V_{CC}	—	− 0.1	—	+ 0.1	V/µs	dV/dt at low voltage reset
				− 0.004	—	+ 0.004	V/µs	dV/dt at standard value of low voltage detection/release voltage
Detection delay time	t_d	—	—	—	—	3.2	µs	When |dV/dt| ≤ 0.004 V/µs

Note: When the change ratio of the power supply voltage is 0.004 V/µs < | dV/dt | ≤ 0.1 V/µs, reset may be generated or released after the power supply voltage has exceeded the detection voltage range.



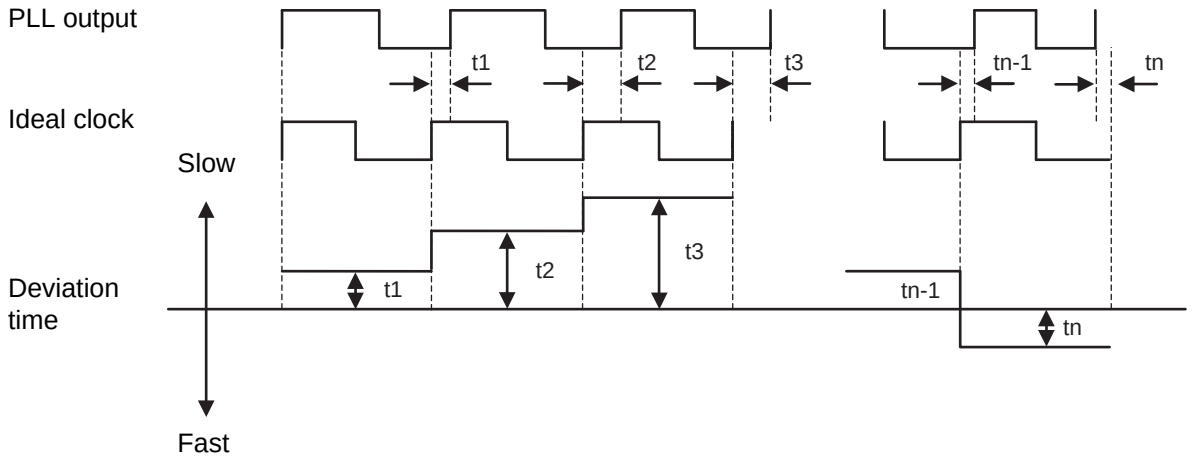
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(9) CAN PLL cycle jitter

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
CAN PLL cycle jitter (When locked)	t_{PJ}	—	—	− 10	—	+ 10	ns	F_{CP} = 16 MHz (4 MHz × multiplied by 4) 24 MHz (4 MHz × multiplied by 6) 32 MHz (4 MHz × multiplied by 8)

• CAN PLL cycle jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.



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5. A/D Converter

($3.0\ V \le AVR = AV_{SS}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN15	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN15	AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 0.5 LSB	V	
Compare time	—	—	0.66	—	16500	µs	$4.5\ V \le AV_{CC} \le 5.5\ V$
			2.2				$3.0\ V \le AV_{CC} < 4.5\ V$
Sampling time	—	—	0.4	—	∞	µs	$4.5\ V \le AV_{CC} \le 5.5\ V$
			1.0				$3.0\ V \le AV_{CC} < 4.5\ V$
Analog port input current	I_{AIN}	AN0 to AN15	–0.3	—	+0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN15	AV_{SS}	—	AVR	V	
Reference voltage range	—	AVR	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVR	—	600	900	µA	
	I_{RH}	AVR	—	—	5	µA	*
Offset between input channels	—	AN0 to AN15	—	—	4	LSB	

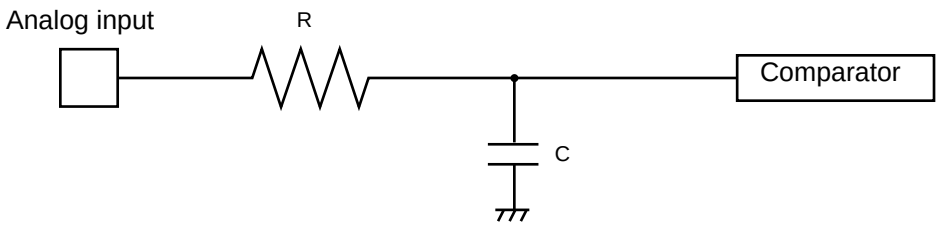
* : If A/D converter is not operating, a current when CPU is stopped is applicable ($V_{CC} = AV_{CC} = AVR = 5.0\ V$) .

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- **About the external impedance of analog input and its sampling time**

  A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage changed to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. And, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input equivalent circuit model



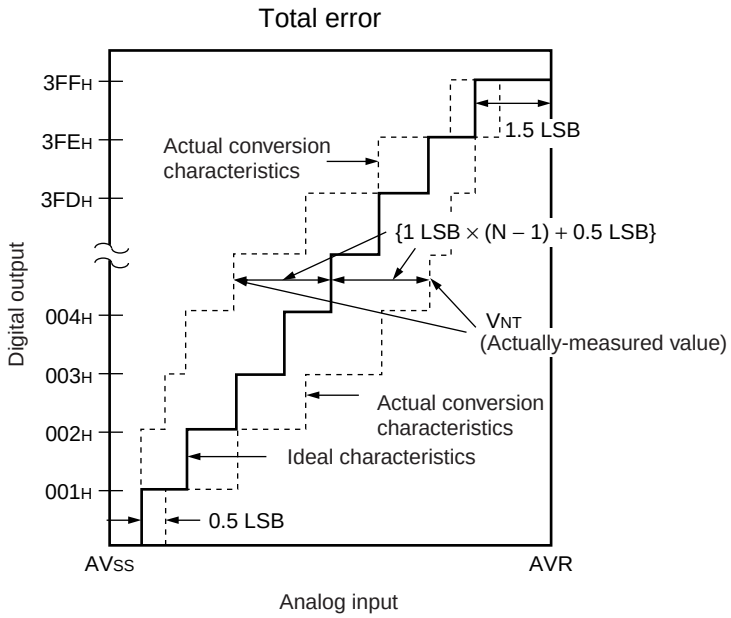
MB90V950AMAS	4.5 V ≤ AV_{CC} ≤ 5.5 V : R ≒ 2.52 kΩ, C ≒ 10.7 pF
MB90V950AJAS	4.0 V ≤ AV_{CC} < 4.5 V : R ≒ 13.6 kΩ, C ≒ 10.7 pF
MB90F997MBS	4.5 V ≤ AV_{CC} ≤ 5.5 V : R ≒ 4.1 kΩ, C ≒ 8.5 pF
MB90F997JBS	3.0 V ≤ AV_{CC} < 4.5 V : R ≒ 10.33 kΩ, C ≒ 8.5 pF

Note : The values are reference values.

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6. Definition of A/D Converter Terms

Resolution	:	Analog variation that is recognized by an A/D converter.
Non linearity error	:	Deviation between a line across zero-transition line (“00 0000 0000$_B$” ← → “00 0000 0001$_B$”) and full-scale transition line (“11 1111 1110$_B$” ← → “11 1111 1111$_B$”) and actual conversion characteristics.
Differential linearity error	:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	:	Difference between an actual value and an theoretical value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{AVR - AV_{SS}}{1024}\ [\text{V}]$$

N : A/D converter digital output value

V_{OT} (Ideal value) = AV_{SS} + 0.5 LSB [V]

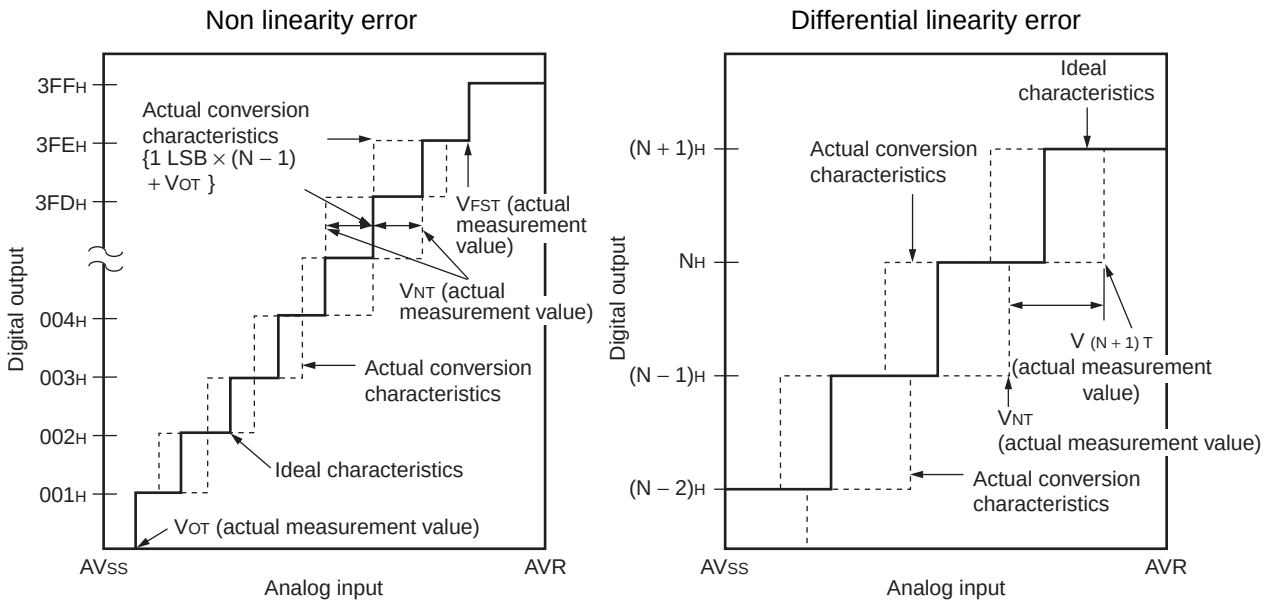
V_{FST} (Ideal value) = AVR – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transits from (N – 1) $_H$ to N_H.

(Continued)

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(Continued)



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)\,T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

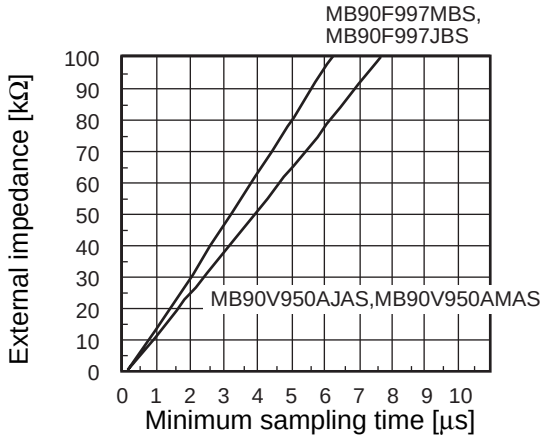
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

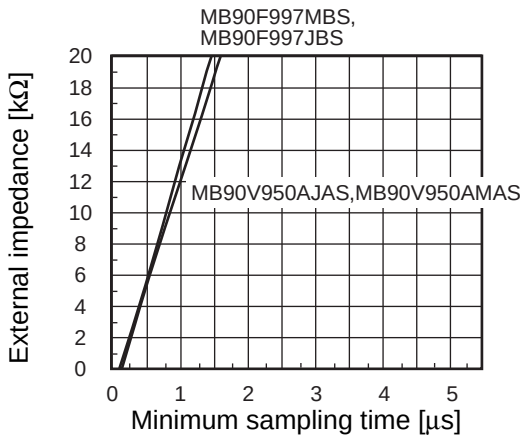
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- The relationship between external impedance and minimum sampling time
  - At 4.5 V ≤ AVcc ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)



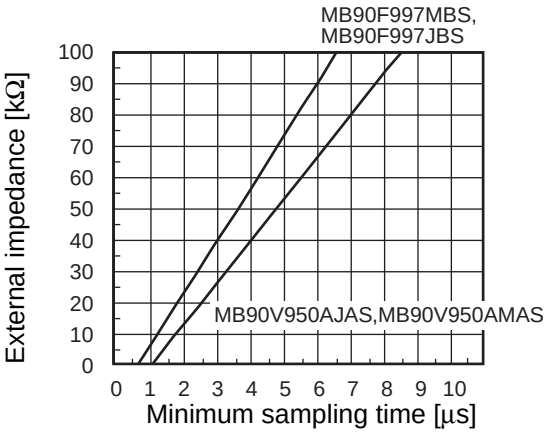
(External impedance = 0 kΩ to 20 kΩ)



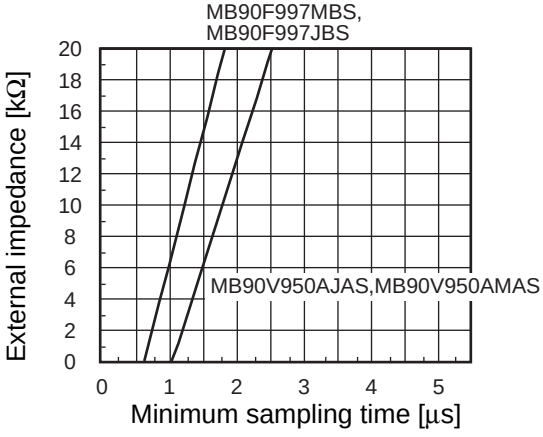
	Minimum sampling time [µs] (4.5 V ≤ AVcc ≤ 5.5 V)		
External impedance [kΩ]	5	10	50
MB90F997MBS, MB90F997JBS	0.54	0.84	3.22
MB90V950AJAS,MB90V950AMAS	0.56	0.94	3.93

  - At 3.0 V ≤ AVcc < 4.5 V

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



	Minimum sampling time [µs] (3.0 V ≤ AVcc < 4.5 V)		
External impedance [kΩ]	5	10	50
MB90F997MBS, MB90F997JBS	0.91	1.21	3.59
MB90V950AJAS,MB90V950AMAS	1.39	1.77	4.76

- **About errors**

As | AVR – AVss | becomes smaller, values of relative errors grow larger.

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7. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	—	—	0.9	3.6	s	Excludes programming prior to erasure
Chip erase time		—	5.4	21.6	s	Main Flash
		—	3.6	14.4	s	Satellite Flash
Byte (8-bit width) programming time	—	—	15	240	µs	Except for the overhead time of the system level
Word (16-bit width) programming time	—	—	23	370	µs	
Program/Erase cycle	T_A > +85 °C	10000	—	—	cycle	
	T_A ≤ +85 °C	100000	—	—	cycle	
Flash memory data retention time	Average T_A = +85 °C	20	—	—	year	*

* : Corresponding value comes from the technology reliability evaluation result (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

8. D/A Converter

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	8	—	bit	
Non linearity error	—	—	– 0.5	—	+ 0.5	LSB	
Conversion time	—	—	0.773	0.787	1.078	µs	C_L = 20pF
			2.490	2.535	3.474		C_L = 100pF
Output impedance	Ro	DA0	3.19	3.50	4.80	kΩ	
Power supply current	I_A	AV_{CC}	—	476	920	µA	
	I_{AH}	AV_{CC}	—	—	5	µA	

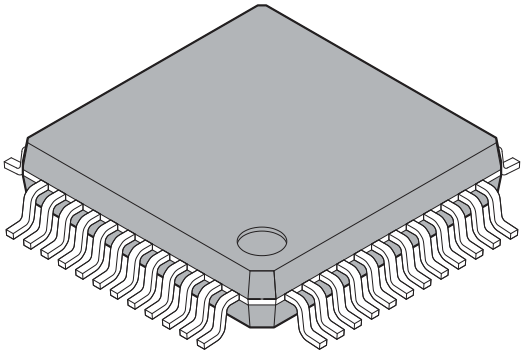
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■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F997JBSPMC	48-pin plastic LQFP (FPT-48P-M26)	
MB90F997MBSPMC		
MB90V950AMASCR-ES	299-pin ceramic PGA (PGA-299C-A01)	For evaluation
MB90V950AJASCR-ES		

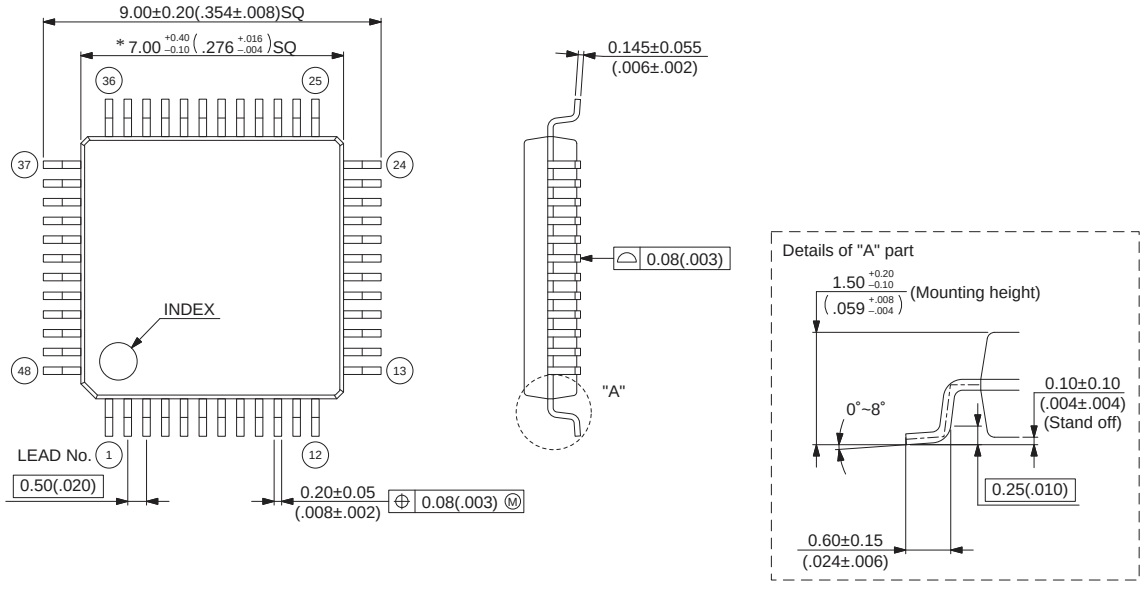
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■ PACKAGE DIMENSION

48-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	7 × 7 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g
(FPT-48P-M26)	Code (Reference)	P-LFQFP48-7×7-0.50

48-pin plastic LQFP
(FPT-48P-M26)

Note 1) * : These dimensions include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Changed the part number. MB90V950MAS → MB90V950AMAS MB90V950JAS → MB90V950AJAS
56	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics	Added the item “(9) CAN PLL cycle jitter”.

The vertical lines marked in the left side of the page show the changes.

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MB90990 Series

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