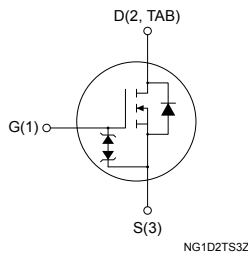
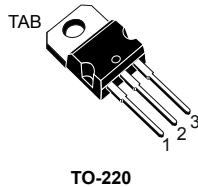


N-channel 500 V, 2.8 Ω typ., 2.3 A SuperMESH Power MOSFET in a TO-220 package

Features



Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP3NK50Z	500 V	3.3 Ω	2.3 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Zener-protected

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.



Product status link

[STP3NK50Z](#)

Product summary

Order code	STP3NK50Z
Marking	P3NK50Z
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	2.3	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	1.45	
$I_{DM}^{(1)}$	Drain current (pulsed)	9.2	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	45	W
ESD	Gate-source human body model ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$)	2	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		

1. Pulse width is limited by safe operating area.

2. $I_{SD} \leq 2\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	2.78	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	$^{\circ}\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	2.3	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	120	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	500	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$	-	-	50	
I_{GSS}	Gate-body leakage current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$	-	-	± 10	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.15\text{ A}$	-	2.8	3.3	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	280	-	pF
C_{oss}	Output capacitance		-	42	-	pF
C_{rss}	Reverse transfer capacitance		-	8	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }400\text{ V}$	-	27.5	-	pF
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 2.3\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 14. Test circuit for gate charge behavior)	-	11	15 ⁽²⁾	nC
Q_{gs}	Gate-source charge		-	2.5	-	nC
Q_{gd}	Gate-drain charge		-	5.6	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

2. Specified by design, not tested in production.

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 1.15\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	8	-	ns
t_r	Rise time		-	13	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	24	-	ns
t_f	Fall time		-	14	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	2.3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	9.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.3 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	-	1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 2.3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 40 \text{ V}$	-	250	-	ns
Q_{rr}	Reverse recovery charge		-	0.745	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	6	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 2.3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 40 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$	-	300	-	ns
Q_{rr}	Reverse recovery charge		-	0.96	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	6.2	-	A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

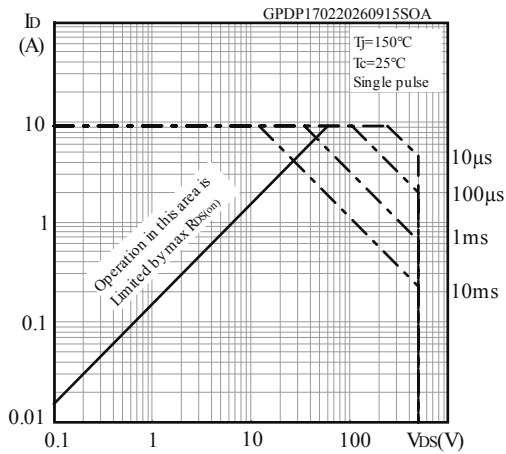
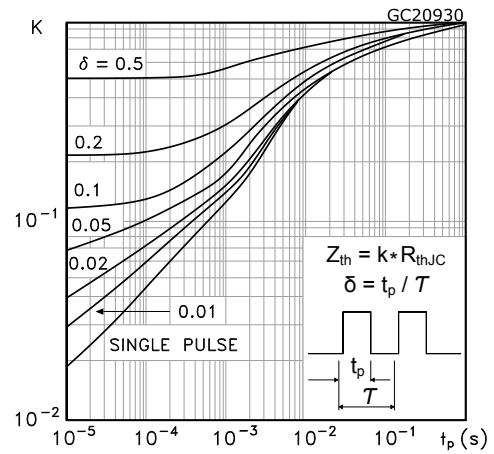
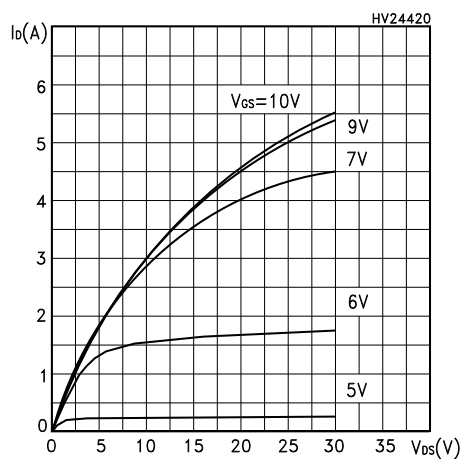
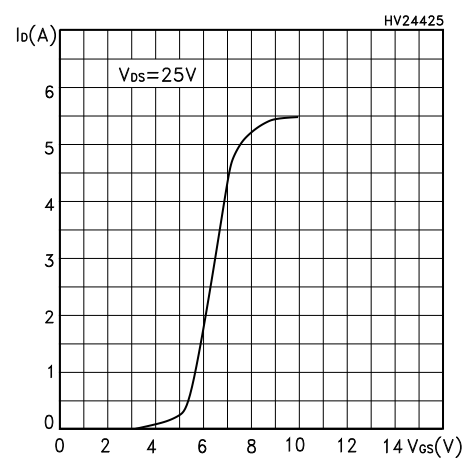
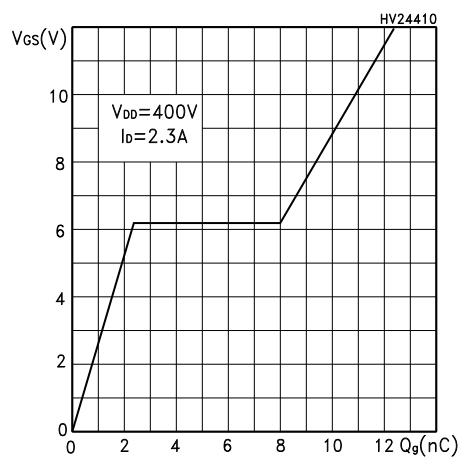
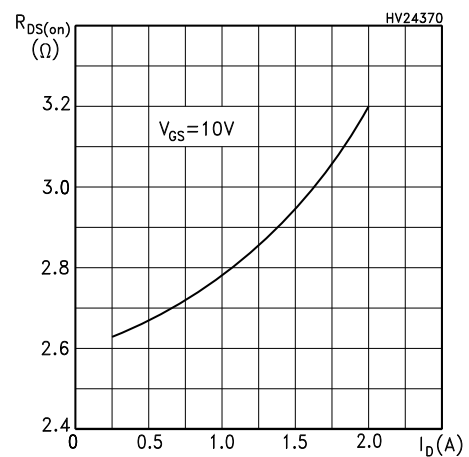
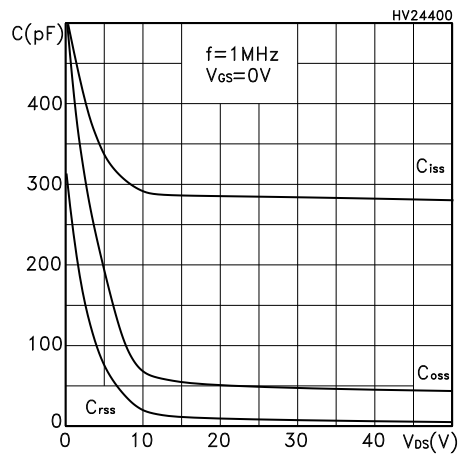
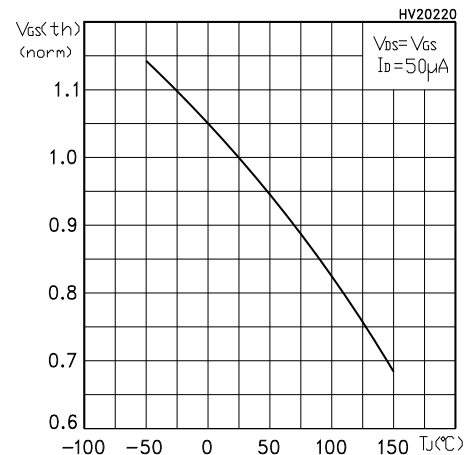
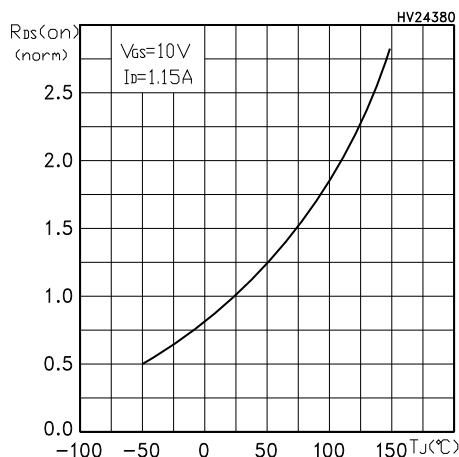
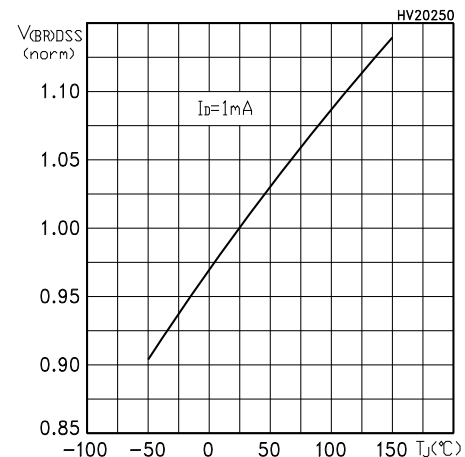
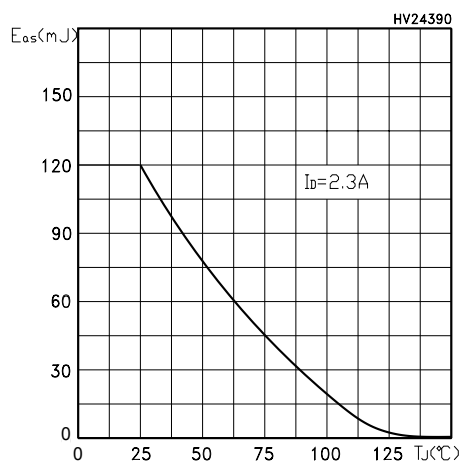
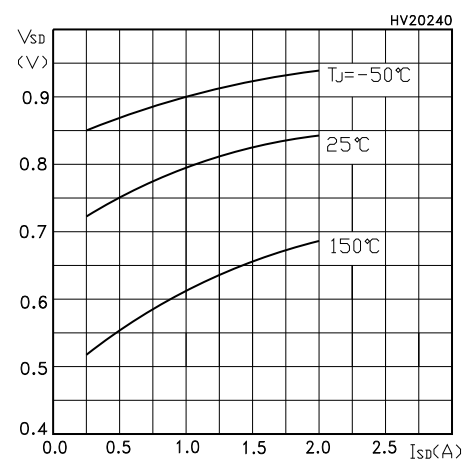
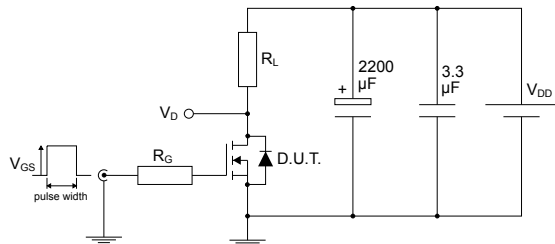
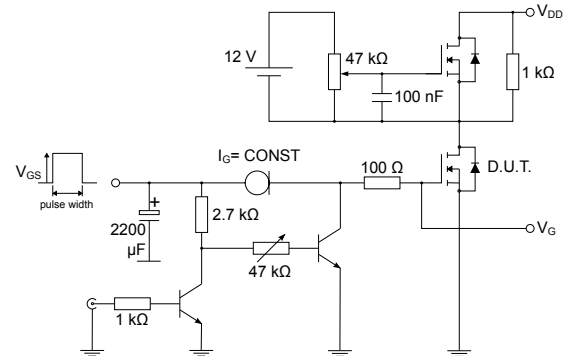
Figure 1. Safe operating area

Figure 2. Normalized transient thermal impedance

Figure 3. Typical output characteristics

Figure 4. Typical transfer characteristics

Figure 5. Typical gate charge characteristics

Figure 6. Typical drain-source on-resistance


Figure 7. Typical capacitance characteristics

Figure 8. Normalized gate threshold vs temperature

Figure 9. Normalized on-resistance vs temperature

Figure 10. Normalized breakdown voltage vs temperature

Figure 11. Maximum avalanche energy vs temperature

Figure 12. Typical reverse diode forward characteristics


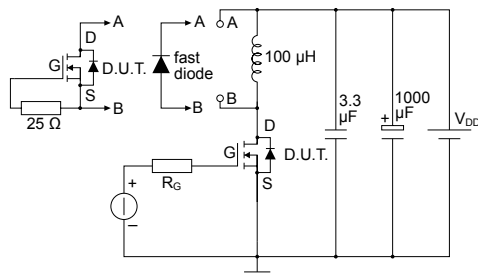
3 Test circuits

Figure 13. Test circuit for resistive load switching times


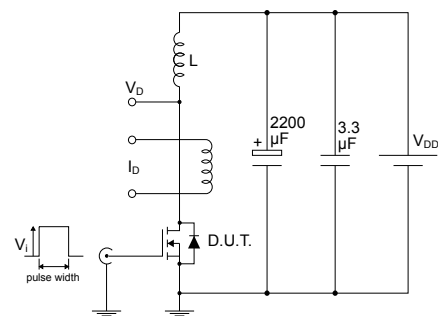
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Figure 14. Test circuit for gate charge behavior


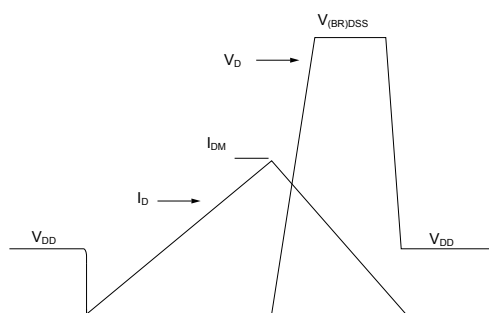
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Figure 15. Test circuit for inductive load switching and diode recovery times


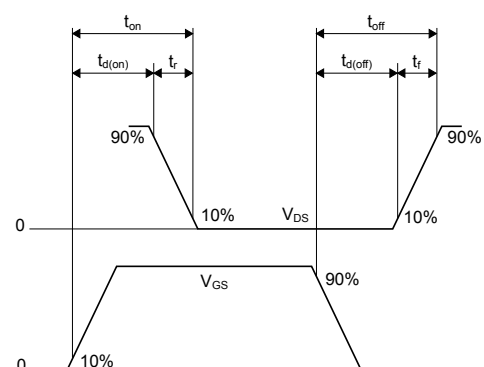
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


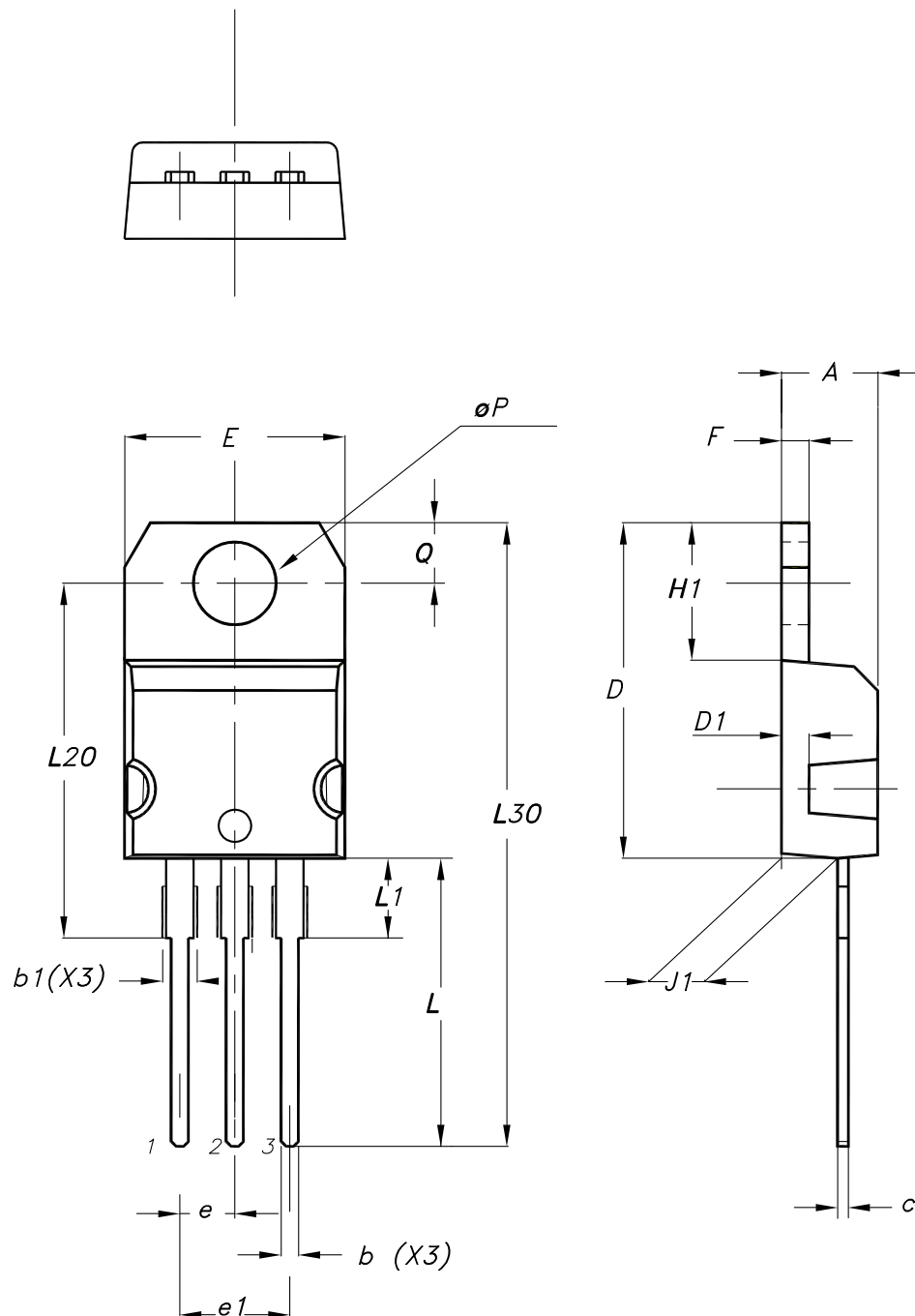
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 19. TO-220 type A package outline



0015988_typeA_Rev_24

Table 8. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 9. Document revision history

Date	Revision	Changes
13-Aug-2013	1	First release.
17-Feb-2026	2	Updated Section 4: Package information . Minor text changes.

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