

MC74HC4020A

14-Stage Binary Ripple Counter

High-Performance Silicon-Gate CMOS

The MC74C4020A is identical in pinout to the standard CMOS MC14020B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master-slave flip-flops with 12 stages brought out to pins. The output of each flip-flop feeds the next and the frequency at each output is half of that of the preceding one. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4020A for some designs.

Features

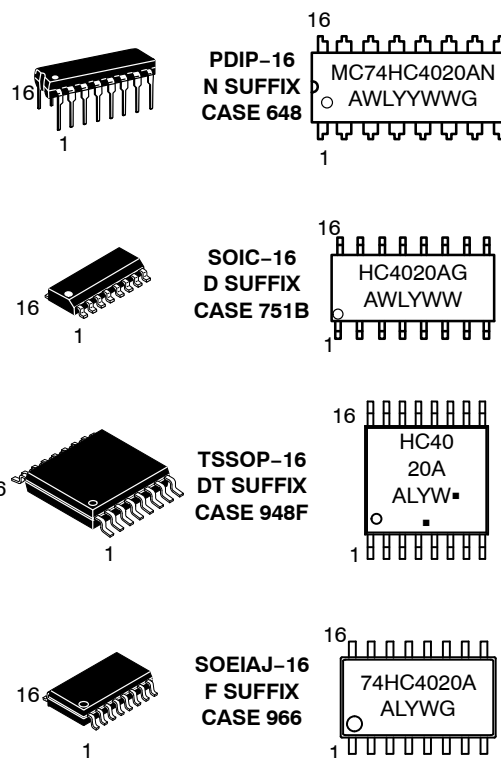
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates
- Pb-Free Packages are Available



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MARKING DIAGRAMS



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC74HC4020A

FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to Next State
X	H	All Outputs Are Low

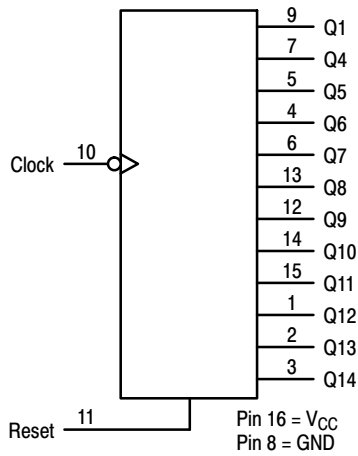


Figure 1. Logic Diagram

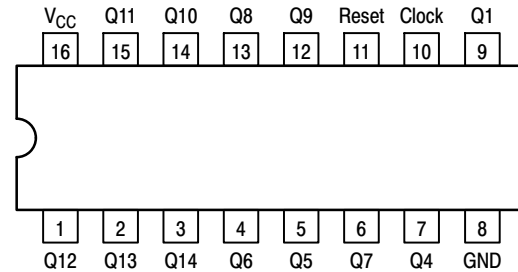


Figure 2. Pinout: 16-Lead Plastic Package
(Top View)

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC4020AN	PDIP-16	500 Units / Rail
MC74HC4020ANG	PDIP-16 (Pb-Free)	500 Units / Rail
MC74HC4020AD	SOIC-16	48 Units / Rail
MC74HC4020ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC4020ADR2	SOIC-16	2500 / Tape & Reel
MC74HC4020ADR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC74HC4020ADTR2	TSSOP-16*	2500 / Tape & Reel
MC74HC4020ADTR2G	TSSOP-16*	2500 / Tape & Reel
MC74HC4020AF	SOEIAJ-16	50 Units / Rail
MC74HC4020AFG	SOEIAJ-16 (Pb-Free)	50 Units / Rail
MC74HC4020AFEL	SOEIAJ-16	2000 / Tape & Reel
MC74HC4020AFELG	SOEIAJ-16 (Pb-Free)	2000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MC74HC4020A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature Range, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise/Fall Time (Figure 1)	V _{CC} = 2.0 V	0	1000	ns
		V _{CC} = 3.0 V	0	600	
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	

MC74HC4020A

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4mA I _{out} ≤ 4.0mA I _{out} ≤ 5.2mA	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4mA I _{out} ≤ 4.0mA I _{out} ≤ 5.2mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0μA	6.0	4	40	160	μA

MC74HC4020A

AC CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	10	9.0	8.0	MHz
		3.0	15	14	12	
		4.5	30	28	25	
		6.0	50	50	40	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4)	2.0	96	106	115	ns
		3.0	63	71	88	
		4.5	31	36	40	
		6.0	25	30	35	
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0	65	72	90	ns
		3.0	30	36	40	
		4.5	30	35	40	
		6.0	26	32	35	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Qn to Qn+1 (Figures 3 and 4)	2.0	69	80	90	ns
		3.0	40	45	50	
		4.5	17	21	28	
		6.0	14	15	22	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	15	19	
C_{in}	Maximum Input Capacitance		10	10	10	pF

* For $T_A = 25^\circ\text{C}$ and $C_L = 50 \text{ pF}$, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

$$V_{CC} = 2.0 \text{ V: } t_p = [93.7 + 59.3 (n-1)] \text{ ns}$$

$$V_{CC} = 4.5 \text{ V: } t_p = [30.25 + 14.6 (n-1)] \text{ ns}$$

$$V_{CC} = 3.0 \text{ V: } t_p = [61.5 + 34.4 (n-1)] \text{ ns}$$

$$V_{CC} = 6.0 \text{ V: } t_p = [24.4 + 12 (n-1)] \text{ ns}$$

C_{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	pF
		38	

MC74HC4020A

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	30	40	50	ns
		3.0	20	25	30	
		4.5	5	8	12	
		6.0	4	6	9	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	15	19	24	
		6.0	13	16	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	15	19	24	
		6.0	13	16	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

Clock (Pin 10)

Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter.

Reset (Pin 11)

Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

OUTPUTS

Q1, Q4—Q14 (Pins 9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3)

Active-high outputs. Each Q_n output divides the Clock input frequency by 2^N.

SWITCHING WAVEFORMS

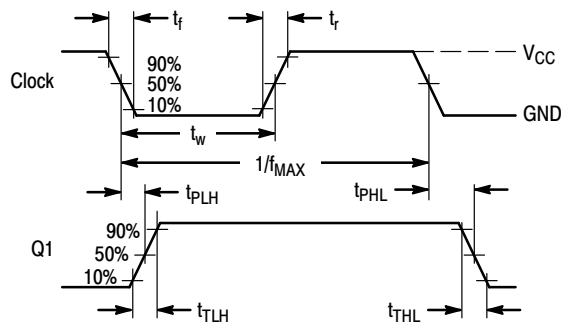


Figure 3.

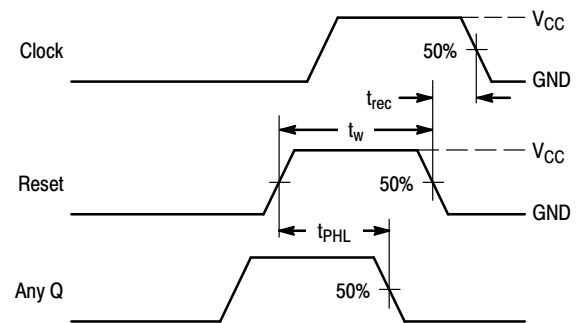


Figure 4.

MC74HC4020A

SWITCHING WAVEFORMS (continued)

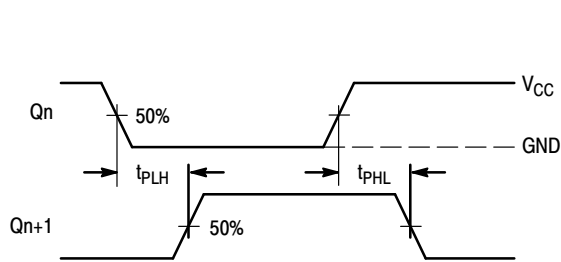
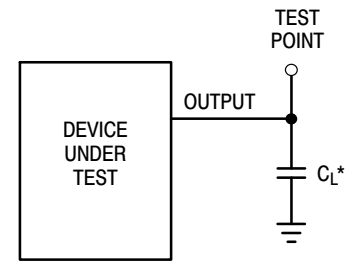


Figure 5.



*Includes all probe and jig capacitance

Figure 6. Test Circuit

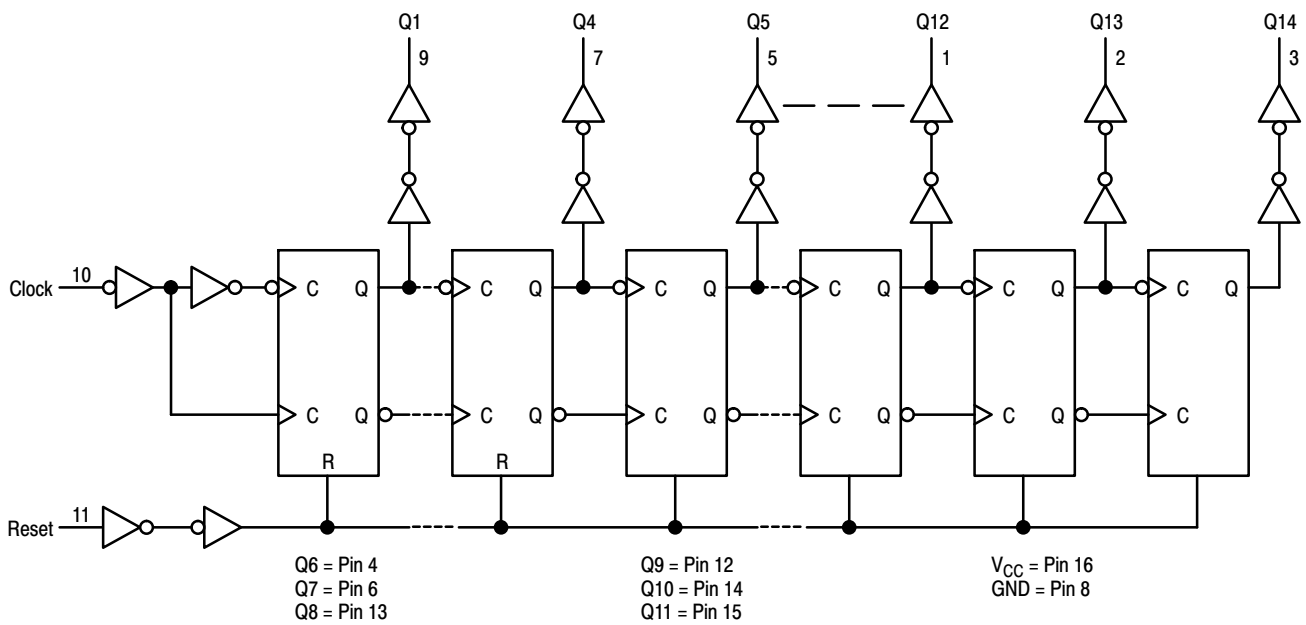


Figure 7. Expanded Logic Diagram

MC74HC4020A

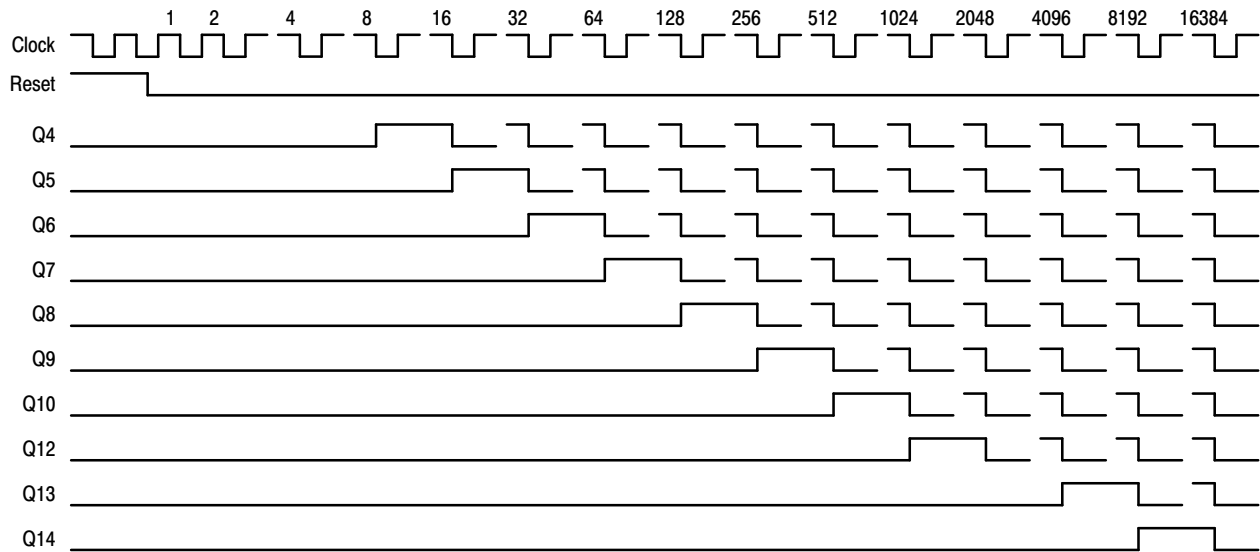


Figure 8. Timing Diagram

APPLICATIONS INFORMATION

Time-Base Generator

A 60Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the input of the MC54/74HC14A, Schmitt-trigger inverter. The HC14A squares-up the input waveform and

feeds the HC4020A. Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.

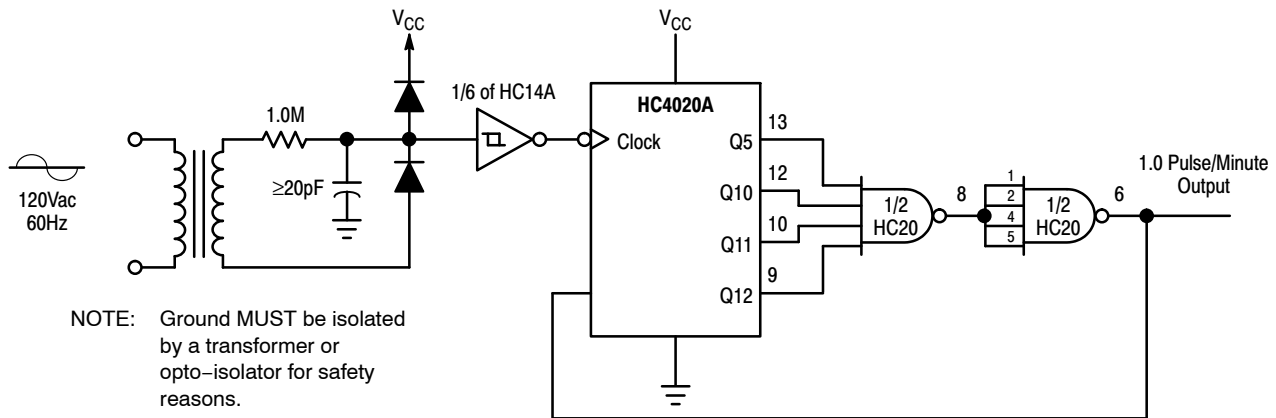
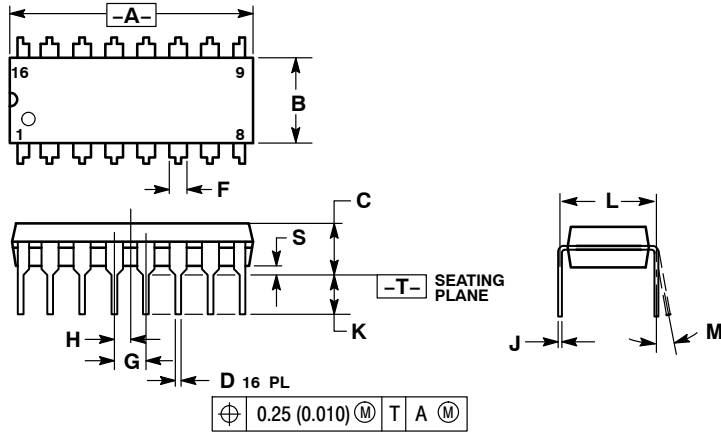


Figure 9. Time-Base Generator

MC74HC4020A

PACKAGE DIMENSIONS

PDIP-16
N SUFFIX
CASE 648-08
ISSUE T



NOTES:

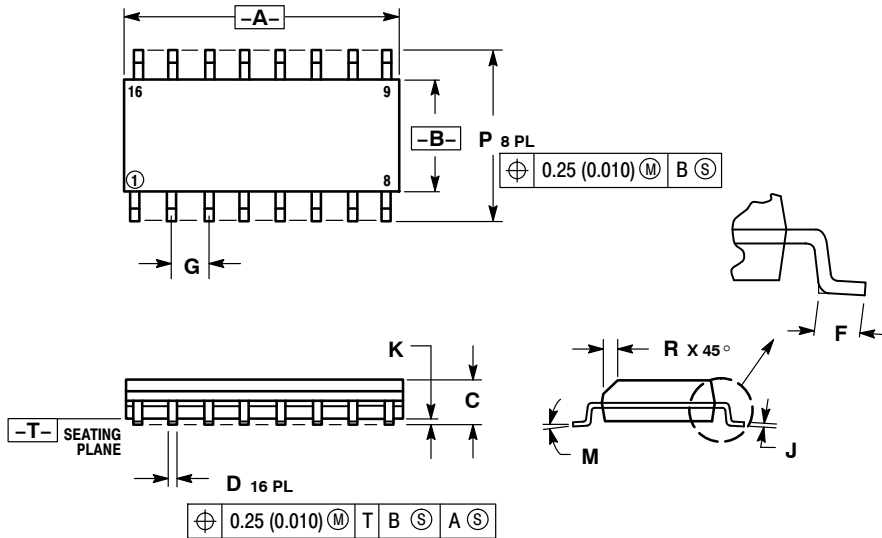
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

MC74HC4020A

PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

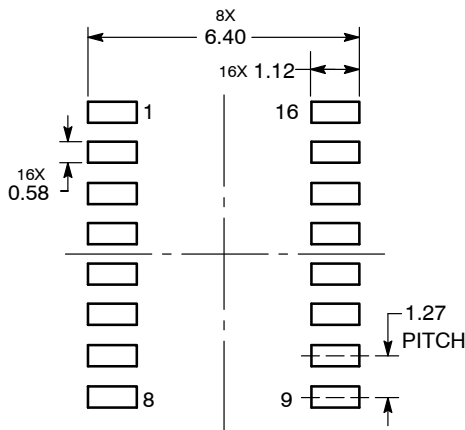


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT



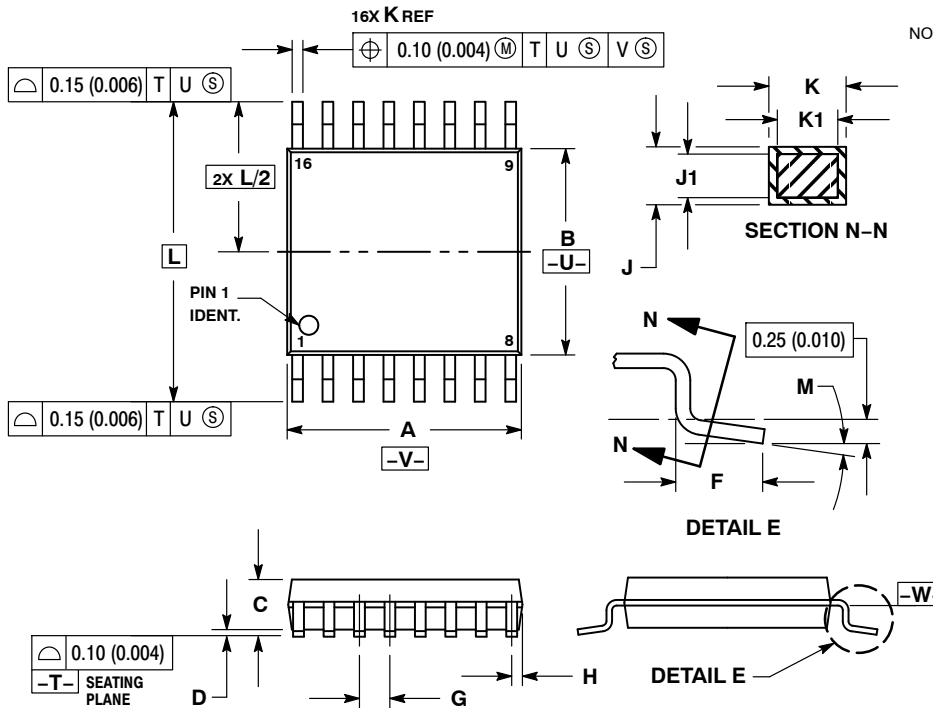
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HC4020A

PACKAGE DIMENSIONS

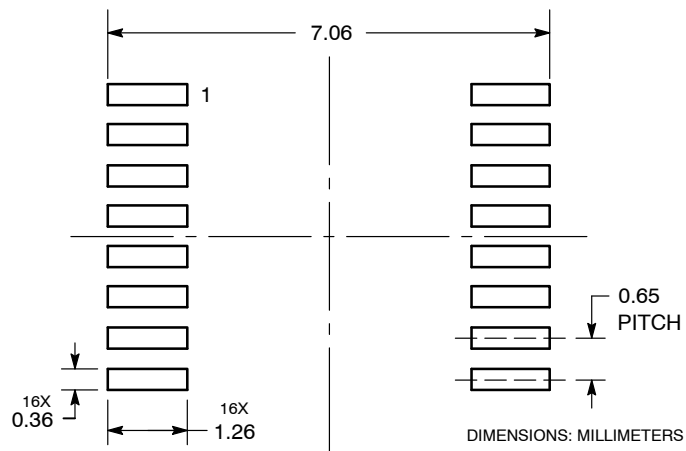
TSSOP-16
CASE 948F-01
ISSUE B



NOTES:

- 1.DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2.CONTROLLING DIMENSION: MILLIMETER.
- 3.DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 4.DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 5.DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6.TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7.DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

SOLDERING FOOTPRINT

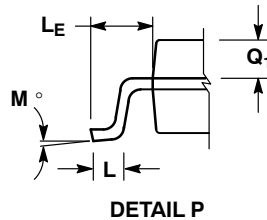
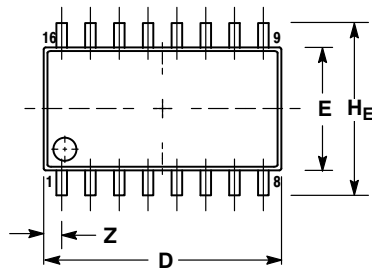


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

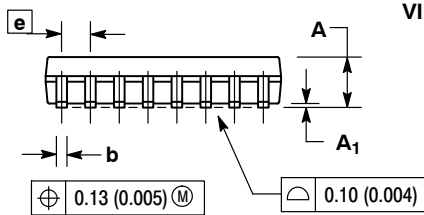
MC74HC4020A

PACKAGE DIMENSIONS

SOEIAJ-16
CASE 966-01
ISSUE A



DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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