TPS22907 3.6-V, 1-A, 44-mΩ ON-Resistance Load Switch With Controlled Turnon

1 Features

- Integrated P-Channel Load Switch
- Low Input Voltage: 1.1 V to 3.6 V
- ON-Resistance (Typical Values):
  - R_{ON} = 44 mΩ at V_{IN} = 3.6 V
  - R_{ON} = 50 mΩ at V_{IN} = 2.5 V
  - R_{ON} = 58 mΩ at V_{IN} = 1.8 V
  - R_{ON} = 83 mΩ at V_{IN} = 1.2 V
- 1-A Maximum Continuous Switch Current
- Maximum Quiescent Current (I_Q) < 1 µA
- Maximum Shutdown Current (I_{SD}) < 1 µA
- Low Control Input Thresholds Enable Use of 1.2-V, 1.8-V, 2.5-V, and 3.3-V Logic
- Controlled Slew-Rate to Avoid Inrush Currents
  - t_R = 25 µs at V_{IN} = 3.6 V
  - t_R = 36 µs at V_{IN} = 1.8 V
- ESD Performance Tested Per JESD 22
  - 3000-V Human Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Ultra-Small 4-Terminal Wafer-Chip-Scale Package (WCSP)
  - Nominal Dimensions Shown – See Addendum for Details
  - 0.9 mm × 0.9 mm, 0.5-mm Pitch, 0.5-mm Height (YZT)

2 Applications

- Battery-Powered Equipment
- Portable Industrial Equipment
- Portable Medical Equipment
- Portable Media Players
- Point-of-Sale Terminal
- GPS Devices
- Digital Cameras
- Portable Instrumentation
- Smart Phones and Tablets

3 Description

The TPS22907 is a small, low R_{ON} load switch with controlled turnon. The device contains a P-channel MOSFET that operates over an input voltage range of 1.1 V to 3.6 V. The switch is controlled by an on and off input (ON), which can interface directly with low-voltage control signals.

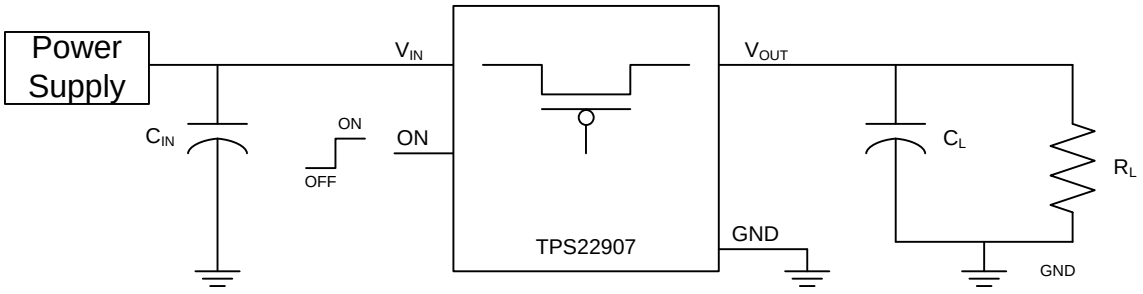
The TPS22907 is available in a space-saving 4-terminal WCSP with 0.5-mm pitch (YZT). The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22907	DSBGA (4)	0.90 mm × 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2013) to Revision B — **Page**

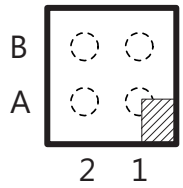
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 3

Changes from Original (November 2009) to Revision A — **Page**

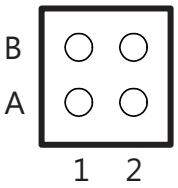
- Changed Feature from: Ultra-Low ON-State Resistance to: Ultra-Low ON-State Resistance (R_{ON}) ... 1
- Changed the Feature for the Wafer-Chip-Scale Package ... 1
- Changed Application from: Point Of Sales Terminal to: Point of Sale Terminal ... 1
- Changed Application from: Smartphones to: Smartphones / Tablets ... 1
- Deleted the *Ordering Information* table ... 1
- Changed the I_{IN} Test Condition from: I_{OUT} = 0 to I_{OUT} = 0 mA ... 4
- Changed the $I_{IN(OFF)}$ Test Condition from: V_{ON} = GND to V_{ON} = 0 V ... 4
- Changed the $I_{IN(LEAKAGE)}$ Test Condition from: V_{ON} = GND, V_{OUT} = 0 to V_{ON} = 0 V, V_{OUT} = 0 V ... 4
- Changed Table 1, Device Feature List ... 11

5 Pin Configuration and Functions

YZT Package
4-Pin DSBGA
(Laser Marking View)



YZT Package
4-Pin DSBGA
(Bump View)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	V_{OUT}	O	Switch output
A2	V_{IN}	I	Switch input, bypass capacitor recommended for minimizing V_{IN} dip. See *Feature Description*.
B1	GND	-—	Ground
B2	ON	I	Switch control input, active high. Do not leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	4	V
V_{OUT}	Output voltage	–0.3	(V_{IN} + 0.3)	V
V_{ON}	Input voltage	–0.3	4	V
I_{MAX}	Maximum continuous switch current		1	A
I_{PLS}	Maximum pulsed current (100-µs pulse, 2% duty cycle), T_A = –40°C to +85°C		2.7	A
T_J	Maximum junction temperature		125	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage range	1.1	3.6	V
V_{OUT}	Output voltage range		V_{IN}	V
V_{IH}	High-level input voltage, ON	0.85	3.6	V
V_{IL}	Low-level input voltage, ON		0.4	V
C_{IN}	Input capacitor	1 (1)		µF
T_A	Operating free-air temperature	–40	85	°C

(1) See *Application Information*.

6.4 Thermal Information

THERMAL METRIC (1) (2)		TPS22907 YZT (DSBGA) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	1.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	37.2	
Ψ_{JT}	Junction-to-top characterization parameter	10.2	
Ψ_{JB}	Junction-to-board characterization parameter	37	
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	—	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

6.5 Electrical Characteristics

Unless otherwise noted, the specification applies over the operating ambient temperature -40°C ≤ T_A ≤ 85°C and V_{IN} = 1.1 V to 3.6 V. Typical values are for V_{IN} = 3.6 V and T_A = 25°C.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_Q	Quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON}	Full		0.07	1	µA
I_{SD}	Off supply current	V_{ON} = 0 V, OUT = Open	Full		0.05	1	µA
$I_{IN(LEAKAGE)}$	Leakage current	V_{ON} = 0 V, V_{OUT} = 0 V	Full		0.05	1	µA
R_{ON}	ON-state resistance	V_{IN} = 3.6 V, I_{OUT} = –200 mA	25°C		44	60	mΩ
			Full			67	
		V_{IN} = 2.5 V, I_{OUT} = –200 mA	25°C		50	63	
			Full			70	
		V_{IN} = 1.8 V, I_{OUT} = –200 mA	25°C		58	72	
			Full			80	
		V_{IN} = 1.2 V, I_{OUT} = –200 mA	25°C		83	106	
			Full			117	
		V_{IN} = 1.1 V, I_{OUT} = –200 mA	25°C		97	125	
			Full			140	
I_{ON}	ON input leakage current	V_{ON} = 0 V to 3.6 V	Full		0.005	1	µA

6.6 Switching Characteristics: V_{IN} = 3.6 V

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 500 Ω, C_L = 0.1 µF		28		µs
t_{OFF}	Turn-OFF time	R_L = 500 Ω, C_L = 0.1 µF		40		µs
t_r	V_{OUT} rise time	R_L = 500 Ω, C_L = 0.1 µF		25		µs
t_f	V_{OUT} fall time	R_L = 500 Ω, C_L = 0.1 µF		116		µs

6.7 Switching Characteristics: V_{IN} = 1.8 V

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 500 Ω, C_L = 0.1 µF		48		µs
t_{OFF}	Turn-OFF time	R_L = 500 Ω, C_L = 0.1 µF		40		µs
t_r	V_{OUT} rise time	R_L = 500 Ω, C_L = 0.1 µF		36		µs
t_f	V_{OUT} fall time	R_L = 500 Ω, C_L = 0.1 µF		113		µs

6.8 Switching Characteristics: V_{IN} = 1.1 V

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 500 Ω, C_L = 0.1 µF		81		µs
t_{OFF}	Turn-OFF time	R_L = 500 Ω, C_L = 0.1 µF		42		µs
t_r	V_{OUT} rise time	R_L = 500 Ω, C_L = 0.1 µF		57		µs
t_f	V_{OUT} fall time	R_L = 500 Ω, C_L = 0.1 µF		113		µs

6.9 Typical DC Characteristics

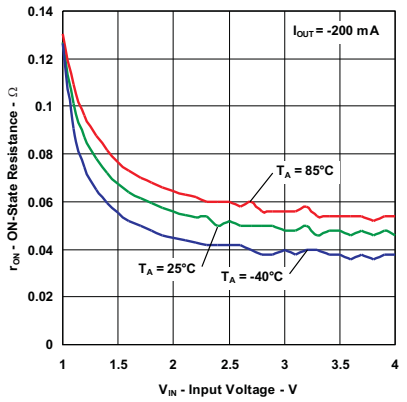


Figure 1. ON-State Resistance vs. Input Voltage

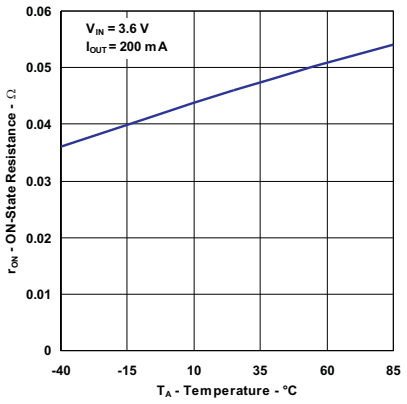


Figure 2. ON-State Resistance vs. Temperature

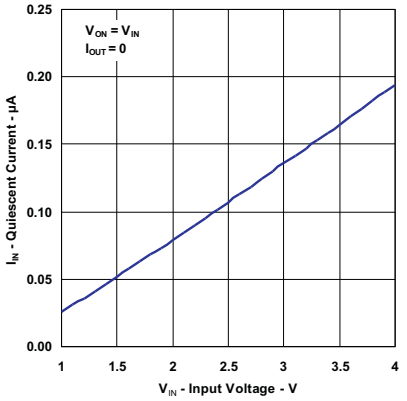


Figure 3. V_{IN} Quiescent Current vs. Input Voltage

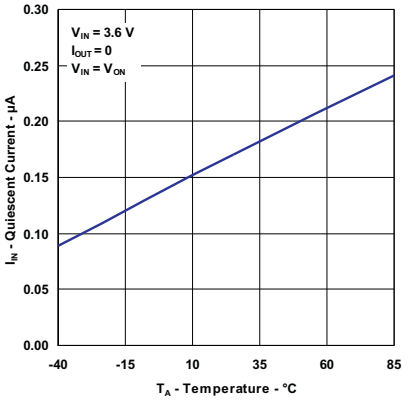


Figure 4. V_{IN} Quiescent Current vs. Temperature

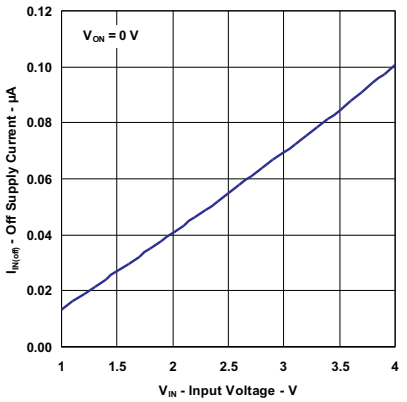


Figure 5. V_{IN} Off Supply Current vs. Input Voltage

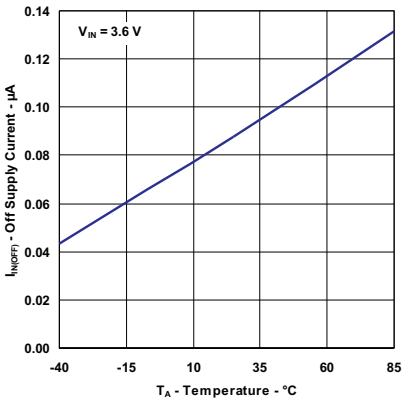


Figure 6. V_{IN} OFF Supply Current vs. Temperature

Typical DC Characteristics (continued)

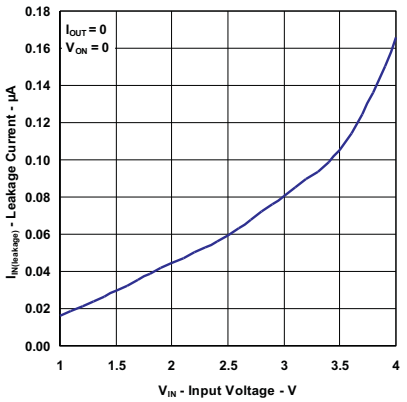


Figure 7. V_{IN} Leakage Current vs. Input Voltage

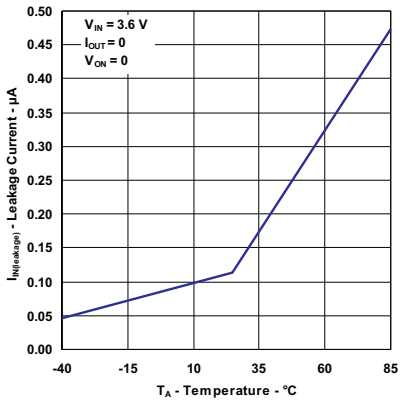


Figure 8. V_{IN} Leakage Current vs. Temperature

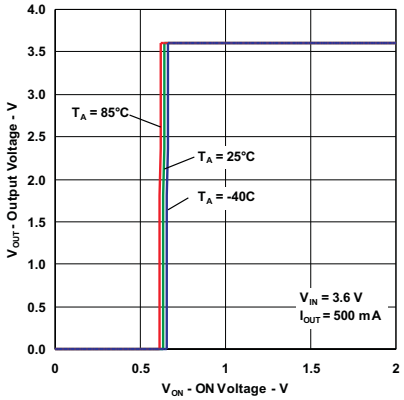


Figure 9. ON Input Threshold

6.10 Typical AC Characteristics

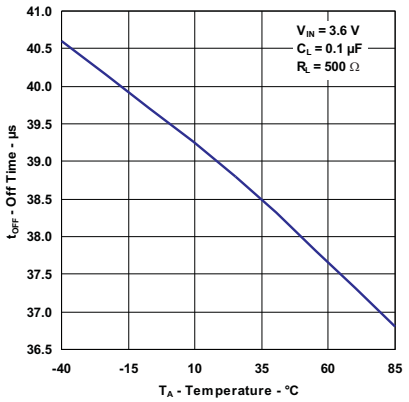


Figure 10. OFF Time vs. Temperature

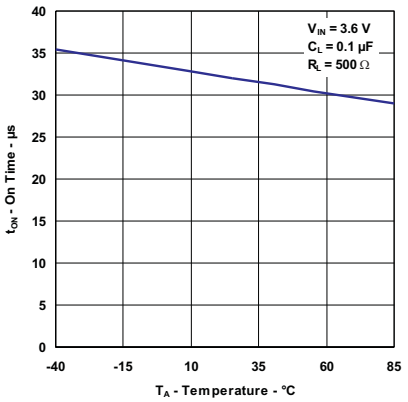


Figure 11. ON Time vs. Temperature

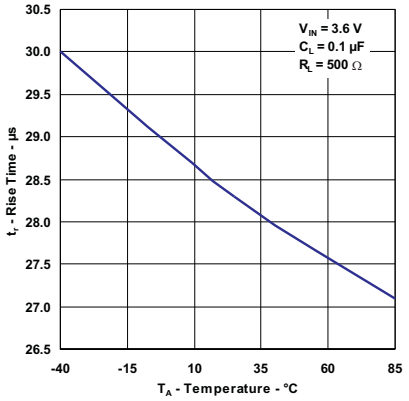


Figure 12. Rise Time vs. Temperature

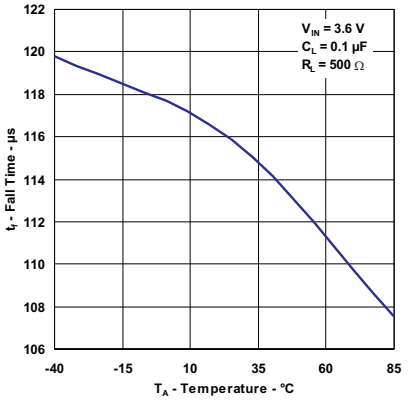


Figure 13. Fall Time vs. Temperature

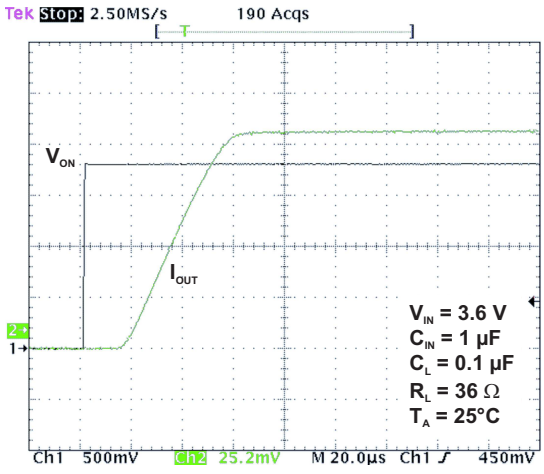


Figure 14. t_{ON} Response

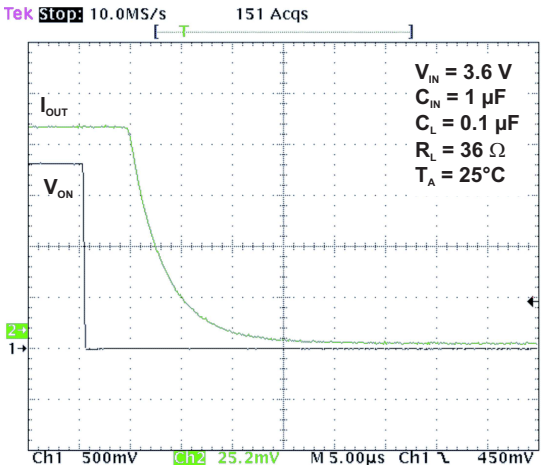


Figure 15. t_{OFF} Response

Typical AC Characteristics (continued)

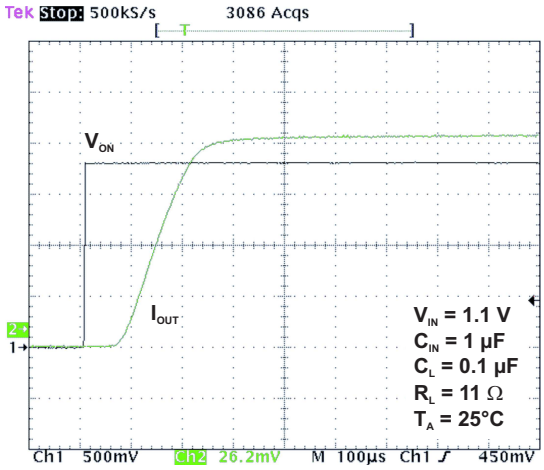


Figure 16. t_{ON} Response

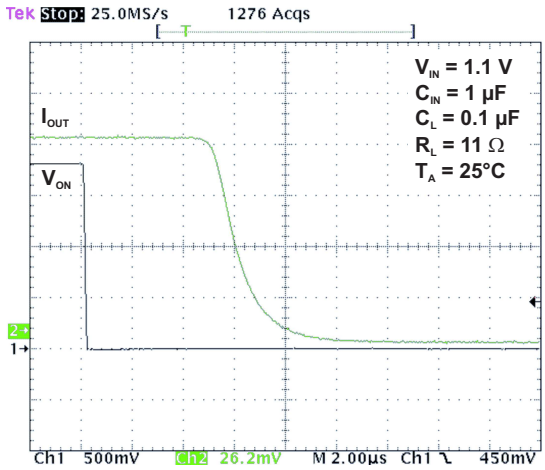


Figure 17. t_{OFF} Response

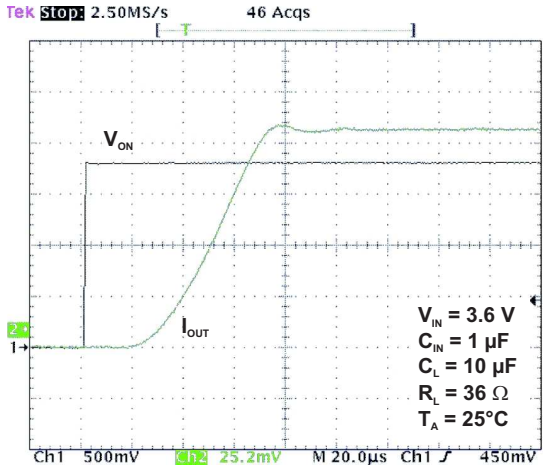


Figure 18. t_{ON} Response

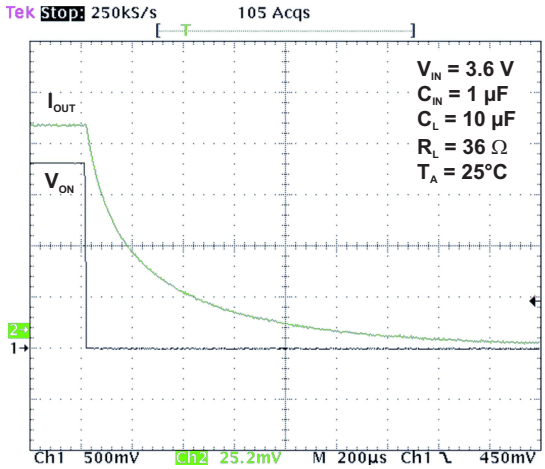


Figure 19. t_{OFF} Response

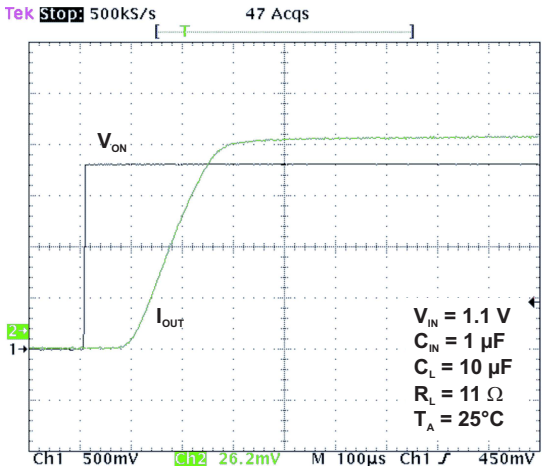


Figure 20. t_{ON} Response

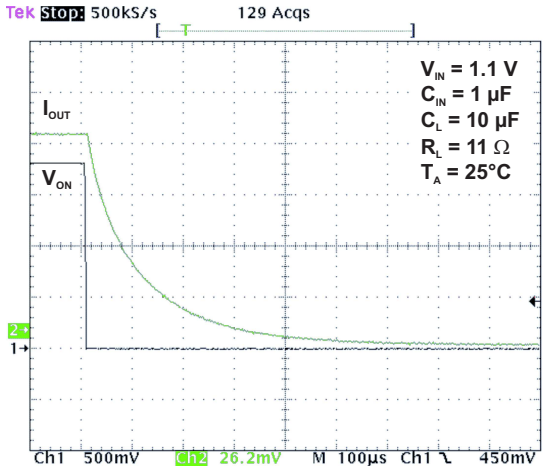
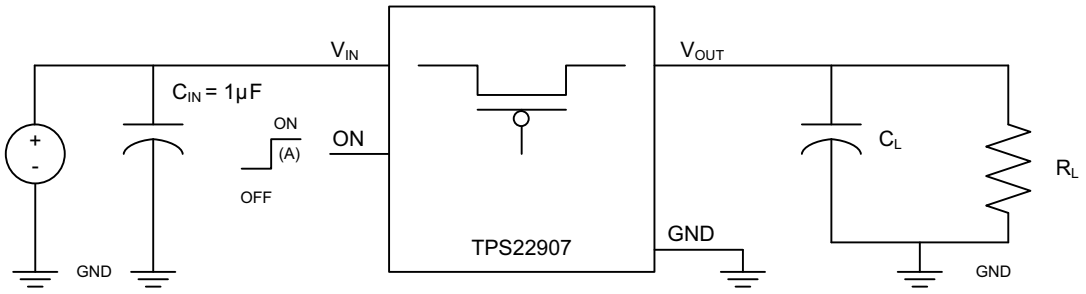
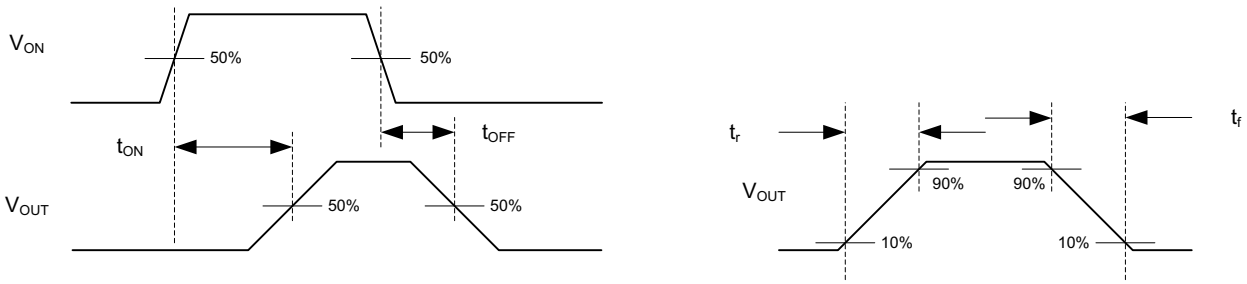


Figure 21. t_{OFF} Response

7 Parameter Measurement Information



TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

(A) Control signal rise and fall times are 100 ns.

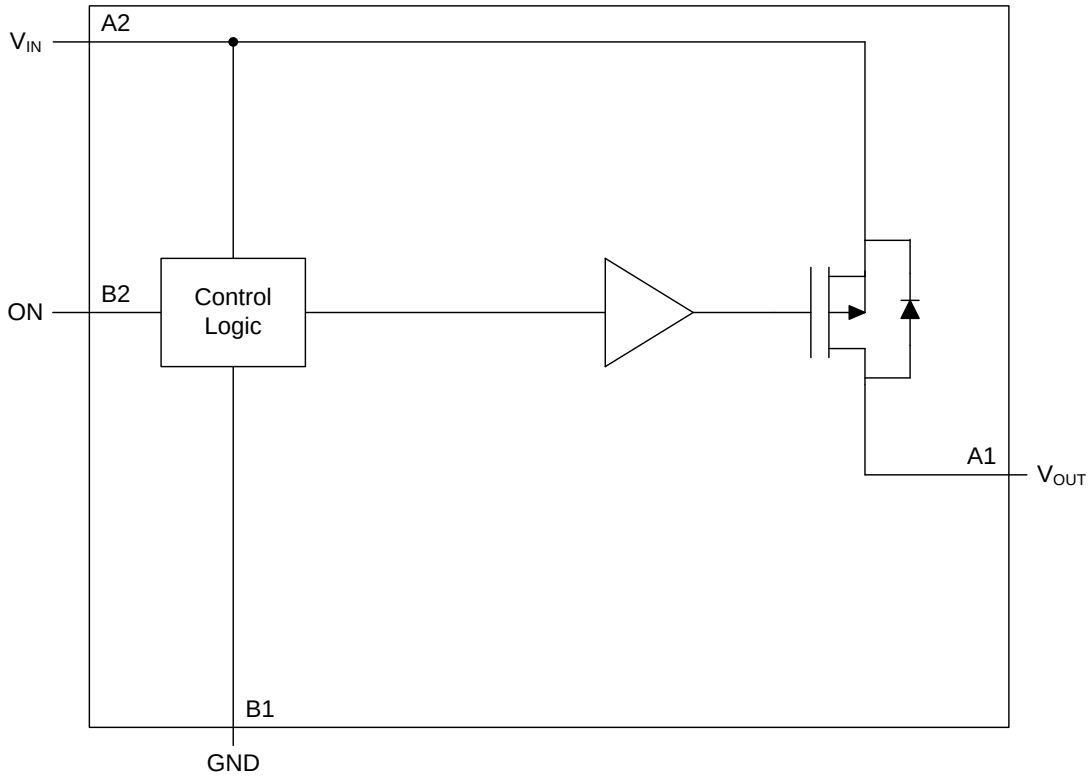
Figure 22. Test Circuit and t_{ON}/t_{OFF} Waveforms

8 Detailed Description

8.1 Overview

The TPS22907 is a single-channel, 1-A load switch in a small, space-saving DSBGA-4 package. This device implements a P-channel MOSFET to provide a low ON-resistance for a low-voltage drop across the device. A controlled rise time is used in applications to limit the inrush current.

8.2 Functional Block Diagram



8.3 Feature Description

Table 1. Device Feature List

DEVICE	R_{ON} (Typical) V_{IN} = 1.8 V	SLEW RATE (Typical) V_{IN} = 1.8 V	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22907	58 mΩ	36 µs	1 A	Active high

8.3.1 On and Off Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, or 3.3-V GPIOs.

8.4 Device Functional Modes

Table 2. Function Table

ON (Control Input)	V_{IN} to V_{OUT}
L	OFF
H	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between V_{IN} and GND. A 1-µF ceramic capacitor, C_{IN}, place close to the pins is usually sufficient. Higher values of C_{IN} can be use to further reduce the voltage drop during high-current application. When switching heavy loads, TI recommends having an input capacitor approximately ten times higher than the output capacitor to avoid excessive voltage drop.

9.1.2 Output Capacitor

Due to the integrated body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of at least 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip at turnon due to inrush currents.

9.2 Typical Application

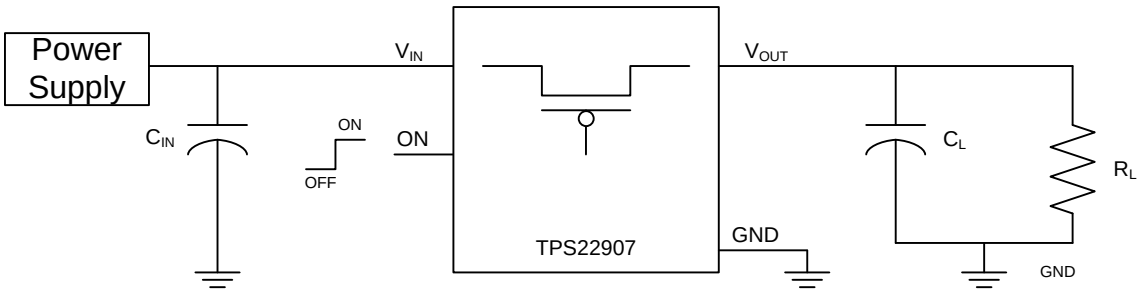


Figure 23. Typical Application Schematic

9.2.1 Design Requirements

Table 3 lists the design requirements for the device.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.6 V
C_L	4.7 µF
Load current	1 A
Ambient Temperature	25 °C
Maximum inrush current	750 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Managing Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.6 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt}$$

where:

- C_L = Output capacitance
- dV_{OUT} = Output voltage
- dt = Rise time (1)

The TPS22907 offers a controlled rise time for minimizing inrush current. This device can be selected based upon the minimum acceptable rise time which can be calculated using the design requirements and the inrush current equation. An output capacitance of 4.7 µF will be used because the amount of inrush current increases with output capacitance:

750 mA = 4.7 µF × 3.6 V / dt

where

- dt = 22.56 µs (2)

To ensure an inrush current of less than 750 mA, a device with a rise time greater than 22.56 µs must be used. The TPS22907 has a typical rise time of 25 µs at 3.6 V which meets the above design requirements.

9.2.2.2 Voltage Drop from V_{IN} to V_{OUT}

The voltage drop from V_{IN} to V_{OUT} is determined by the ON-resistance of the device and the load current. R_{ON} can be found in *Electrical Characteristics* and is dependent on temperature. When the value of R_{ON} is found, the following equation can be used to calculate the voltage drop across the device:

$\Delta V = I_{LOAD} \times R_{ON}$

where:

- ΔV = Voltage drop across the device
- I_{LOAD} = Load current
- R_{ON} = ON-resistance of the device (3)

At V_{IN} = 3.6 V, the TPS22907 has an R_{ON} value of 44 mΩ. Using this value and the defined load current, the above equation can be evaluated:

$\Delta V = 1\ A \times 44\ m\Omega$ (4)

$\Delta V = 44\ mV$

Therefore, the voltage drop across the device will be 44 mV.

9.2.3 Application Curve

Figure 24 shows the inrush current expected for different load capacitances at varying V_{IN} voltages.

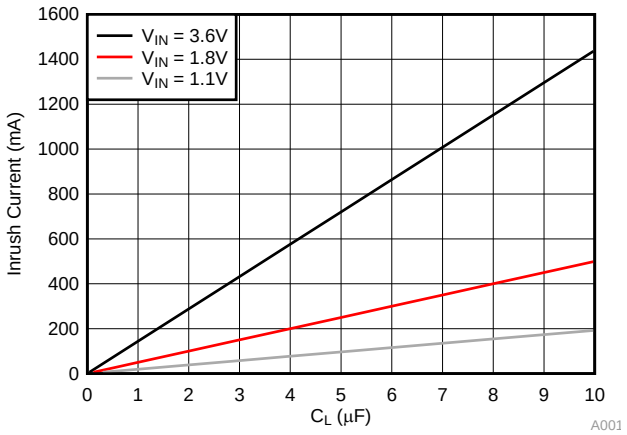


Figure 24. Expected Inrush Current vs Load Capacitance

10 Power Supply Recommendations

The device is designed to operate with a V_{IN} voltage range of 1.1 V to 3.6 V. The power supply should be well regulated and placed as close to the device terminals as possible. It must be able to withstand all transient and load current steps. In most situations, using the minimum recommended input capacitance of 1 uF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

11 Layout

11.1 Layout Guidelines

For best performance, VIN and VOUT traces should be as short and wide as possible to help minimize the parasitic electrical effects. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation.

11.2 Layout Example

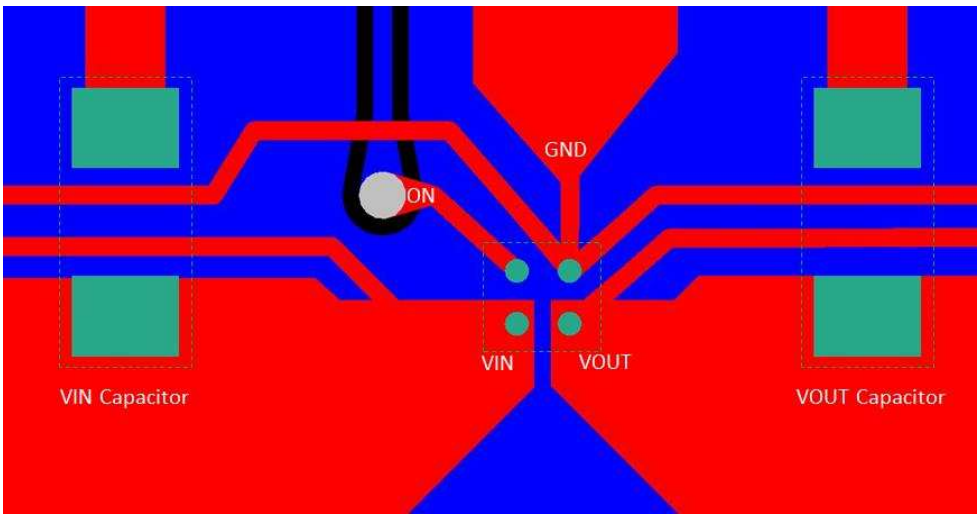


Figure 25. Example Layout for the TPS22907

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22907YZTR	NRND	Production	DSBGA (YZT) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5K (F, G)
TPS22907YZTT	NRND	Production	DSBGA (YZT) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5K (F, G)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

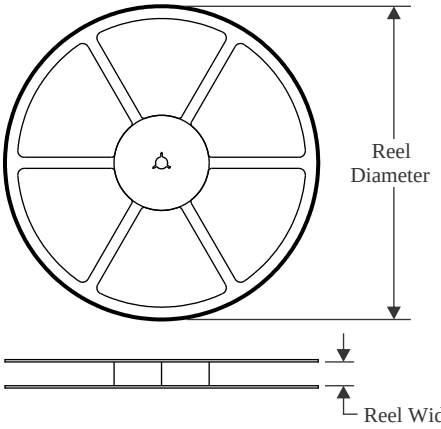
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

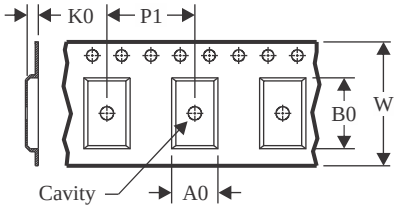
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

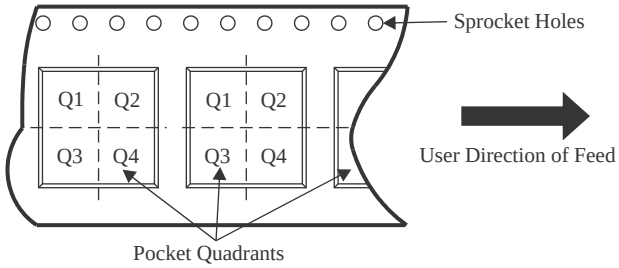


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

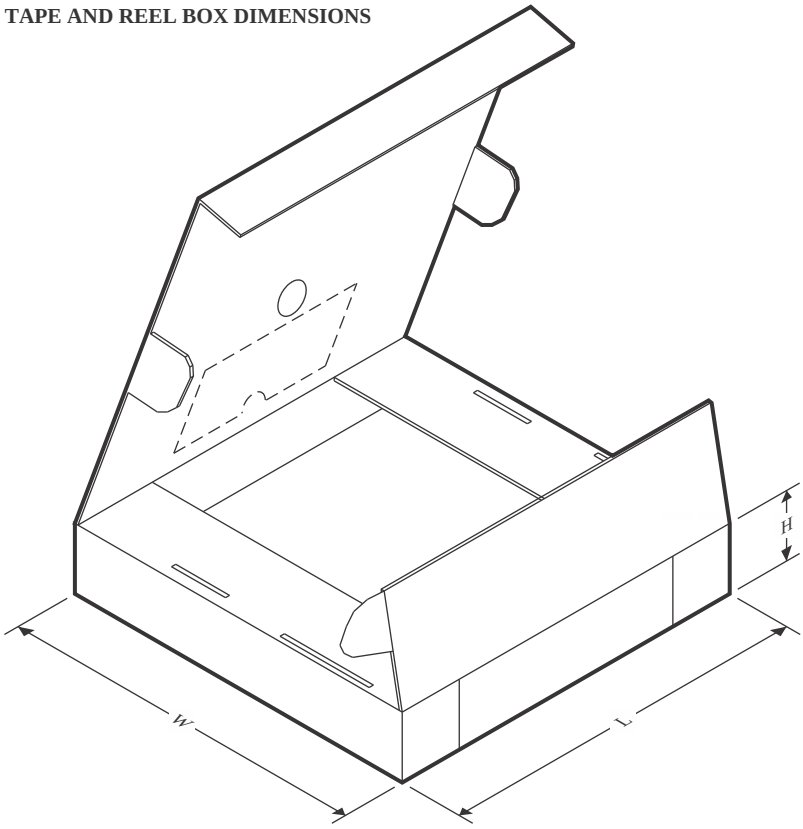
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22907YZTR	DSBGA	YZT	4	3000	178.0	9.2	1.0	1.0	0.73	4.0	8.0	Q1
TPS22907YZTT	DSBGA	YZT	4	250	178.0	9.2	1.0	1.0	0.73	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

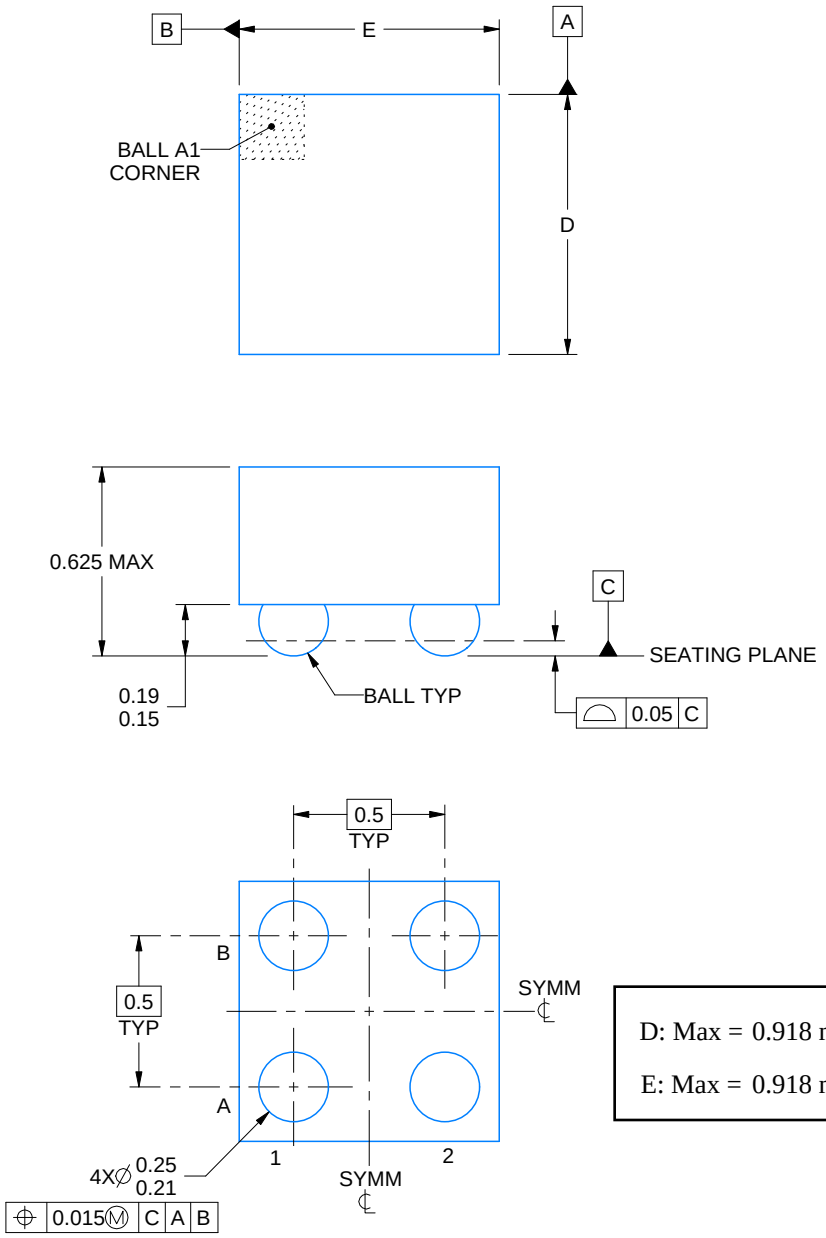
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22907YZTR	DSBGA	YZT	4	3000	220.0	220.0	35.0
TPS22907YZTT	DSBGA	YZT	4	250	220.0	220.0	35.0

PACKAGE OUTLINE

YZT0004

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

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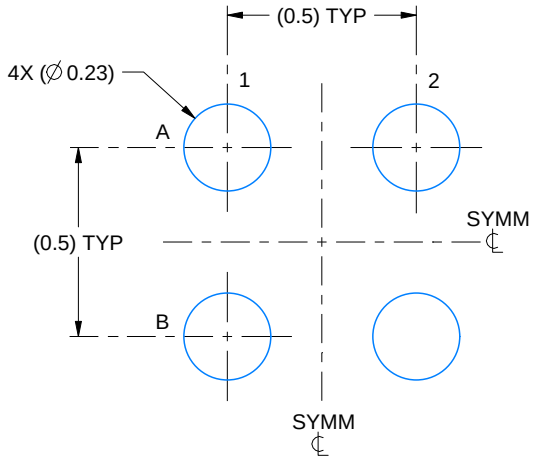
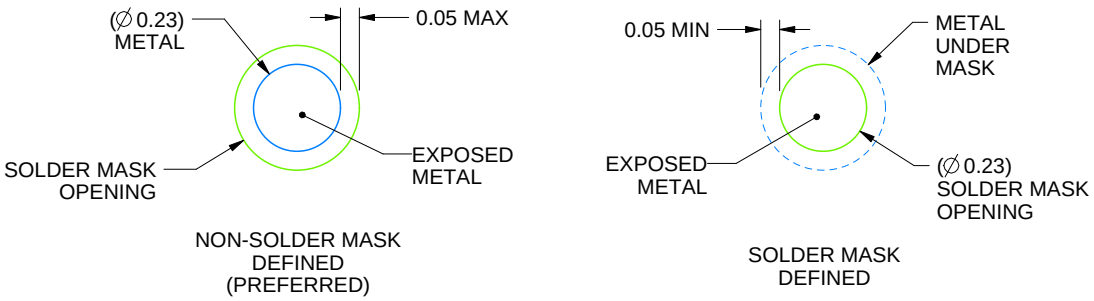
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

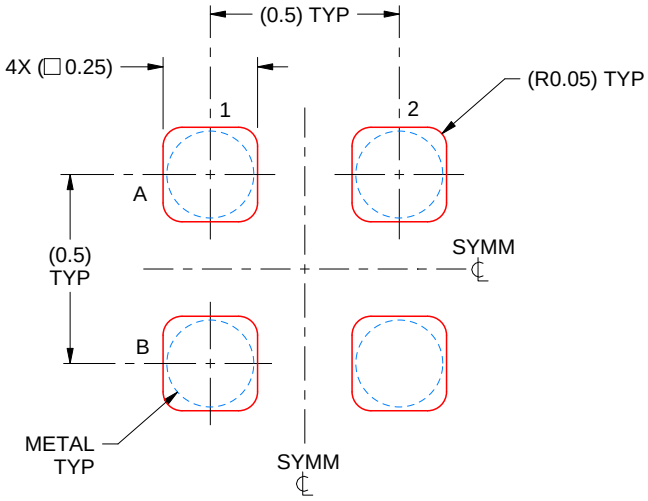
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZT0004

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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