

E4MS025120J2

Automotive Silicon Carbide Power MOSFET



Features

- Industry compatible drive voltage 15 V ...18 V/-4 V ...0 V
- Low $R_{DS(on)}$ at high operating temperatures
- Improved device capacitance ratio (C_{iss}/C_{rss})
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

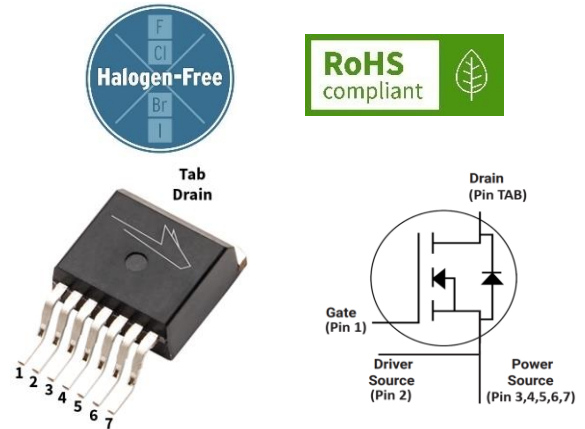
Benefits

- Higher efficiency with lower switching losses and EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system level cooling requirements

Typical Applications

- Onboard charger
- High voltage DC/DC converters
- HVAC compressors
- Battery management systems

Package



Orderable Part Number	Package Type	Marking
E4MS025120J2-TR	TO-263-7 XL	E4MS025120J2

Absolute Maximum Ratings

Stress beyond those listed under absolute maximum ratings may damage the device.

Symbol	Parameter	Min.	Max.	Unit	Conditions	Note
$V_{DS(max)}$	Drain-Source Voltage		1200	V		
$V_{GS(max)}$	Maximum Gate – Source Voltage (Transient)	-10	23			Note 1
I_D	DC Continuous Drain Current		82	A	$V_{GS} = 18\text{ V}, T_c = 25\text{ }^\circ\text{C}, T_J \leq 175\text{ }^\circ\text{C}$	Note 2
			59		$V_{GS} = 18\text{ V}, T_c = 100\text{ }^\circ\text{C}, T_J \leq 175\text{ }^\circ\text{C}$	
I_{DM}	Pulsed Drain Current		274		$V_{GS} = 18\text{ V}, T_c = 25\text{ }^\circ\text{C}, t_{pmax} \text{ limited by } T_{Jmax}$	
P_D	Power Dissipation		330	W	$T_c = 25\text{ }^\circ\text{C}, T_J = 175\text{ }^\circ\text{C}$	Note 3
T_J, T_{stg}	Operating Junction and Storage Temperature	-55	+175	$^\circ\text{C}$		
T_L	Solder Temperature		260		According to JEDEC J-STD-020	

Note (1): Refer to AN PRD-09634

Note (2): Current limit calculated by $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)}(T_{J(max)}, I_{D(max)}))}$

Note (3): $P_D = (T_J - T_c) / R_{th(JC, Max)}$


Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain – Source Breakdown Voltage	1200			V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	3.9	V	$V_{DS} = V_{GS}, I_D = 10.8\text{ mA}$	Fig. 11, Note 1
			2.0		V	$V_{DS} = V_{GS}, I_D = 10.8\text{ mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 18\text{ V}, V_{DS} = 0\text{ V}$	
$V_{GS(op)}$	Recommended Turn on Gate-Source Voltage		15...18		V		Note 4
	Recommended Turn off Gate-Source Voltage		-4...0				
$R_{DS(on)}$	Drain-Source On-State Resistance		25	33	m Ω	$V_{GS} = 18\text{ V}, I_D = 39.2\text{ A}$	Fig. 4, 5, 6
			47			$V_{GS} = 18\text{ V}, I_D = 39.2\text{ A}, T_J = 175^\circ\text{C}$	
			29			$V_{GS} = 15\text{ V}, I_D = 39.2\text{ A}$	
g_{fs}	Transconductance		28		S	$V_{DS} = 20\text{ V}, I_D = 39.2\text{ A}$	Fig. 7
			27			$V_{DS} = 20\text{ V}, I_D = 39.2\text{ A}, T_J = 175^\circ\text{C}$	
$R_{DS(on)Tempco}$	On Resistance Temperature Coefficient		1.88			$V_{GS} = 18\text{ V}, I_D = 39.2\text{ A}$	Note 5
C_{iss}	Input Capacitance		3087		pF	$V_{GS} = 0\text{ V}, V_{DS} = 1000\text{ V}$ $f = 100\text{ kHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
C_{oss}	Output Capacitance		103				
C_{rss}	Reverse Transfer Capacitance		4.9				
C_{iss}/C_{rss}	Capacitance Ratio		630				Note 6
E_{oss}	C_{oss} Stored Energy		63		μJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		145		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V} \dots 800\text{ V}$	Note 7
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		238				
E_{on}	Turn-On Switching Energy (Body Diode FWD) $T_J = 25^\circ\text{C}$ $T_J = 175^\circ\text{C}$		394 470		μJ	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V} / 18\text{ V},$ $I_D = 39.2\text{ A}, R_{G(ext)} = 1\text{ }\Omega, L_o = 25\text{ nH}$	Fig. 25, 27, 29
E_{off}	Turn-Off Switching Energy (Body Diode FWD) $T_J = 25^\circ\text{C}$ $T_J = 175^\circ\text{C}$		57 64				Fig. 25, 28, 29
$t_{d(on)}$	Turn-On Delay Time		12		ns	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V} / 18\text{ V},$ $I_D = 39.2\text{ A}, R_{G(ext)} = 1\text{ }\Omega, L_o = 25\text{ nH}$ Timing relative to I_{DS} Inductive load	Fig. 26, 27, 29
t_r	Rise Time		4				Fig. 26, 28, 29
$t_{d(off)}$	Turn-Off Delay Time		36				
t_f	Fall Time		11				
$R_{G(int)}$	Internal Gate Resistance		2.6		Ω	$f = 1\text{ MHz}$	
Q_{gs}	Gate to Source Charge		35		nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V} / 18\text{ V}$ $I_D = 39.2\text{ A}$	Fig. 12
Q_{gd}	Gate to Drain Charge		30				
Q_g	Total Gate Charge		125				

Note (4): Refer to AN PRD-08999.

Note (5): $R_{DS(on)Tempco}$ refers to $R_{DS(on)}$ at 175°C / $R_{DS(on)}$ at 25°C . This is a E4MS 1200V product family value.

Note (6): Capacitance ratio is a FOM for partial turn-on immunity AN PRD-06933. This is a E4MS 1200V product family value.

Note (7): $C_{o(er)}$, a lumped capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0V to 800V.

$C_{o(tr)}$, a lumped capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0V to 800V.



Reverse Diode Characteristics ($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	$V_{GS} = -4\text{ V}, I_{SD} = 19.6\text{ A}, T_J = 25\text{ }^\circ\text{C}$	Fig. 8, 9, 10
		4.6			$V_{GS} = -4\text{ V}, I_{SD} = 19.6\text{ A}, T_J = 175\text{ }^\circ\text{C}$	
I_S	Continuous Diode Forward Current		54	A	$V_{GS} = -4\text{ V}, T_C = 25\text{ }^\circ\text{C}$	
I_{SM}	Diode Pulse Current		274		$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{Jmax}	
t_{rr}	Reverse Recovery Time	14		ns	$V_{GS} = -4\text{ V}, I_{SD} = 39.2\text{ A}, V_R = 800\text{ V}, T_J = 175\text{ }^\circ\text{C}, di/dt = 15.8\text{ A/ns}$	Fig. 30
Q_{rr}	Reverse Recovery Charge	742		nC		
I_{RRM}	Peak Reverse Recovery Current	94		A		
E_{RR}	Reverse Recovery Energy $T_J = 25\text{ }^\circ\text{C}$ $T_J = 175\text{ }^\circ\text{C}$	102 256		μJ	$V_{DS} = 800\text{ V}, I_{DS} = 39.2\text{ A},$ $V_{GS} = -4\text{ V} / 18\text{ V}, R_{G(ext)} = 1\text{ }\Omega, L_G = 25\text{ nH}$	

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.35	0.46	$^\circ\text{C/W}$		

Typical Performance

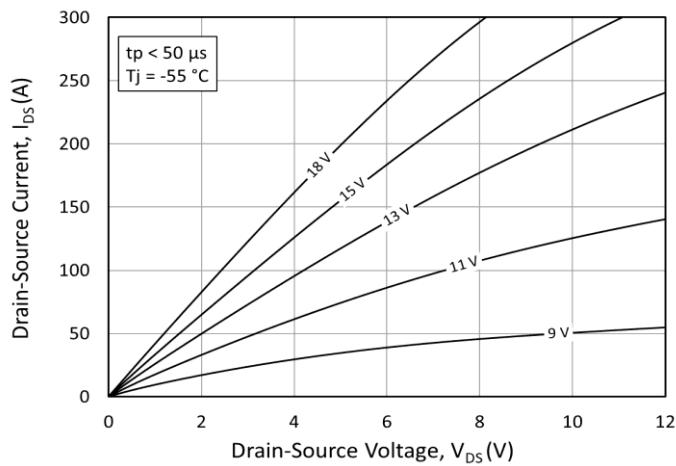


Figure 1. Output Characteristics $T_{vj} = -55\text{ }^{\circ}\text{C}$

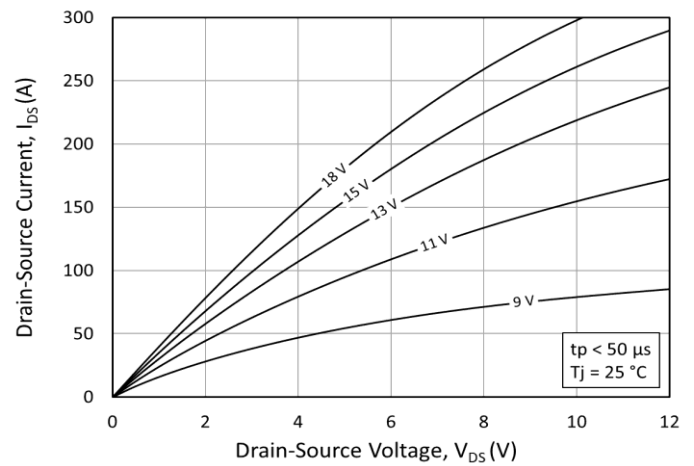


Figure 2. Output Characteristics $T_{vj} = 25\text{ }^{\circ}\text{C}$

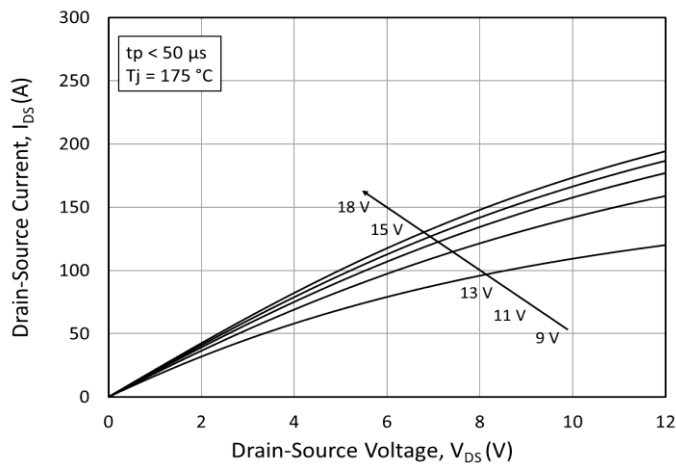


Figure 3. Output Characteristics $T_{vj} = 175\text{ }^{\circ}\text{C}$

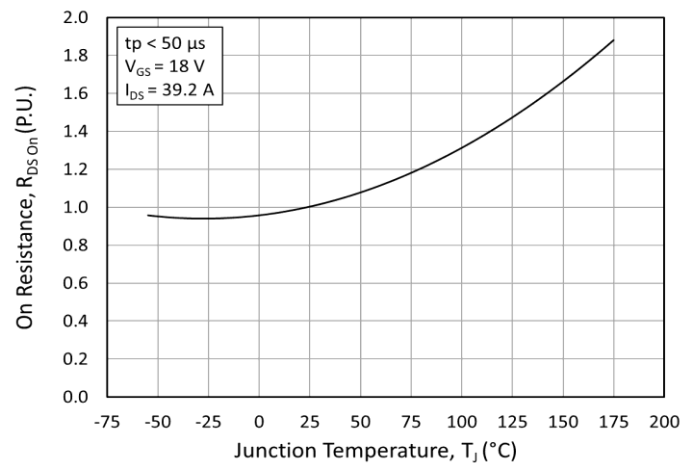


Figure 4. Normalized On-Resistance vs. Temperature

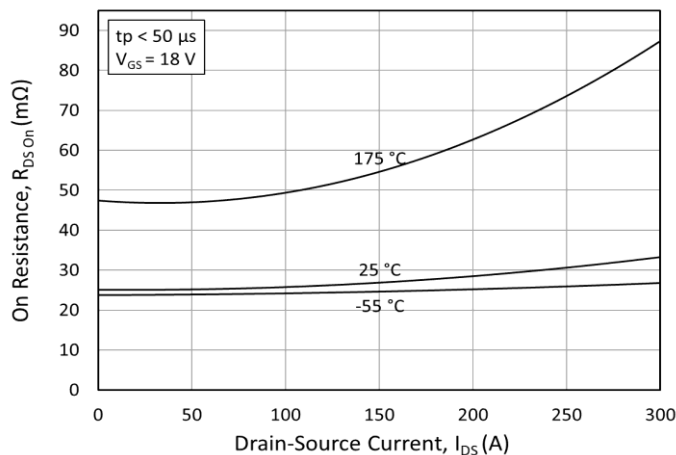


Figure 5. On-Resistance vs. Drain Current for Various Temperatures

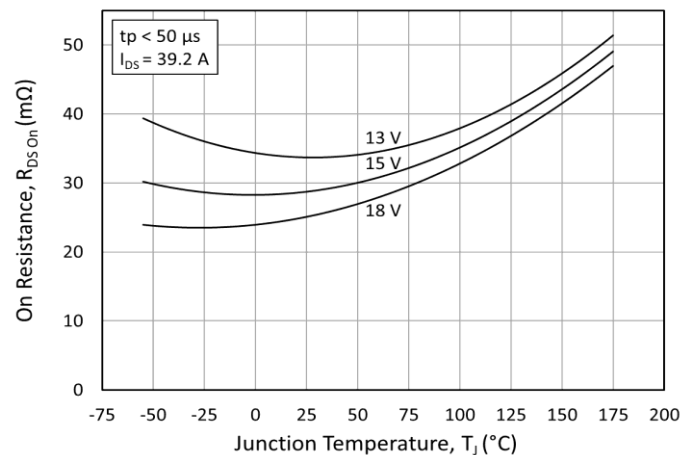


Figure 6. On-Resistance vs. Temperature for Various Gate Voltages

Typical Performance

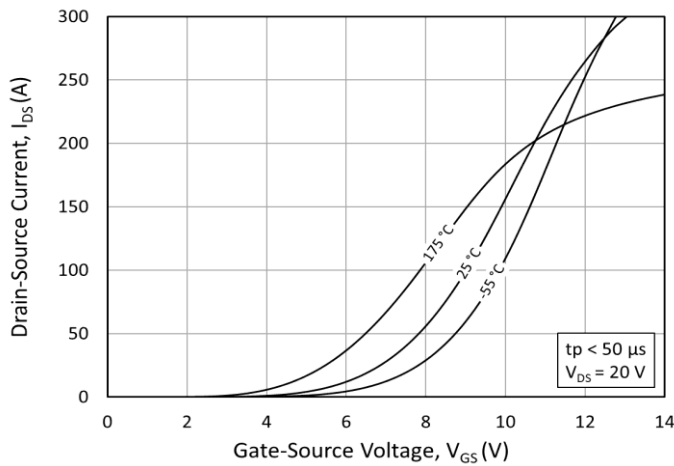


Figure 7. Transfer Characteristic for Various Junction Temperatures

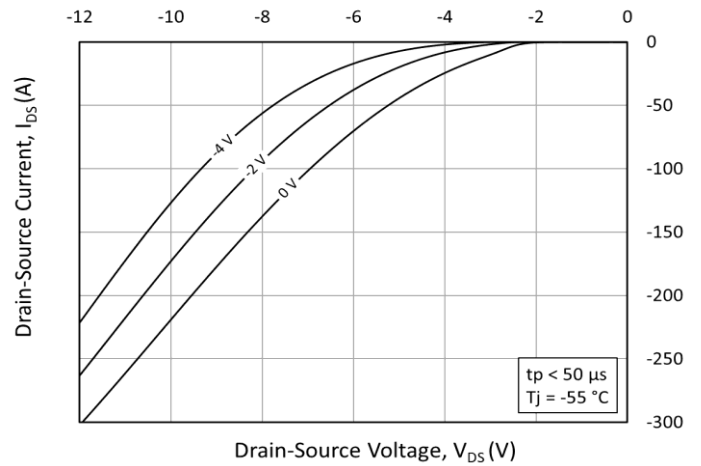


Figure 8. Body Diode Characteristic at $T_{J} = -55\text{ }^{\circ}\text{C}$

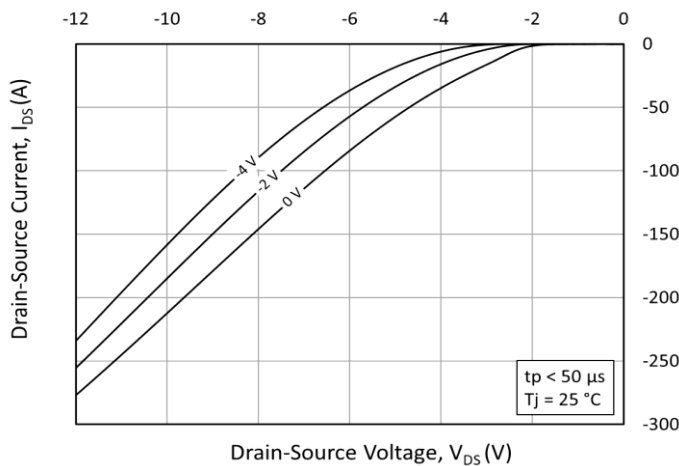


Figure 9. Body Diode Characteristic at $T_{J} = 25\text{ }^{\circ}\text{C}$

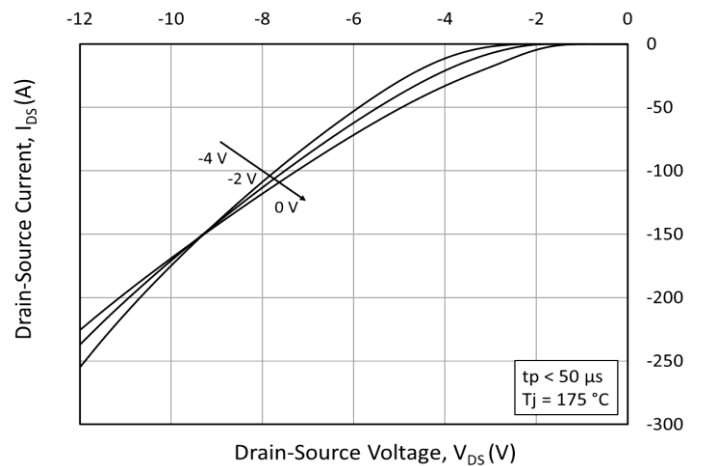


Figure 10. Body Diode Characteristic at $T_{J} = 175\text{ }^{\circ}\text{C}$

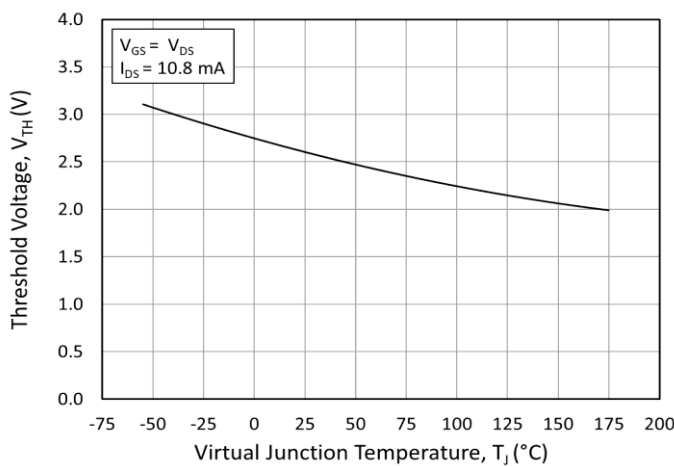


Figure 11. Threshold Voltage vs. Temperature

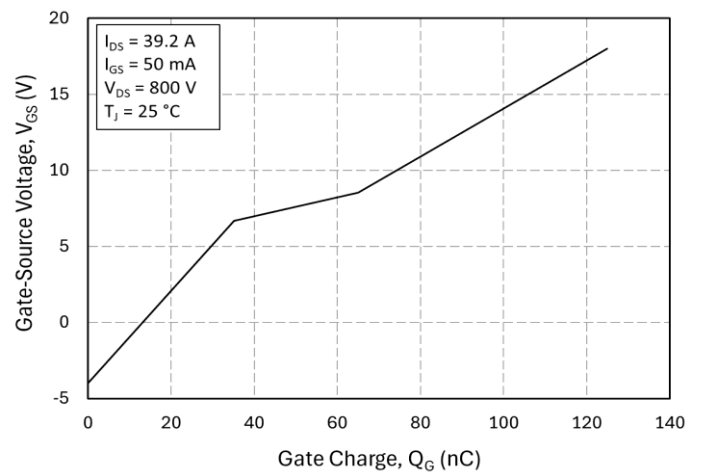


Figure 12. Gate Charge Characteristics

Typical Performance

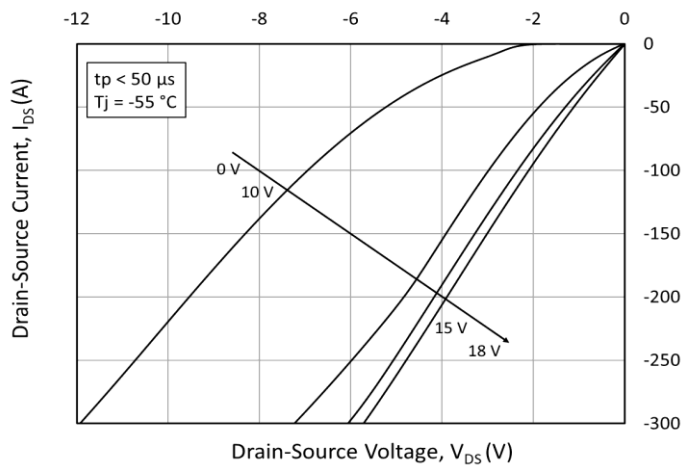


Figure 13. 3rd Quadrant Characteristic at $T_{VJ} = -55\text{ }^{\circ}\text{C}$

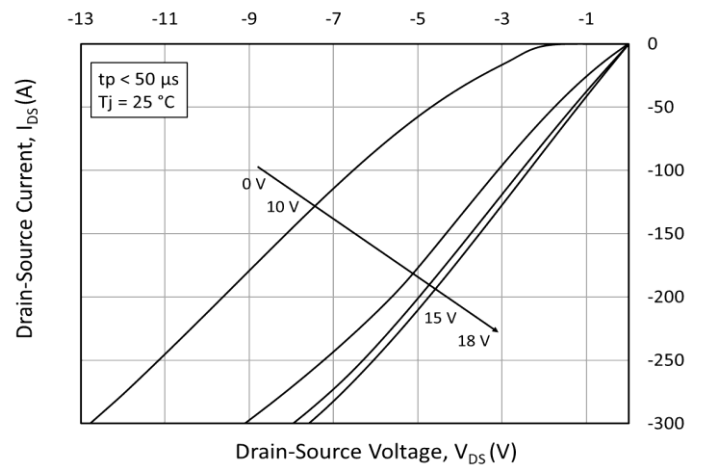


Figure 14. 3rd Quadrant Characteristic at $T_{VJ} = 25\text{ }^{\circ}\text{C}$

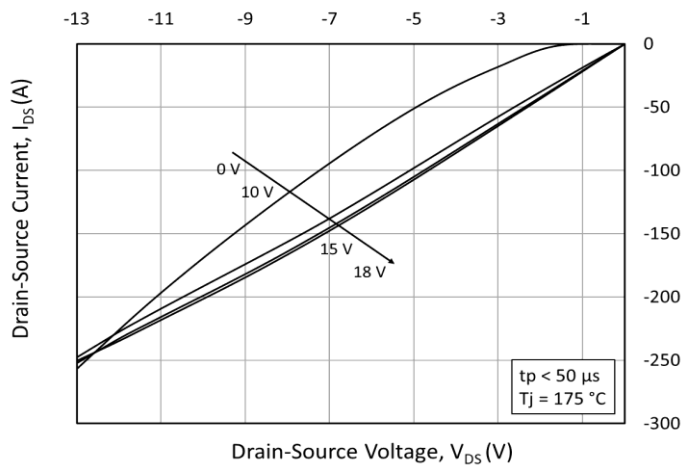


Figure 15. 3rd Quadrant Characteristic at $T_{VJ} = 175\text{ }^{\circ}\text{C}$

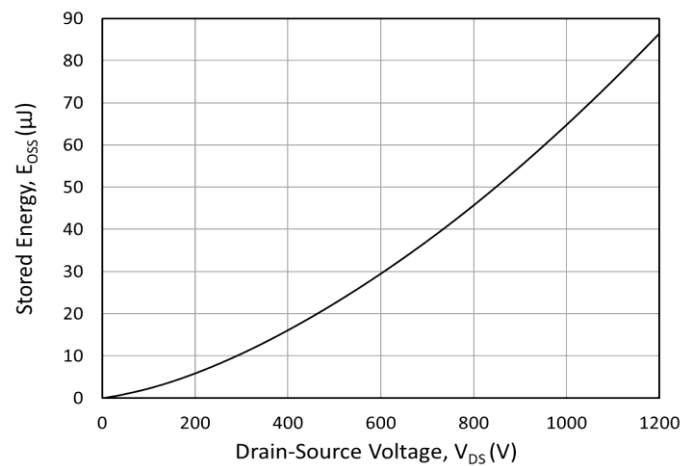


Figure 16. Output Capacitor Stored Energy

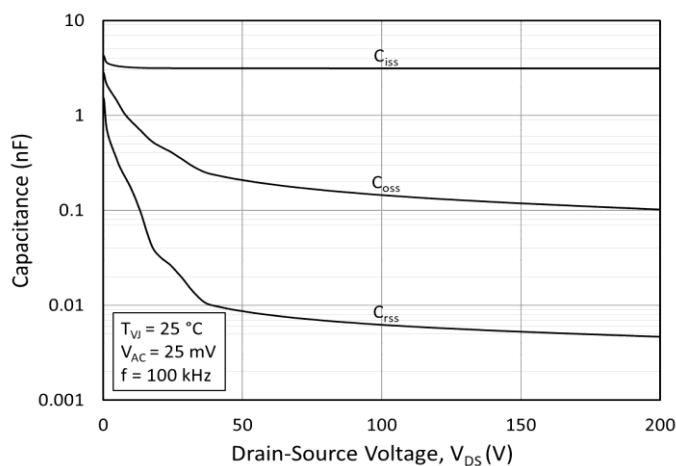


Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

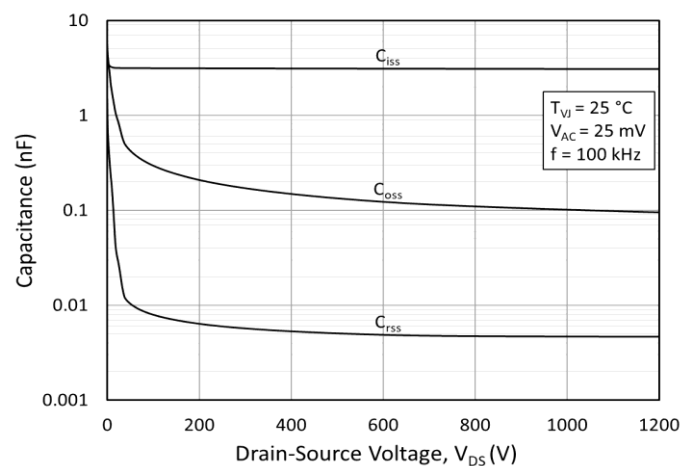


Figure 18. Capacitances vs. Drain-Source Voltage (0-1200 V)

Typical Performance

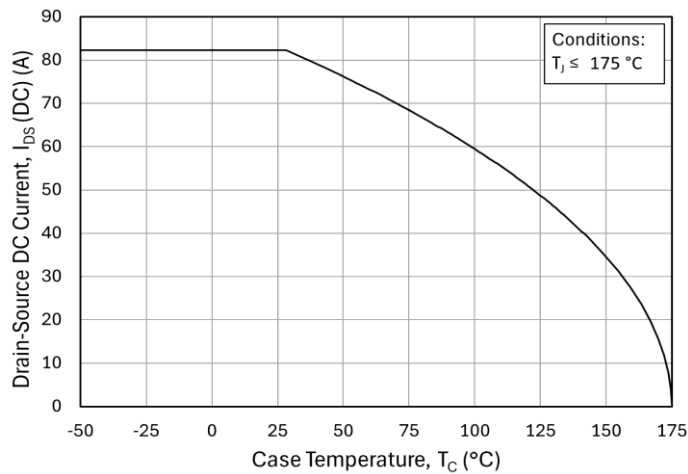


Figure 19. Continuous Drain Current Derating vs. Case Temperature

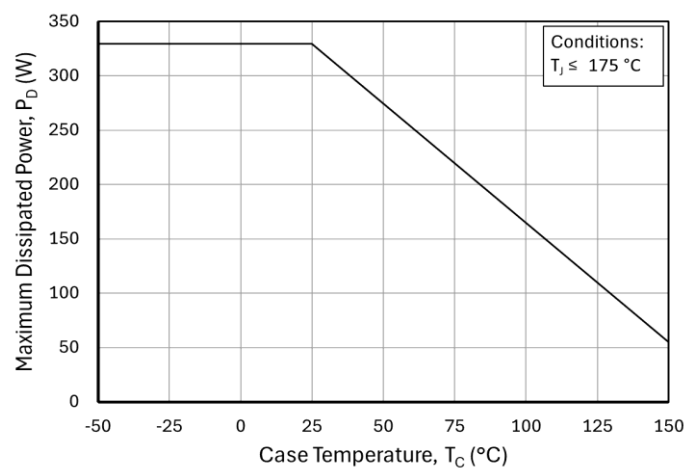


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

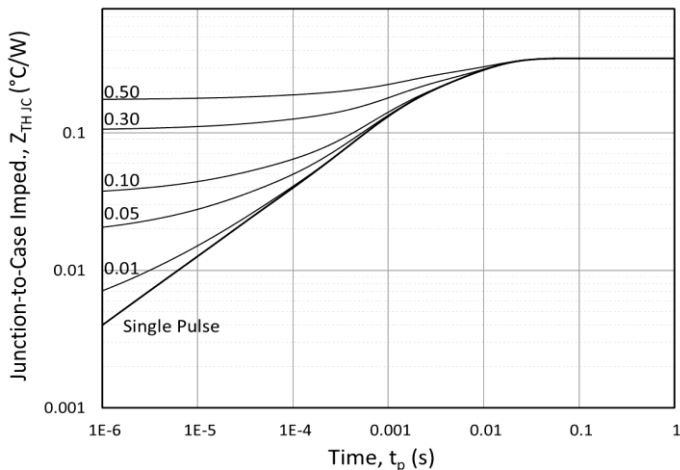


Figure 21. Transient Thermal Impedance (Junction - Case) °C

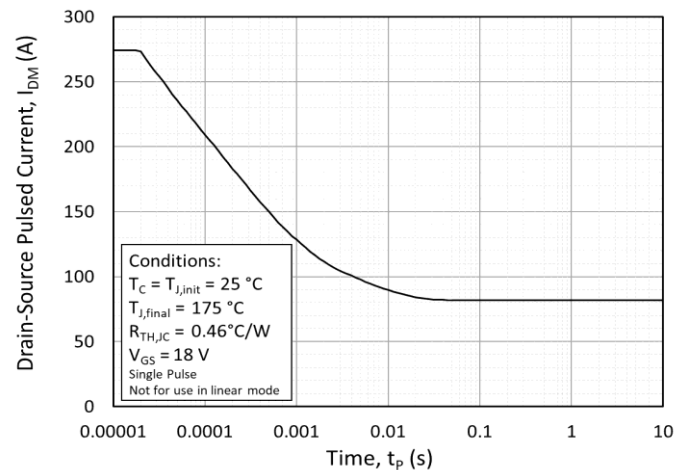


Figure 22. Safe Operating Area

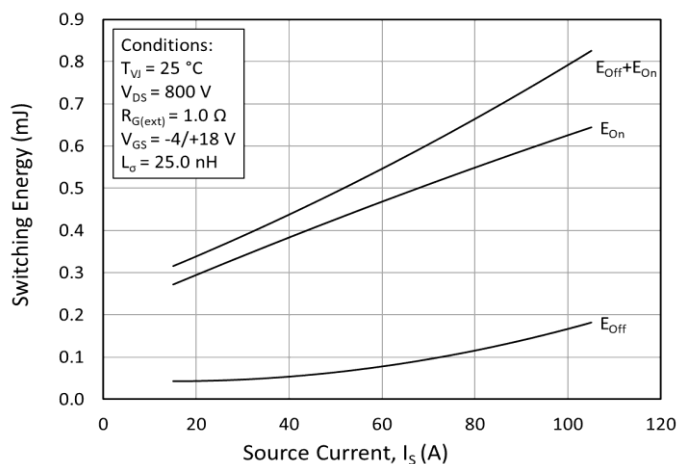


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 800$ V)

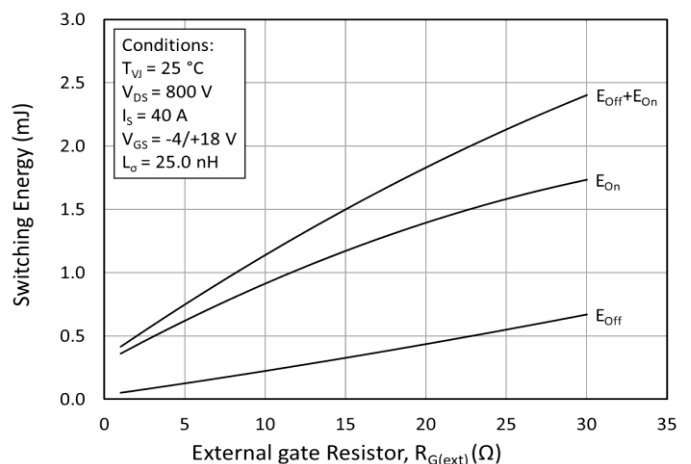


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

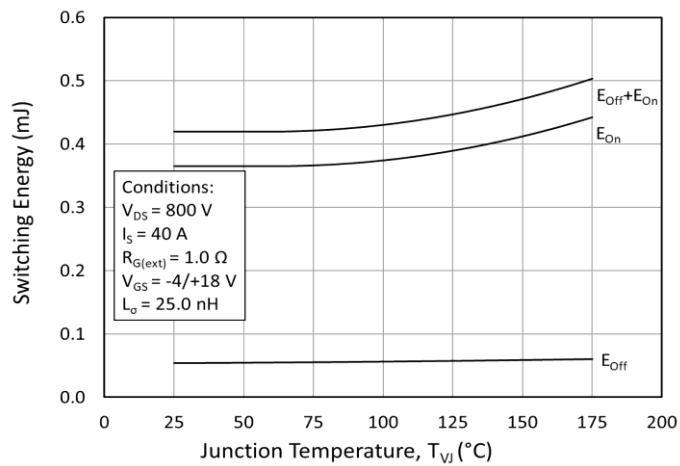


Figure 25. Clamped Inductive Switching Energy vs. Temperature

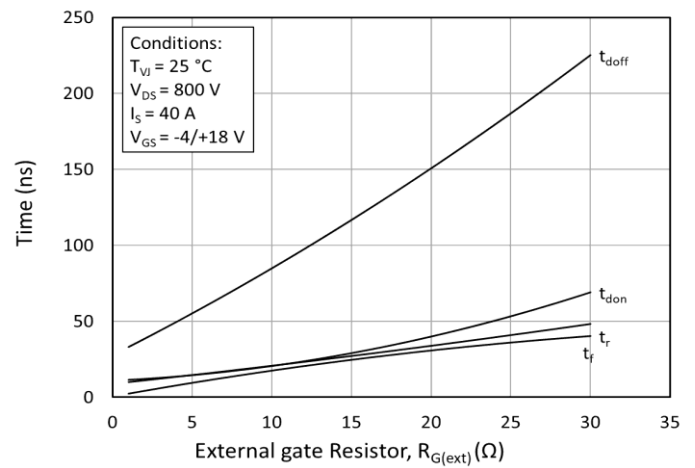


Figure 26. Switching Times vs. $R_{G(ext)}$

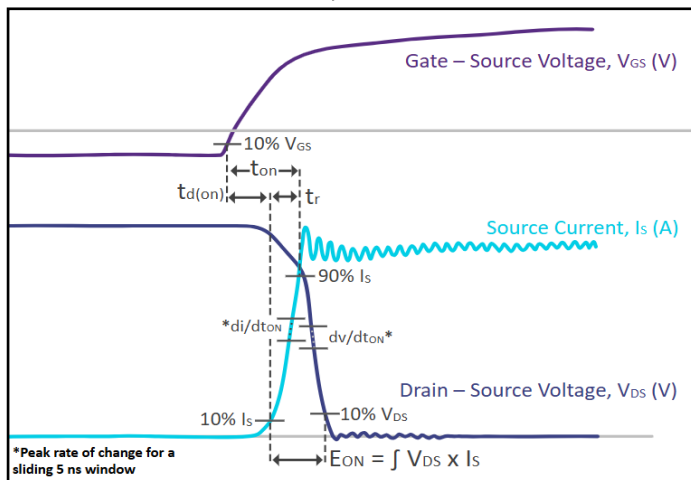


Figure 27. Turn On Switching Time Definition

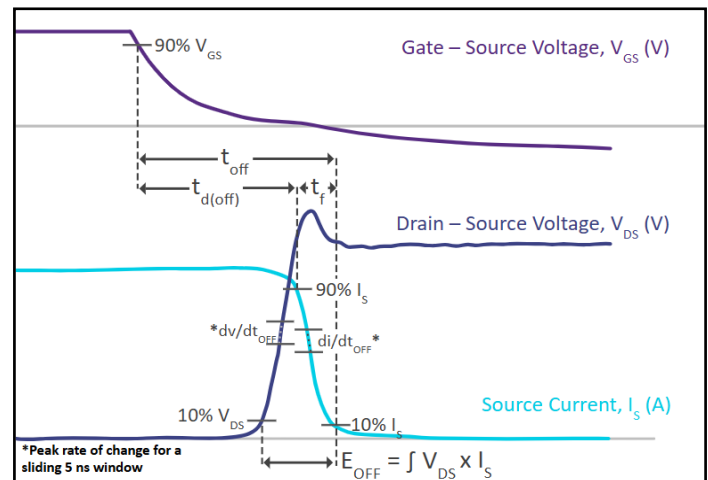


Figure 28. Turn Off Switching Time Definition

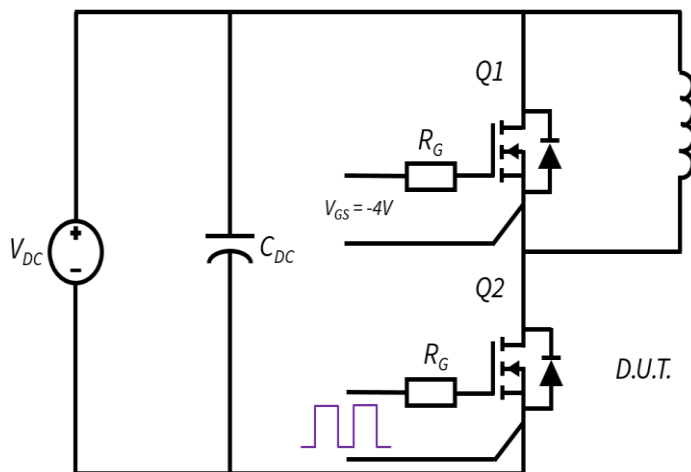


Figure 29. Clamped Inductive MOSFET Switching Waveform Test Circuit

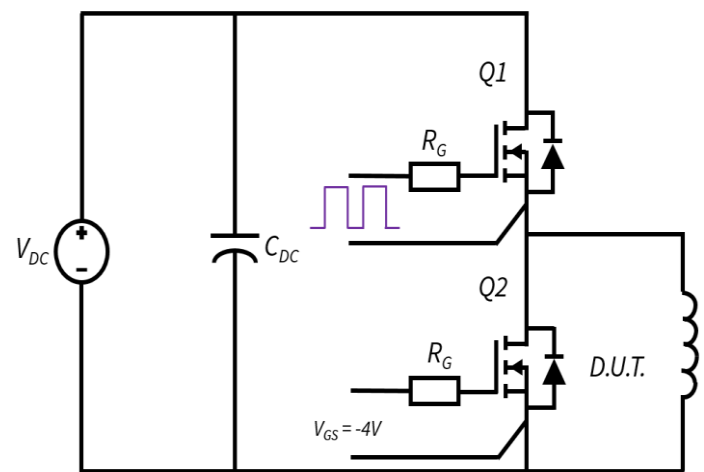
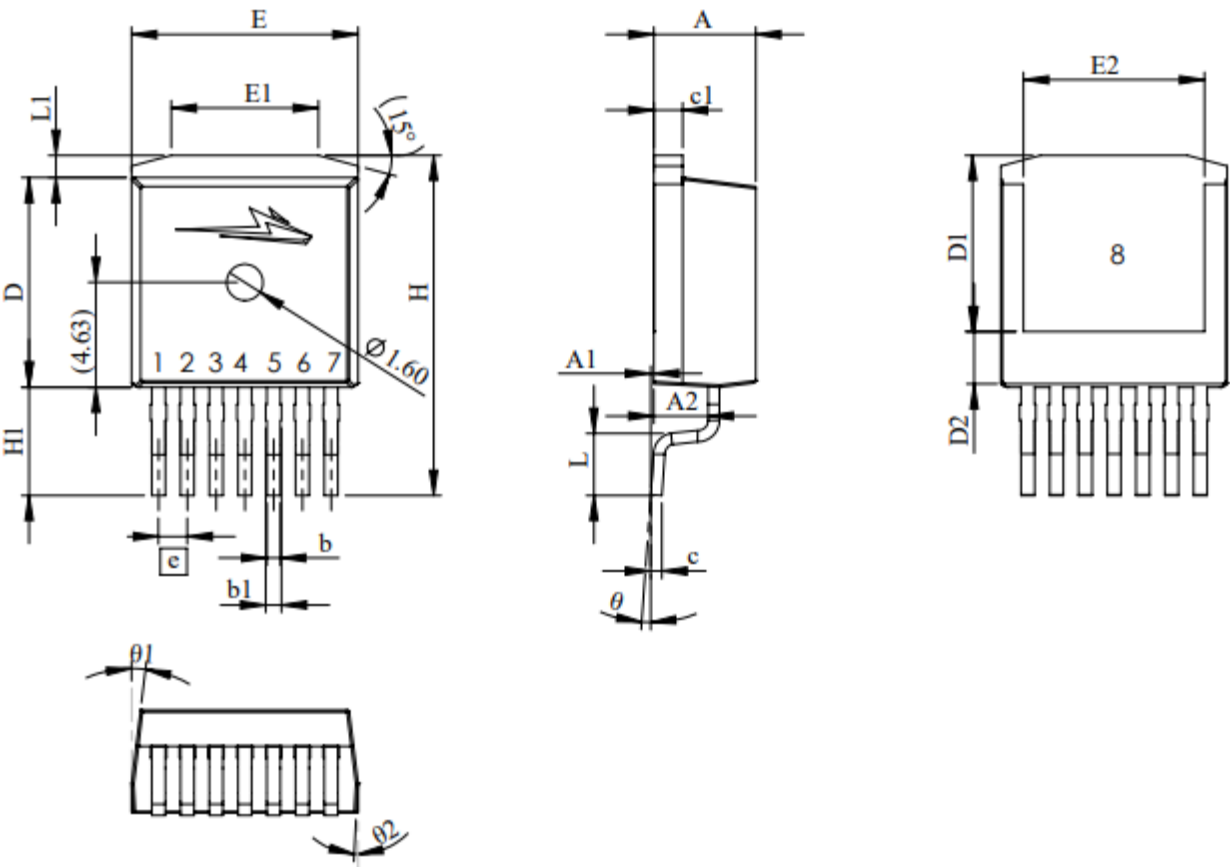


Figure 30. Clamped Inductive Body Diode Switching Waveform Test Circuit

Package Dimensions



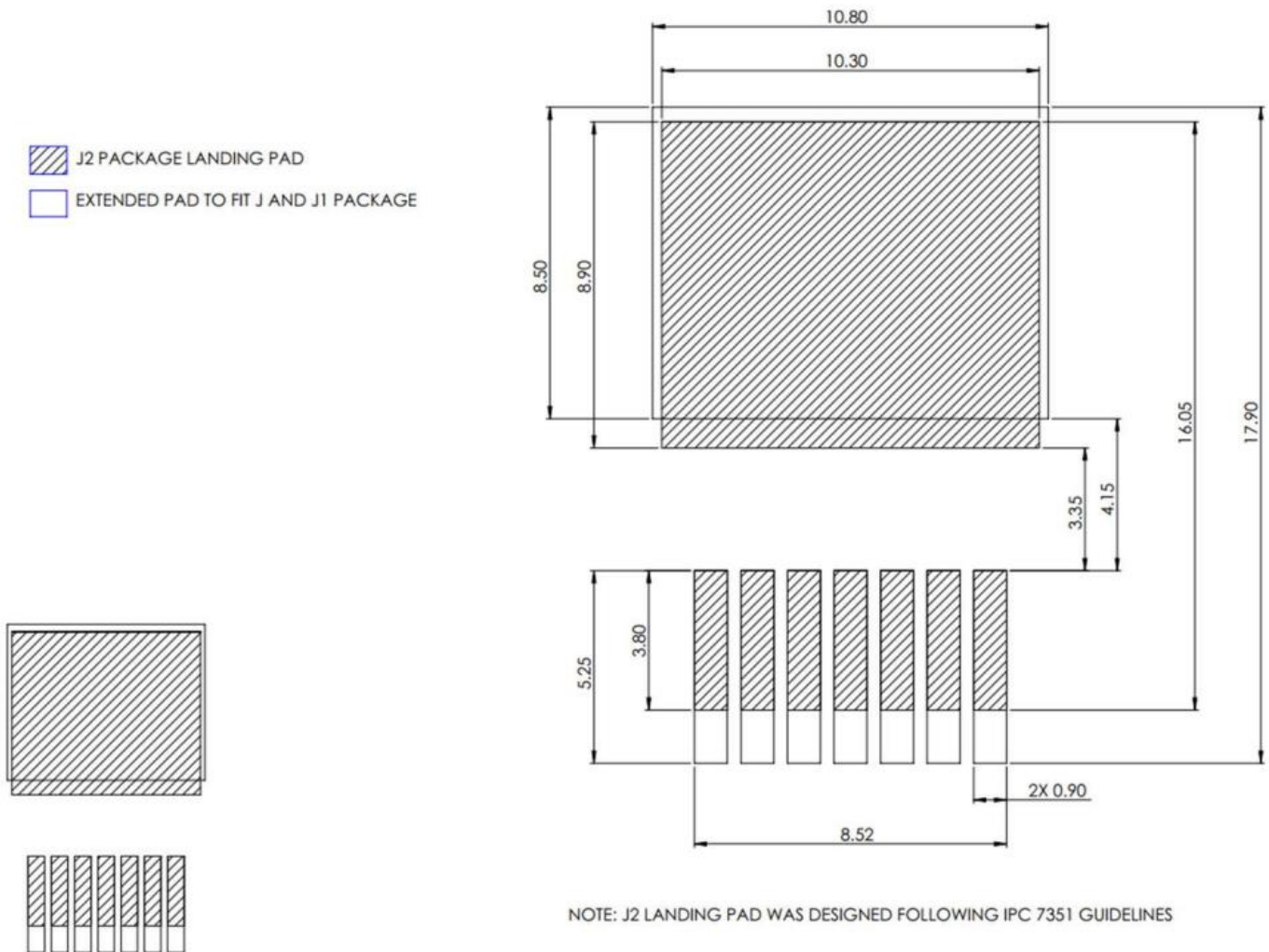
SYMBOL	MIN (mm)	MAX (mm)
A	4.30	4.70
A1	0.00	0.25
A2	2.20	2.60
b	0.52	0.72
b1	0.60	0.80
c	0.42	0.62
c1	1.07	1.47
D	9.05	9.45
D1	7.58	7.98
D2	2.05	2.45
E	9.80	10.20
E1	6.30	6.97
E2	7.80	8.20
c	1.27 BSC	
H	14.87	15.27
H1	4.55	4.95
L	2.48	2.88
L1	0.87	1.27
θ	0°	8°
θ1	4°	10°
θ2	0°	6°

1	GATE
2	KELVIN
3	SOURCE
4	
5	
6	
7	
8	DRAIN

- NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
 2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
 3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
 4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Recommended Solder Pad Layout

All dimensions in mm



Revision History

Documents Version	Date of Change	Description of Changes
1	November 2025	Initial Release
2	January 2026	Addition of Note (1)
3	March 2026	Corrected the labels on Figures 8 and 9
4	7/17/2026	- Updated the datasheet template and reformatted figures - Corrected the typical values of the following parameters: - Recommended Turn off Gate-Source Voltage $R_{DS(on)}$ at $V_{GS} = 15\text{ V}$ C_{rss} V_{SD} at $T_J = 175\text{ }^{\circ}\text{C}$

Appendix

Appendix Number	Description
A1	The following are recommendations for turning off the MOSFET with 0 V: - Measure the V_{GS} spike accurately using high-CMRR probes and low common mode noise measurements. - For the safe operation of the device, the voltage spike shall remain $< 5\text{ V}$ for a time duration of $< 40\text{ ns}$.



Notes & Disclaimers

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