LM431 Adjustable Precision Zener Shunt Regulator

1 Features

- Average Temperature Coefficient 50 ppm/°C
- Temperature Compensated for Operation Over the Full Temperature Range
- Programmable Output Voltage
- Fast Turnon Response
- Low-Output Noise
- Low-Dynamic Output Impedance
- Available in Space-Saving SOIC-8, SOT-23, and TO-92 Packages

2 Applications

- Adjustable Voltage or Current Linear and Switching Power Supplies
- Voltage Monitoring
- Current Source and Sink Circuits
- Circuits Requiring Precision References
- Zener Diode Replacements

3 Description

The LM431 is a 3-terminal adjustable shunt regulator with ensured temperature stability over the entire temperature range of operation. The output voltage may be set at any level greater than 2.5 V (V_{REF}) up to 36 V merely by selecting two external resistors that act as a voltage divided network. Due to the sharp turnon characteristics this device is an excellent replacement for many Zener diode applications.

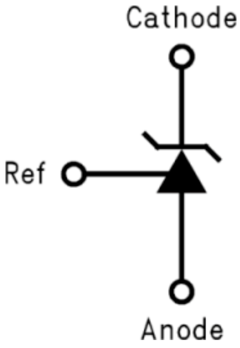
The LM431 is available in space-saving SOIC-8, SOT-23, and TO-92 packages.

Device Information(1)

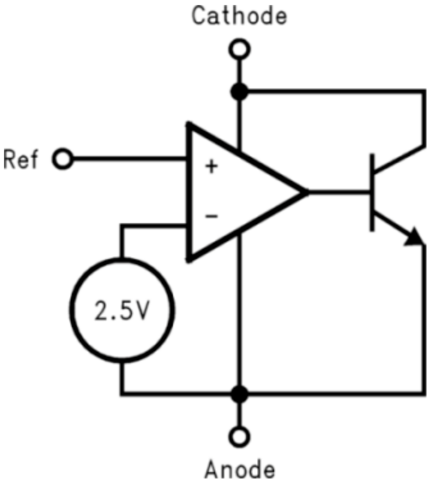
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM431	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (3)	2.92 mm × 1.30 mm
	TO-92 (3)	4.30 mm × 4.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

LM431 Symbol



Functional Block Diagram



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4 Revision History

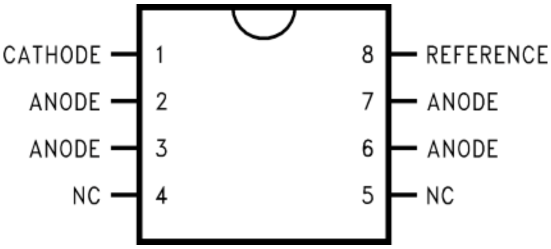
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March 2013) to Revision H	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	18

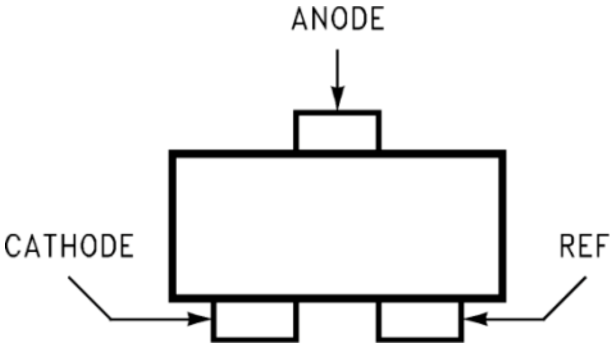
5 Pin Configuration and Functions

**D Package
8-Pin SOIC
Top View**

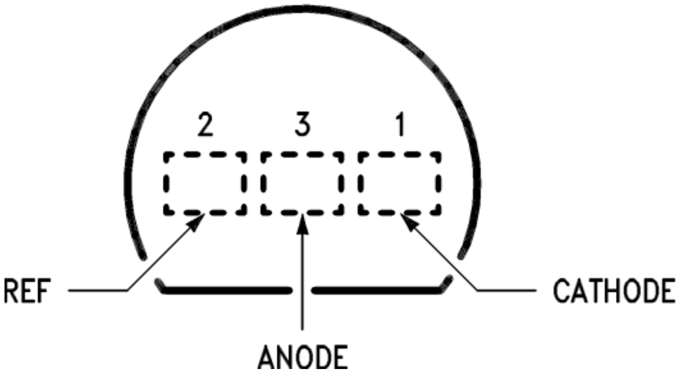


Note: NC = Not internally connected.

**DBZ Package
3-Pin SOT-23
Top View**



**LP Package
3-Pin TO-92
Top View**



Pin Functions

PIN				I/O	DESCRIPTION
NAME	SOIC	SOT-23	TO-92		
Anode	2, 3, 6, 7	3	3	O	Anode pin, normally grounded
Cathode	1	1	1	I/O	Shunt current/output voltage
NC	4, 5	—	—	—	No connect
Reference	8	2	2	I	Reference pin for adjustable output voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Cathode voltage		37		V
Reference voltage		–0.5		V
Continuous cathode current		–10	150	mA
Reference input current		10		mA
Internal power dissipation(3)(4)	TO-92 package	0.78		W
	SOIC package	0.81		W
	SOT-23 package	0.28		W
Operating temperature	Industrial (LM431xI)	–40	85	°C
	Commercial (LM431xC)	0	70	°C
Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) $T_{J\ Max}$ = 150°C.
(4) Ratings apply to ambient temperature at 25°C. Above this temperature, derate the TO-92 at 6.2 mW/°C, the SOIC at 6.5 mW/°C, the SOT-23 at 2.2 mW/°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Cathode voltage	V_{REF}	37	V
Cathode current	1	100	mA

6.4 Thermal Information

THERMAL METRIC(1)		LM431			UNIT
		D (SOIC)	DBZ (SOT-23)	LP (TO-92)	
		8 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.9	267.7	162.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.2	138.3	85.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.5	61	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.1	21.5	29.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67	60.1	141.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

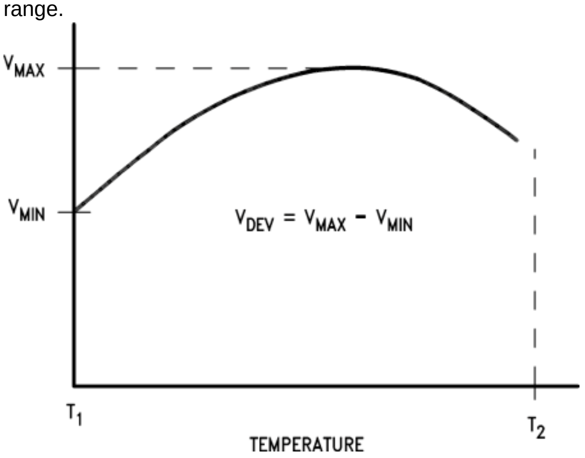
(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C unless otherwise specified

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	$V_Z = V_{REF}$, I_I = 10 mA LM431A (Figure 6)		2.44	2.495	2.55	V
		$V_Z = V_{REF}$, I_I = 10 mA LM431B (Figure 6)		2.47	2.495	2.52	
		$V_Z = V_{REF}$, I_I = 10 mA LM431C (Figure 6)		2.485	2.5	2.51	
V_{DEV}	Deviation of reference input voltage overtemperature (1)	$V_Z = V_{REF}$, I_I = 10 mA, T_A = full range (Figure 6)			8	17	mV
ΔV_{REF}/ ΔV_Z	Ratio of the change in reference voltage to the change in cathode voltage	I_Z = 10 mA (Figure 7)	V_Z from V_{REF} to 10 V		−1.4	−2.7	mV/V
			V_Z from 10 V to 36 V		−1	−2	
I_{REF}	Reference input current	R_1 = 10 kΩ, R_2 = ∞, I_I = 10 mA (Figure 7)			2	4	μA
$\propto I_{REF}$	Deviation of reference input current overtemperature	R_1 = 10 kΩ, R_2 = ∞, I_I = 10 mA, T_A = full range (Figure 7)			0.4	1.2	μA
$I_{Z(MIN)}$	Minimum cathode current for regulation	$V_Z = V_{REF}$(Figure 6)			0.4	1	mA
$I_{Z(OFF)}$	OFF-state current	V_Z = 36 V, V_{REF} = 0 V (Figure 8)			0.3	1	μA

(1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range.



The average temperature coefficient of the reference input voltage, $\propto V_{REF}$, is defined as:

$$\propto V_{REF}\,\frac{ppm}{°C} = \frac{\pm\left[\frac{V_{Max} - V_{Min}}{V_{REF}\,(at\ 25°C)}\right]10^6}{T_2 - T_1} = \frac{\pm\left[\frac{V_{DEV}}{V_{REF}\,(at\ 25°C)}\right]10^6}{T_2 - T_1}$$

Where:
$T_2 - T_1$ = full temperature change (0–70°C).
V_{REF} can be positive or negative depending on whether the slope is positive or negative.
Example: V_{DEV} = 8 mV, V_{REF} = 2495 mV, $T_2 - T_1$ = 70°C, slope is positive.

$$\propto V_{REF} = \frac{\left[\frac{8.0\ mV}{2495\ mV}\right]10^6}{70°C} = +46\ ppm/°C$$

Electrical Characteristics (continued)

T_A = 25°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
r_Z	Dynamic output impedance(2)	$V_Z = V_{REF}$, LM431A, Frequency = 0 Hz (Figure 6)			0.75	Ω
		$V_Z = V_{REF}$, LM431B, LM431C Frequency = 0 Hz (Figure 6)			0.5	

(2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R1 and R2, (see Figure 7), the dynamic output impedance of the overall circuit, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z \left(1 + \frac{R1}{R2} \right) \right]$$

6.6 Typical Characteristics

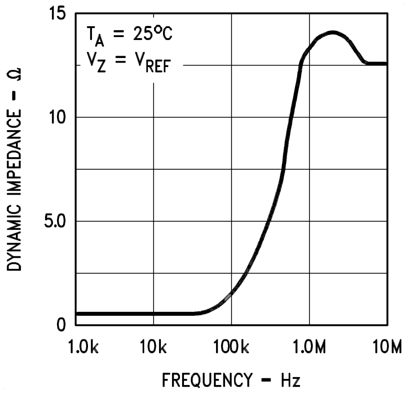
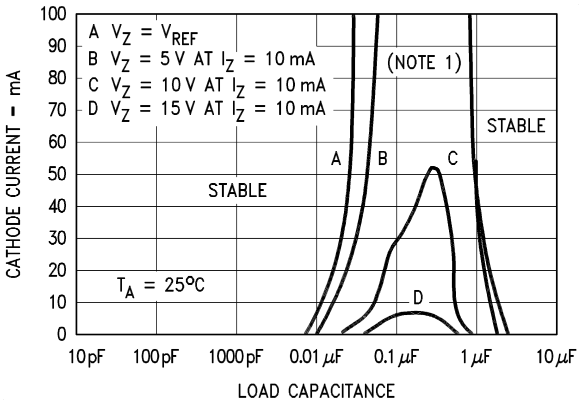


Figure 1. Dynamic Impedance vs Frequency



Note: The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V^+ were adjusted to establish the initial V_Z and I_Z conditions with C_L = 0. V^+ and C_L were then adjusted to determine the ranges of stability.

Figure 2. Stability Boundary Conditions

7 Parameter Measurement Information

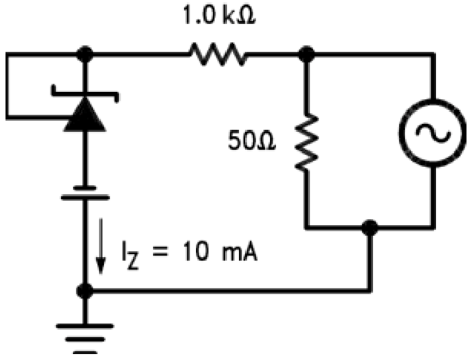


Figure 3. Test Circuit for Dynamic Impedance vs Frequency Curve

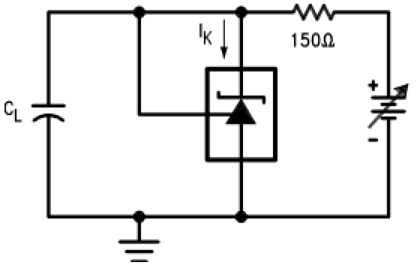


Figure 4. Test Circuit for Curve A Above

Parameter Measurement Information (continued)

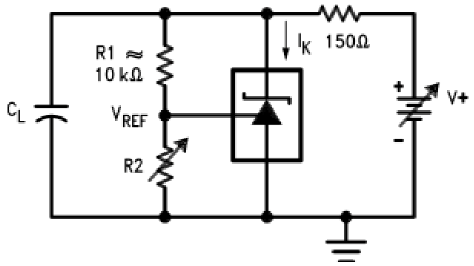


Figure 5. Test Circuit for Curves B, C and D Above

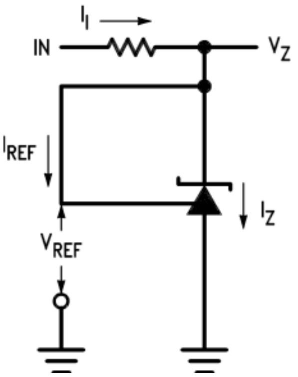
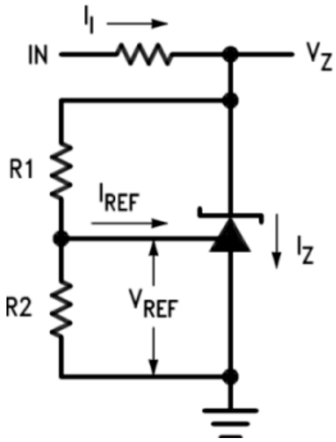


Figure 6. Test Circuit for $V_Z = V_{REF}$



Note: $V_Z = V_{REF} (1 + R1/R2) + I_{REF} \times R1$

Figure 7. Test Circuit for $V_Z > V_{REF}$

Parameter Measurement Information (continued)

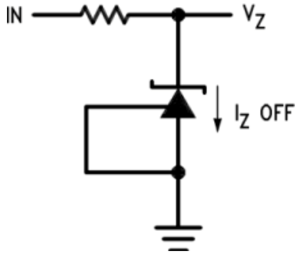


Figure 8. Test Circuit for OFF-State Current

8 Detailed Description

8.1 Overview

The LM431 is an adjustable precision shunt voltage regulator with ensured temperature stability over the entire temperature range. The part has three different packages available to meet small footprint requirements, and is available in three different tolerance grades.

8.2 Functional Block Diagram

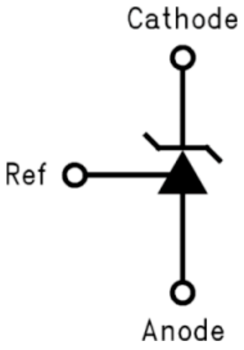


Figure 9. LM431 Symbol

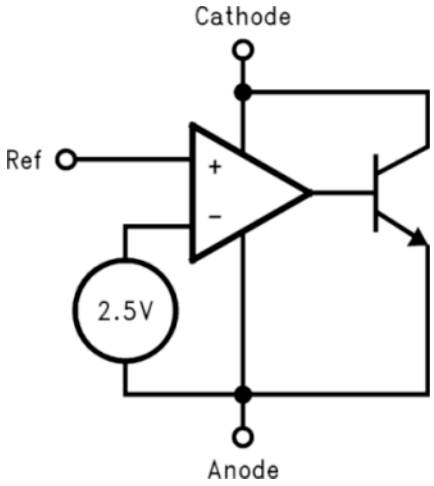


Figure 10. LM431 Block Diagram

8.3 Feature Description

The LM431 is a precision Zener diode. The part requires a small quiescent current for regulation, and regulates the output voltage by shunting more or less current to ground, depending on input voltage and load. The only external component requirement is a resistor between the cathode and the input voltage to set the input current. An external capacitor can be used on the input or output, but is not required.

Feature Description (continued)

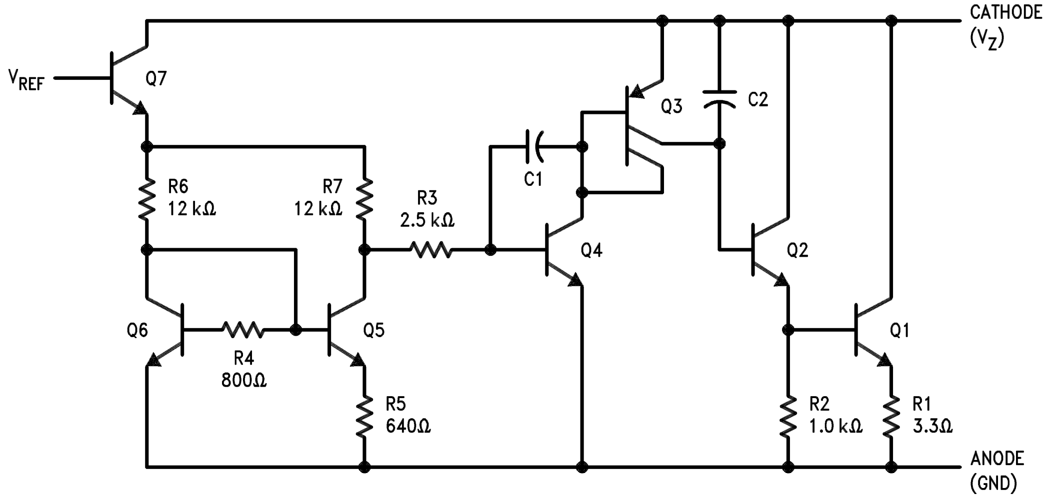


Figure 11. Equivalent Circuit

8.4 Device Functional Modes

The LM431 is most commonly operated in closed-loop mode, where the reference node is tied to the output voltage via a resistor divider. The output voltage remains in regulation as long as I_z is between 1 mA and 100 mA. The part can also be used in open-loop mode to act as a comparator, driving the feedback node from another voltage source.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM431 is an adjustable precision shunt voltage regulator with ensured temperature stability over the entire temperature range. For space critical applications, the LM431 is available in space saving SOIC-8, SOT-23 and TO-92 packages. The minimum operating current is 1 mA while the maximum operating current is 100 mA.

The typical thermal hysteresis specification is defined as the change in 25°C voltage measured after thermal cycling. The device is thermal cycled to temperature 0°C and then measured at 25°C. Next the device is thermal cycled to temperature 70°C and again measured at 25°C. The resulting VOUT delta shift between the 25°C measurements is thermal hysteresis. Thermal hysteresis is common in precision references and is induced by thermal-mechanical package stress. Changes in environmental storage temperature, operating temperature and board mounting temperature are all factors that can contribute to thermal hysteresis.

In a conventional shunt regulator application (Figure 12), an external series resistor (R_S) is connected between the supply voltage and the LM431 cathode pin. R_S determines the current that flows through the load (I_{LOAD}) and the LM431 (I_Z). Since load current and supply voltage may vary, R_S must be small enough to supply at least the minimum acceptable I_Z to the LM431 even when the supply voltage is at its minimum and the load current is at its maximum value. When the supply voltage is at its maximum and I_{LOAD} is at its minimum, R_S must be large enough so that the current flowing through the LM431 is less than 100 mA.

R_S must be selected based on the supply voltage, (V+), the desired load and operating current, (I_{LOAD} and I_Z), and the output voltage, see Equation 1.

$$R_S = \frac{V_+ - V_O}{I_{LOAD} + I_Z} \quad (1)$$

The LM431 output voltage can be adjusted to any value in the range of 2.5 V through 37 V. It is a function of the internal reference voltage (VREF) and the ratio of the external feedback resistors as shown in Figure 12. The output voltage is found using Equation 2.

$$V_O = V_{REF} * (1 + R_1/R_2)$$

where

- V_O is the output voltage (also, cathode voltage, V_Z). The actual value of the internal V_{REF} is a function of V_Z. (2)

The corrected V_{REF} is determined by Equation 3:

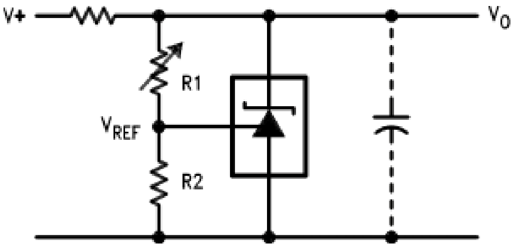
$$V_{REF} = \Delta V_Z * (\Delta V_{REF}/\Delta V_Z) + V_Y$$

where

- V_Y = 2.5 V and $\Delta V_Z = (V_Z - V_Y)$
- $\Delta V_{REF}/\Delta V_Z$ is found in the *Electrical Characteristics* and is typically −1.4 mV/V for V_Z raging from V_{REF} to 10 V and –1 mV/V for V_Z raging from 10 V to 36 V. (3)

9.2 Typical Applications

9.2.1 Shunt Regulator



$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{REF}$$

Figure 12. Shunt Regulator

9.2.1.1 Design Requirements

Design a shunt regulator with the following requirements:

- $V_+ > V_O$
- $V_O = 5$ V

Select R_S (a resistor between V_+ and V_O) such that: 1 mA < I_Z < 100 mA

9.2.1.2 Detailed Design Procedure

The resistor R_S must be selected such that current I_Z remains in the operational region of the part for the entire V_+ range and load current range. The two extremes to consider are V_+ at its minimum, and the load at its maximum, where R_S must be small enough for I_Z to remain above 1 mA. The other extreme is V_+ at its maximum, and the load at its minimum, where R_S must be large enough to maintain I_Z < 100 mA. If unsure, try using 1 mA ≤ I_R ≤ 10 mA as a starting point; just remember the value of I_Z varies with input voltage and load.

Use Equation 4 and Equation 5 to set R_S between R_{S_MIN} and R_{S_MAX}.

$$R_{S\_MIN} = \frac{V_{+\_MAX} - V_O}{I_{LOAD\_MIN} + I_{Z\_MAX}} \tag{4}$$

$$R_{S\_MAX} = \frac{V_{+\_MIN} - V_O}{I_{LOAD\_MAX} + I_{Z\_MIN}} \tag{5}$$

Set feedback resistors R_1 and R_2 for a resistor divider based on Equation 2 and reproduced in Equation 6

$$V_O = V_{REF} * (1 + R_1/R_2) \tag{6}$$

So, for a 5-V output voltage, V_O, and V_{REF} of 2.5 V, simple calculation yields $R_1/R_2 = 1$. Based on this, select R_1 = 1 kΩ and R2 = 1 kΩ.

Typical Applications (continued)

9.2.1.3 Application Curves

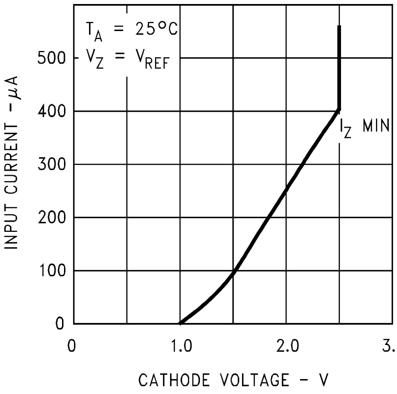


Figure 13. Input Current vs V_Z

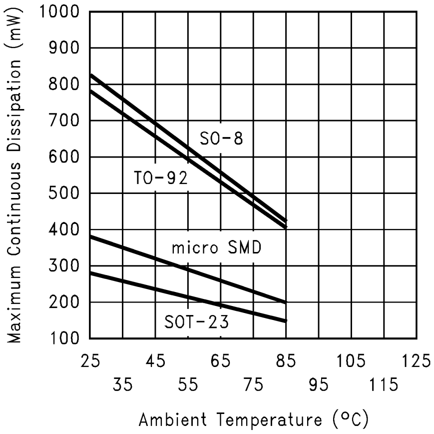


Figure 14. Thermal Information

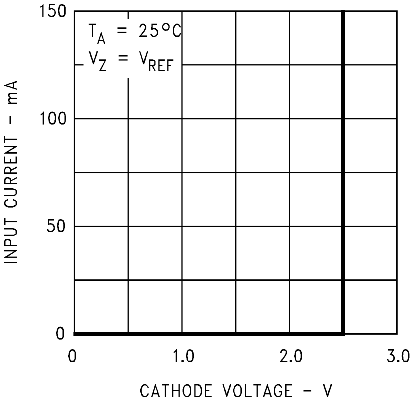


Figure 15. Input Current vs V_Z

9.2.2 Other Applications

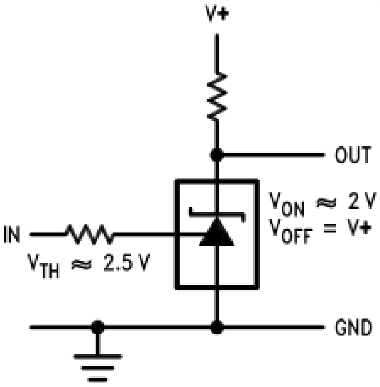
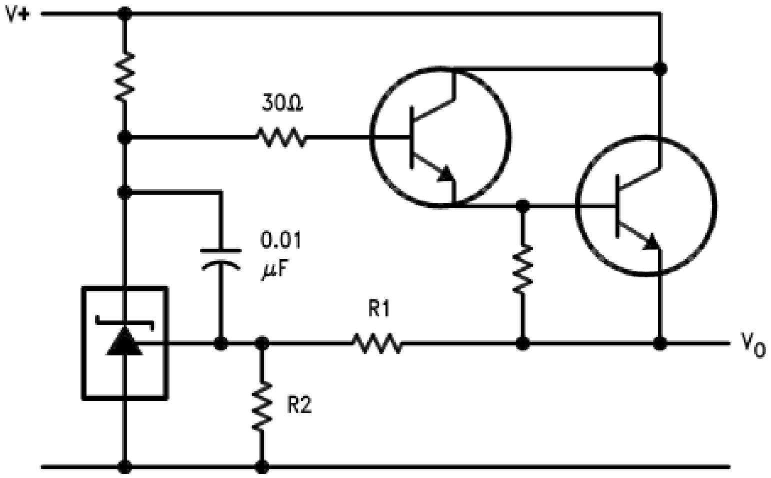


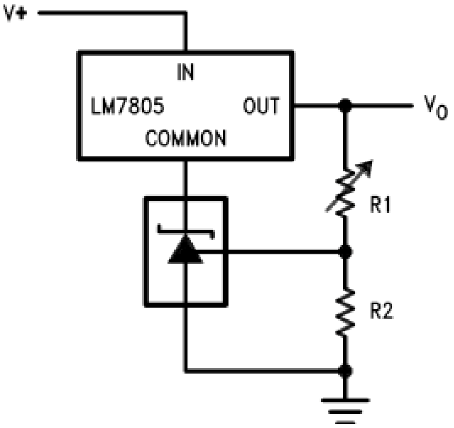
Figure 16. Single Supply Comparator With Temperature Compensated Threshold

Typical Applications (continued)



$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{REF}$$

Figure 17. Series Regulator

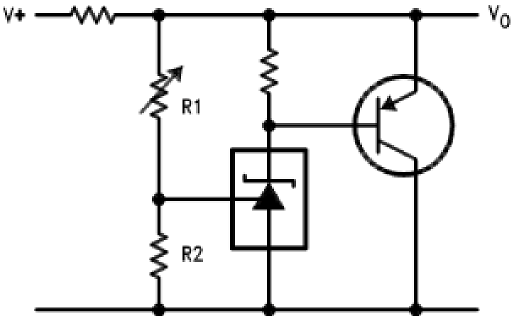


$$V_O = \left(1 + \frac{R1}{R2}\right) V_{REF}$$

$$V_{O\ MIN} = V_{REF} + 5V$$

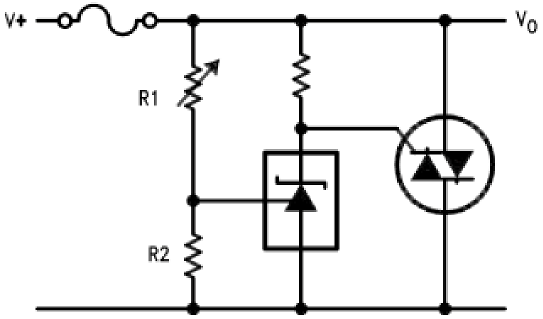
Figure 18. Output Control of a Three Terminal Fixed Regulator

Typical Applications (continued)



$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{REF}$$

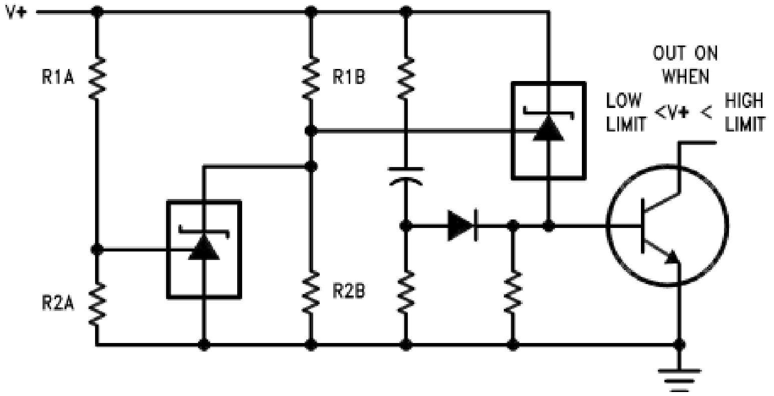
Figure 19. Higher Current Shunt Regulator



$$V_{LIMIT} \approx \left(1 + \frac{R1}{R2}\right) V_{REF}$$

Figure 20. Crow Bar

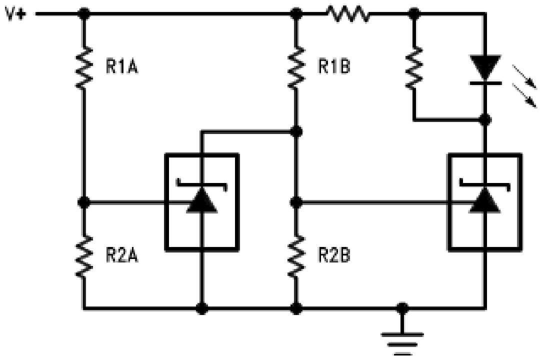
Typical Applications (continued)



$$\text{LOW LIMIT} \approx V_{REF}\left(1 + \frac{R1B}{R2B}\right) + V_{BE}$$

$$\text{HIGH LIMIT} \approx V_{REF}\left(1 + \frac{R1A}{R2A}\right)$$

Figure 21. Over Voltage and Under Voltage Protection Circuit



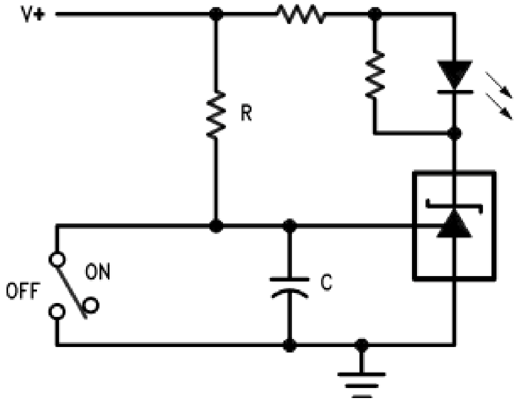
$$\text{LOW LIMIT} \approx V_{REF}\left(1 + \frac{R1B}{R2B}\right)$$

LED ON WHEN
LOW LIMIT $< V^{+} <$ HIGH LIMIT

$$\text{HIGH LIMIT} \approx V_{REF}\left(1 + \frac{R1A}{R2A}\right)$$

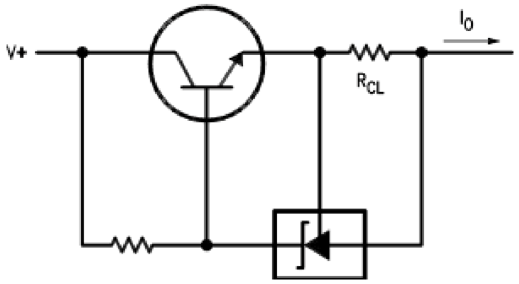
Figure 22. Voltage Monitor

Typical Applications (continued)



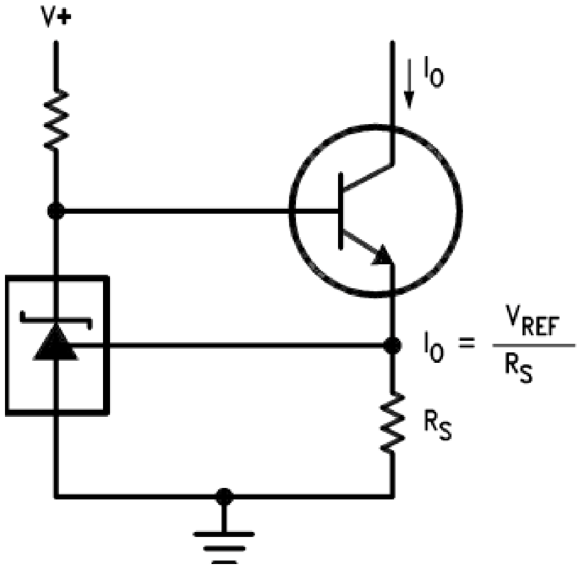
$$\text{DELAY} = R \bullet C \bullet \ell n \frac{V+}{(V^{+}) - V_{REF}}$$

Figure 23. Delay Timer



$$I_O = \frac{V_{REF}}{R_{CL}}$$

Figure 24. Current Limiter or Current Source



$$I_O = \frac{V_{REF}}{R_S}$$

Figure 25. Constant Current Sink

10 Power Supply Recommendations

While a bypass capacitor is not required on the input voltage line, TI recommends reducing noise on the input which could affect the output. TI recommends a 0.1-µF ceramic capacitor or larger.

11 Layout

11.1 Layout Guidelines

Place external components as close to the device as possible. Place R_S close to the cathode, as well as the input bypass capacitor, if used. Keep feedback resistor close the device whenever possible.

11.2 Layout Example

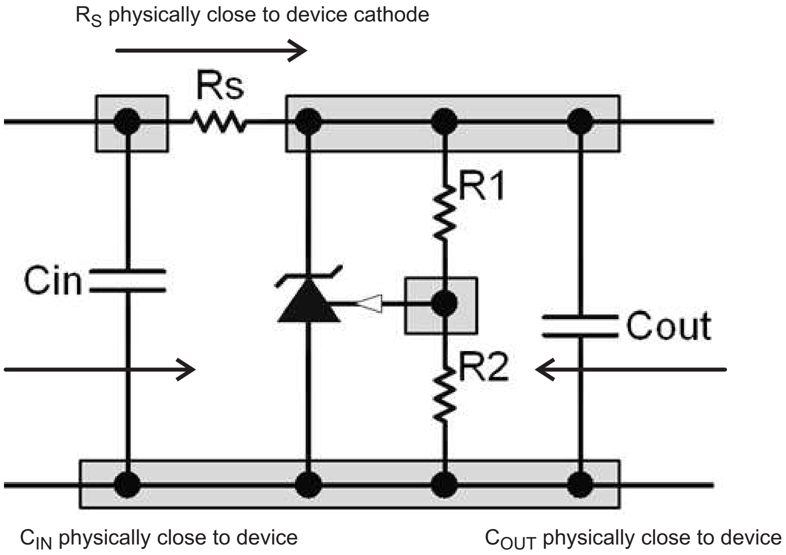


Figure 26. LM431 Layout Recommendation

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM431ACM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM431 ACM
LM431ACM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM431 ACM
LM431ACM3/NOPB	Active	Production	SOT-23 (DBZ) | 3	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N1F
LM431ACM3/NOPB.B	Active	Production	SOT-23 (DBZ) | 3	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1F
LM431ACM3X/NOPB	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N1F
LM431ACM3X/NOPB.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1F
LM431ACMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM431 ACM
LM431ACMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM431 ACM
LM431ACZ/LFT3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-	LM431 ACZ
LM431ACZ/LFT3.B	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 85	LM431 ACZ
LM431ACZ/LFT4	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-	LM431 ACZ
LM431ACZ/LFT4.B	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 85	LM431 ACZ
LM431ACZ/NOPB	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	Call TI	N/A for Pkg Type	0 to 70	LM431 ACZ
LM431ACZ/NOPB.B	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	Call TI	N/A for Pkg Type	-40 to 85	LM431 ACZ
LM431AIM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM431 AIM
LM431AIM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM431 AIM
LM431AIM3/NOPB	Active	Production	SOT-23 (DBZ) | 3	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1E
LM431AIM3/NOPB.B	Active	Production	SOT-23 (DBZ) | 3	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1E
LM431AIM3X/NOPB	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1E
LM431AIM3X/NOPB.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1E

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM431AIMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM431 AIM
LM431AIMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM431 AIM
LM431AIZ/LFT1	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-	LM431 AIZ
LM431AIZ/LFT1.B	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 85	LM431 AIZ
LM431AIZ/NOPB	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	Call TI	N/A for Pkg Type	-40 to 85	LM431 AIZ
LM431AIZ/NOPB.B	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	Call TI	N/A for Pkg Type	-40 to 85	LM431 AIZ
LM431BCM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	431 BCM
LM431BCM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	431 BCM
LM431BCM3/NOPB	Active	Production	SOT-23 (DBZ) | 3	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N1D
LM431BCM3/NOPB.B	Active	Production	SOT-23 (DBZ) | 3	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1D
LM431BCM3X/NOPB	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N1D
LM431BCM3X/NOPB.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1D
LM431BCMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	431 BCM
LM431BCMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	431 BCM
LM431BCZ/NOPB	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	Call TI	N/A for Pkg Type	0 to 70	LM431 BCZ
LM431BCZ/NOPB.B	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	Call TI	N/A for Pkg Type	-40 to 85	LM431 BCZ
LM431BIM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	431 BIM
LM431BIM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	431 BIM
LM431BIM3/NOPB	Active	Production	SOT-23 (DBZ) | 3	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1C
LM431BIM3/NOPB.B	Active	Production	SOT-23 (DBZ) | 3	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1C

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM431BIM3X/NOPB	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1C
LM431BIM3X/NOPB.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1C
LM431BIMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	431 BIM
LM431BIMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	431 BIM
LM431CCM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	431 CCM
LM431CCM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	431 CCM
LM431CCM3/NOPB	Active	Production	SOT-23 (DBZ) | 3	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N1B
LM431CCM3/NOPB.B	Active	Production	SOT-23 (DBZ) | 3	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1B
LM431CCM3X/NOPB	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N1B
LM431CCM3X/NOPB.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1B
LM431CCZ/NOPB	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	Call TI	N/A for Pkg Type	0 to 70	LM431 CCZ
LM431CCZ/NOPB.B	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	Call TI	N/A for Pkg Type	-40 to 85	LM431 CCZ
LM431CIM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	431 CIM
LM431CIM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	431 CIM
LM431CIM3/NOPB	Active	Production	SOT-23 (DBZ) | 3	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1A
LM431CIM3/NOPB.B	Active	Production	SOT-23 (DBZ) | 3	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1A
LM431CIM3X/NOPB	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1A
LM431CIM3X/NOPB.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N1A
LM431CIZ/NOPB	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	Call TI	N/A for Pkg Type	-40 to 85	LM431 CIZ
LM431CIZ/NOPB.B	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	Call TI	N/A for Pkg Type	-40 to 85	LM431 CIZ

(1) **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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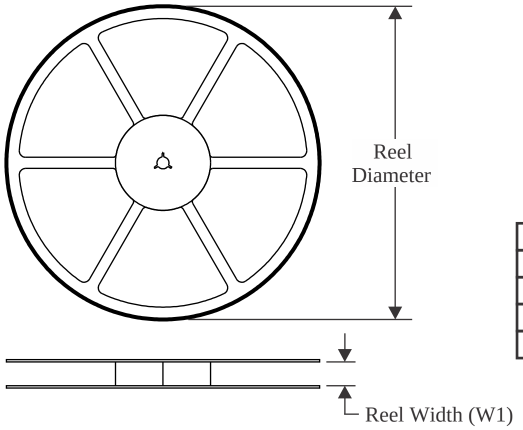
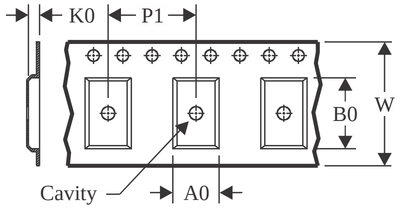
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

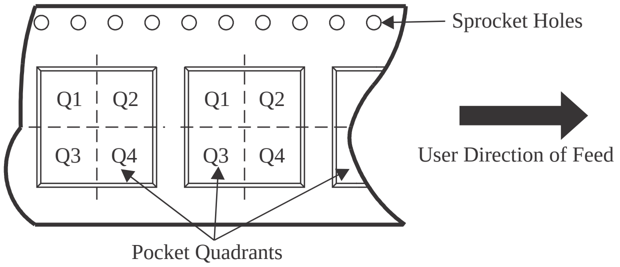


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

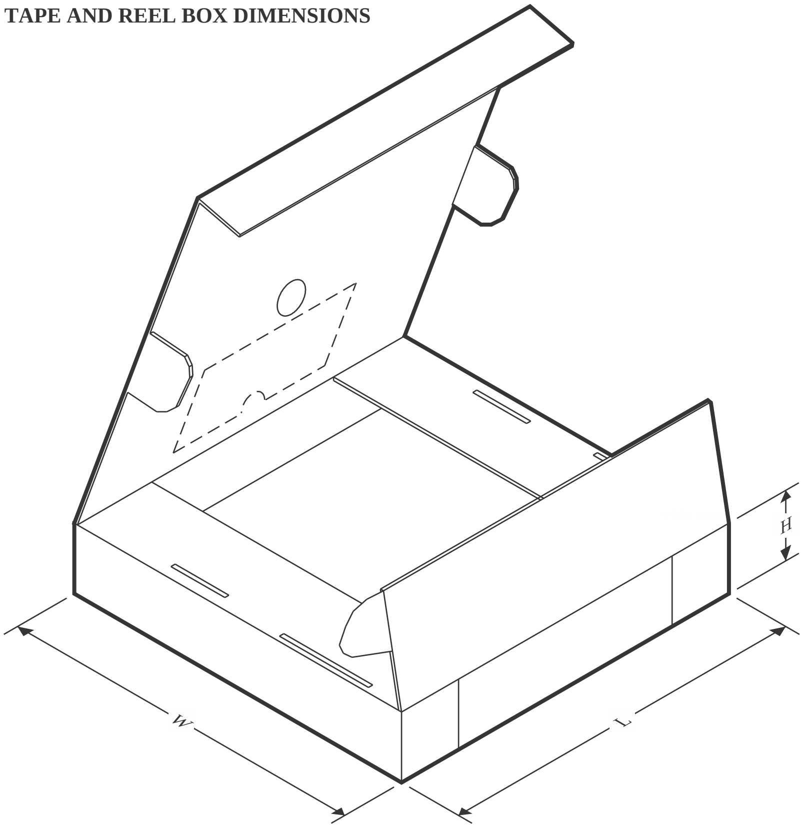
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM431ACM3/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM431ACM3X/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM431ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM431AIM3/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM431AIM3X/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM431AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM431BCM3/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM431BCM3X/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM431BCMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM431BIM3/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM431BIM3X/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM431BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM431CCM3/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM431CCM3X/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM431CIM3/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM431CIM3X/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3

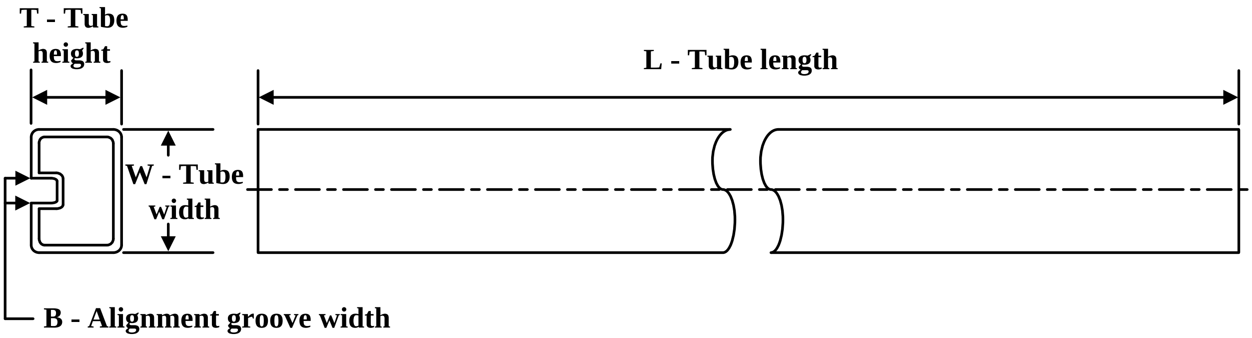
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

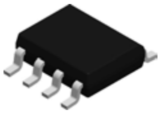
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM431ACM3/NOPB	SOT-23	DBZ	3	1000	208.0	191.0	35.0
LM431ACM3X/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM431ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM431AIM3/NOPB	SOT-23	DBZ	3	1000	208.0	191.0	35.0
LM431AIM3X/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM431AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM431BCM3/NOPB	SOT-23	DBZ	3	1000	208.0	191.0	35.0
LM431BCM3X/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM431BCMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM431BIM3/NOPB	SOT-23	DBZ	3	1000	208.0	191.0	35.0
LM431BIM3X/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM431BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM431CCM3/NOPB	SOT-23	DBZ	3	1000	208.0	191.0	35.0
LM431CCM3X/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM431CIM3/NOPB	SOT-23	DBZ	3	1000	208.0	191.0	35.0
LM431CIM3X/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM431ACM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM431ACM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM431AIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM431AIM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM431BCM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM431BCM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM431BIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM431BIM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM431CCM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM431CCM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM431CIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM431CIM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

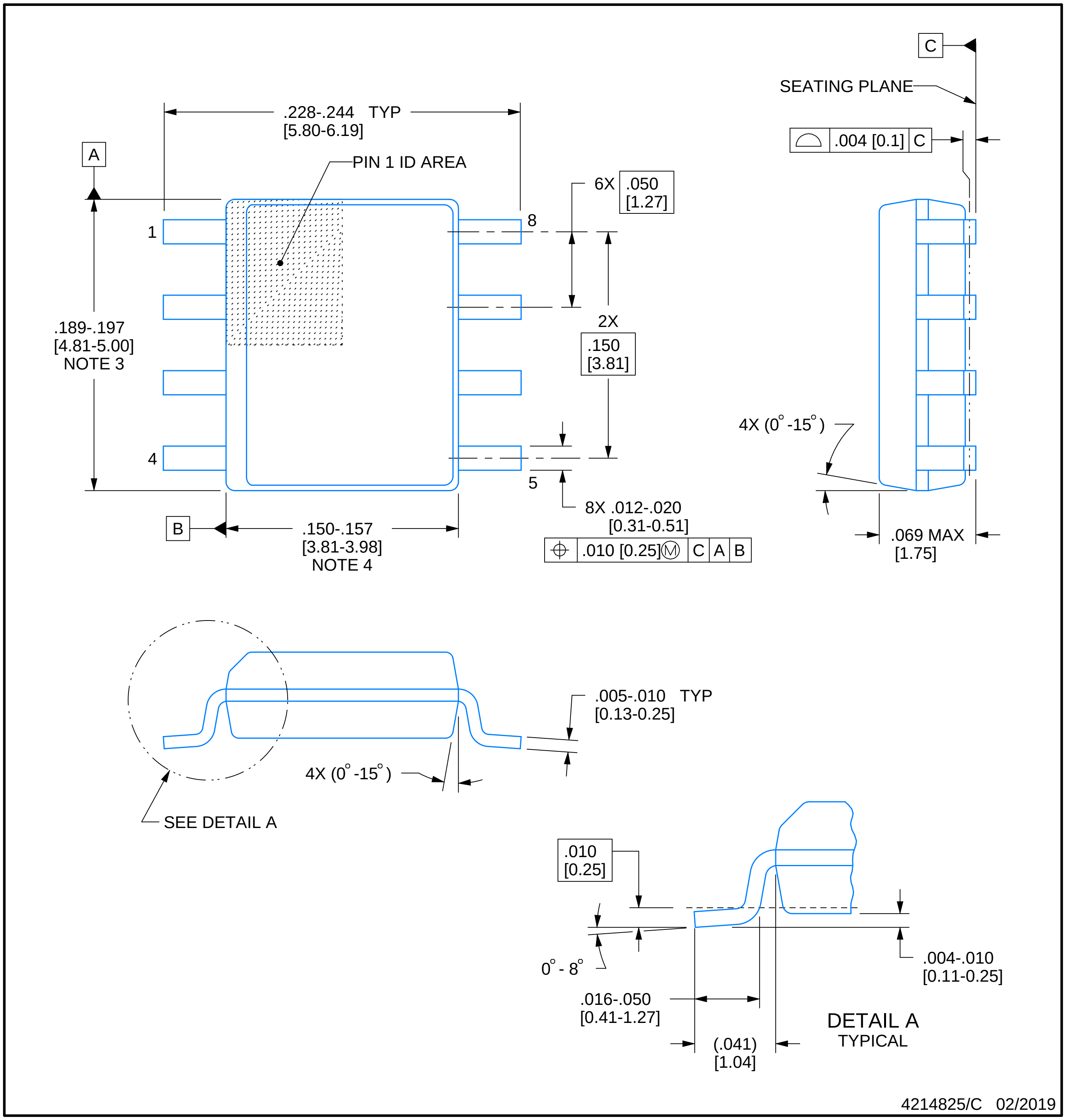


PACKAGE OUTLINE

D0008A

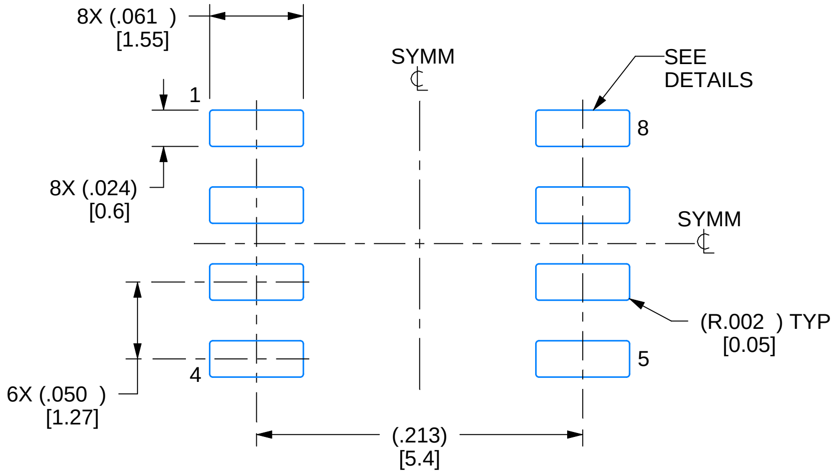
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

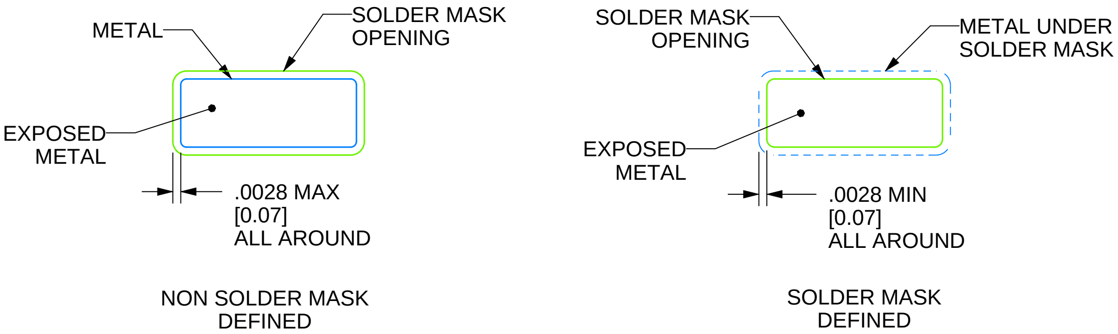


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



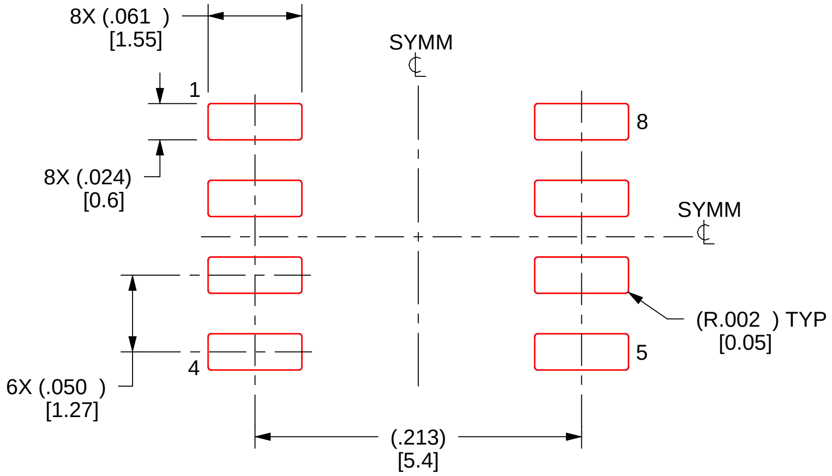
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

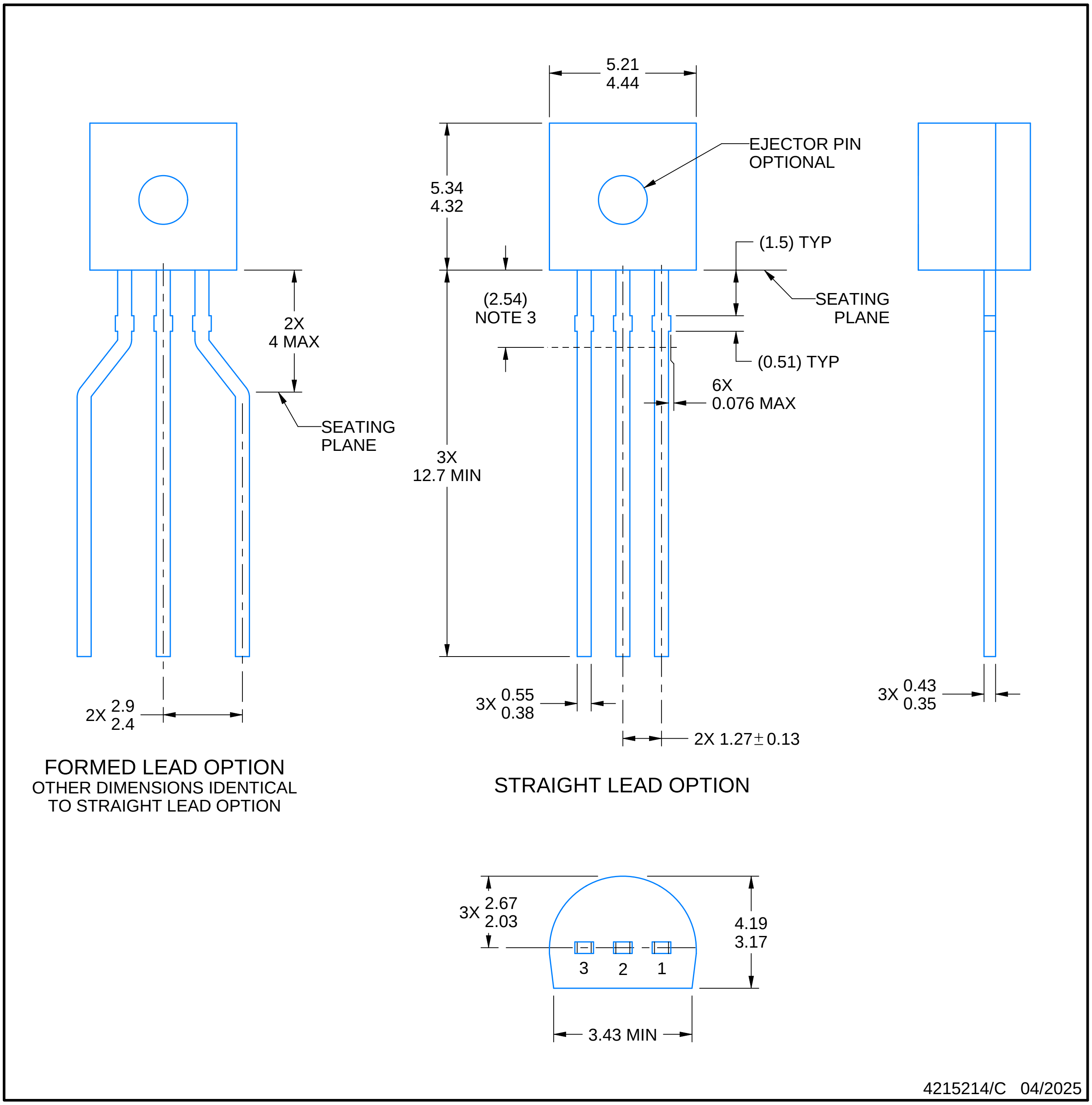
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

LP0003A

TO-92 - 5.34 mm max height

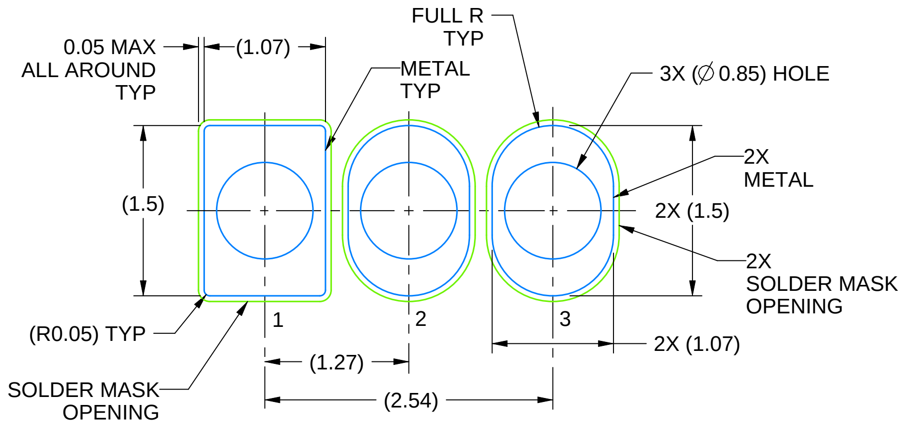
TO-92



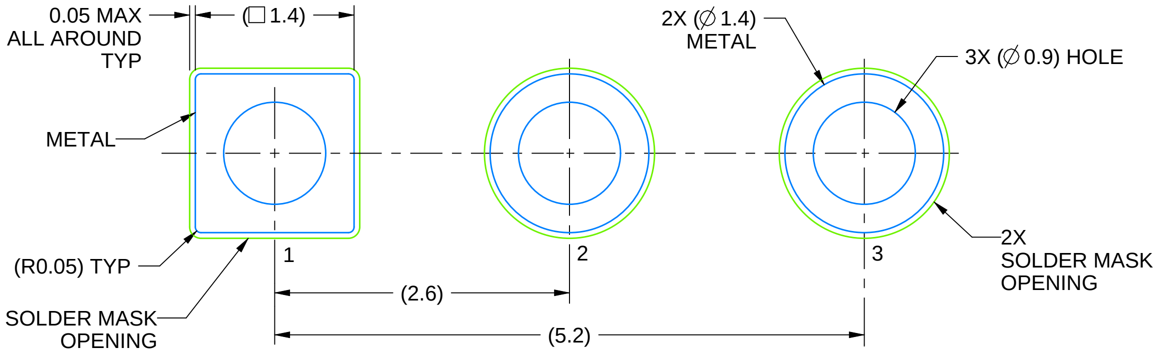
4215214/C 04/2025

NOTES:

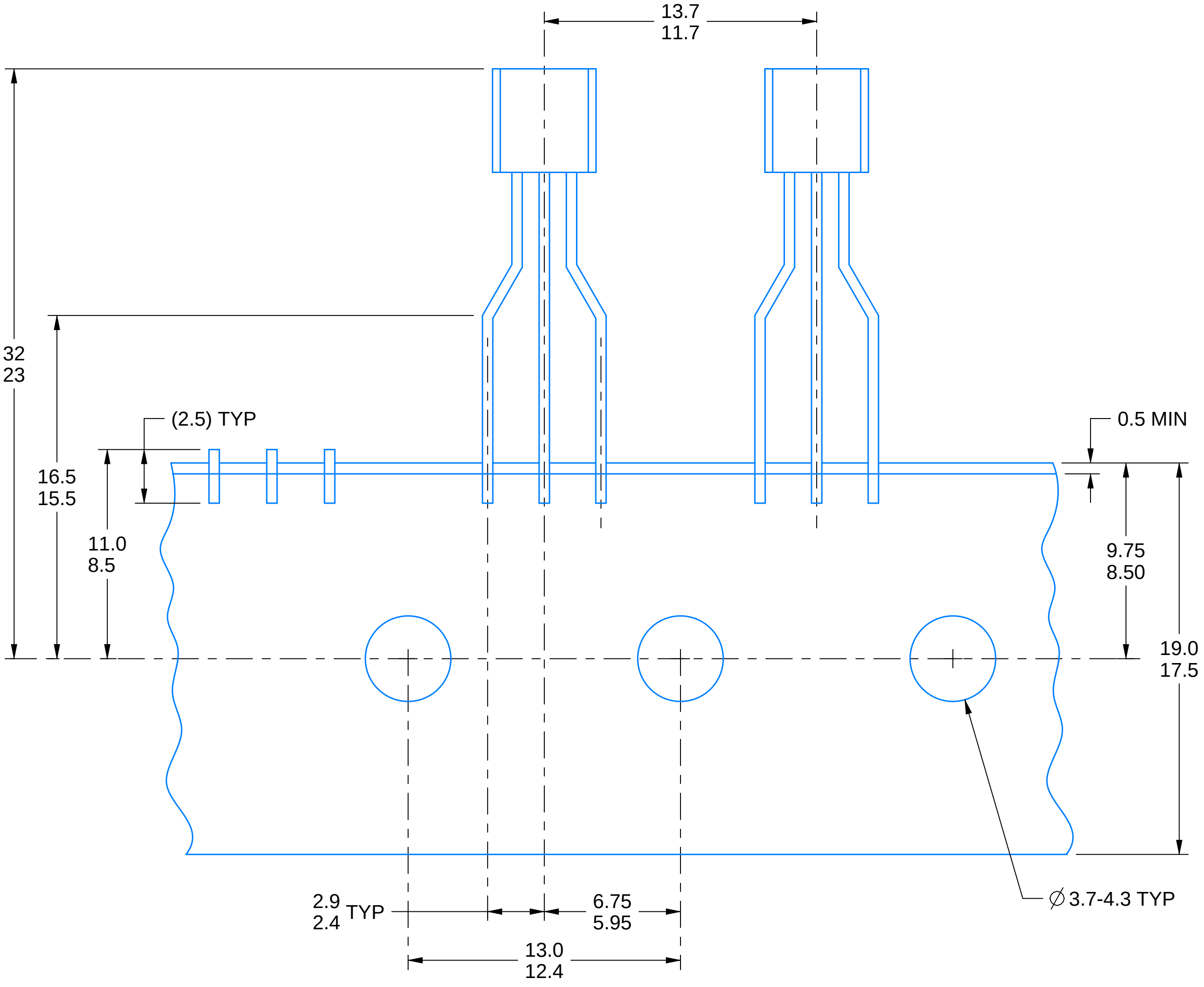
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
    a. Straight lead option available in bulk pack only.
    b. Formed lead option available in tape and reel or ammo pack.
    c. Specific products can be offered in limited combinations of shipping medium and lead options.
    d. Consult product folder for more information on available options.



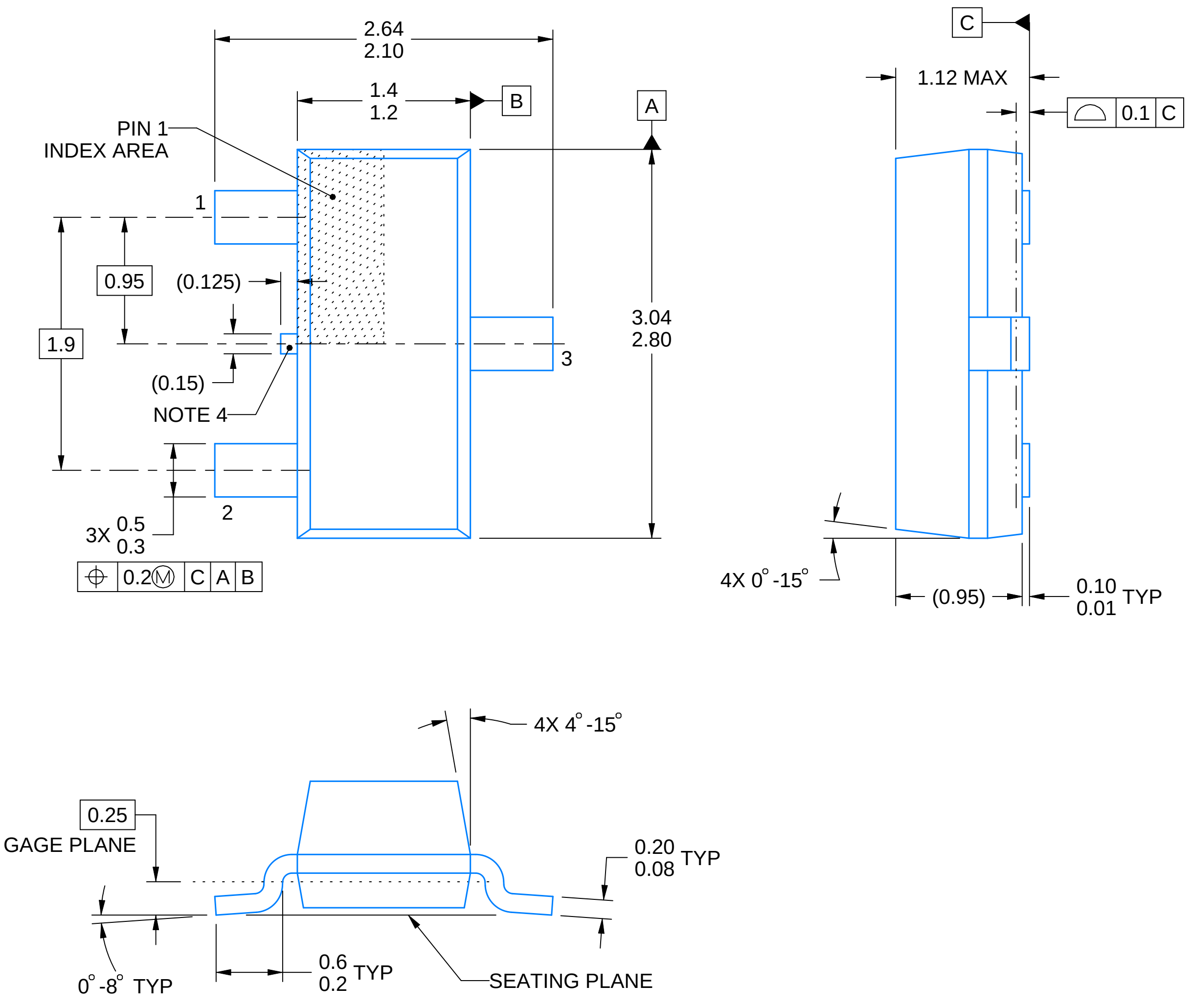
LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



FOR FORMED LEAD OPTION PACKAGE

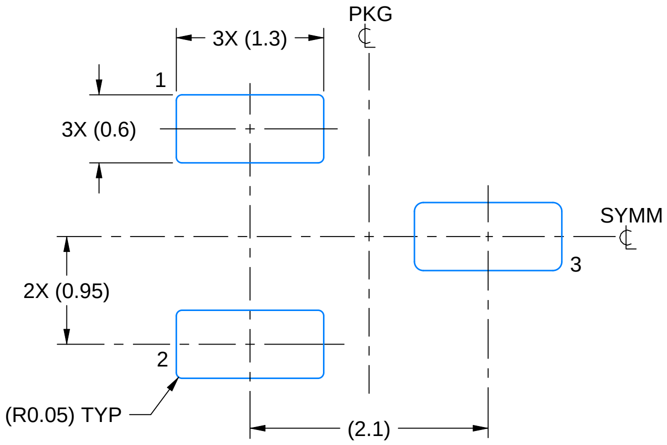


4214838/F 08/2024

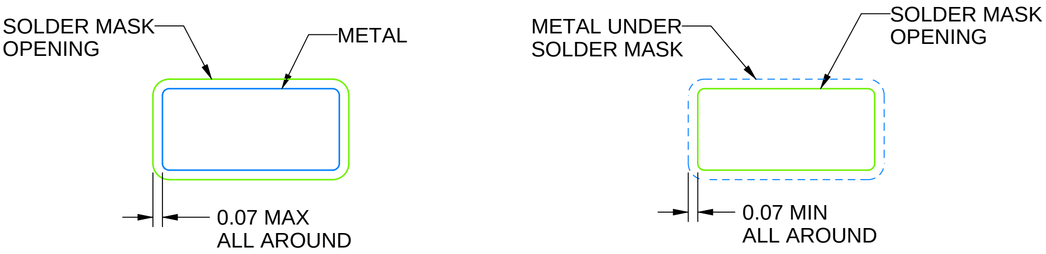
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
SCALE:15X



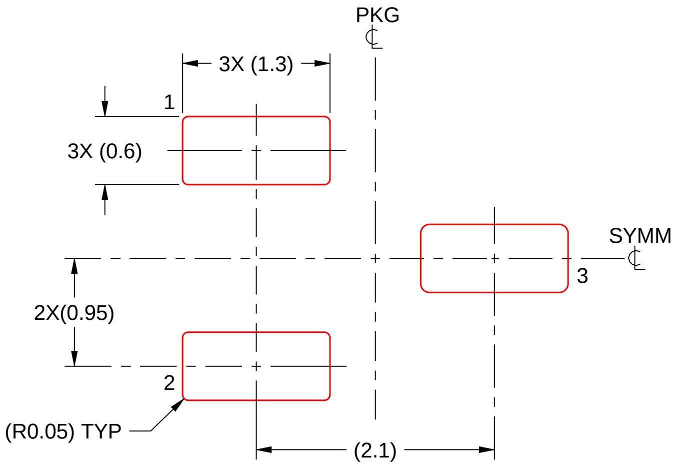
NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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