

SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LV5684PVC — For Car Audio Systems **Multi-Power Supply IC**

Overview

The LV5684PVC is a power supply IC suitable for USB/CD receiver system for car audio system.

This IC integrates 5 systems of regulator output, 2 systems of high side power switch, overcurrent protector, overvoltage protector and overheat protector

Bi-CMOS LSI

Supply for V_{DD} and SW33V outputs is low voltage specification, which enables drastic reduction of power dissipation compared to the existing model. (the package is HZIP15J).

Features

• Low consumption current: 50μA (typ, only V_{DD} output is in operation)

• 5 systems of regulator output

VDD for microcontroller: output voltage: 3.3V, maximum output current: 350mA reverse current protection implemented.

For system: output voltage: 3.3V, maximum output current: 450mA

For audio: output voltage: 5 to 9V (set by external resistors), maximum output current: 250mA

For illumination: output voltage: 5 to 12V (set by external resistors), maximum output current: 300mA

For CD: output voltage: 5V/8V, maximum output current: 1300mA

• 2 lines of high side switch with interlock VCC

EXT: Maximum output current: 350mA, voltage difference between input and output: 0.5V

ANT: Maximum output current: 300mA, voltage difference between input and output: 0.5V

• Supply input

V6IN: 6V for VDD, system (SW33V)

V_{CC}1: For internal reference voltage, control circuits

In case of voltage drop of V6IN, VCC1 supplies to VDD output.

V_{CC}2: For AUDIO, illumination, CD, EXT/ANT

- Overcurrent protector
- Overvoltage protector(OVP): VCC1,VCC2 Typ 23V (All outputs except VDD are turned off) Overvoltage shutdown(OVS): V6IN Typ 23V (All outputs except V_{DD} are turned off)
- Overheat protector: Typ 175°C

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• PchLDMOS is used in power output block

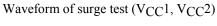
(Warning) The protector functions only improve the IC's tolerance and they do not guarantee the safety of the IC if used under the conditions out of safety range or ratings. Use of the IC such as use under overcurrent protection range, thermal shutdown state or V6IN OVS condition may degrade the IC's reliability and eventually damage the IC.

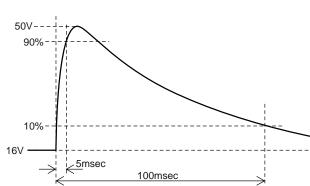
Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Conditions	Conditions		Ratings	Unit
Supply voltage	V _{CC} max	V _{CC} 1, V _{CC} 2		36	V
	V6IN max	V6IN (*)		7	V
Input voltage	V _{IN} max	CTRL1, CTRL2		7	V
Allowable power dissipation	Pd max	Independent IC	Ta ≤ 25°C	1.5	W
		Al heat sink *		5.6	W
		With an infinity heat sink		32.5	W
Peak supply voltage	V _{CC} peak	See below for the waveform ap	plied.	50	V
Operating ambient temperature	Topr				°C
Storage temperature	Tstg			-55 to +150	°C
Junction temperature	Tj max			150	°C

^{* :} When the Aluminum heat sink (50mm \times 50mm \times 1.5mm) is used





*V6IN is designed to tolerant toward short period of over-voltage (max 20V) which is assumed in condition of short circuit between V_{CC1}/V_{CC2} and V6IN.

However, applying over-voltage higher than maximum rating (7V) to V6IN may degrade the device reliability

Recommended Operating range at $Ta = 25^{\circ}C$

Vcc1

Parameter	Conditions	Ratings	Unit
Operating supply voltage 1	V _{DD} output	7 to 16	V

V_{CC^2}

Parameter	Conditions	Ratings	Unit
Operating supply voltage 2	ILM output (10V)	12 to 16	V
	ILM output (8V)	10 to 16	V
Operating supply voltage 3	AUDIO output (9V)	10 to 16	V
Operating supply voltage 4	CD output (I _O = 1.3A)	10.5 to 16	V
	CD output (I _O ≤ 1A)	10 to 16	V
Operating supply voltage 5	EXT output, ANT output	10 to 16	V

V6IN

Parameter	Conditions	Ratings	Unit
Operating supply voltage 6	perating supply voltage 6 V _{DD} output, SW33V output		V

Electrical Characteristics at $V_{CC}1 = V_{CC}2 = 14.4V$, V6IN = 6V at $Ta = 25^{\circ}C$ (*1)

Licetifical Offaracteris	1	V((2 14.4 V, VOIIV 0 V at 1a 2.	3 C (1)	Ratings		
Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	Icc	V _{DD} w/out load, CTRL1/2 = "L/L"		50	100	μА
CTRL1 input (ANT/EXT/ILM)		,	I			
Low input voltage	V _{IL} 1		0		0.5	V
M1 input voltage	V _{IM1} 1		0.8	1.1	1.4	V
M2 input voltage	V _{IM2} 1		1.9	2.2	2.5	V
High input voltage	V _{IH} 1		2.9	3.3	5.5	V
Input impedance	R _{IH} 1	input voltage ≤ 3.3V	280	400	480	kΩ
CTRL2 input (CD/AUDIO/SW3	ı	<u> </u>	I			
Low input voltage	V _{IL} 2		0		0.5	V
M1 input voltage	V _{IM1} 2		0.8	1.1	1.4	V
M2 input voltage	V _{IM2} 2		1.9	2.2	2.5	V
High input voltage	V _{IH} 2		2.9	3.3	5.5	V
Input impedance	R _{IH} 2	input voltage ≤ 3.3V	280	400	480	kΩ
V _{DD} output (3.3V) (reverse cu	1		200	400	400	
Output voltage	V _O 1	I _O 1 = 200mA	3.13	3.3	3.47	V
Output current		-	350	3.3	3.47	mA
-	101	$V_{O}1 \ge 3.1V$ 5.7V < V6IN < 6.5V, $I_{O}1 = 200$ mA or	330	30	90	mV
Line regulation	∆V _{OLN} 1	V6IN = 0V, 7.5V < V _{CC} 1 < 16V, I _O 1 = 200mA		30	90	IIIV
Load regulation	ΔV _{OLD} 1	1mA < I _O 1 < 200mA		70	150	mV
Dropout voltage	V _{DROP} 1	I _O 1 = 200mA, V6IN = 0V		2.8	3.5	٧
Ripple rejection (*2)	R _{REJ} 1	(applicable to V _{CC} 1) f = 120Hz, V6IN or V _{CC} 1 = 0.5Vpp	40	50		dB
Reverse current	Irev	I _O 1 = 200mA V _O 1 = 3.3V, V _{CC} 1 = V6IN = 0V		1	50	μА
SW33V output (3.3V) ; CTRL2				'	30	μΛ
Output voltage	V _O 2	$I_{O}^2 = 200 \text{mA}$	3.13	3.3	3.47	V
Output current	I _O 2	$V_{O2} \ge 3.1V$	450	0.0	0.41	mA
Line regulation		-	430	30	90	mV
	ΔV _{OLN} 2	5.7V < V6IN < 6.5V, I _O 2 = 200mA		70	150	mV
Load regulation	ΔV _{OLD} 2	1mA < I _O 2 < 200mA				
Dropout voltage	V _{DROP} 2	I _O 2 = 200mA	40	0.25	0.5	V
Ripple rejection (*2)	R _{REJ} 2	$f = 120$ Hz, V6IN or $V_{CC}1 = 0.5$ Vpp $I_{Q}2 = 200$ mA	40	50		dB
AUDIO (5-9V)output ; CTRL2	= "M1 or M2 or H	,				
AUDIO_F voltage	V _I 3		1.212	1.25	1.288	V
AUDIO_F input current	I _{IN} 3		-1		1	μΑ
AUDIO output voltage 1	V _O 3	$I_{O}3 = 150 \text{mA}, R3 = 30 \text{k}\Omega, R4 = 5.6 \text{k}\Omega (*3)$	7.65	8.0	8.35	V
AUDIO output voltage 2	V _O 3'	$I_{O}3 = 150$ mA, R3 = 27k Ω , R4 = 4.7k Ω (*3)	8.13	8.5	8.87	V
AUDIO output voltage 3	V _O 3''	$I_{O}3 = 150$ mA, R3 = 24k Ω , R4 = 3.9k Ω (*3)	8.6	9.0	9.4	V
AUDIO output voltage 4	V _O 3'''	$I_{O}3 = 150$ mA, R3 = 30k Ω , R4 = 10k Ω (*3)	4.75	5.0	5.25	V
AUDIO output current	I _O 3		250			mA
Line regulation	ΔV _{OLN} 3	10V < V _{CC} 2 < 16V, I _O 3 = 150mA		30	90	mV
Load regulation	ΔV _{OLD} 3	1mA < I _O 3 < 150mA		70	150	mV
Dropout voltage 1	V _{DROP} 3	I _O 3 = 150mA		0.3	0.45	V
Ripple rejection (*2)	R _{REJ} 3	f = 120Hz, I _O 3 = 150mA	40	50		dB
ILM (5-12V) output ; CTRL1 =	L L		I			
ILM_F voltage	V _I 4		1.212	1.25	1.288	V
ILM_F input current	I _{IN} 4		-1		1	μА
ILM output voltage 1	V _O 4	$I_{\Omega}4 = 200 \text{mA}, R1 = 43 \text{k}\Omega, R2 = 5.1 \text{k}\Omega (*3)$	11.21	11.8	12.39	V
ILM output voltage 2	V _O 4'	$I_{\Omega}4 = 200\text{mA}, R1 = 56\text{k}\Omega, R2 = 7.5\text{k}\Omega \text{ (*3)}$	9.97	10.5	11.03	V
	1.0.	0 - 200, 00, 7.0 (0)	5.07	. 5.0		

^{*1 :} All the specification is defined based on the tests performed under the conditions where Tj and Ta (= 25°C) are almost equal. These tests were performed with pulse load to minimize the increase of junction temperature (Tj).

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^{*2 :} guaranteed by design

^{*3 :} Using resistors of tolerance within 1%.

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Parameter	Cymph ol	Conditions		Ratings		Unit
Parameter	Symbol	Conditions	min	typ	max	Unit
ILM output voltage 3	V _O 4''	I_O 4 = 200mA, R1 = 30kΩ, R2 = 5.6kΩ (*3)	7.6	8.0	8.4	V
ILM output voltage 4	V _O 4'''	$I_{O}4 = 200 \text{mA}, R1 = 30 \text{k}\Omega, R2 = 10 \text{k}\Omega \text{ (*3)}$	4.75	5.0	5.25	V
ILM output current	I _O 4		300			mA
Line regulation	ΔV _{OLN} 4	$10V < V_{CC}2 < 16V, I_{O}4 = 200$ mA R1 = 30 kΩ, R2 = 5.6 kΩ		30	90	mV
Load regulation	∆V _{OLD} 4	1mA < I _O 4 < 200mA		70	150	mV
Dropout voltage 1	V _{DROP} 4	I _O 4 = 200mA		0.7	1.05	V
Dropout voltage 2	V _{DROP} 4'	I _O 4 = 100mA		0.35	0.53	V
Ripple rejection (*2)	R _{REJ} 4	f = 120Hz, I _O 4 = 200mA	40	50		dB
CD (5V/8V output) ; CTRL2	= "H" : 8V, CTRL2 :	= "M2" : 5V				
Output voltage	V _O 51	I _O 5 = 1000mA	4.75	5.0	5.25	V
	V _O 52	I _O 5 = 1000mA	7.6	8.0	8.4	V
Output current	I _O 5	$V_{O}51 \ge 4.7V, V_{O}52 \ge 7.6V$	1300			mA
Line regulation	ΔV _{OLN} 5	10.5V < V _{CC} 2 < 16V, I _O 5 = 1000mA		50	100	mV
Load regulation	ΔV _{OLD} 5	10mA < I _O 5 < 1000mA		100	200	mV
Dropout voltage 1	V _{DROP} 5	I _O 5 = 1000mA		1.0	1.5	V
Dropout voltage 2	V _{DROP} 5'	I _O 5 = 500mA		0.5	0.75	V
Ripple rejection (*2)	R _{REJ} 5	f = 120Hz, I _O 5 = 1000mA	40	50		dB
EXT_HS-SW ; CTRL1 = "M2	2 or H"	•	•			
Output voltage	V _O 6	I _O 6 = 350mA	V _{CC} 2-1.0	V _{CC} 2-0.5		V
Output current	I _O 6	V _O 6 ≥ V _{CC} 2-1.0	350			mA
ANT_HS-SW ; CTRL1 = "H"	,	•		•		
Output voltage	V _O 7	I _O 7 = 300mA	V _{CC} 2-1.0	V _{CC} 2-0.5		V
Output current	I _O 7	V _O 7 ≥ V _{CC} 2-1.0	300			mA

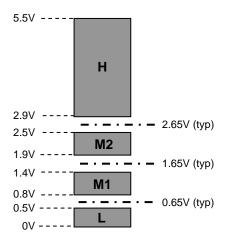
^{*2 :} guaranteed by design

CTRL logic truth table

CTRL1	ANT	EXT	ILM
Н	ON	ON	ON
M2	OFF	ON	ON
M1	OFF	OFF	ON
L	OFF	OFF	OFF

CTRL2	CD	AUDIO	SW33V
Н	ON (8V)	ON	ON
M2	ON (5V)	ON	ON
M1	OFF	ON	ON
L	OFF	OFF	OFF

CTRL1/2 voltage range and threshold

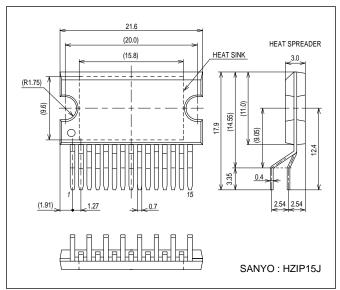


 $^{^{\}star}3$: Using resistors of tolerance within 1%.

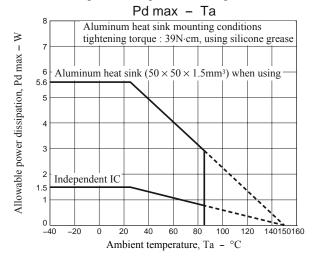
Package Dimensions

unit: mm (typ)

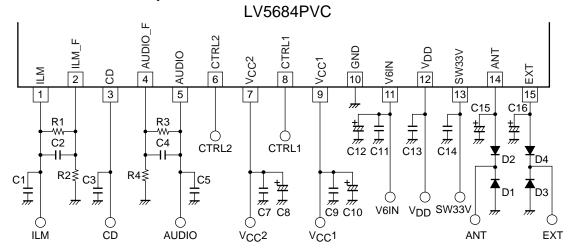
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• Allowable power dissipation derating curve



Application Circuit Example

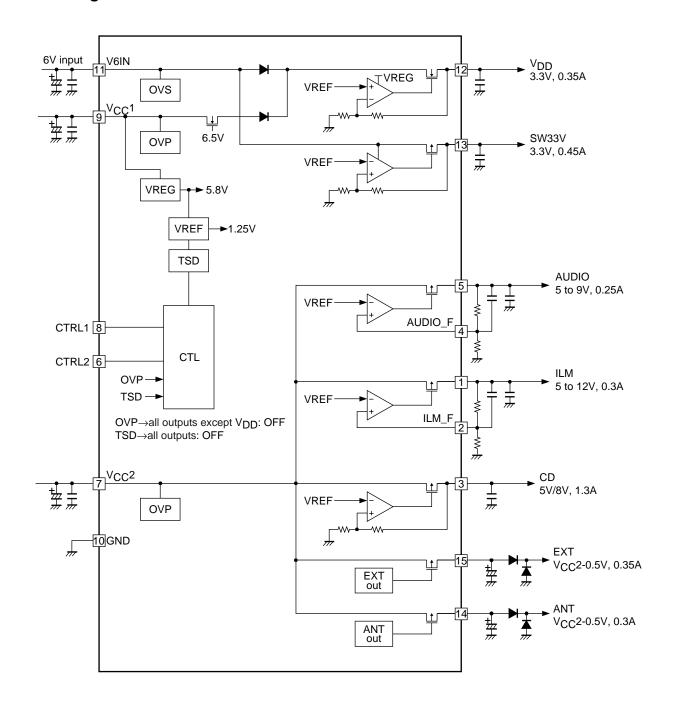


Peripheral parts

Part name	Description	Recommended value	Note
C1, C3, C5, C13, C14	output stabilization capacitor	greater than10μF (*1)	
C2, C4	output stabilization capacitor	0pF	Ceramic capacitor
C8, C10, C12	Capacitor for bypass power supply	C8: greater than 100μF C10,C12: greater than 47μF	Make sure to implement close to V _{CC} and GND.
C7, C9, C11	Capacitor for oscillation protector	greater than 0.22μF	
C15, C16	Capacitor for EXT/ANT output stabilization	greater than 2.2μF	
R1, R2	ILM voltage setting	R1/R2 43kΩ/5.1kΩ : V_O = 12V 56kΩ/7.5kΩ : V_O = 10.5V 30kΩ/5.6kΩ : V_O = 8V 30kΩ/10kΩ : V_O = 5V	Use resistors of tolerance within 1%
R3, R4	AUDIO voltage setting	R3/R4 $30k\Omega/10k\Omega : V_O = 5V$ $30k\Omega/5.6k\Omega : V_O = 8.0V$ $27k\Omega/4.7k\Omega : V_O = 8.5V$ $24k\Omega/3.9k\Omega : V_O = 9V$	Use resistors of tolerance within 1%
D1, D2, D3, D4	Internal device protector diode	SANYO SB1003M3	

^(*1) Make sure that output capacitors are greater than 10uF and meets the condition of ESR = 0.001 to 10Ω, in which voltage/ temperature dependence and unit differences are taken into consideration. Moreover, in case of electrolytic capacitor, high-frequency characteristics should be sufficiently good.

Block Diagram



Pin Function

<u> </u>	IIICUOII		
Pin No.	Pin name	Description	Equivalent Circuit
1	ILM	ILM output When CTRL1 = M1, M2, H, ILM is ON	7 Vcc2
2	ILM_F	ILM voltage adjust	$ \begin{array}{c c} \hline 2 & \downarrow & \downarrow \\ \hline 1 & \downarrow & \downarrow \\ \hline 10 & \downarrow & \downarrow \\ \hline GND \end{array} $

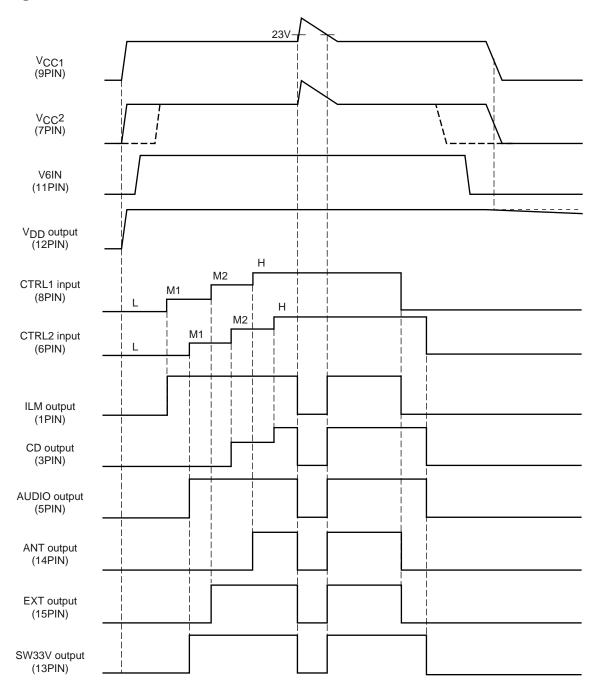
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	om preceding pa		Fauivalent Circuit
<u>Pin No.</u> 3	Pin name	Description CD output When CTRL2 = M2, H, CD is ON 5V or 8V/1.3A	Equivalent Circuit 7 3 $108k\Omega$ $108k\Omega$ $108k\Omega$ $108k\Omega$ $108k\Omega$ $108k\Omega$ $108k\Omega$ $108k\Omega$ $108k\Omega$
4	AUDIO_F	AUDIO voltage adjust	7 Vcc2 Vcc2 5 H W
5	AUDIO	AUDIO output When CTRL2 = M1, M2, H, AUDIO is ON	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
6	CTRL2	CTRL2 input 4-value input	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$
7 8	Vcc ² CTRL1	Power supply CTRL1 input 4-value input	$ \begin{array}{c c} 9 & V_{CC1} \\ \hline 6 & 85k\Omega \\ \hline 185k\Omega \\ \hline 75k\Omega \\ \end{array} $ $ \begin{array}{c c} 6 & GND \end{array} $
9	V _{CC} 1	Power supply	V _{CC} ² V _{CC} ¹ V _{6IN} 7 V _C 9 V _C 11
10	GND	GND	
11	V6IN	Power supply	(10) GND

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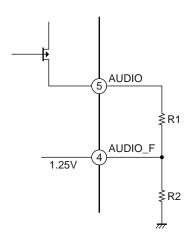
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Pin No.	Pin name	Description	Equivalent Circuit
12	VDD	V _{DD} output 3.3V/0.35A	11 Vcc1 Vcc1 Vcc1 Vcc1 Vcc1 Vcc1 Vcc1 V
13	SW33V	SW33V output When CTRL2 = M1, M2, H, SW33V is ON 3.3V/0.45A	13 × 230kΩ × 140kΩ × 1kΩ GND
14	ANT	ANT output When CTRL1 = H, ANT is ON V _{CC} -0.5V/300mA	7 $100k\Omega$ 14 $5k\Omega$ $SK\Omega$ $SK\Omega$
15	EXT	EXT output When CTRL1 = M2, H, EXT is ON VCC-0.5V/350mA	7 $100k\Omega$ 15 $5k\Omega$ SND

Timing Chart



Caution: The above values are obtained when typ.

• How to set AUDIO output voltage



AUDIO_F is determined by internal band-gap reference voltage (typ = 1.25V).

AUDIO output voltage expression

$$AUDIO = (\frac{R_1}{R_2} + 1) \times 1.25[V]$$

$$\frac{R_1}{R_2} = \frac{AUDIO}{1.25} - 1$$

Set the ratio of R1 and R2 to satisfy above expression.

(ex) AUDIO = 9V setting

$$\frac{R_1}{R_2} = \frac{9}{1.25} - 1 = 6.2$$

$$\frac{R_1}{R_2} = \frac{24k\Omega}{3.9k\Omega} \cong 6.15$$

$$\frac{R_1}{R_2} = \frac{24k\Omega}{3.9k\Omega} \cong 6.15$$
 $AUDIO = (6.15+1) \times 1.25V \cong 8.94V$

• ILM output voltage is similarly calculated as AUDIO output.

(ex)
$$ILM = 10.5V$$
 setting

$$\frac{R_1}{R_2} = \frac{10.5}{1.25} - 1 = 7.4$$

$$\frac{R_1}{R_2} = \frac{56k\Omega}{7.5k\Omega} \cong 7.46$$

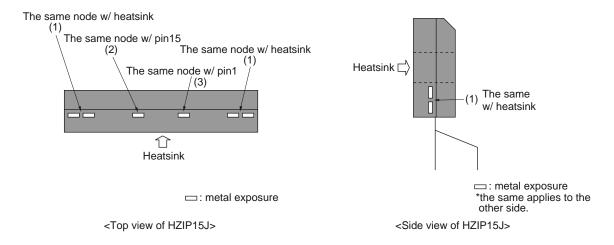
$$ILM = (7.46 + 1) \times 1.25V \cong \boxed{10.575V}$$

Note: The above values are typical values. These values have variation among the range of their tolerances.

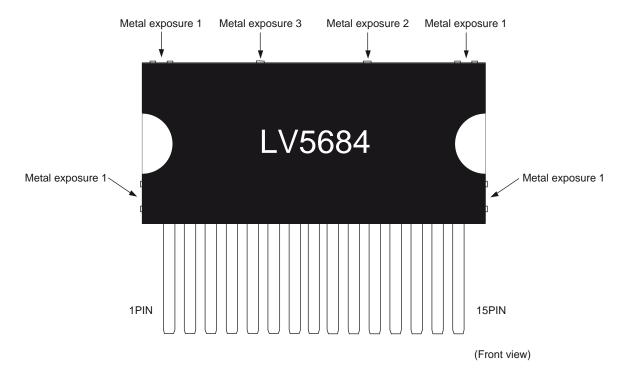
Warning: Implementing LV5684PVC to the set board

The package of LV5684PVC is HZIP15J which has some metal exposures other than connection pins and heatsink as shown in the diagram below. The electrical potentials of (2) and (3) are the same as those of pin15 and pin1, respectively. (2) (= pin15) is the EXT (High-side switch) output pin and (3) (= pin1) is the ILM (regulator) output pin. When you implement the IC to the set board, make sure that the bolts and the heatsink are out of touch from (2) and (3). If the metal exposures touch the bolts which has the same electrical potential with GND, GND short occurs in ILM output and EXT output. The exposures of (1) are connected to heatsink which has the same electrical potential with substrate of the IC chip (GND). Therefore, (1) and GND electrical potential of the set board can contact each other.

HZIP15J outline



Frame diagram (HZIP15J)



HZIP15J Heat sink attachment

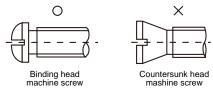
Heat sinks are used to lower the semiconductor device junction temperature by leading the head generated by the device to the outer environment and dissipating that heat.

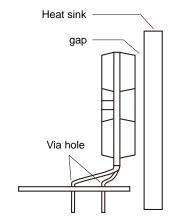
a. Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.

b. Heat sink attachment

- Use flat-head screws to attach heat sinks.
- Use also washer to protect the package.
- Use tightening torques in the ranges 39-59Ncm (4-6kgcm).
- If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
- Do not make gap, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- Take care a position of via hole.
- Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- Verify that there are no press burrs or screw-hole burrs on the heat sink.
- Warping in heat sinks and printed circuit boards must be no more than 0.05 mm between screw holes, for either concave or convex warping.
- Twisting must be limited to under 0.05 mm.
- Heat sink and semiconductor device are mounted in parallel.

 Take care of electric or compressed air drivers
- The speed of these torque wrenches should never exceed 700 rpm, and should typically be about 400 rpm.





c. Silicone grease

- Spread the silicone grease evenly when mounting heat sinks.
- Sanyo recommends YG-6260 (Momentive Performance Materials Japan LLC)

d. Mount

- First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.
- When attaching a heat sink after mounting a semiconductor device into the printed circuit board, when tightening up a heat sink with the screw, the mechanical stress which is impossible to the semiconductor device and the pin doesn't hang.
- e. When mounting the semiconductor device to the heat sink using jigs, etc.,
 - Take care not to allow the device to ride onto the jig or positioning dowel.
 - Design the jig so that no unreasonable mechanical stress is applied to the semiconductor device.

f. Heat sink screw holes

- Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.
- When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15% larger than the diameter of the screw is desirable.
- When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15% smaller than the diameter of the screw is desirable.
- g. There is a method to mount the semiconductor device to the heat sink by using a spring band. But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.

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