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AUTOMOTIVE, 125°C OPERATION, LOW INPUT OFFSET VOLTAGE CMOS OPERATIONAL AMPLIFIER

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Rev.1.1_00

This IC incorporates a general purpose analog circuit in a small package. This is a zero-drift operational amplifier with Rail-to-Rail input and output, which uses chopper-stabilizing techniques to provide low input offset voltage.
The S-19630AB is a dual operational amplifier (2 circuits), which is suitable for applications requiring less offset voltage.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.**

■ Features

- Low input offset voltage: V_{IO} = +50 µV max. (Ta = –40°C to +125°C)
- Low input offset voltage drift: $\frac{\Delta V_{IO}}{\Delta Ta}$ = ±25 nV/°C typ. (V_{DD} = 30.0 V, Ta = –40°C to +125°C)
- Operation power supply voltage range: V_{DD} = 4.0 V to 36.0 V
- Low current consumption (Per circuit): I_{DD} = 250 µA typ.
- Low input noise voltage: V_{NOISE_pp} = 0.8 µVpp typ. (f = 0.1 Hz to 10 Hz)
- Low input noise voltage density: V_{NOISE} = 25 nV/√Hz typ. (f = 1 kHz)
- Built-in output current limit circuit: Overcurrent limit when output pin is short-circuited
- Internal phase compensation: No external parts required
- Rail-to-Rail input and output
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified*1

***1.** Contact our sales representatives for details.

■ Applications

- High-accuracy current detection
- Various sensor interfaces
- Strain gauge amplifier

■ Package

- TMSOP-8

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■ Block Diagram

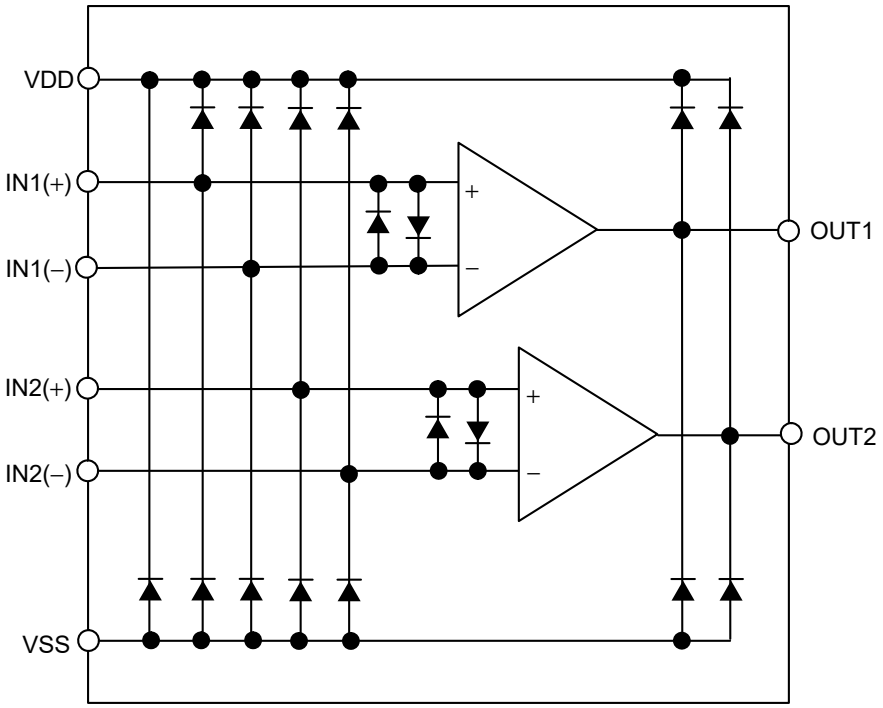


Figure 1

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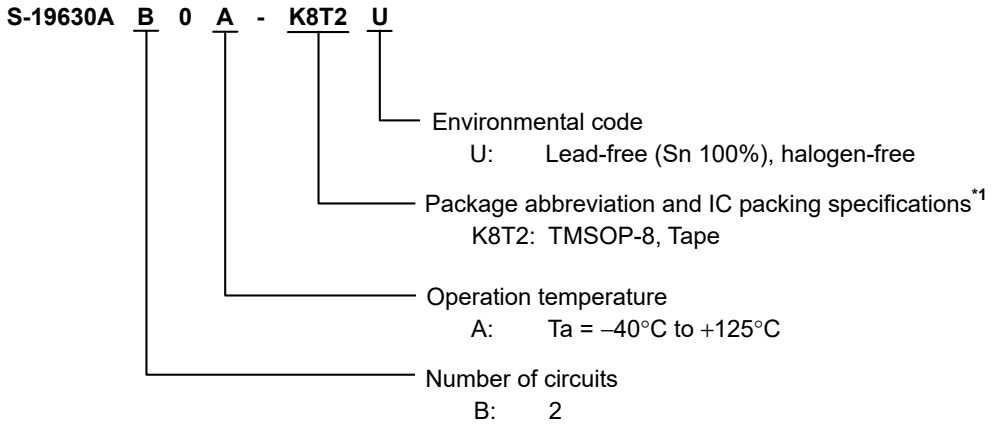
■ AEC-Q100 Qualified

This IC supports AEC-Q100 for the operation temperature grade 1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

Refer to "**1. Product name**" regarding the contents of product name, "**2. Package**" regarding the package drawings and "**3. Product name list**" regarding the product type.

1. Product name



***1.** Refer to the tape drawing.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

3. Product name list

Table 2

Product Name	Package
S-19630AB0A-K8T2U	TMSOP-8

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■ Pin Configuration

1. TMSOP-8

Top view

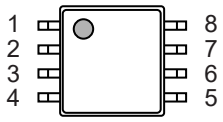


Figure 2

Table 3

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(−)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(−)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

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■ Absolute Maximum Ratings

Table 4

(T_j = –40°C to +150°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	V_{SS} – 0.3 to V_{SS} + 45.0	V
Input voltage	$V_{IN(+)}$, $V_{IN(-)}$	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Differential input voltage	V_{IND}	±0.5	V
Input pin current	I_{IN}	±10.0	mA
Junction temperature	T_j	–40 to +150	°C
Operation ambient temperature	T_{opr}	–40 to +125	°C
Storage temperature	T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TMSOP-8	Board A	–	160	–	°C/W
			Board B	–	133	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

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■ Electrical Characteristics

1. Recommended operation conditions

Table 6

(Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation power supply voltage range	V_{DD}	–	4.0	–	36.0	V	–

2. V_{DD} = 5.0 V

Table 7

DC Electrical Characteristics (Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (2 circuits)	I_{DD}	$V_{CMR} = V_{OUT} = \frac{V_{DD}}{2}$	–	500	760	µA	5
Input offset voltage	V_{IO}	$V_{CMR} = \frac{V_{DD}}{2}$	–50	±10	+50	µV	1
Input offset voltage drift	$\frac{\Delta V_{IO}}{\Delta Ta}$	$V_{CMR} = \frac{V_{DD}}{2}$	–125	±30	+125	nV/°C	1
Input bias current	I_{BIAS}	–	–	3	10	nA	9,10
Input offset current	I_{IO}	–	–	3	10	nA	9,10
Common-mode input voltage range	V_{CMR}	–	V_{SS}	–	V_{DD}	V	2
Voltage gain (open loop)	A_{VOL}	$V_{SS} + 0.5\ V \le V_{OUT} \le V_{DD} - 0.5\ V$, $V_{CMR} = \frac{V_{DD}}{2}$, R_L = 10 kΩ	93	110	–	dB	8
Maximum output swing voltage	V_{OH}	I_{SOURCE} = 100 µA	4.9	–	–	V	3
		I_{SOURCE} = 1 mA	4.7	–	–	V	3
	V_{OL}	I_{SINK} = 100 µA	–	–	0.1	V	4
		I_{SINK} = 1 mA	–	–	0.3	V	4
Common-mode input signal rejection ratio	CMRR	$V_{SS} \le V_{CMR} \le V_{DD}$	93	110	–	dB	2
Power supply voltage rejection ratio	PSRR	4.0 V ≤ V_{DD} ≤ 36.0 V	116	130	–	dB	1
Source current	I_{SOURCE}	$V_{OUT} = V_{DD} - 0.1$ V	0.40	0.60	–	mA	6
Sink current	I_{SINK}	V_{OUT} = 0.1 V	0.25	0.50	–	mA	7
Output pin short-circuit current (source)	I_{SHORT_SOURCE}	V_{OUT} = 0 V	–	16.0	–	mA	–
Output pin short-circuit current (sink)	I_{SHORT_SINK}	$V_{OUT} = V_{DD}$	–	15.0	–	mA	–

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Table 8

AC Electrical Characteristics (Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L = 1.0 MΩ, C_L = 15 pF (Refer to **Figure 13** and **Figure 14**), $V_{IN(+)}$ = 1.5 V ↔ 3.5 V	–	0.45	–	V/µs
Gain-bandwidth product	GBP	C_L = 0 pF	–	1.2	–	MHz
Maximum load capacitance	C_L	–	–	470	–	pF
Input noise voltage	V_{NOISE_pp}	f = 0.1 Hz to 10 Hz	–	0.8	–	µVpp
Input noise voltage density	V_{NOISE}	f = 1 kHz	–	25	–	nV/√Hz

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3. V_{DD} = 30.0 V

Table 9

DC Electrical Characteristics (Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (2 circuits)	I_{DD}	$V_{CMR} = V_{OUT} = \frac{V_{DD}}{2}$	–	500	760	µA	5
Input offset voltage	V_{IO}	$V_{CMR} = \frac{V_{DD}}{2}$	–50	±10	+50	µV	1
Input offset voltage drift	$\frac{\Delta V_{IO}}{\Delta Ta}$	$V_{CMR} = \frac{V_{DD}}{2}$	–120	±25	+120	nV/°C	1
Input bias current	I_{BIAS}	–	–	3	10	nA	9,10
Input offset current	I_{IO}	–	–	3	10	nA	9,10
Common-mode input voltage range	V_{CMR}	–	V_{SS}	–	V_{DD}	V	2
Voltage gain (open loop)	A_{VOL}	$V_{SS} + 0.5\ V \le V_{OUT} \le V_{DD} - 0.5\ V$, $V_{CMR} = \frac{V_{DD}}{2}$, R_L = 10 kΩ	106	120	–	dB	8
Maximum output swing voltage	V_{OH}	I_{SOURCE} = 100 µA	29.9	–	–	V	3
		I_{SOURCE} = 1 mA	29.7	–	–	V	3
	V_{OL}	I_{SINK} = 100 µA	–	–	0.1	V	4
		I_{SINK} = 1 mA	–	–	0.3	V	4
Common-mode input signal rejection ratio	CMRR	$V_{SS} \le V_{CMR} \le V_{DD}$	106	120	–	dB	2
Power supply voltage rejection ratio	PSRR	4.0 V ≤ V_{DD} ≤ 36.0 V	116	130	–	dB	1
Source current	I_{SOURCE}	$V_{OUT} = V_{DD} - 0.1$ V	0.40	0.60	–	mA	6
Sink current	I_{SINK}	V_{OUT} = 0.1 V	0.25	0.50	–	mA	7
Output pin short-circuit current (source)	I_{SHORT_SOURCE}	V_{OUT} = 0 V	–	16.0	–	mA	–
Output pin short-circuit current (sink)	I_{SHORT_SINK}	$V_{OUT} = V_{DD}$	–	15.0	–	mA	–

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Table 10

AC Electrical Characteristics (Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L = 1.0 MΩ, C_L = 15 pF (Refer to **Figure 13** and **Figure 14**), $V_{IN(+)}$ = 14.0 V ↔ 16.0 V	–	0.45	–	V/µs
Gain-bandwidth product	GBP	C_L = 0 pF	–	1.2	–	MHz
Maximum load capacitance	C_L	–	–	470	–	pF
Input noise voltage	V_{NOISE_pp}	f = 0.1 Hz to 10 Hz	–	0.8	–	µVpp
Input noise voltage density	V_{NOISE}	f = 1 kHz	–	25	–	nV/√Hz

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■ Test Circuits (Per circuit)

1. Power supply voltage rejection ratio, input offset voltage, input offset voltage drift

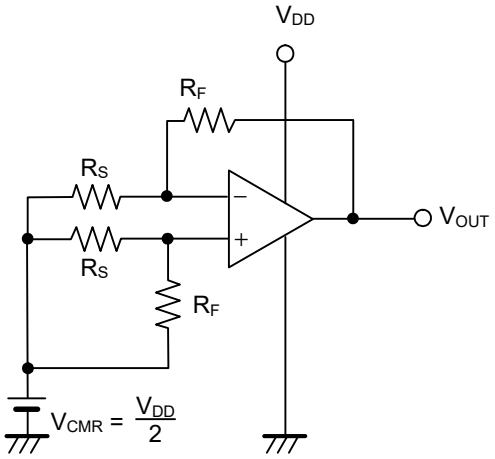


Figure 3 Test Circuit 1

- **Power supply voltage rejection ratio (PSRR)**

The power supply voltage rejection ratio (PSRR) can be calculated by the following expression, with V_{OUT} measured at each V_{DD}.

Test conditions:
V_{DD} = 4.0 V: $V_{DD} = V_{DD1}$, $V_{OUT} = V_{OUT1}$
V_{DD} = 36.0 V: $V_{DD} = V_{DD2}$, $V_{OUT} = V_{OUT2}$

$$PSRR = 20 \log \left(\left| \frac{V_{DD1} - V_{DD2}}{\left(V_{OUT1} - \frac{V_{DD1}}{2}\right) - \left(V_{OUT2} - \frac{V_{DD2}}{2}\right)} \right| \times \frac{R_F + R_S}{R_S} \right)$$

- **Input offset voltage (V_{IO})**

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

- **Input offset voltage drift $\left(\frac{\Delta V_{IO}}{\Delta Ta}\right)$**

The input offset voltage drift $\left(\frac{\Delta V_{IO}}{\Delta Ta}\right)$ can be calculated by the following expression, with V_{OUT} measured at each temperature.

Test conditions:
Ta = –40°C: $V_{IO} = V_{IO1}$
Ta = +125°C: $V_{IO} = V_{IO2}$

$$\frac{\Delta V_{IO}}{\Delta Ta} = \frac{V_{IO2} - V_{IO1}}{+125°C - (-40°C)}$$

2. Common-mode input signal rejection ratio, common-mode input voltage range

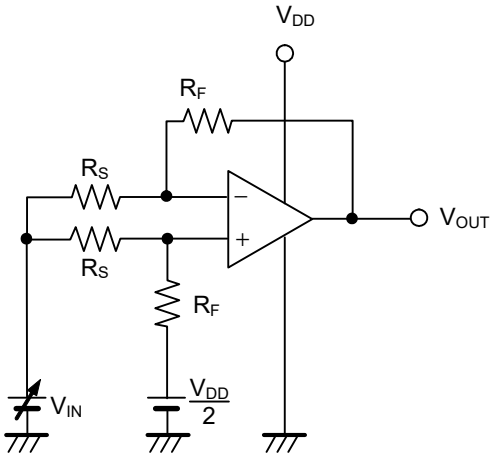


Figure 4 Test Circuit 2

- **Common-mode input signal rejection ratio (CMRR)**

The common-mode input signal rejection ratio (CMRR) can be calculated by the following expression, with V_{OUT} measured at each V_{IN}.

Test conditions:
$V_{IN} = V_{CMR\ Max.}$: $V_{IN} = V_{IN1}$, $V_{OUT} = V_{OUT1}$
$V_{IN} = V_{CMR\ Min.}$: $V_{IN} = V_{IN2}$, $V_{OUT} = V_{OUT2}$

$$CMRR = 20 \log \left(\left| \frac{V_{IN1} - V_{IN2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

- **Common-mode input voltage range (V_{CMR})**

The common-mode input voltage range is the range of V_{IN} in which V_{OUT} satisfies the common-mode input signal rejection ratio specifications when V_{IN} is changed.

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3. Maximum output swing voltage

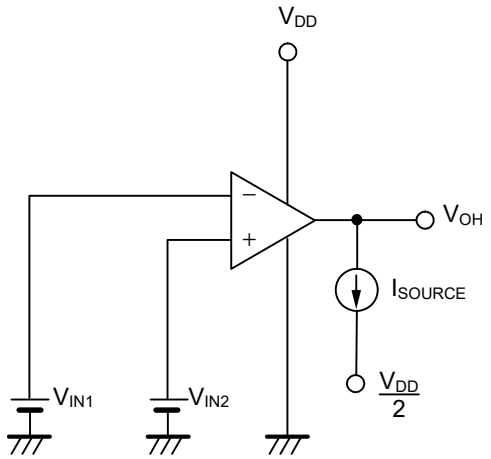


Figure 5 Test Circuit 3

- **Maximum output swing voltage (V_{OH})**

  Test conditions:

  $V_{IN1} = \frac{V_{DD}}{2} - 0.1$ V

  $V_{IN2} = \frac{V_{DD}}{2} + 0.1$ V

  I_{SOURCE} = 100 µA, 1 mA

4. Maximum output swing voltage

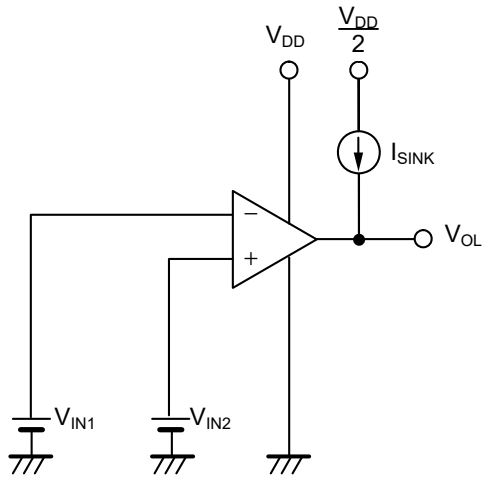


Figure 6 Test Circuit 4

- **Maximum output swing voltage (V_{OL})**

  Test conditions:

  $V_{IN1} = \frac{V_{DD}}{2} + 0.1$ V

  $V_{IN2} = \frac{V_{DD}}{2} - 0.1$ V

  I_{SINK} = 100 µA, 1 mA

5. Current consumption

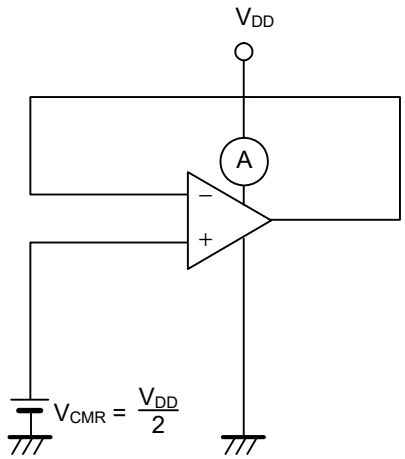


Figure 7 Test Circuit 5

- **Current consumption (I_{DD})**

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6. Source current

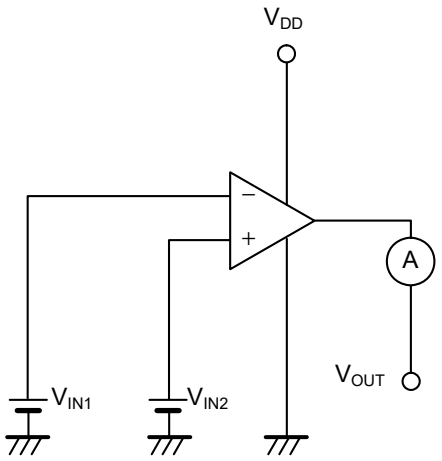


Figure 8 Test Circuit 6

- **Source current (I_{SOURCE})**

Test conditions:

$V_{OUT} = V_{DD} - 0.1$ V

$V_{IN1} = \frac{V_{DD}}{2} - 0.1$ V

$V_{IN2} = \frac{V_{DD}}{2} + 0.1$ V

7. Sink current

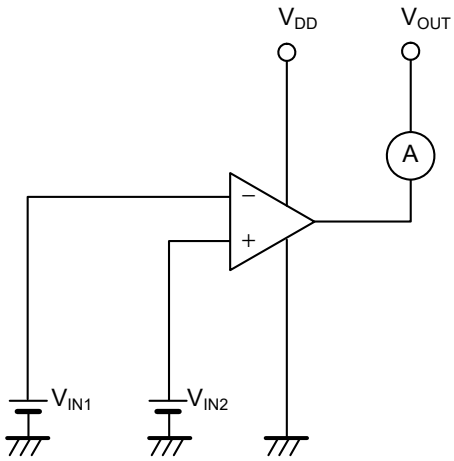


Figure 9 Test Circuit 7

- **Sink current (I_{SINK})**

Test conditions:

$V_{OUT} = 0.1$ V

$V_{IN1} = \frac{V_{DD}}{2} + 0.1$ V

$V_{IN2} = \frac{V_{DD}}{2} - 0.1$ V

8. Voltage gain

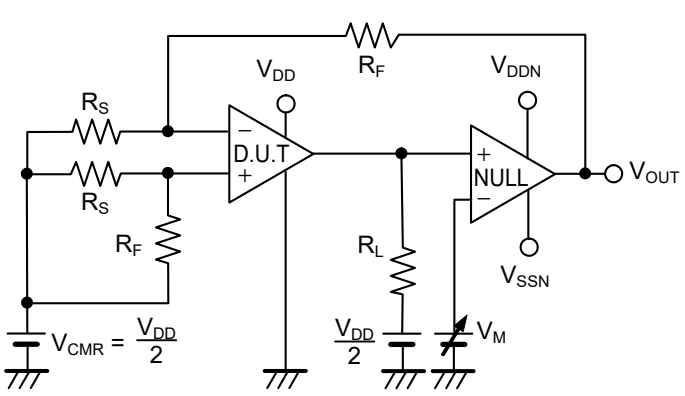


Figure 10 Test Circuit 8

- **Voltage gain (open loop) (A_{VOL})**

The voltage gain (A_{VOL}) can be calculated by the following expression, with V_{OUT} measured at each V_M.

Test conditions:

$V_M = V_{DD} - 0.5$ V: $V_M = V_{M1}$, $V_{OUT} = V_{OUT1}$

$V_M = V_{SS} + 0.5$ V: $V_M = V_{M2}$, $V_{OUT} = V_{OUT2}$

$$A_{VOL} = 20 \log \left(\left| \frac{V_{M1} - V_{M2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

$R_L = 10$ kΩ

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9. Input bias current, input offset current

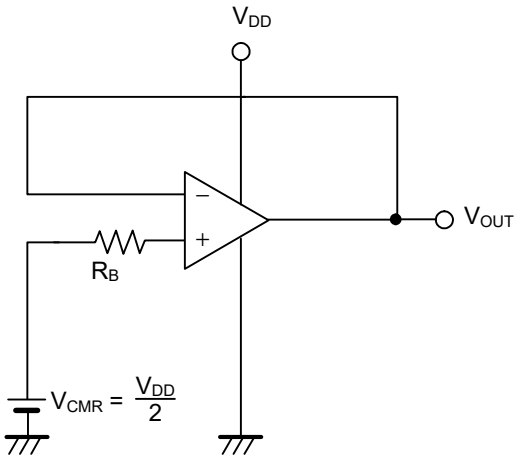


Figure 11 Test Circuit 9

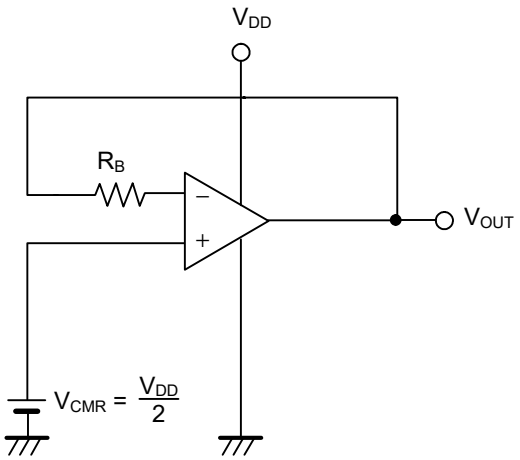


Figure 12 Test Circuit 10

・Input bias current (I_{BIAS})

Test conditions:

$$\text{IN(+) pin input bias current } (I_{BIAS(+)}) = \frac{-1 \times (V_{OUT} - \frac{V_{DD}}{2})}{R_B}$$

$$\text{IN(−) pin input bias current } (I_{BIAS(-)}) = \frac{V_{OUT} - \frac{V_{DD}}{2}}{R_B}$$

$$I_{BIAS} = \frac{|I_{BIAS(+)} + I_{BIAS(-)}|}{2}$$

・Input offset current (I_{IO})

$$I_{IO} = |I_{BIAS(-)} - I_{BIAS(+)}|$$

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10. Slew rate

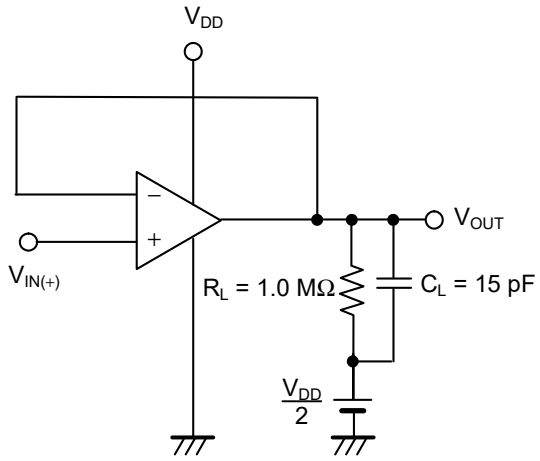


Figure 13 Test Circuit 11

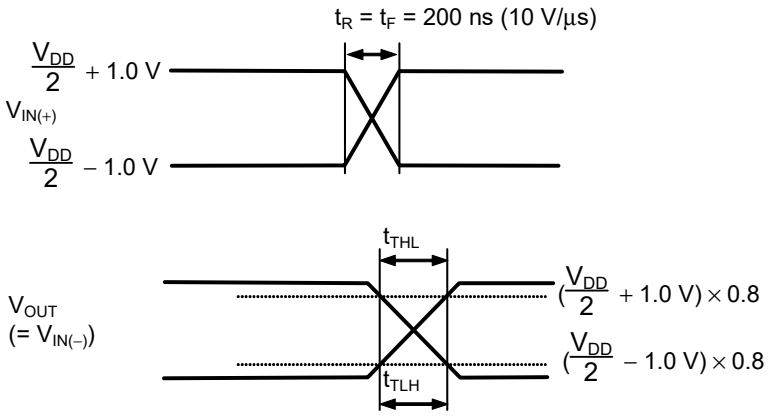


Figure 14

- **Slew rate (SR)**

When falling

$$SR = \frac{1.6\ V}{t_{THL}}$$

When rising

$$SR = \frac{1.6\ V}{t_{TLH}}$$

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■ Precautions

- Generally an operational amplifier may cause oscillation depending on the selection of external parts. Perform thorough evaluation using the actual application to set the constants.
- Do not apply an electrostatic discharge to this IC that exceeds performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.
- This IC operates stably even directly connecting a load capacitance of 470 pF or less to the output pin, as shown in **Figure 15**. When connecting a load capacitance of 470 pF or more, connect a resistor of 100 Ω or more as shown in **Figure 16**. In case of connecting a filter for noise prevention, and connecting a load capacitance of 470 pF or more, also connect a resistor of 100 Ω or more as shown in **Figure 17**.

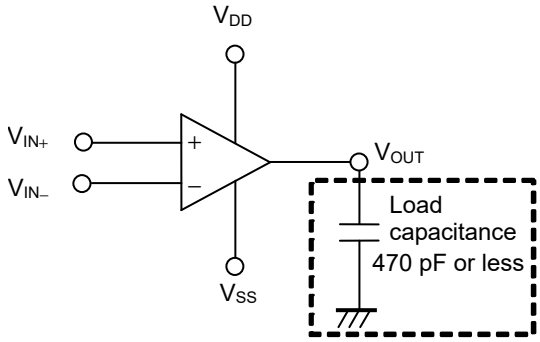


Figure 15

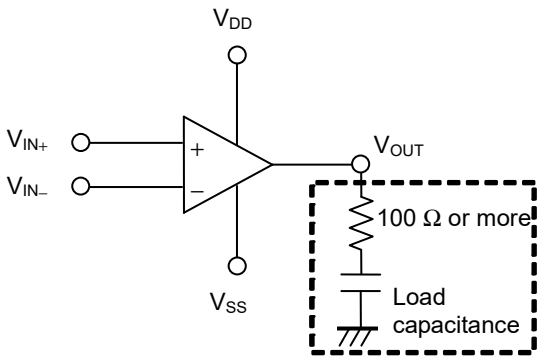


Figure 16

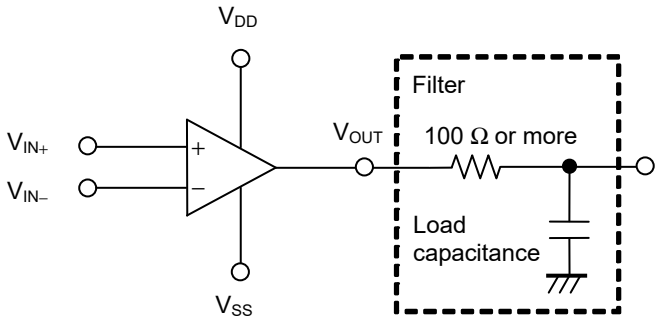


Figure 17

Caution **The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.**

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■ Precaution for use

1. Methods for protection against application of overvoltage to input pin

ESD protection elements are connected to the input pins as shown in **Figure 1**. If the input voltage (V_{IN}) exceeds the V_{IN} absolute maximum rating V_{DD} + 0.3 V, there is a risk of the input pin current which flows through the ESD protection element exceeding ±10.0 mA (the absolute maximum rating). In this case, connect a current limiting resistor (R_{LIMT}) to the input pin as shown in **Figure 18** to limit the input pin current to less than ±10.0 mA.
However, error voltage and noise generate as a result of input bias current and input offset current. Select the lowest possible resistance when connecting the R_{LIMT}.

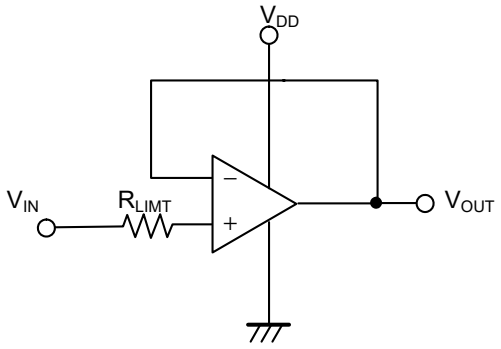


Figure 18

2. Input voltage range (input crossover distortion)

This IC has two sets of differential circuits in order to achieve the Rail-to-Rail input voltage range. The differential circuits used switch based on the common-mode input voltage range (V_{CMR}). Differences in the characteristics of the two sets of differential circuits result in the generation of distortion of the output voltage which is referred to as "input crossover distortion" when the differential circuits switch.
The differential circuit switching voltage of this IC is approximately between V_{DD} – 2.2 V and V_{DD} – 1.2 V. When using this IC in applications which require high-accuracy measurement, avoid the range near the differential circuit switching voltage in order to avoid changes in input offset voltage caused by input crossover distortion and changes in input offset voltage drift.
This IC is a chopper-stabilized zero-drift amplifier; therefore, it always cancels input offset voltage. For this reason, the input crossover distortion is kept extremely small when compared to standard operational amplifiers. However, please contact our sales representatives when using this IC near the differential circuit switching voltage.
Refer to "**8. Input offset voltage (V_{IO}) vs. Common-mode input voltage range (V_{CMR})**" in "**■ Characteristics (Typical Data)**".

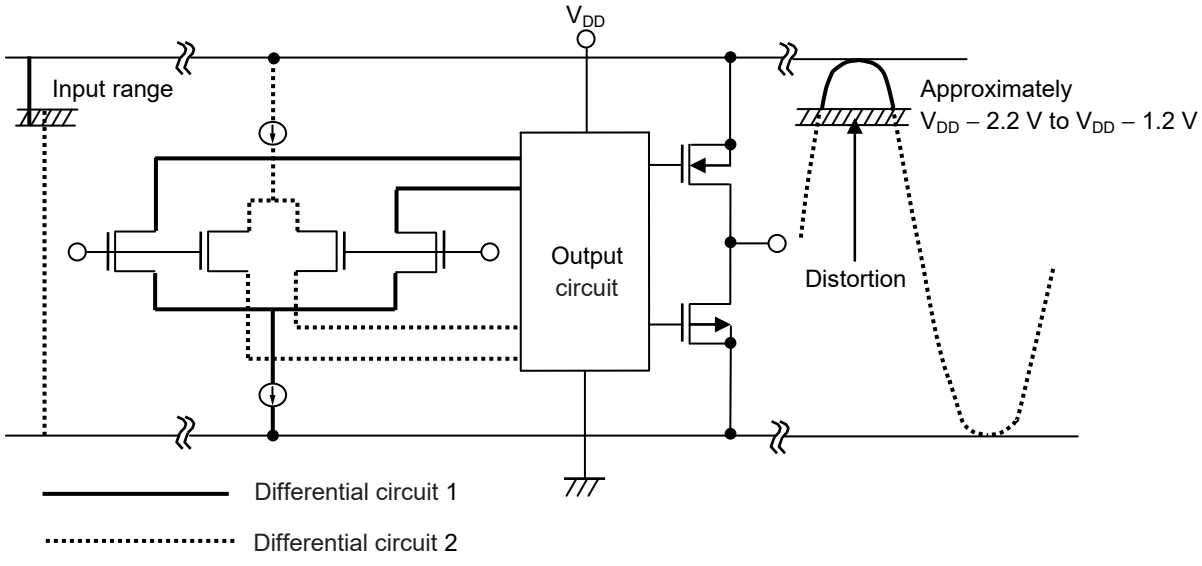


Figure 19

Downloaded from Arrow.com.

3. Recommended processing methods for unused circuit

When using only a single circuit of this IC, it is recommended that the unused circuit be connected as shown in **Figure 20**. Set the non-inverted input pin voltage ($V_{IN(+)}$) within the common-mode input voltage range (V_{CMR}).

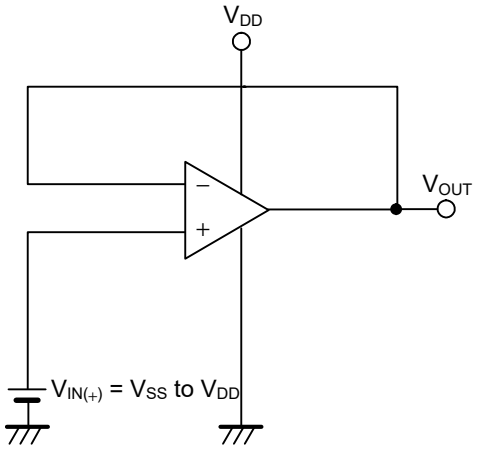
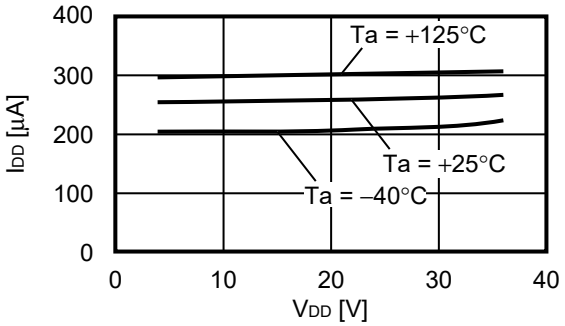


Figure 20

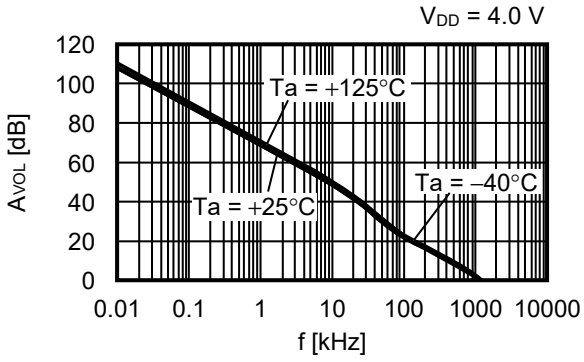
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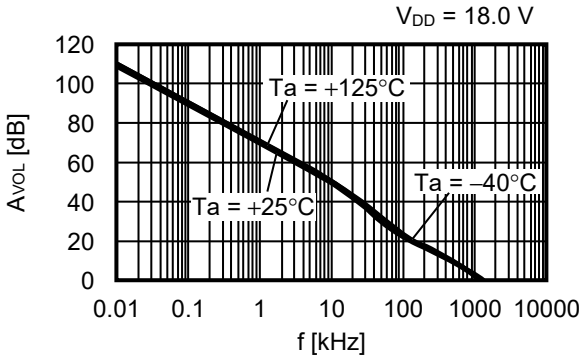
■ Characteristics (Typical Data)

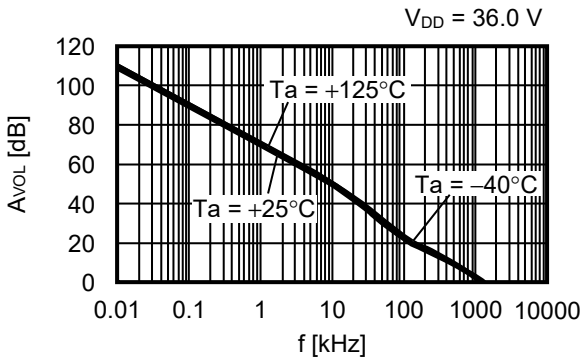
1. Current consumption (I_{DD}) (Per circuit) vs. Power supply voltage (V_{DD})



2. Voltage gain (A_{VOL}) vs. Frequency (f)



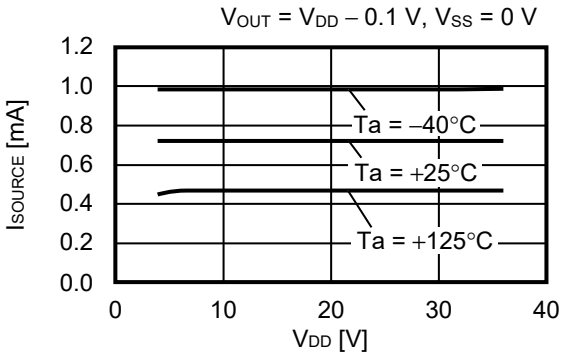


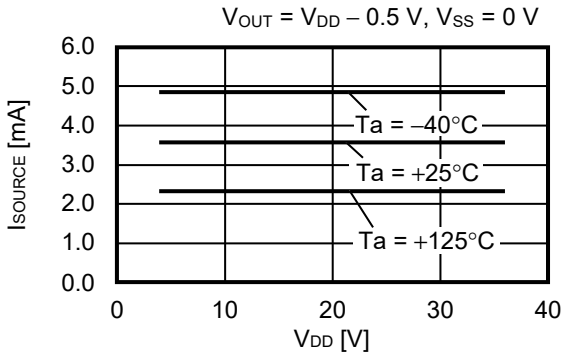


Downloaded from Arrow.com.

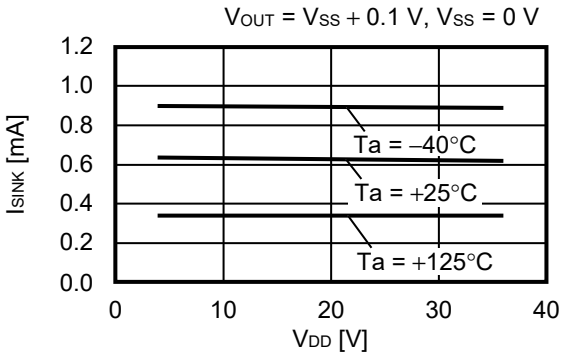
3. Output current

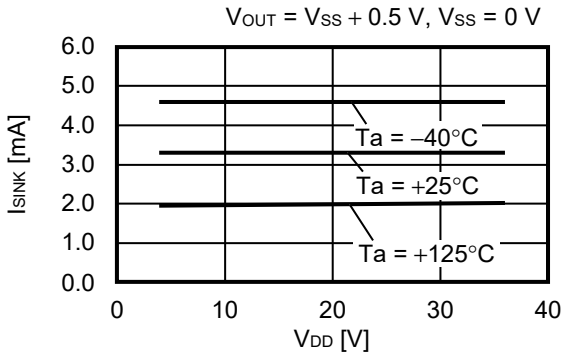
3. 1 Source current (I_{SOURCE}) vs. Power supply voltage (V_{DD})



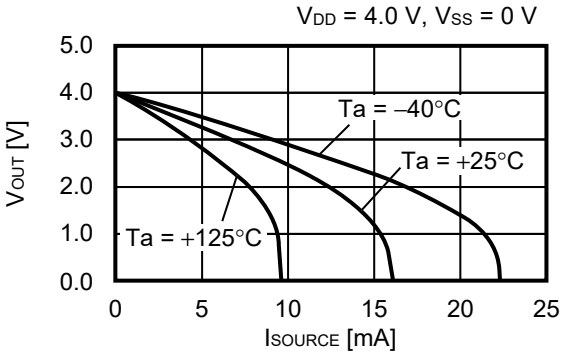


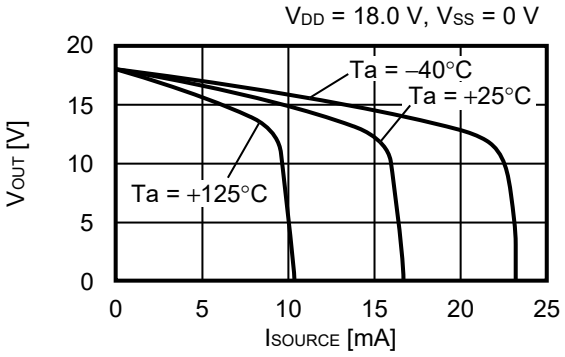
3. 2 Sink current (I_{SINK}) vs. Power supply voltage (V_{DD})

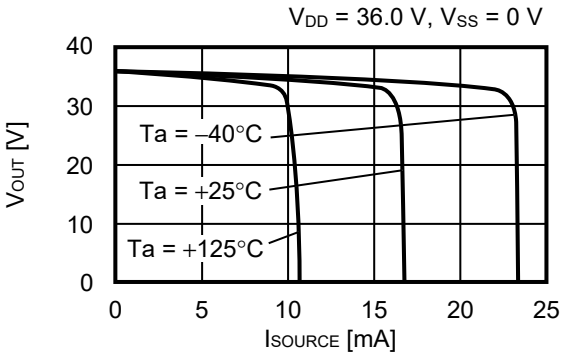




3. 3 Output voltage (V_{OUT}) vs. Source current (I_{SOURCE})

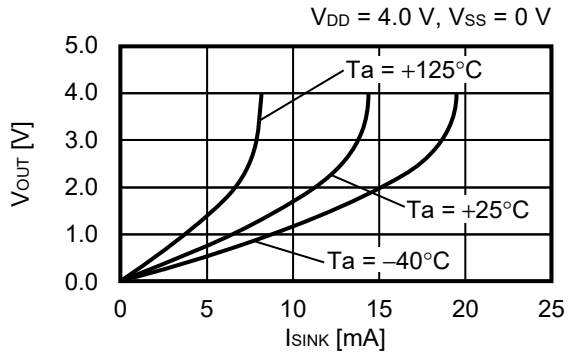


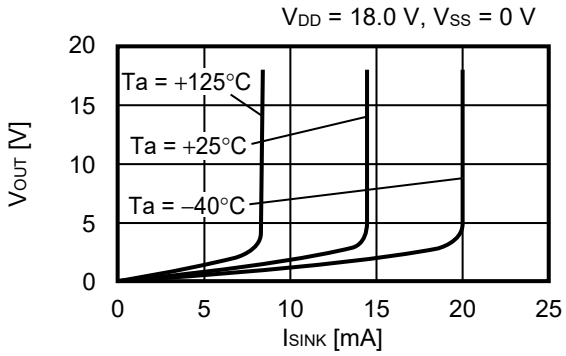


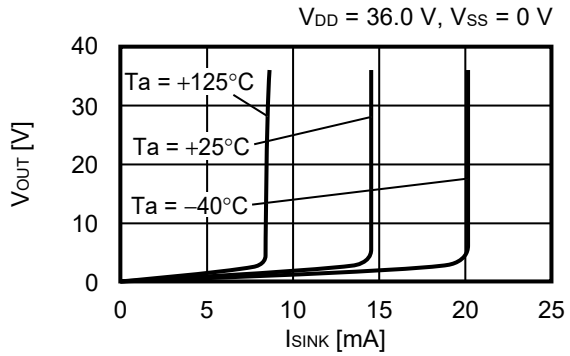


Downloaded from Arrow.com.

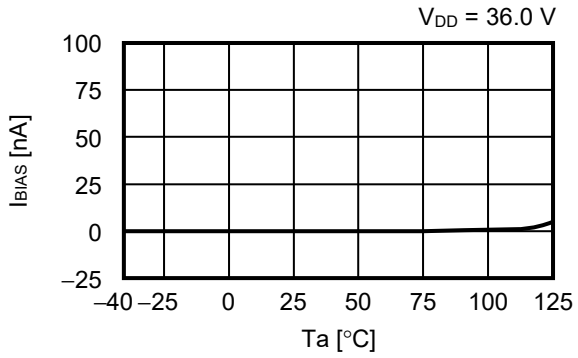
3. 4 Output voltage (V_{OUT}) vs. Sink current (I_{SINK})





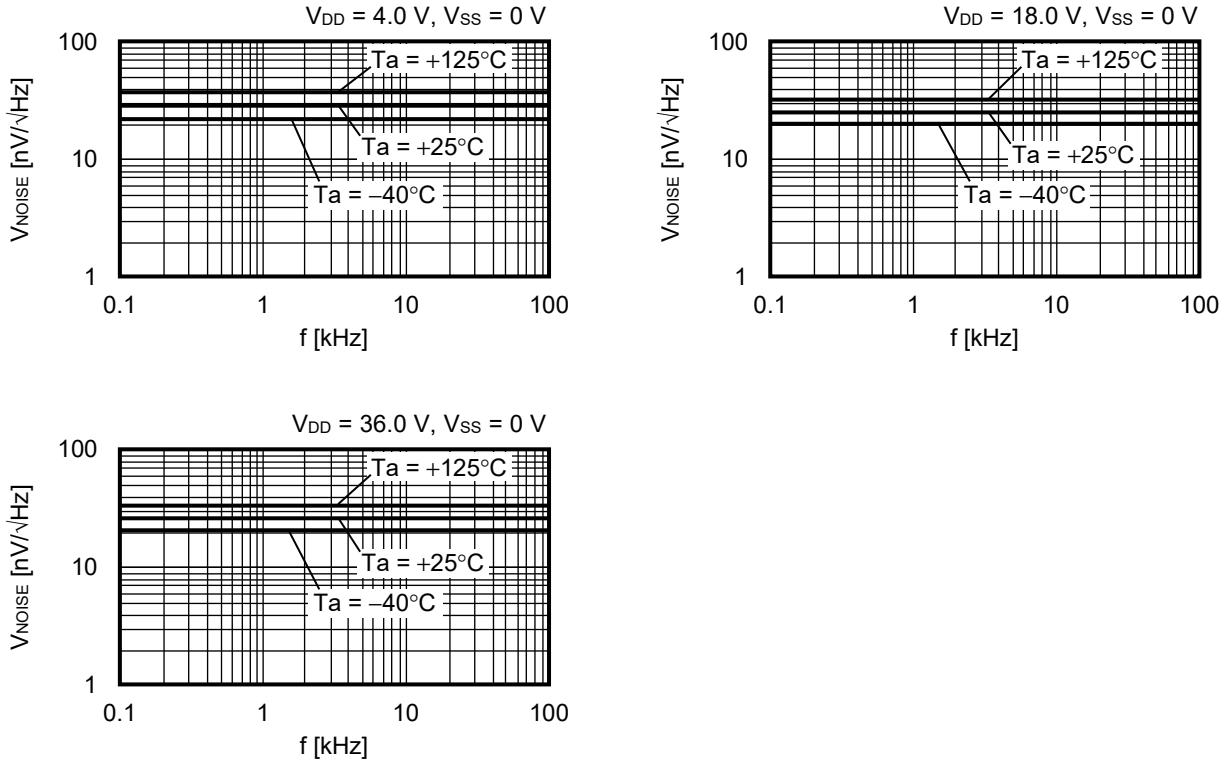


4. Input bias current (I_{BIAS}) vs. Temperature (Ta)

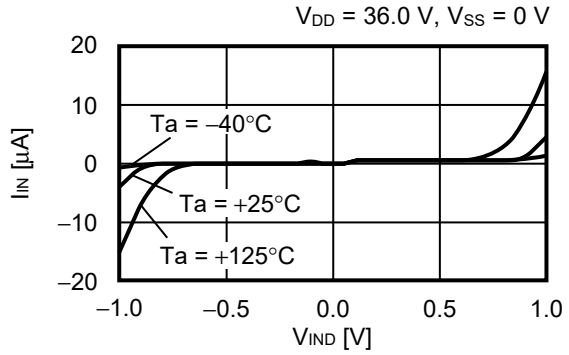


Downloaded from Arrow.com.

5. Input noise voltage density (V_{NOISE}) vs. Frequency (f)

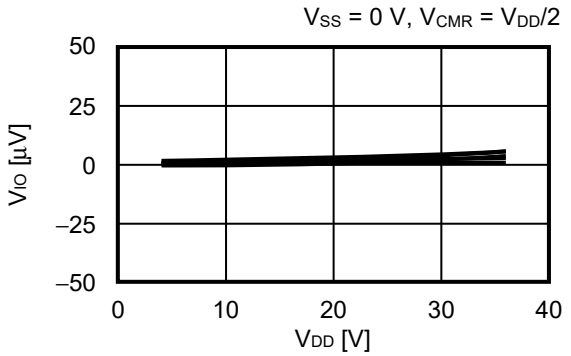


6. Input pin current (I_{IN}) vs. Differential input voltage (V_{IND})



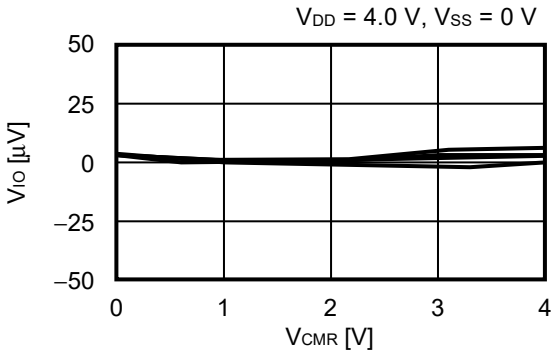
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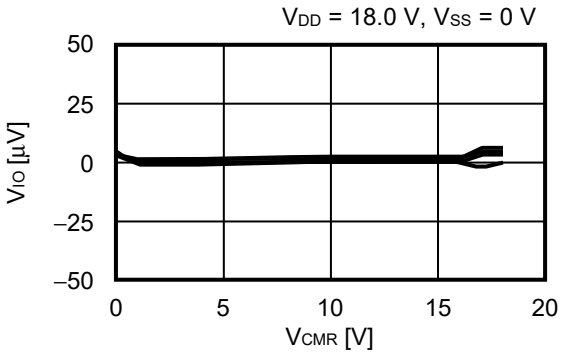
7. Input offset voltage (V_{IO}) vs. Power supply voltage (V_{DD})

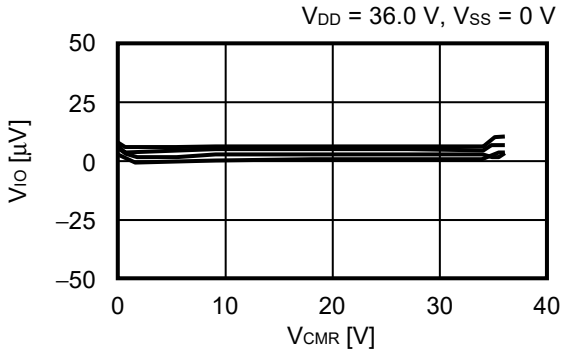


Remark Measured six samples

8. Input offset voltage (V_{IO}) vs. Common-mode input voltage range (V_{CMR})



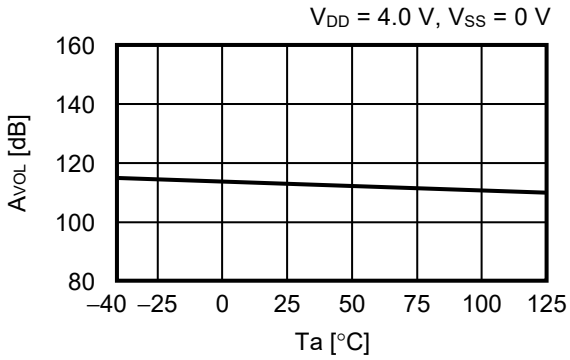


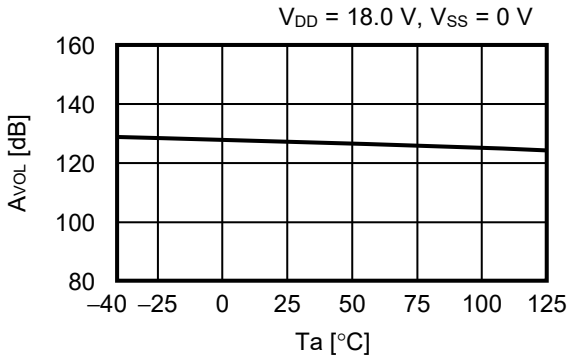


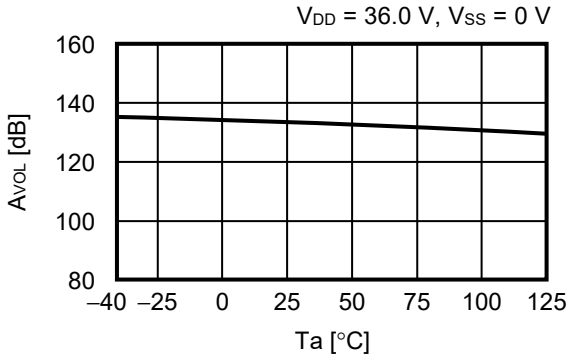
Remark Measured four samples

Downloaded from Arrow.com.

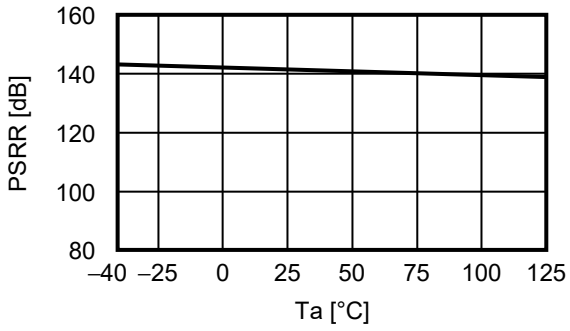
9. Voltage gain (open loop) (A_{VOL}) vs. Temperature (Ta)





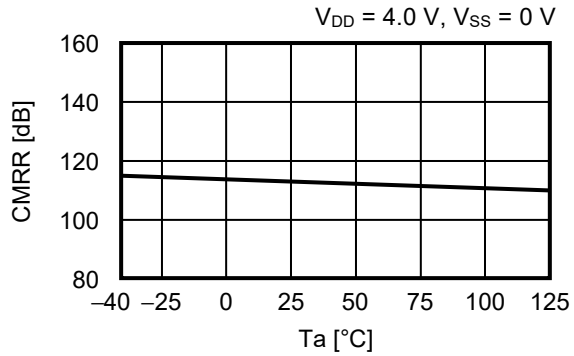


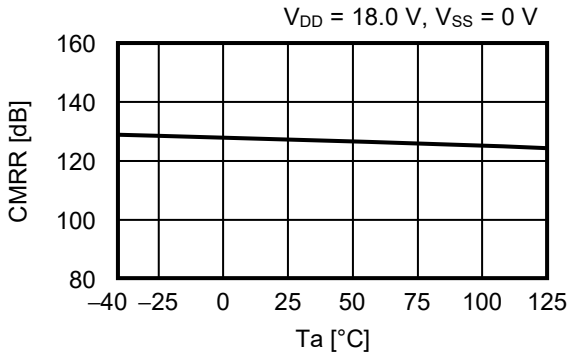
10. Power supply voltage rejection ratio (PSRR) vs. Temperature (Ta)

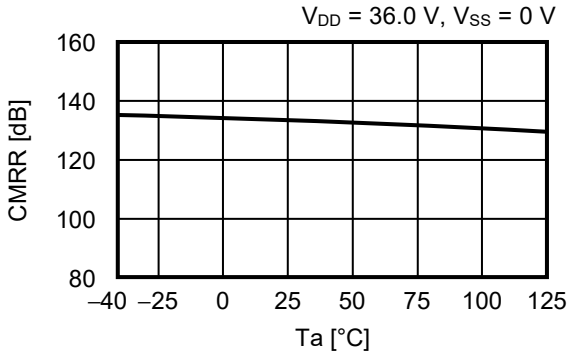


Downloaded from Arrow.com.

11. Common-mode input signal rejection ratio (CMRR) vs. Temperature (Ta)





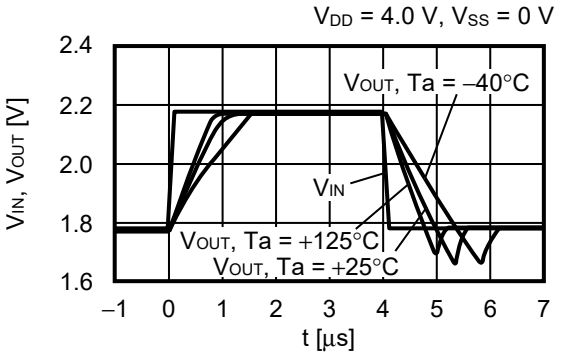


Downloaded from Arrow.com.

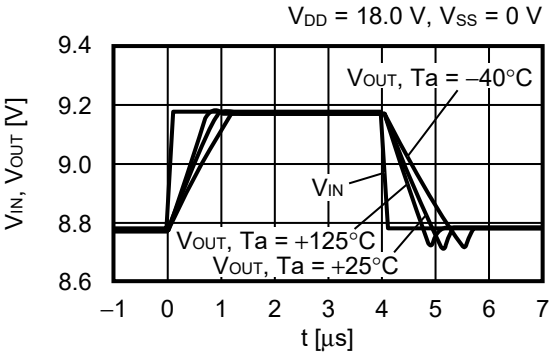
12. Step response (Slew rate)

12. 1 Input signal width (0.4 V)

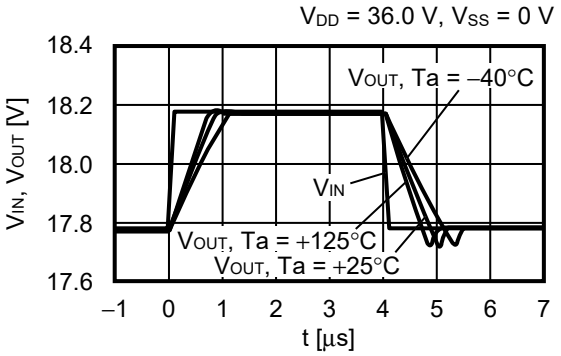
12. 1. 1 $V_{IN(+)}$ = 1.8 V ↔ 2.2 V



12. 1. 2 $V_{IN(+)}$ = 8.8 V ↔ 9.2 V



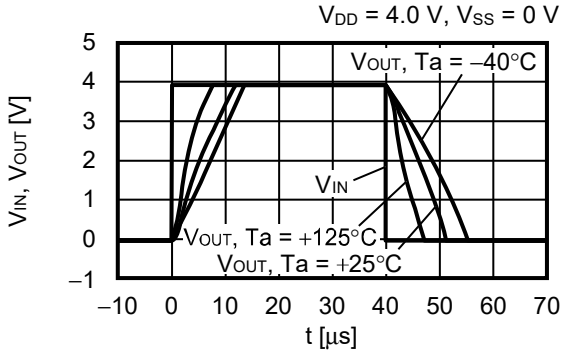
12. 1. 3 $V_{IN(+)}$ = 17.8 V ↔ 18.2 V



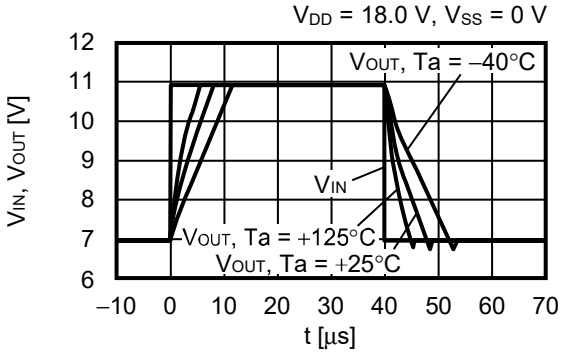
Downloaded from Arrow.com.

12. 2 Input signal width (4.0 V)

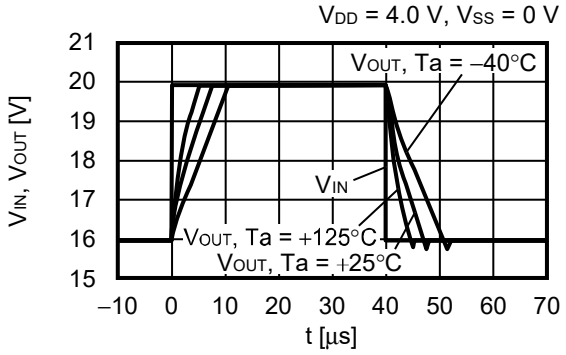
12. 2. 1 $V_{IN(+)}$ = 0 V ↔ 4.0 V



12. 2. 2 $V_{IN(+)}$ = 7.0 V ↔ 11.0 V

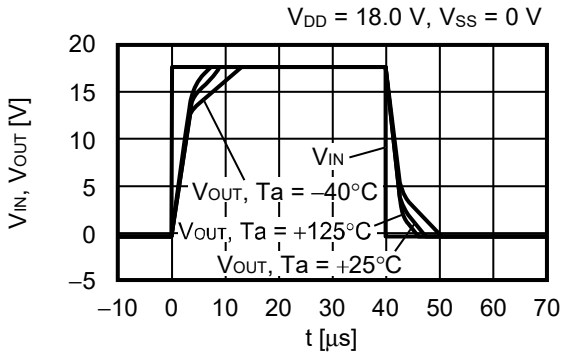


12. 2. 3 $V_{IN(+)}$ = 16.0 V ↔ 20.0 V

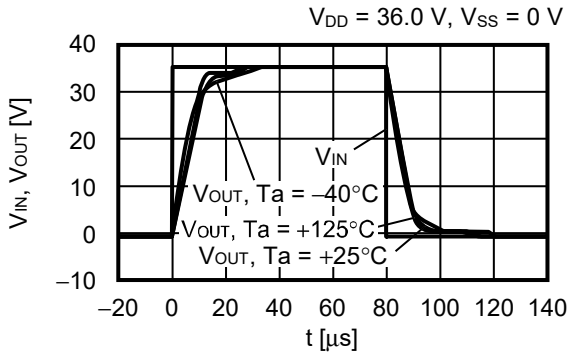


12. 3 Input signal width (V_{SS} ↔ V_{DD})

12. 3. 1 $V_{IN(+)}$ = 0 V ↔ 18.0 V



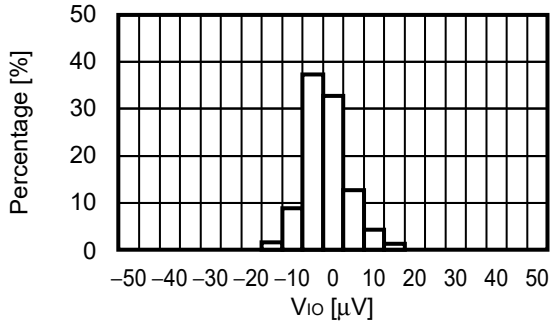
12. 3. 2 $V_{IN(+)}$ = 0 V ↔ 36.0 V



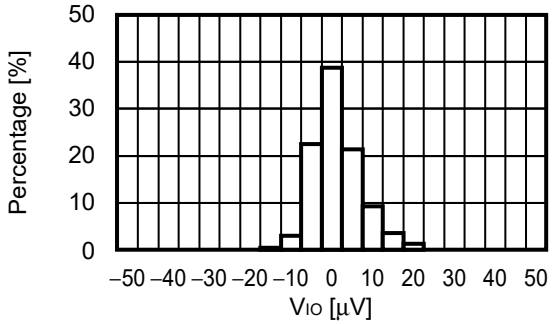
Downloaded from Arrow.com.

13. Input offset voltage distribution

V_{DD} = 5.0 V, V_{SS} = 0 V, Ta = +25°C

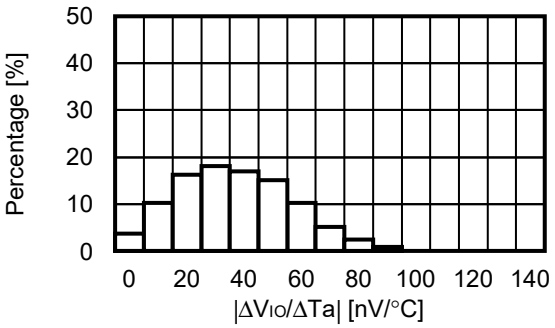


V_{DD} = 30.0 V, V_{SS} = 0 V, Ta = +25°C

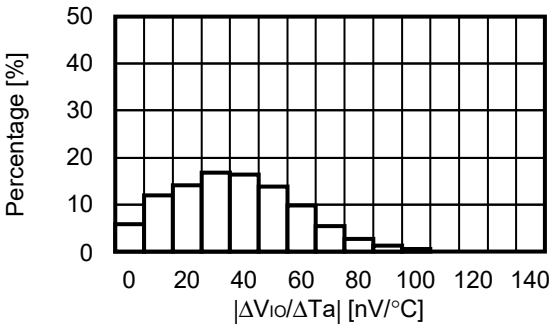


14. Input offset voltage drift distribution

V_{DD} = 5.0 V, V_{SS} = 0 V, Ta = –40°C to +125°C



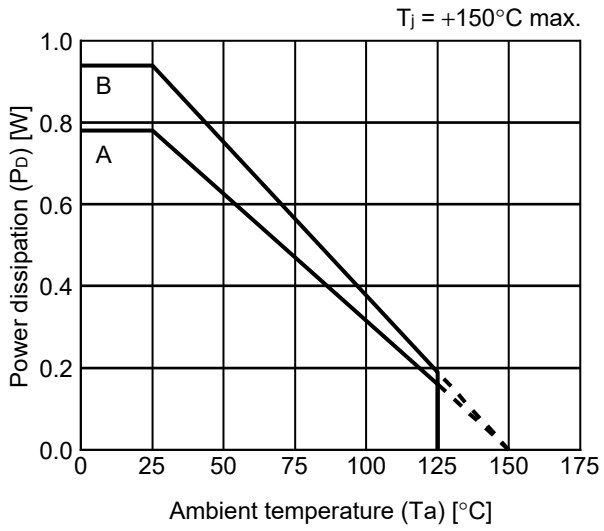
V_{DD} = 30.0 V, V_{SS} = 0 V, Ta = –40°C to +125°C



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■ Power Dissipation

TMSOP-8



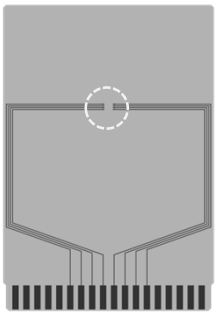
Board	Power Dissipation (P_D)
A	0.78 W
B	0.94 W
C	–
D	–
E	–

Downloaded from Arrow.com.

TMSOP-8 Test Board

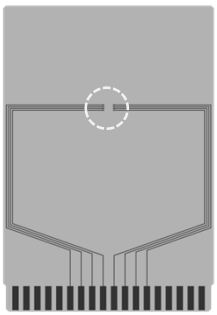
(1) Board A

IC Mount Area



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

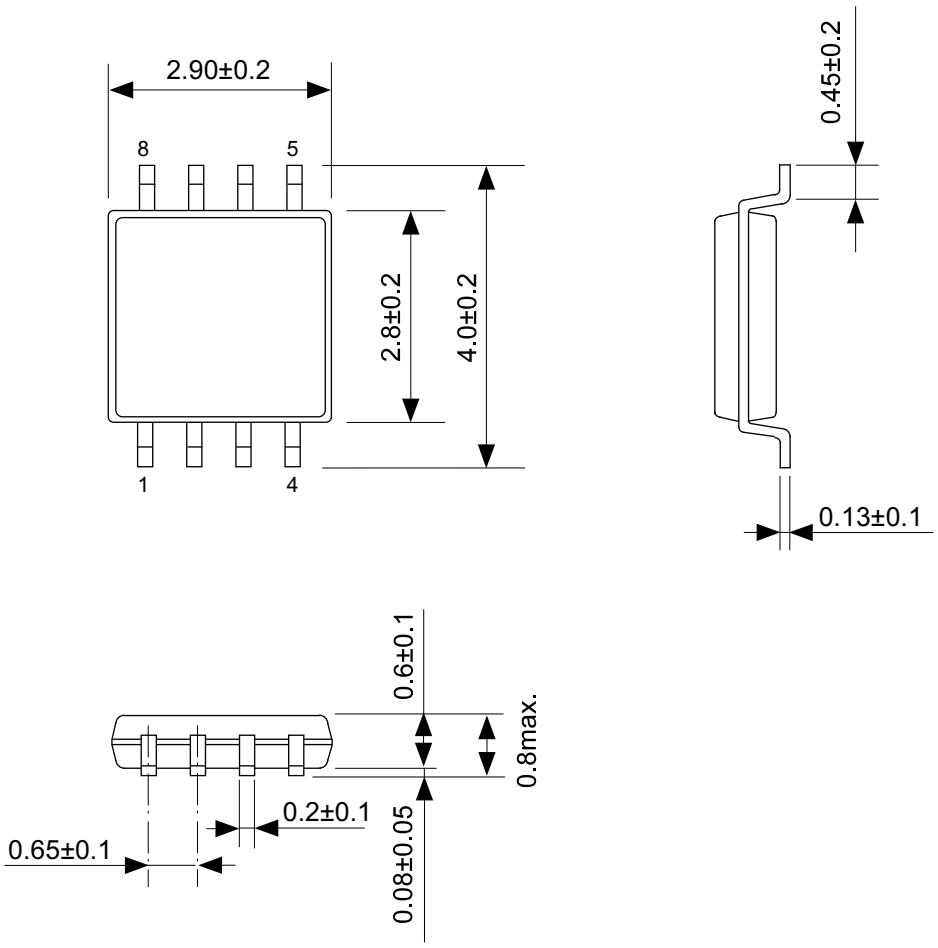
(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. TMSOP8-A-Board-SD-1.0

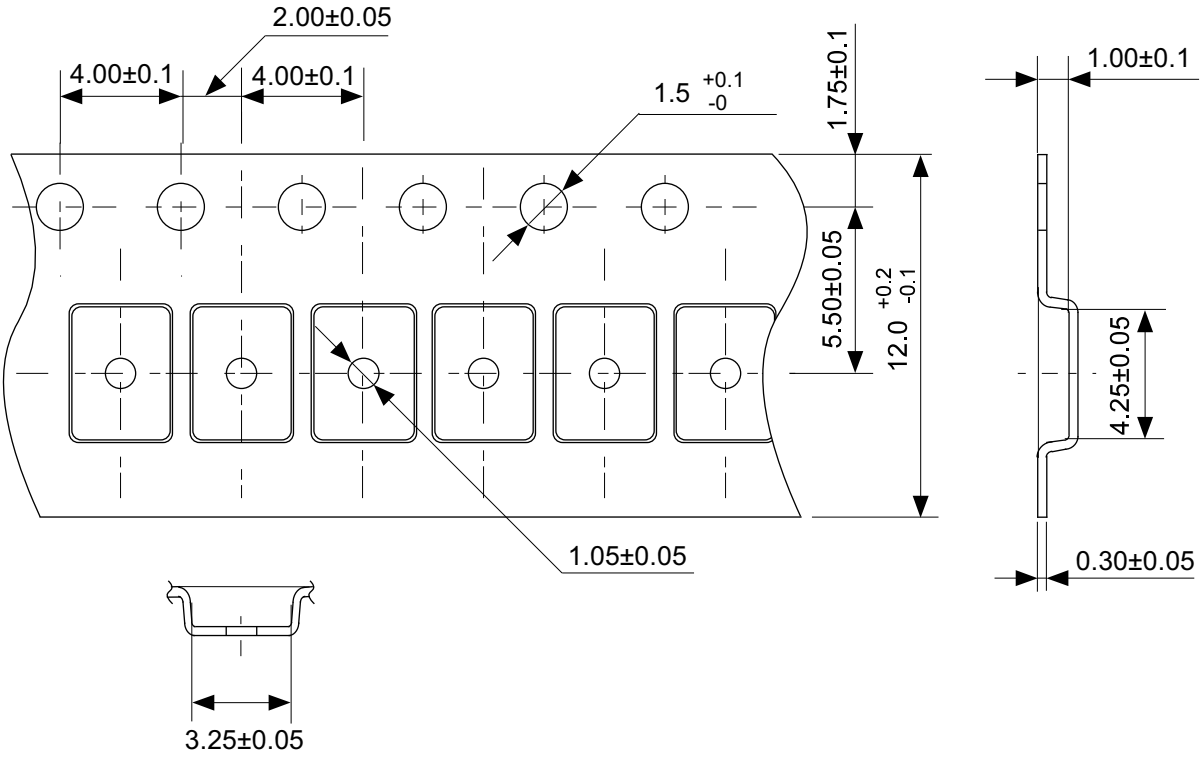
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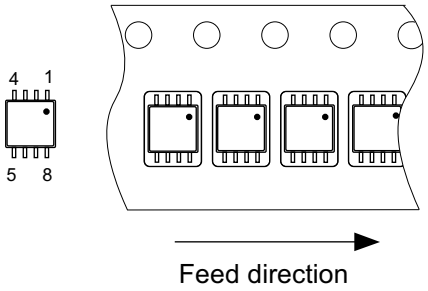


No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	

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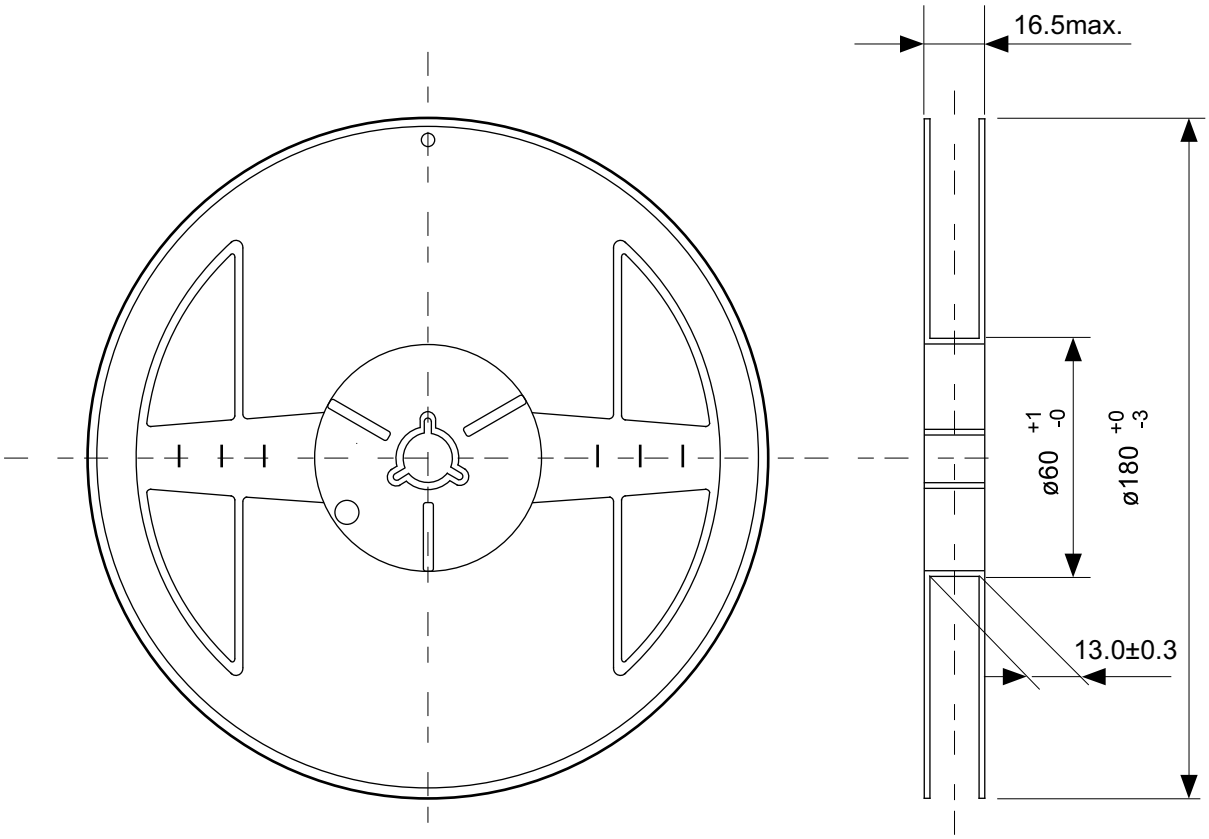




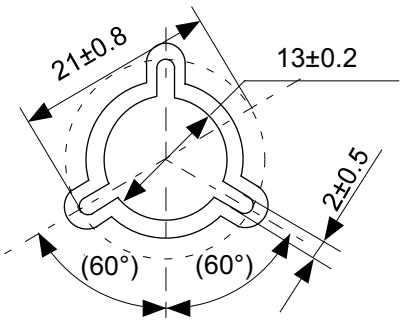
No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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