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DATA SHEET

74ALVCH16652
16-bit transceiver/register with dual enable; 3-state

Product specification
Supersedes data of 1998 Aug 31
File under Integrated Circuits, IC24

1999 Nov 23

Philips
Semiconductors

16-bit transceiver/register with dual enable; 3-state 74ALVCH16652

FEATURES

- In accordance with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through pin-out architecture
- Low inductance, multiple supply and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold
- Output drive capability 50 Ω transmission lines at 85 °C
- Current drive ±24 mA at 3.0 V.

DESCRIPTION

The 74ALVCH16652 consists of 16 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Data on the 'A' or 'B', or both buses, will be stored in the internal registers, at the appropriate clock inputs (nCP_{AB} or nCP_{BA}) regardless of the select inputs (nS_{AB} and nS_{BA}) or output enable (nOE_{AB} and $n\overline{OE}_{BA}$) control inputs.

Depending on the select inputs nS_{AB} and nS_{BA} data can directly go from input to output (real-time mode) or data can be controlled by the clock (storage mode), when OE inputs permit this operating mode.

The output enable inputs nOE_{AB} and $n\overline{OE}_{BA}$ determine the operation mode of the transceiver. When nOE_{AB} is LOW, no data transmission from nB_n to nA_n is possible and when $n\overline{OE}_{BA}$ is HIGH, no data transmission from nB_n to nA_n is possible.

When nS_{AB} and nS_{BA} are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling nOE_{AB} and $n\overline{OE}_{BA}$. In this configuration each output reinforces its input.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

Ground = 0; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA_n, nB_n to nB_n, nA_n	C_L = 50 pF; V_{CC} = 3.3 V	2.6	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		4.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2		
		outputs enabled	22	pF
		outputs disabled	4.0	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   C_L = output load capacitance in pF;
   f_o = output frequency in MHz;
   V_{CC} = supply voltage in Volts;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUTS						DATA I/O		FUNCTION
nOE_{AB}	$n\overline{OE}_{BA}$	nCP_{AB}	nCP_{BA}	nS_{AB}	nS_{BA}	nA_0 to nA_7	nB_0 to nB_7	
L L	H H	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
X H	H H	↑ ↑	H or L ↑	X L	X X	input input	unspecified(2) output	store A, hold B store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X L	unspecified(2) output	input input	hold A, store B store B in both registers
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
H H	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

Notes

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   ↑ = LOW-to-HIGH.
2. The data output functions may be enabled or disabled by various signals at the nOE_{AB} and $n\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

ORDERING INFORMATION

OUTSIDE NORTH AMERICA	NORTH AMERICA	PACKAGE				
		TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74ALVCH16652DGG	ACH16652 DGG	–40 to +85 °C	56	TSSOP	plastic	SOT364-1

PINNING

PIN	SYMBOL	DESCRIPTION
1 and 28	$1OE_{AB}$, $2OE_{AB}$	output enable A-to-B
2 and 27	$1CP_{AB}$, $2CP_{AB}$	clock input A-to-B
3 and 26	$1S_{AB}$, $2S_{AB}$	select input A-to-B
5, 6, 8, 9, 10, 12, 13 and 14	$1A_0$ to $1A_7$	‘1A’ data inputs/outputs
4, 11, 18, 25, 32, 39, 46 and 53	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
15, 16, 17, 19, 20, 21, 23 and 24	$2A_0$ to $2A_7$	‘2A’ data inputs/outputs
29 and 56	$2\overline{OE}_{BA}$, $1\overline{OE}_{BA}$	output enable B-to-A
30 and 55	$2CP_{BA}$, $1CP_{BA}$	clock input B-to-A
31 and 54	$2S_{BA}$, $1S_{BA}$	select input B-to-A
33, 34, 36, 37, 38, 40, 41 and 42	$2B_0$ to $2B_7$	‘2B’ data inputs/outputs
43, 44, 45, 47, 48, 49, 51 and 52	$1B_7$ to $1B_0$	‘1B’ data inputs/outputs

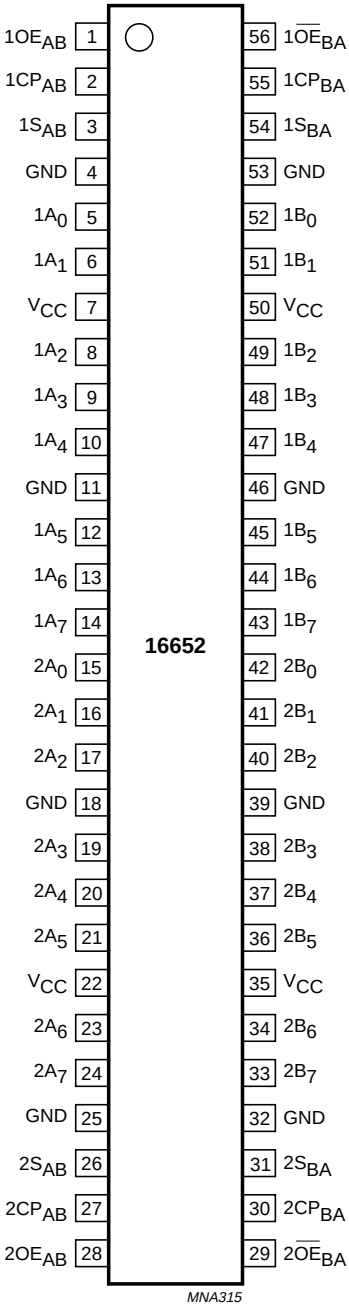


Fig.1 Pin configuration.

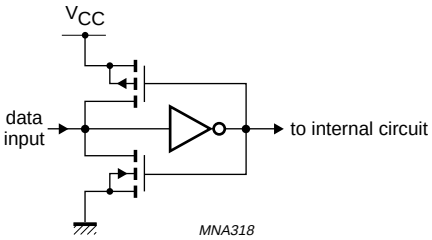


Fig.2 Bus hold circuit.

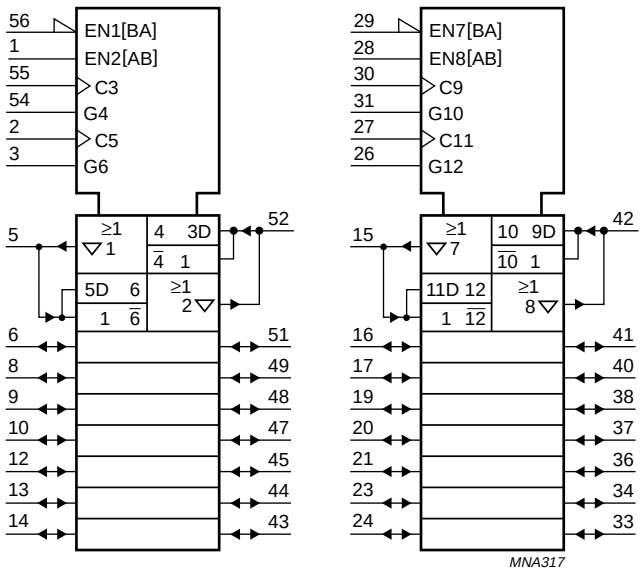


Fig.3 IEC logic symbol.

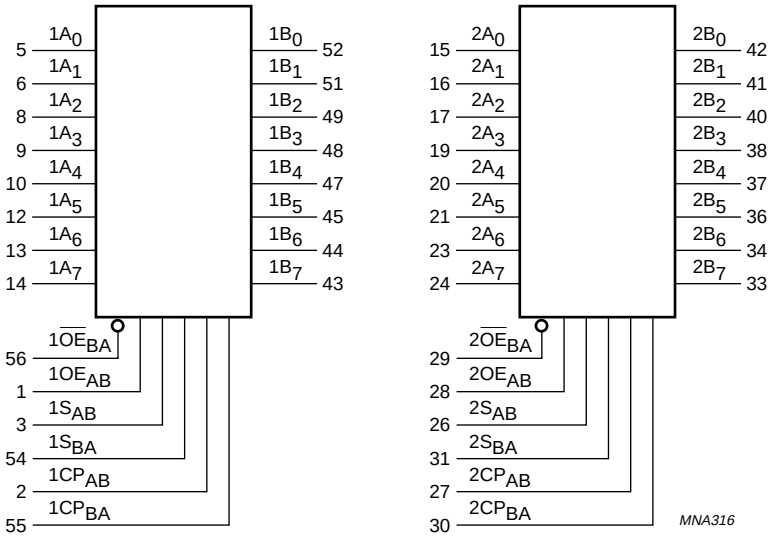


Fig.4 Logic symbol.

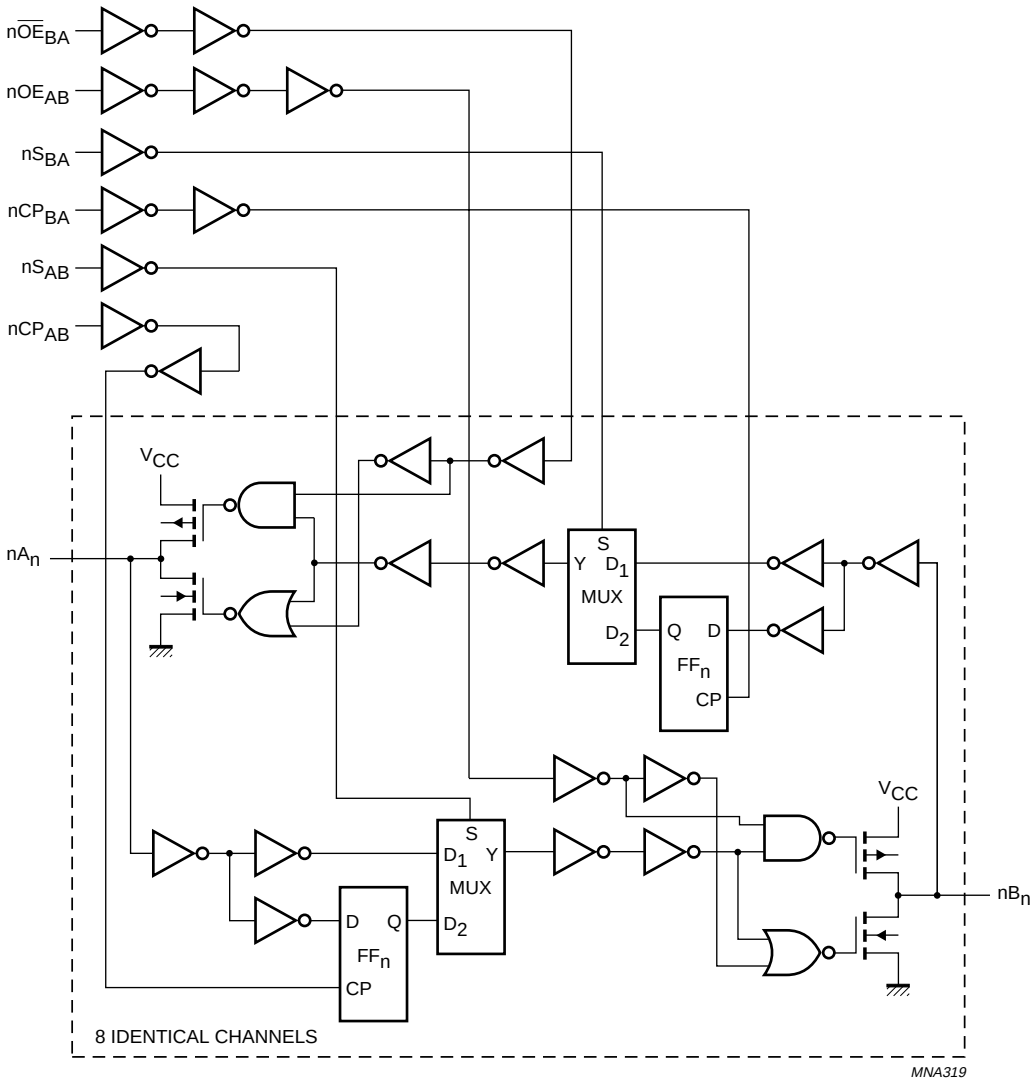


Fig.5 Logic diagram (one section).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage					
	for maximum speed performance	C_L = 30 pF	2.3	2.5	2.7	V
	for maximum speed performance	C_L = 50 pF	3.0	3.3	3.6	V
	for low-voltage applications		1.2	2.4	3.6	V
V_I	DC input voltage		0	–	V_{CC}	V
V_O	DC output voltage		0	–	V_{CC}	V
T_{amb}	operating ambient temperature	in free air	–40	–	+85	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.3 to 3.0 V	0	–	20	ns/V
		V_{CC} = 3.0 to 3.6 V	0	–	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
V_I	DC input voltage	note 1	–0.5	+4.6	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	DC output voltage	note 1	–0.5	V_{CC} + 0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	for temperature range: –40 to +125 °C; note 2	–	600	mW

Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 55 °C the value of P_{tot} derates linearly with 8 mW/K.

DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS			T_{amb} = −40 TO +85 °C			UNIT
		V_I (V)	OTHER	V_{CC} (V)	MIN.	TYP.(1)	MAX.	
V_{IH}	HIGH-level input voltage			2.3 to 2.7	1.7	1.2	–	V
				2.7 to 3.6	2.0	1.5	–	
V_{IL}	LOW-level input voltage			2.3 to 2.7	–	1.2	0.7	V
				2.7 to 3.6	–	1.5	0.8	
V_{OH}	HIGH-level output voltage	V_{IH} or V_{IL}	I_O = −100 µA	2.3 to 3.6	V_{CC} − 0.2	V_{CC}	–	V
			I_O = −6 mA	2.3	V_{CC} − 0.3	V_{CC} − 0.08	–	
			I_O = −12 mA	2.3	V_{CC} − 0.6	V_{CC} − 0.26	–	
			I_O = −12 mA	2.7	V_{CC} − 0.5	V_{CC} − 0.14	–	
			I_O = −12 mA	3.0	V_{CC} − 0.6	V_{CC} − 0.09	–	
			I_O = −24 mA	3.0	V_{CC} − 1.0	V_{CC} − 0.28	–	
V_{OL}	LOW-level output voltage	V_{IH} or V_{IL}	I_O = 100 µA	2.3 to 3.6	–	GND	0.20	V
			I_O = 6 mA	2.3	–	0.07	0.40	
			I_O = 12 mA	2.3	–	0.15	0.70	
			I_O = 12 mA	2.7	–	0.14	0.40	
			I_O = 24 mA	3.0	–	0.27	0.55	
I_I	input leakage current	V_{CC} or GND		2.3 to 3.6	–	0.1	5	µA
I_{OZ}	3-state output OFF-state current	V_{IH} or V_{IL}	V_O = V_{CC} or GND	2.3 to 3.6	–	0.1	10	µA
I_{CC}	quiescent supply voltage	V_{CC} or GND	I_O = 0	2.3 to 3.6	–	0.2	40	µA
ΔI_{CC}	additional quiescent supply current given per data I/O pin with bus hold	V_{CC} − 0.6	I_O = 0	2.3 to 3.6	–	150	750	µA
I_{BHL}	bus hold LOW sustaining current	0.7(2)		2.3(2)	45	–	–	µA
		0.8(2)		3.0(2)	75	150	–	
I_{BHH}	bus hold HIGH sustaining current	1.7(2)		2.3(2)	−45	–	–	µA
		2.0(2)		3.0(2)	−75	−175	–	
I_{BHLO}	bus hold LOW overdrive current			3.6(2)	500	–	–	µA
I_{BHHO}	bus hold LOW overdrive current			3.6(2)	−500	–	–	µA

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3 TO 2.7 V

Ground = 0 V; $t_r = t_f \leq 2.0$ ns; C_L = 30 pF.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} = −40 TO +85 °C			UNIT
		WAVEFORMS	V_{CC} (V)	MIN.	TYP.(1)	MAX.	
t_{PHL}/t_{PLH}	propagation delay nA_n, nB_n to nB_n, nA_n	see Figs 6 and 10	2.3 to 2.7	1.0	2.7	4.8	ns
	propagation delay nCP_{AB}, nCP_{BA} to nB_n, nA_n	see Figs 8 and 10	2.3 to 2.7	1.0	3.4	6.8	ns
	propagation delay nS_{AB}, nS_{BA} to nB_n, nA_n	see Figs 7 and 10	2.3 to 2.7	1.0	3.4	5.6	ns
t_{PZH}/t_{PZL}	3-state output enable time nOE_{AB} to nB_n	see Figs 9 and 10	2.3 to 2.7	1.0	2.6	4.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time nOE_{AB} to nB_n	see Figs 9 and 10	2.3 to 2.7	1.6	2.7	4.5	ns
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}_{BA}$ to nA_n	see Figs 9 and 10	2.3 to 2.7	3.3	2.8	4.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}_{BA}$ to nA_n	see Figs 9 and 10	2.3 to 2.7	3.3	2.5	4.5	ns
t_W	clock pulse width HIGH or LOW nCP_{AB} or nCP_{BA}	see Figs 8 and 10	2.3 to 2.7	2.2	1.2	–	ns
t_{su}	set-up time nA_n, nB_n to nCP_{AB}, nCP_{BA}	see Figs 8 and 10	2.3 to 2.7	2.2	0.2	–	ns
t_h	hold time nA_n, nB_n to nCP_{AB}, nCP_{BA}	see Figs 8 and 10	2.3 to 2.7	0.6	0.1	–	ns
f_{max}	maximum clock pulse frequency	see Figs 8 and 10	2.3 to 2.7	150	300	–	MHz

Note

1. All typical values are measured at T_{amb} = 25 °C and V_{CC} = 2.5 V.

AC CHARACTERISTICS FOR V_{CC} = 2.7 V AND V_{CC} = 3.0 TO 3.6 V

Ground = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} = −40 TO +85 °C			UNIT
		WAVEFORMS	V_{CC} (V)	MIN.	TYP.(1)	MAX.	
t_{PHL}/t_{PLH}	propagation delay nA_n, nB_n to nB_n, nA_n	see Figs 6 and 10	2.7	–	2.8	4.5	ns
			3.0 to 3.6	1.0	2.6(2)	3.9	
	propagation delay nCP_{AB}, nCP_{BA} to nB_n, nA_n	see Figs 8 and 10	2.7	–	3.1	5.2	ns
			3.0 to 3.6	1.4	2.9(2)	4.5	
	propagation delay nS_{AB}, nS_{BA} to nB_n, nA_n	see Figs 7 and 10	2.7	–	3.5	6.4	ns
			3.0 to 3.6	1.3	3.1(2)	5.3	
t_{PZH}/t_{PZL}	3-state output enable time nOE_{AB} to nB_n	see Figs 9 and 10	2.7	–	2.4	4.6	ns
			3.0 to 3.6	1.0	2.2(2)	4.0	
t_{PHZ}/t_{PLZ}	3-state output disable time nOE_{AB} to nB_n	see Figs 9 and 10	2.7	–	3.4	5.1	ns
			3.0 to 3.6	1.4	2.7(2)	4.5	
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}_{BA}$ to nA_n	see Figs 9 and 10	2.7	–	3.0	4.6	ns
			3.0 to 3.6	1.0	2.2(2)	4.0	
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}_{BA}$ to nA_n	see Figs 9 and 10	2.7	–	3.1	5.1	ns
			3.0 to 3.6	1.1	2.9(2)	4.5	
t_W	clock pulse width HIGH or LOW nCP_{AB} or nCP_{BA}	see Figs 8 and 10	2.7	3.3	1.0	–	ns
			3.0 to 3.6	3.3	0.7(2)	–	
t_{su}	set-up time nA_n, nB_n to nCP_{AB}, nCP_{BA}	see Figs 8 and 10	2.7	1.7	0.2	–	ns
			3.0 to 3.6	1.4	0.3(2)	–	
t_h	hold time nA_n, nB_n to nCP_{AB}, nCP_{BA}	see Figs 8 and 10	2.7	0.4	0.1	–	ns
			3.0 to 3.6	0.7	0.2(2)	–	
f_{max}	maximum clock pulse frequency	see Figs 8 and 10	2.7	150	320	–	MHz
			3.0 to 3.6	150	320(2)	–	

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. Typical values at V_{CC} = 3.3 V.

AC WAVEFORMS

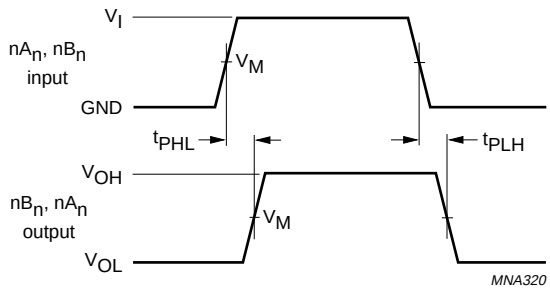


Fig.6 The inputs nA_n, nB_n to outputs nB_n, nA_n propagation delay times.

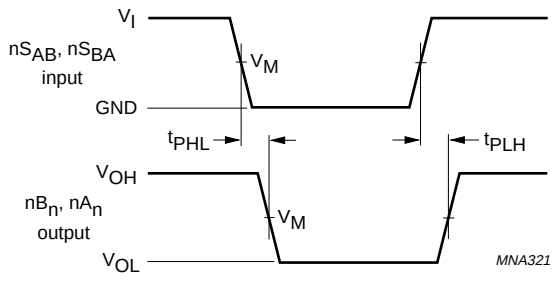


Fig.7 The inputs nS_{AB}, nS_{BA} to outputs nB_n, nA_n propagation delays.

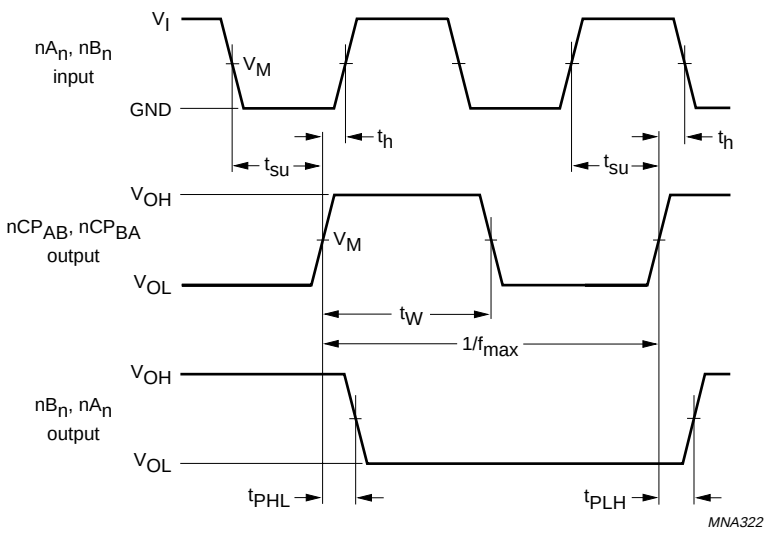


Fig.8 The nA_n, nB_n to nCP_{AB}, nCP_{BA} set-up and hold times, clock nCP_{AB}, nCP_{BA} pulse width, maximum clock pulse frequency and the nCP_{AB}, nCP_{BA} to output nB_n, nA_n propagation delay times.

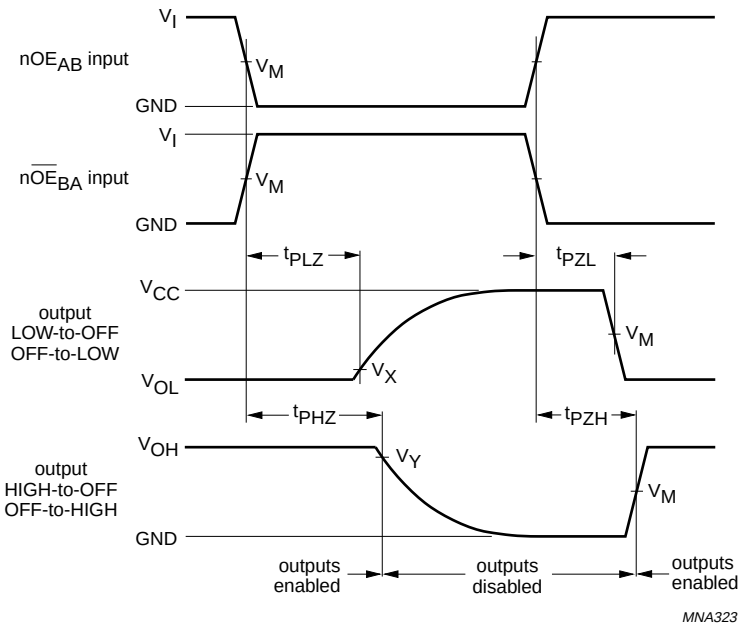


Fig.9 The OE inputs (nOE_{AB}, $n\overline{OE}_{BA}$) to outputs nA_n, nB_n enable and disable times and the input rise and fall times.

Notes: V_{CC} = 2.3 to 2.7 V

$V_M = 0.5V_{CC}$;

$V_X = V_{OL} + 150$ mV;

$V_Y = V_{OH} - 150$ mV;

$V_I = V_{CC}$;

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Notes: V_{CC} = 3.0 to 3.6 V and V_{CC} = 2.7 V

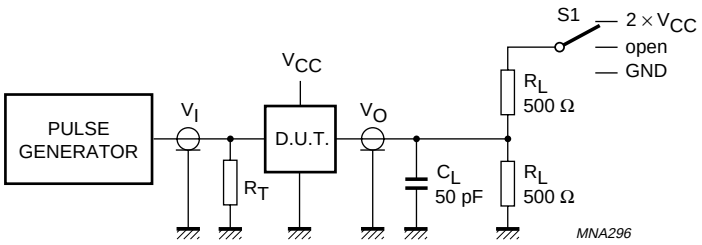
$V_M = 1.5$ V;

$V_X = V_{OL} + 300$ mV;

$V_Y = V_{OH} - 300$ mV;

$V_I = 2.7$ V;

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.



TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
<2.7 V	V_{CC}
2.7 to 3.6 V	2.7 V

Definitions for test circuit.

C_L = load capacitance including jig and probe capacitance (See Chapter “AC characteristics”).

R_L = load resistance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.10 Load circuitry for switching times.

APPLICATION INFORMATION

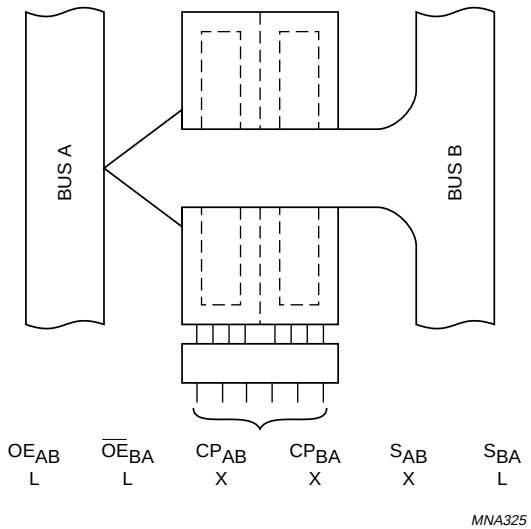


Fig.11 Real-time transfer; bus B to bus A.

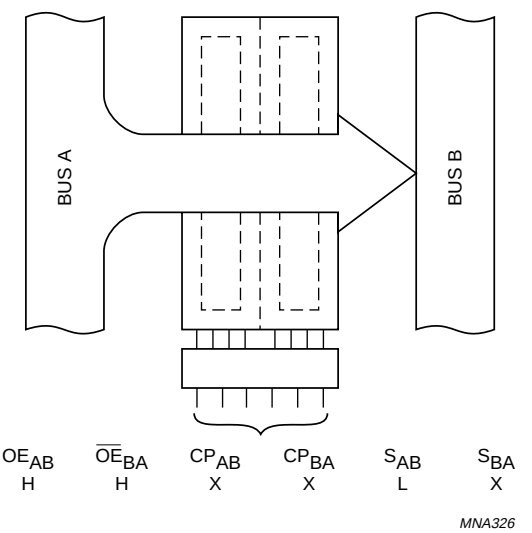
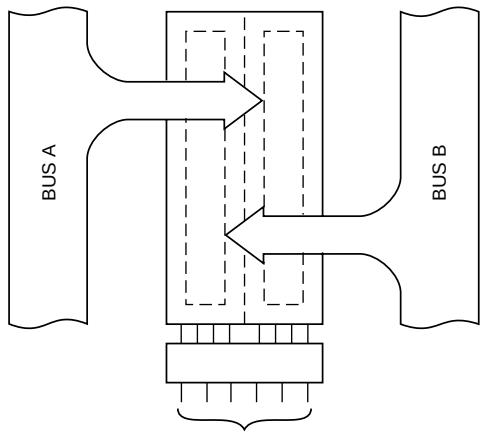
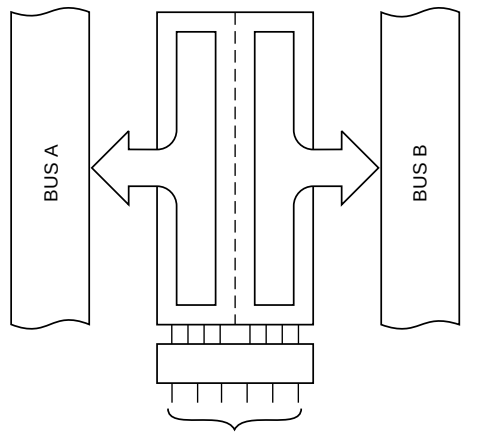


Fig.12 Real-time transfer; bus A to bus B.



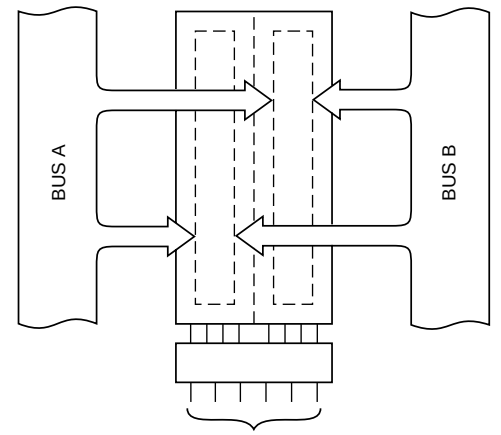
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Fig.13 Store A, B or A and B in one register.



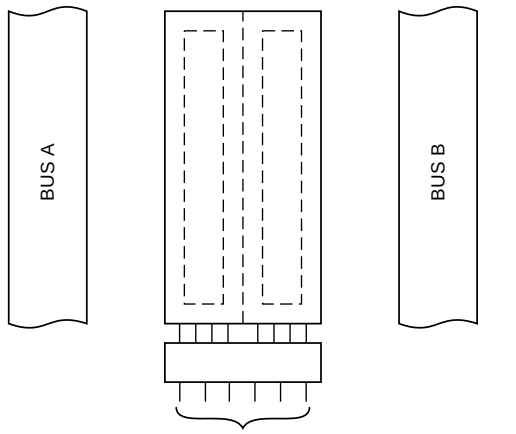
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Fig.14 Transfer A stored data to B bus or B stored data to A bus or both at the same time.



OE_{AB}	$\overline{OE}_{AB}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	H	↑	↑	X	X
L	L	↑	↑	X	L

Fig.15 Store bus A in both registers or store bus B in both registers.

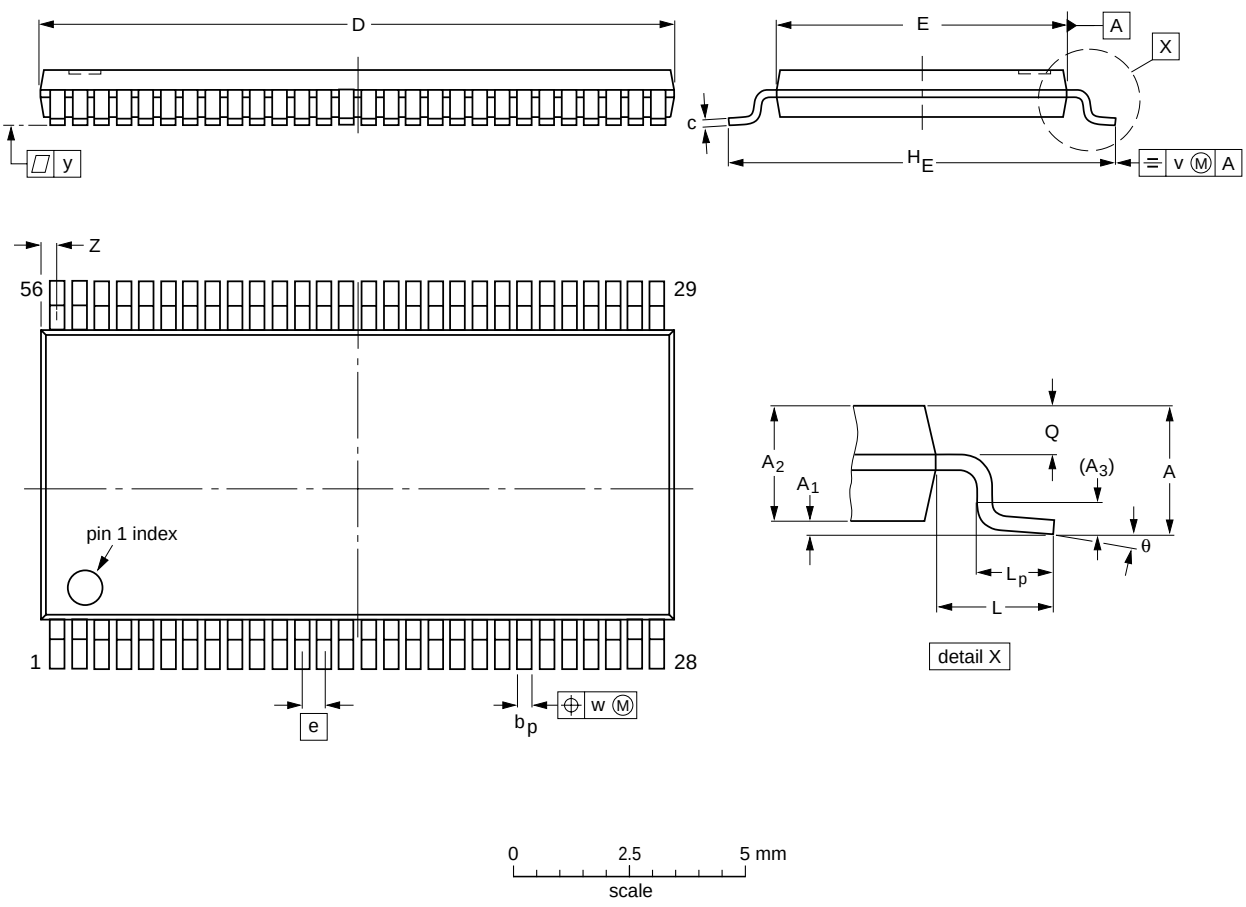


OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	H or L	H or L	X	X

Fig.16 Isolation.

PACKAGE OUTLINE

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT364-1		MO-153EE					~~93-02-03~~ 95-02-10

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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Where application information is given, it is advisory and does not form part of the specification.	

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