M24C32-U

Datasheet

32-Kbit serial I²C bus EEPROM with unique identifier



SO8N (MN)

150 mil width

Product status

M24C32-U

Product label

Features

I²C interface

- Compatible with the following I²C bus modes:
  - 100 kHz (Standard-mode)
  - 400 kHz (Fast-mode)
  - 1 MHz (Fast-mode Plus)

Memory

- 32-Kbit (4-Kbyte) of EEPROM
- Page size: 32-byte

Identification page

- 256-bit (32-byte) locked in read-only on delivery from the factory

UID

- 128-bit (16-byte) unique factory-programmed serial number

Supply voltage

- Wide voltage range: 1.7 V to 5.5 V

Temperature

- Operating temperature range: -40 °C to +85 °C

Fast write cycle time

- Byte and page write within 5 ms (typically 3.2 ms)

Performance

- Enhanced ESD and latch-up protection
- ESD protection: 4 kV (HBM)
- More than 4 million write cycles
- More than 200-year data retention

Advanced features

- Random and sequential read modes
- Hardware write protection of the whole memory array

Package

- SO8N (ECOPACK2 compliant)

Application

Applications of EEPROM UID include:

- Improved traceability for accessory recognition
- Enhanced repairability

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- Promoting sustainability in the consumer and industrial segments, such as:
  - Data centers
  - Logistics
  - Healthcare
  - Personal electronics

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1 Description

The M24C32-U is a 32-Kbit I²C-compatible EEPROM (electrically erasable programmable memory) organized as 4 K × 8 bits. It can operate with a supply voltage of 1.7 V to 5.5 V, over an ambient temperature range from -40 °C to +85 °C.

The device offers an additional page, named the identification page (32 bytes). This page stores a 128-bit (16 bytes) unique factory-programmed serial number, which is frozen in read-only mode on delivery from the factory.

The uniqueness of the serial number is ensured across the whole portfolio of serial EEPROMs manufactured by STMicroelectronics, offering a unique identifier.

Figure 1. Logic diagram

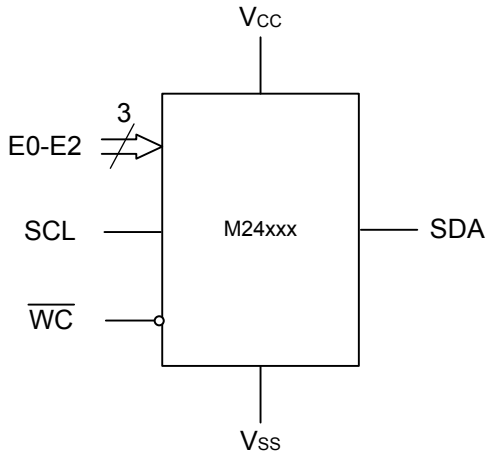
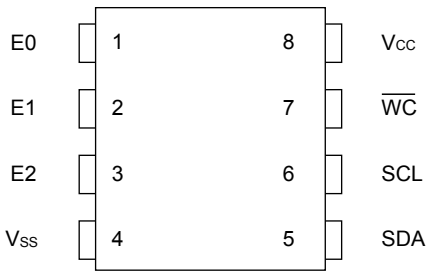


Table 1. Signal names

Signal name	Function	Direction
E2, E1, E0	Chip enable	Input
SDA	Serial data	I/O
SCL	Serial clock	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-
$\overline{WC}$	Write control	Input

Figure 2. 8-pin package connections, top view



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2 Signal description

2.1 Serial clock (SCL)

SCL is an input. The signal applied on it is used to strobe the data available on SDA(in) and to output the data on SDA(out).

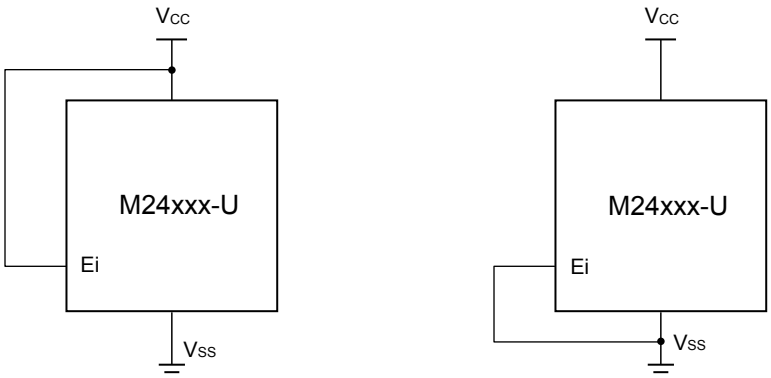
2.2 Serial data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wired-AND with other open drain or open collector signals on the bus. A pull-up resistor must be connected from serial data (SDA) to V_{CC} (Figure 14 and Figure 15 indicate how to calculate the value of the pull-up resistor).

2.3 Chip enable (E2, E1, E0)

The input signals E2, E1, and E0 set the value for the three least significant bits (b3, b2, and b1) of the 7-bit device select code (see Table 3). They must be connected to V_{CC} or V_{SS} to establish the device select code, as shown in Figure 3. When they are not connected (left floating), these inputs are read as low (0, 0, 0).

Figure 3. Chip enable inputs connection



2.4 Write control ($\overline{WC}$)

This input signal is useful for protecting the whole content of the memory from inadvertent write operations. Write operations are:

- Disabled to the whole memory array when write control is driven high.
- Enabled when write control is either driven low or left floating.

When the write control signal is driven high, the device select and address bytes are acknowledged, but data bytes are not acknowledged.

2.5 V_{SS} (ground)

V_{SS} is the reference for all signals, including the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage (V_{CC})

Before selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Table 7). To secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually from 10 to 100 nF) close to the VCC/VSS package pins.

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This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

The V_{CC} voltage must rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Table 7).

2.6.3 Device reset

To prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Table 7). When V_{CC} passes over the POR threshold, the device is reset and enters the standby power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see Table 7).

Similarly, during power-down, when V_{CC} decreases, the device must not be accessed once V_{CC} drops below V_{CC}(min). When V_{CC} drops below the POR threshold voltage, the device stops responding to any instruction sent to it.

2.6.4 Power-down conditions

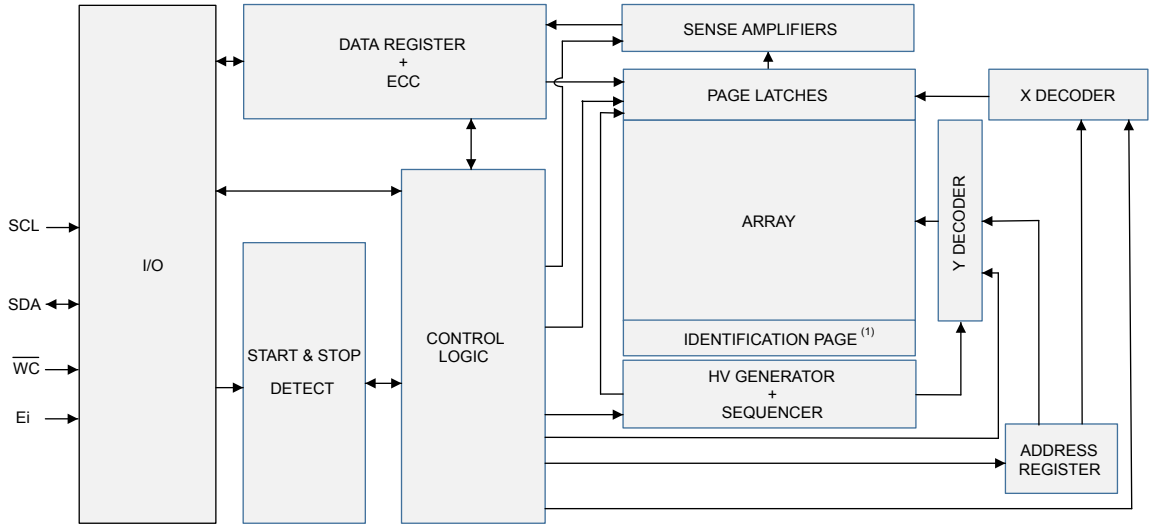
During power-down, when V_{CC} decreases, the device must be in the standby power mode (the mode is reached after decoding a stop condition, with no internal write cycle in progress).

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3 Memory organization

The memory is organized as shown in the following figure.

Figure 4. Block diagram



1. *Identification page with the UID*

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4 Device features

4.1 Identification page

This is an additional 32-byte page, permanently locked in read-only mode. The user can read it by issuing the read identification page instruction. This instruction uses the same protocol and format as the random address read (from the memory array), except for the following differences (refer to Table 3, Table 4, and Table 5):

- Device type identifier = 1011
- MSB address bits from A15 to A8 are *Don't care* except A10 which must be "0"
- LSB address bits from A7 to A5 are *Don't care*
- LSB address bits from A4 to A0 define the byte address within the identification page

4.2 Unique identifier (UID)

The M24C32-U provides an additional feature: a serial number programmed at factory level, and locked in read-only mode within the identification page. This preprogrammed, 16-byte unique ID is a 128-bit serial number and is unique across the all STMicroelectronics UID-family EEPROM devices.

This UID can be read by issuing the read identification page instruction.

- Device type identifier = 1011
- MSB address bits from A15 to A8 must be equal to 0
- LSB address bits from A7 to A4 must be equal to 0
- LSB address bits from A3 to A0 define the UID byte address within the identification page

The description of the UID is given in the following table.

Table 2. UID address in the identification page

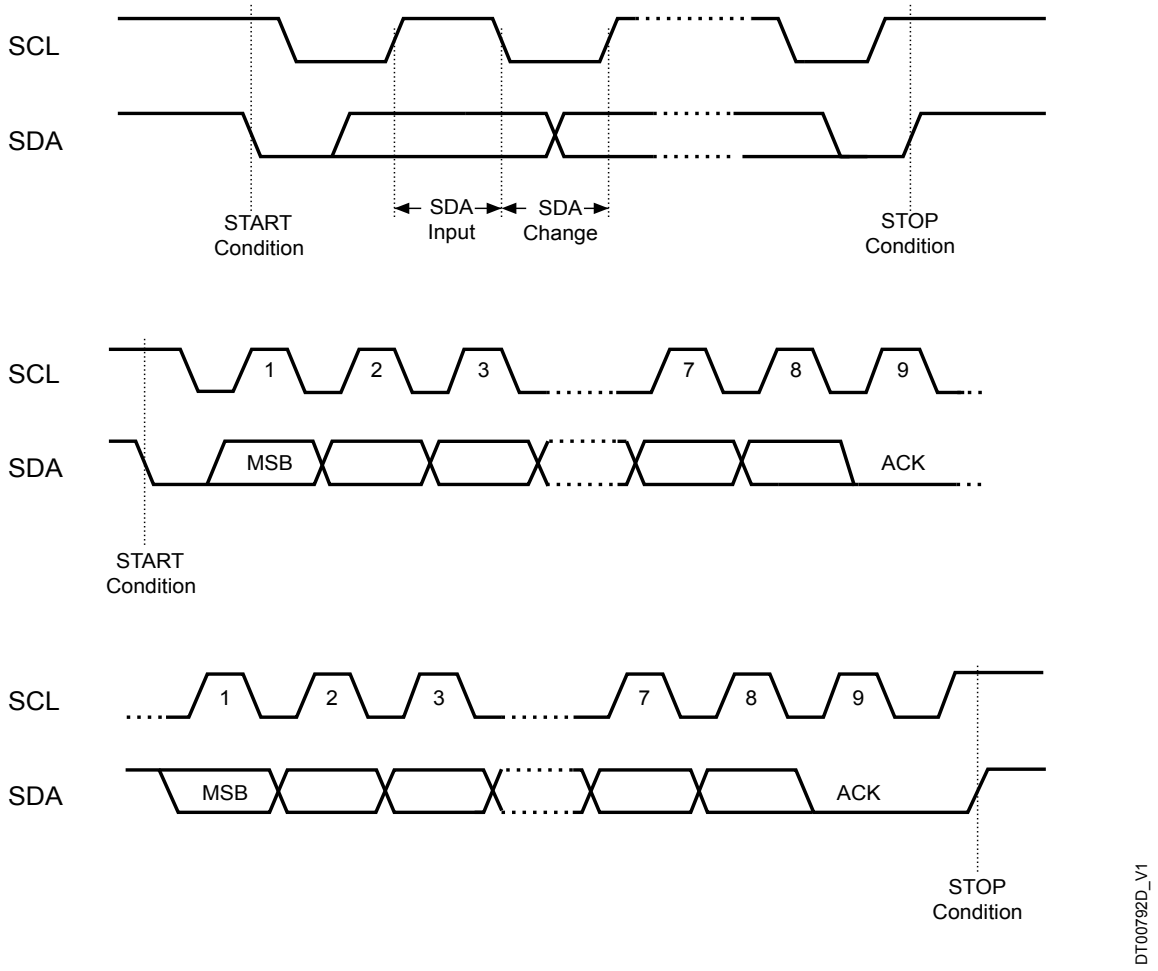
UID address in the identification page (hex)	Description	Value (hex)
00	Header – STM code	20
01	Header – Bus protocol	E0
02	Header - Density	0C
03	Header – Unused	FF
04	UID	
05		
06		
07		
08		
09		
0A		
0B		
0C		
0D		
0E		
0F		

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5 Device operation

The device supports the I²C protocol. This is summarized in Figure 5. Any device that sends data onto the bus is defined to be a transmitter, and any device that reads the data is defined to be a receiver. The device that controls the data transfer is known as the bus controller, and the other as the target device. A data transfer can only be initiated by the bus controller, which it also provides the serial clock for synchronization. The device is always a target in all communications.

Figure 5. I²C bus protocol



5.1 Start condition

Start is identified by a falling edge of serial data (SDA) while the serial clock (SCL) is stable in the high state. A start condition must precede any data transfer instruction. The device continuously monitors (except during a write cycle) serial data (SDA) and serial clock (SCL) for a start condition.

5.2 Stop condition

Stop is identified by a rising edge of serial data (SDA) while the serial clock (SCL) is stable in the high state. A Stop condition terminates communication between the device and the bus controller. A read instruction that is followed by no ACK can be followed by a stop condition to force the device into the standby mode.

A stop condition at the end of a write instruction triggers the internal write cycle.

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5.3 Data input

During data input, the device samples serial data (SDA) on the rising edge of serial clock (SCL). For correct device operation, serial data (SDA) must be stable during the rising edge of serial clock (SCL), and the serial data (SDA) signal must change only when serial clock (SCL) is driven low.

5.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus controller or target device, releases serial data (SDA) after sending eight bits of data. During the ninth clock pulse period, the receiver pulls serial data (SDA) low to acknowledge the receipt of the eight data bits.

5.5 Device addressing

To start communication between the bus controller and the target device, the bus controller must initiate a start condition. Following this, the bus controller sends the device select code and bytes address as specified in Table 3, Table 4, and Table 5.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on the serial data (SDA) during the interval. If the device does not match the device select code, it deselects itself from the bus, and goes into standby mode.

The eighth bit is the read/write bit ($R\overline{W}$), set to 1 for read operations and to 0 for write operations.

Table 3. Device select code

Features	Device type identifier				Chip enable address(1)			$R\overline{W}$
	Bit 7 (MSB)(2)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Memory	1	0	1	0	E2	E1	E0	$R\overline{W}$
Identification page	1	0	1	1	E2	E1	E0	$R\overline{W}$
UID	1	0	1	1	E2	E1	E0	$R\overline{W}$

1. *E0, E1 and E2 are compared with the value read on E2, E1, E0 input pins .*
2. *The most significant bit, b7, is sent first.*

Table 4. First byte address

Features	Bit 7 (MSB)(1)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Memory	A15(2)	A14(2)	A13(2)	A12(2)	A11	A10	A9	A8
Identification page	X(3)	X	X	X	X	0	X	X
UID	0	0	0	0	0	0	0	0

1. *The most significant bit, b7, is sent first.*
2. *Don't care*
3. *X = Don't care bit.*

Table 5. Second byte address

Features	Bit 7 (MSB)(1)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Memory	A7	A6	A5	A4	A3	A2	A1	A0
Identification page	X (2)	X	X	A4	A3	A2	A1	A0
UID	0	0	0	0	A3	A2	A1	A0

1. *The most significant bit, b7, is sent first.*
2. *X = Don't care bit.*

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6 Instructions

6.1 Write operations on memory array

Following a start condition, the bus controller sends a device select code with the R$\overline{W}$ bit reset to 0. The device acknowledges this, as shown in Figure 6, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte. Refer to Section 5.5: Device addressing including Table 3, Table 4, and Table 5 for a descriptiopn on how to address the memory.

When the bus controller generates a stop condition immediately after a data byte ACK bit (in the tenth bit time slot), either at the end of a byte write or a page write, the internal write cycle t_W is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

After the stop condition and the successful completion of an internal write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests.

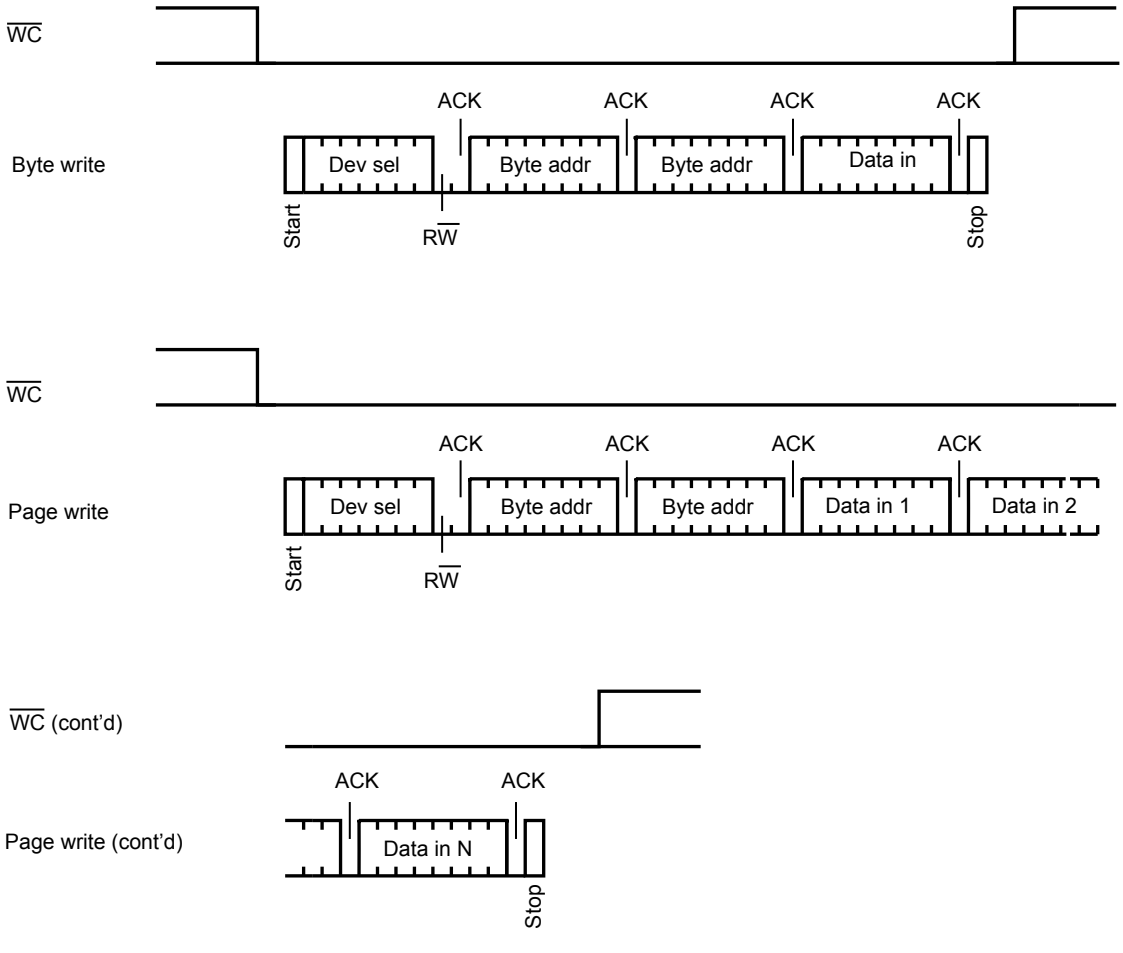
If the addressed area is write protected with the write control input ($\overline{WC}$) driven high, the write instruction is not executed and the accompanying data bytes are not acknowledged, as shown in Figure 7.

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6.1.1 Byte write

After the device select code and the address bytes, the bus controller sends one data byte. If the addressed location is write-protected, by write control ($\overline{WC}$) being driven high, the device replies with NO ACK, and the location is not modified. If, instead, the addressed location is not write-protected, the device replies with ACK. The bus controller terminates the transfer by generating a stop condition, as shown in the following figure.

Figure 6. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)



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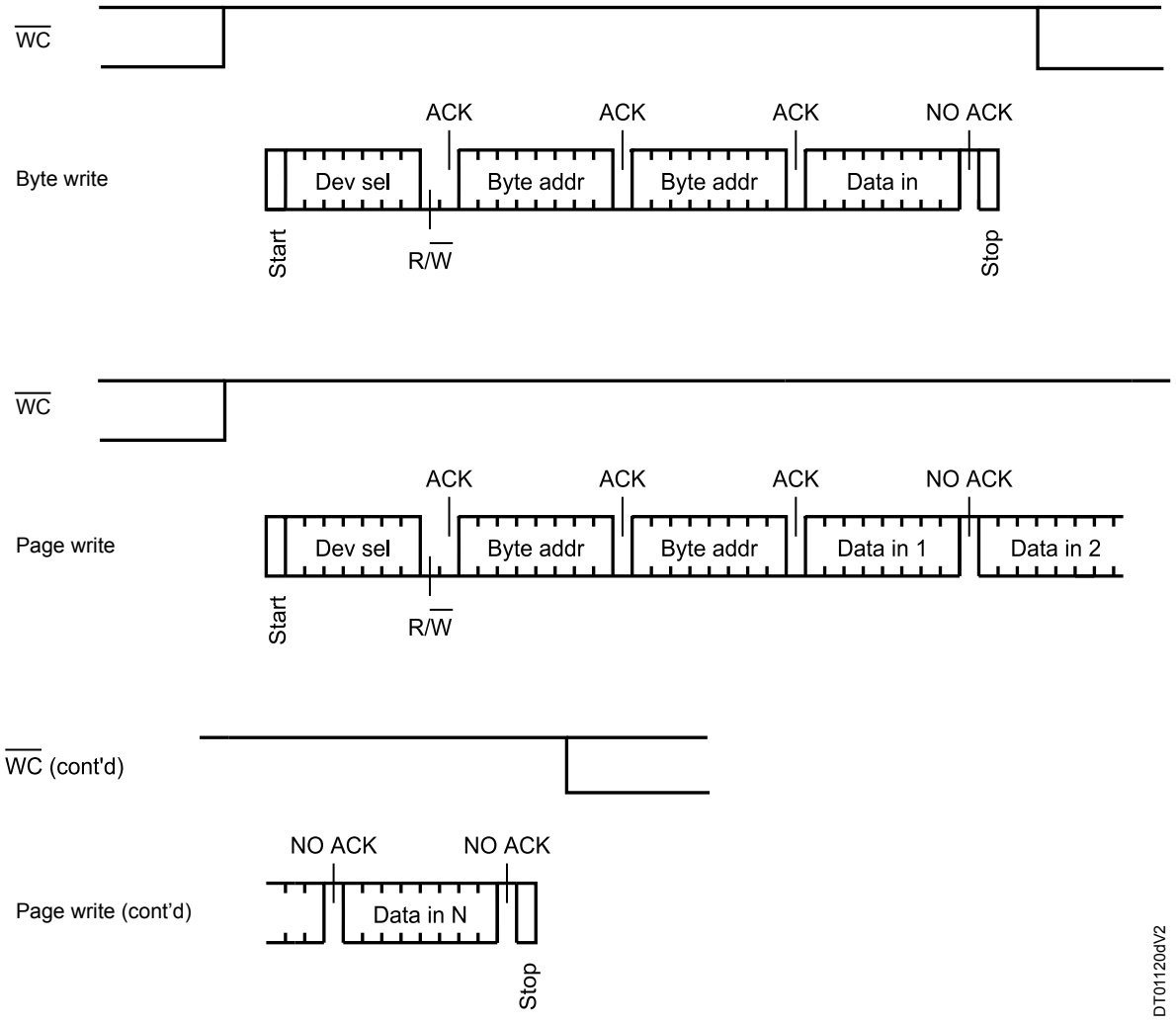
6.1.2 Page write

The page write allows up to 32-byte to be written in a single write cycle, provided that they are all located in the same page. This means the most significant memory address bits from A15 to A5 are the same. If more bytes are sent than fit within the page, a roll-over occurs: the bytes exceeding the page end are written from location 0 on the same page.

The bus controller sends from 1 to 32 bytes of data, each of them is acknowledged by the device if write control ($\overline{WC}$) is low. If write control ($\overline{WC}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NO ACK, as shown in Figure 7. After each transferred byte, the internal page address counter increments.

The transfer is terminated by the bus controller generating a stop condition.

Figure 7. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



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6.2 Write operations on the identification page

Write operations on the identification page are not allowed, as this page is delivered locked in read-only.

6.3 Error correction code (ECC) and write cycling

The ECC is an internal logic function transparent for the I^2C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes. Within a group, if a single bit happens to be erroneous during a read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group (a group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.)

As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the four bytes of the group: the sum of the cycles seen by byte 0, byte 1, byte 2, and byte 3 of the same group must remain below the maximum value defined in Table 10.

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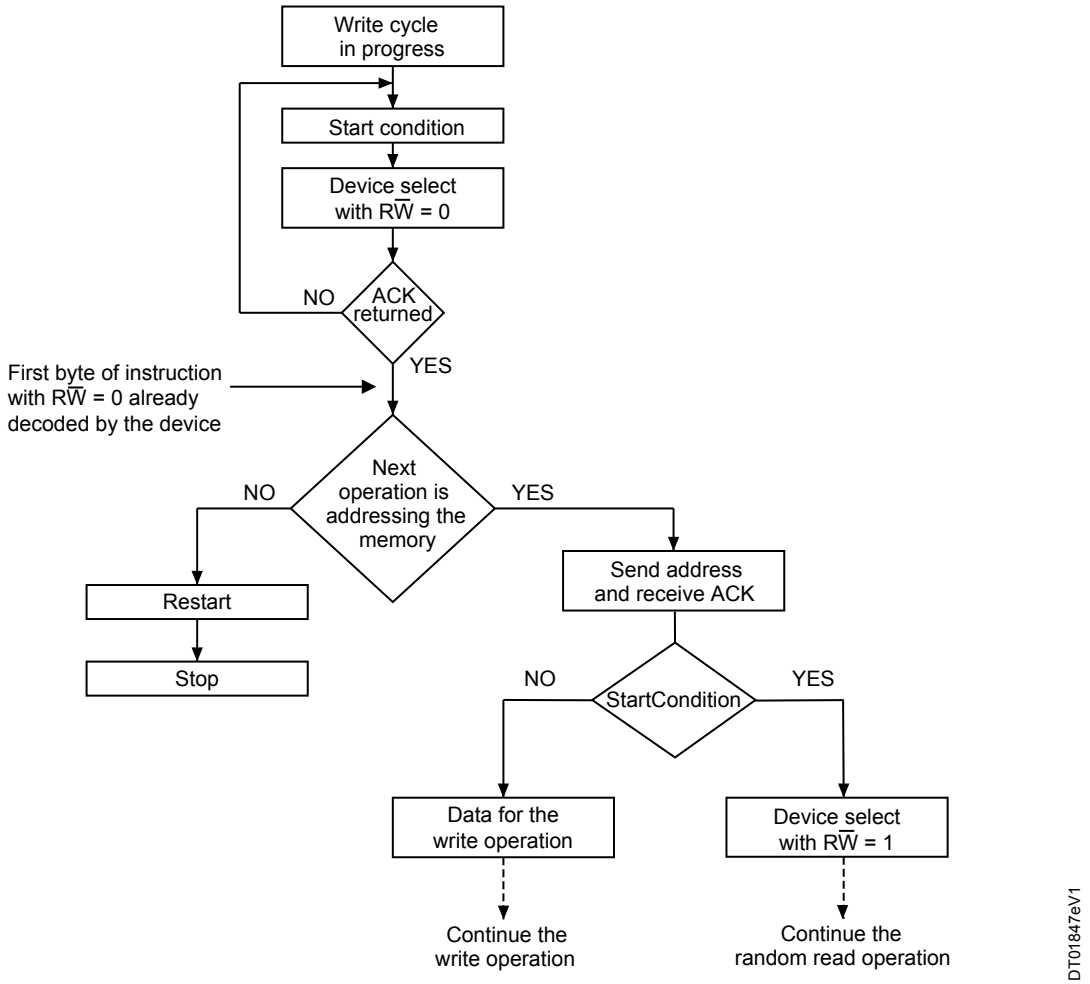
6.4 Minimizing write delays by polling on ACK

During the internal write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum write time (t_w) is shown in the AC characteristics tables in Section 9: DC and AC parameters, but the typical time is shorter. The bus controller can implement a polling sequence to utilize this feature.

The sequence, as shown in Figure 8, is:

- Initial condition: A write cycle is in progress.
- Step 1: The bus controller issues a start condition followed by a device select code (the first byte of the new instruction).
- Step 2: If the device is busy with the internal write cycle, NO ACK is returned and the bus controller goes back to step 1. If the device has terminated the internal write cycle, it responds with an ACK, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during step 1).

Figure 8. Write cycle polling flowchart using ACK



1. *The seven most significant bits of the device select code in a random read (bottom right box in the figure) must match those of the device select code in the write operation (polling instruction in the figure).*

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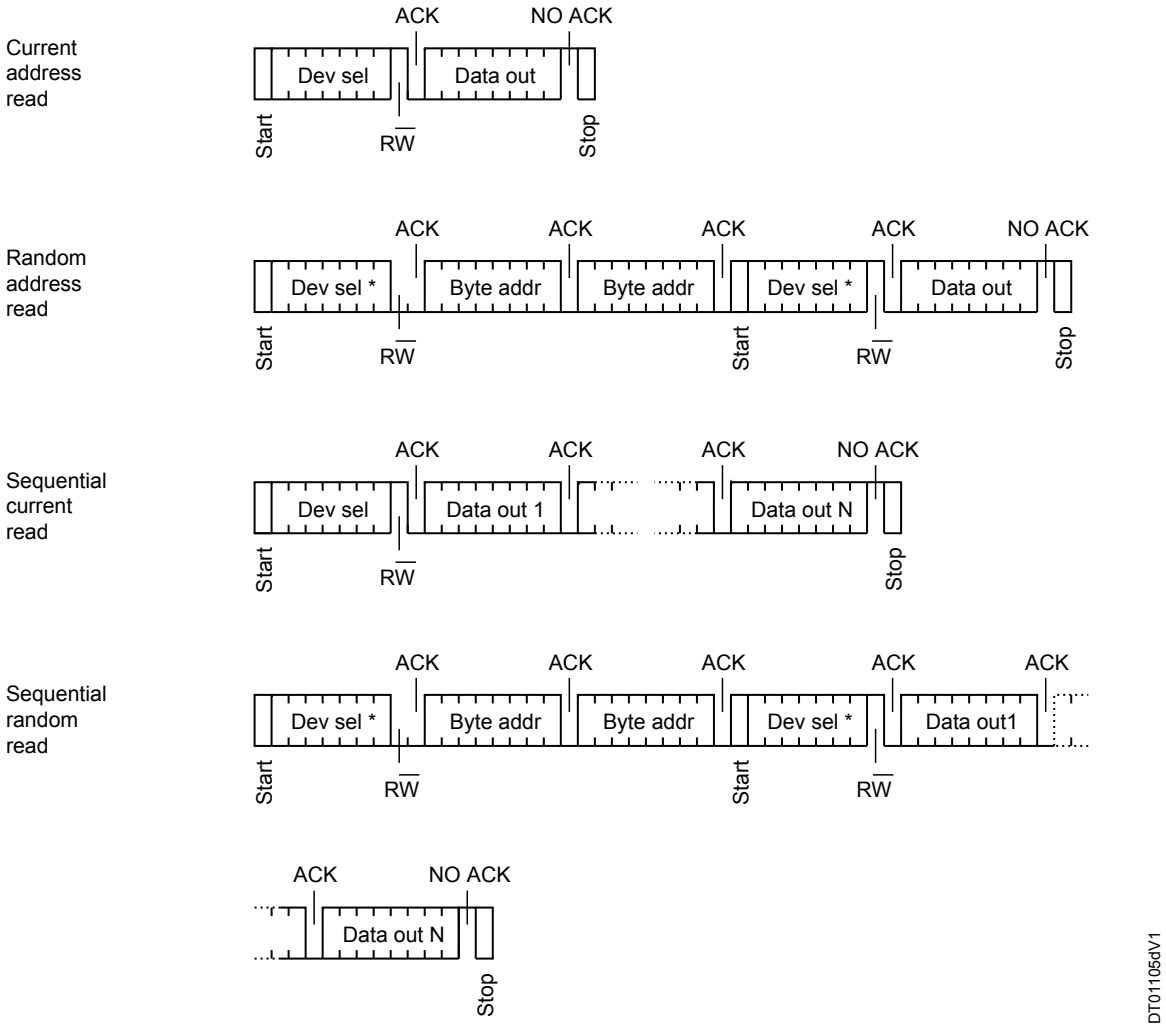
6.5 Read operations on the memory array

Following a start condition the bus controller sends a device select code with the RW bit set to 0. The device acknowledges this and waits for the two-bytes address. The device responds to each address byte with an acknowledge bit. Then, the bus controller sends another start condition, and repeats the device select code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the data. See in Section 5.5: Device addressing (Table 3, Table 4, and Table 5) how to address the memory array.

After each byte read (data out), the device waits for an acknowledgment (data in) during the ninth bit time. If the bus controller does not acknowledge during this interval, the device terminates the data transfer and switches to its standby mode after a stop condition.

After successfully completing a read operation, the system increments the internal address counter by one to point to the next byte address.

Figure 9. Read mode sequences



*Note: *: The seven most significant bits of the first device select code in a random read must match those of the device select code in the write operation.*

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6.5.1 Random address read

A dummy write is first performed to load the address into this address counter (as shown in Figure 9. Read mode sequences) without sending a stop condition. Then, the bus controller sends another start condition, and repeats the device select code, with the R$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus controller must not acknowledge the byte, and terminates the transfer with a stop condition.

6.5.2 Current address read

For the current address read operation, following a start condition, the bus controller sends only a device select code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus controller terminates the transfer with a stop condition, as shown in Figure 9. Read mode sequences, without acknowledging the byte.

Note: The address counter value is defined by instructions accessing either the memory or the identification page. When accessing the identification page, the address counter value is loaded with the identification page byte location, therefore the next current address read in the memory uses this new address counter value. When accessing the memory, it is safer to use the random address read instruction (this instruction loads the address counter with the byte location to read in the memory) instead of the current address read instruction.

6.5.3 Sequential read

This operation can be used after a current address read or a random address read. The bus controller does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus controller must not acknowledge the last byte, and must generate a stop condition, as shown in Figure 9. Read mode sequences.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter rolls-over, and the device continues to output data from memory address 00h.

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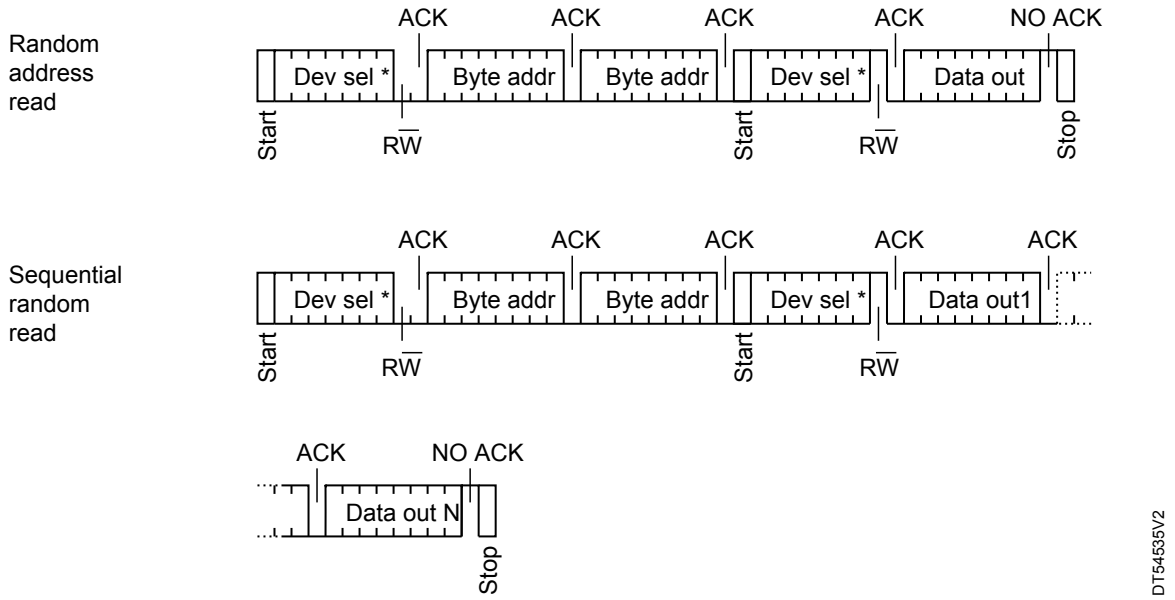
6.6 Read operations on identification page

Following a start condition, the bus controller sends a device select code with the RW bit (RW) set to '0'. The device acknowledges this and waits for the address bytes where the identification page is located. The device responds to each address byte with an acknowledge bit. The bits from A4 to A0 define the byte address inside the identification page. Then, the bus controller sends another start condition, and repeats the same device select code but with the RW bit set to 1. The device acknowledges this, and outputs the contents of the identification page. See in Table 3, Table 4, and Table 5 how to address the identification page.

The number of bytes to read in the ID page must not exceed the page boundary (for instance: when reading the identification page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 bytes).

To terminate the stream of data byte, the bus controller must not acknowledge the byte, and must generate a stop condition, as shown in Figure 10.

Figure 10. Random read on identification page



*Note: *: The seven most significant bits of the first device select code in a random read must match those of the device select code in the write operation.*

6.7 Read lock status on identification page

The lock or unlock status of the identification page can be checked by transmitting a specific truncated command.

Following a start condition the bus controller sends a device select code with the RW bit set to 0. The device acknowledges this and waits for the address bytes where the identification page is located. The device responds to each address byte with an acknowledge bit, and then waits for the data byte. See in Table 3, Table 4, and Table 5 how to address the identification page.

The device returns an acknowledge bit after the data byte if the identification page is unlocked (unlock status) as shown in Figure 11, otherwise a NO ACK bit as shown in Figure 12, if the identification page is locked (lock status).

Right after this, it is recommended to transmit to the device a start condition followed by a stop condition, so that:

- Start: the truncated command is not executed because the start condition resets the device internal logic
- Stop: the device is set back into standby mode by the stop condition

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Figure 11. **Read lock status (identification page unlocked)**

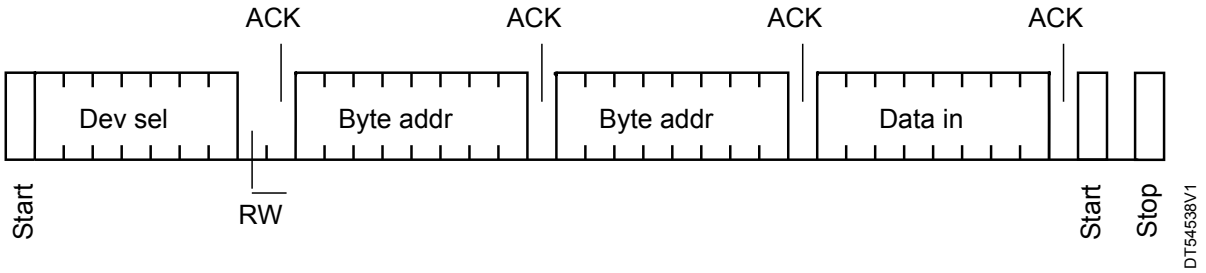
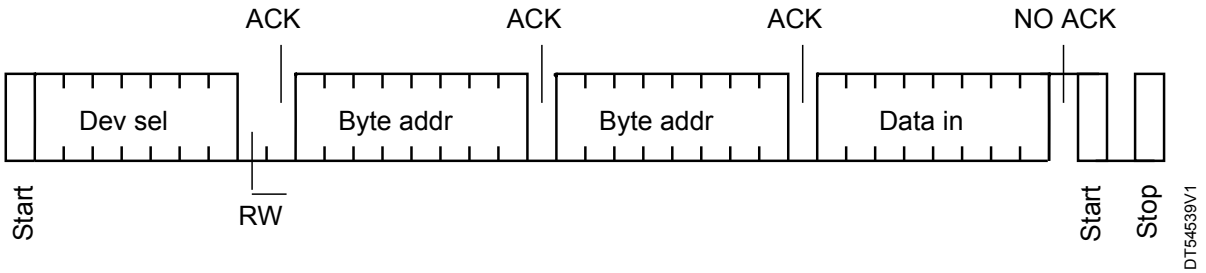


Figure 12. **Read lock status (identification page locked)**



Note: As the identification page is delivered in read-only mode, the EEPROM consistently behaves as described in Figure 12.

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7 Initial delivery state

The device is delivered with:

- All the memory array bits are set to 1 (each byte contains FFh).
- The identification page is locked and set with the first 16 bytes containing the value of the UID. The content of the following bytes is FFh.

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8 Maximum ratings

Stressing the device outside the ratings listed in Table 6 may permanently damage it. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
-	Ambient operating temperature	-40	130	°C
T_{STG}	Storage temperature	-65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{IO}	Input or output range	-0.50	6.5	V
V_{CC}	Supply voltage	-0.50	6.5	V
V_{ESD}	Electrostatic pulse (human body model) (2)	-	4000	V

1. *Compliant with JEDEC standard J-STD-020 (for small-body, Sn-Pb or Pb free assembly), the ST ECOPACK 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001, C1 = 100 pF, R1 = 1500 Ω).*

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9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 7. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	-40	85	°C
f_C	Operating clock frequency	-	1	MHz

Table 8. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	-	100	pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 13. AC measurement I/O waveform

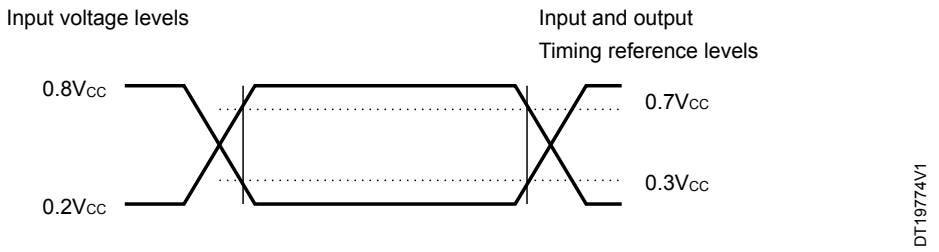


Table 9. Input parameters

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{IN}(1)	Input capacitance (SDA)	-	-	8	pF
C_{IN}(1)	Input capacitance (other pins)	-	-	6	pF
Z_L(2)	Input impedance (E2, E1, E0, $\overline{WC}$)(3)	V_{IN} < 0.3 V_{CC}	50	-	kΩ
Z_H(2)		V_{IN} > 0.7 V_{CC}	500	-	

1. *Specified by design - Not tested in production.*
2. *Evaluated by characterization - Not tested in production.*
3. *The memory is selected (after a start condition).*

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Table 10. Cycling performance by groups of four bytes

Symbol	Parameter	Test condition	Max.	Unit
Ncycle	Write cycle endurance(1)	$T_A \le 25$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	4 000 000	Write cycles(2)
		$T_A = 85$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	1 200 000	

1. *The write cycle endurance is defined by characterization and qualification. The write cycle endurance is defined for group of four bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer.*
2. *A write cycle is executed when a write instruction is decoded. When using the byte write or the page write, refer also to Section 6.3: Error correction code (ECC) and write cycling.*

Table 11. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention (1)	$T_A = 55$ °C	200	Year

1. *The data retention behaviour is checked in production, while the data retention limit is extracted from characterization and qualification results.*

Table 12. DC characteristics ($V_{CC} \ge 1.7$ V)

Symbol	Parameter	Test conditions (in addition to those in Table 7 and Table 8)	Min.	Max.	Unit
I_{LI}	Input leakage current (Ei, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.7 V, f_c= 400 kHz	-	0.8	mA
		f_C = 1 MHz	-	2.5	
I_{CC0}(1)	Supply current (Write)	During t_W, $V_{CC} \le 1.8$ V	-	3	mA
I_{CC1}	Standby supply current	Device not selected(2), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.7 V	-	1	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$, Ei(3))	$V_{CC} < 2.5$ V	-0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	$V_{CC} < 2.5$ V	0.75 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$, Ei(4))	$V_{CC} < 2.5$ V	0.75 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.7 V	-	0.2	V

1. *Evaluated by characterization - Not tested in production.*
2. *The device is not selected after power-up, after a read instruction (after the stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a write instruction).*
3. *Ei inputs should be tied to V_{SS} (see Section 2.3: Chip enable (E2, E1, E0))*
4. *Ei inputs should be tied to V_{CC} (see Section 2.3: Chip enable (E2, E1, E0))*

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Table 13. DC characteristics (V_{CC} ≥ 1.8V)

Symbol	Parameter	Test conditions (in addition to those in Table 7 and Table 8)	Min.	Max.	Unit
I_{LI}	Input leakage current (Ei, ,SCL SDA)	V_{IN} = V_{SS} or V_{CC}, device in standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, f_c = 400 kHz	-	0.8	mA
		f_c= 1 MHz	-	2.5	
I_{CC0}(1)	Supply current (Write)	During t_W, 1.8 V ≤ V_{CC} < 2.5 V	-	3	mA
I_{CC1}	Standby supply current	Device not selected,(2) V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8 V	-	1	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$, Ei(3))	1.8 V ≤ V_{CC} < 2.5 V	-0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	1.8 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$, Ei(4))	1.8 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.8 V	-	0.2	V

1. *Evaluated by characterization - Not tested in production.*
2. *The device is not selected after power-up, after a read instruction (after the stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a write instruction).*
3. *Ei inputs should be tied to V_{SS} (see Section 2.3: Chip enable (E2, E1, E0))*
4. *Ei inputs should be tied to V_{CC} (see Section 2.3: Chip enable (E2, E1, E0))*

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Table 14. DC characteristics (Vcc ≥ 2.5V)

Symbol	Parameter	Test conditions (in addition to those in Table 7 and Table 8)	Min.	Max.	Unit
I_{LI}	Input leakage current (Ei, SCL, SDA)	V_{IN} = V_{SS} or V_{CC}, device in standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	f_C = 400 kHz, 2.5 V ≤ V_{CC} ≤ 5.5 V	-	2	mA
		f_C = 1 MHz, 2.5 V ≤ V_{CC} ≤ 5.5 V	-	2.5	
I_{CC0}(1)	Supply current (Write)	During t_W, 2.5 V ≤ V_{CC} ≤ 5.5 V	-	5	mA
I_{CC1}	Standby supply current	Device not selected(2), V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5 V	-	2	µA
		Device not selected(2), V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5 V	-	3	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$, Ei(3))	-	-0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	-	0.7 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$, Ei(4))	-	0.7 V_{CC}	V_{CC} + 1	
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	V

1. *Evaluated by characterization - Not tested in production.*
2. *The device is not selected after power-up, after a read instruction (after the stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a write instruction).*
3. *Ei inputs should be tied to V_{SS} (see Section 2.3: Chip enable (E2, E1, E0)).*
4. *Ei inputs should be tied to V_{CC} (see Section 2.3: Chip enable (E2, E1, E0))*

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Table 15. AC characteristics (Fast-mode)

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2}(1)	t_F	SDA (out) fall time	20(2)	300	ns
t_{XH1XH2}(1)	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}(1)	t_F	Input signal fall time	(3)	(3)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}(4)	t_{DH}	Data out hold time	100	-	ns
t_{CLQV}(5)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_{WLDL}(1)(6)	$t_{SU:WC}$	$\overline{WC}$ set up time (before the start condition)	0	-	µs
t_{DHWH}(1)(7)	$t_{HD:WC}$	$\overline{WC}$ hold time (after the stop condition)	1	-	
t_W	t_{WR}	Write cycle time	-	5	ms
t_{NS}(1)	-	Pulse width ignored (input filter on SCL and SDA) - single glitch	-	80	ns

1. *Evaluated by characterization - Not tested in production.*
2. *With C_L = 10 pF.*
3. *There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.*
4. *To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.*
5. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that R_{bus} × C_{bus} time constant is within the values specified in Figure 14.*
6. *$\overline{WC}$ = 0 set up time condition to enable the execution of a write command.*
7. *$\overline{WC}$ = 0 hold time condition to enable the execution of a write command.*

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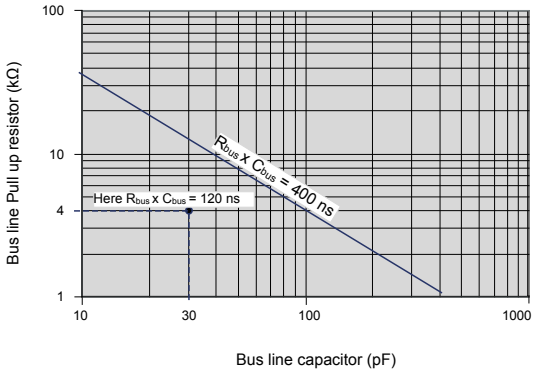
Table 16. AC characteristics (Fast-mode Plus)

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	500	-	ns
t_{XH1XH2}(2)	t_R	Input signal rise time	(1)	(1)	ns
t_{XL1XL2}(2)	t_F	Input signal fall time	(1)	(1)	ns
t_{QL1QL2}(2)	t_F	SDA (out) fall time	20(3)	120	ns
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}(4)	t_{DH}	Data out hold time	100	-	ns
t_{CLQV}(5)	t_{AA}	Clock low to next data valid (access time)	-	450	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_{WLDL}(2)(6)	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	µs
t_{DHWH}(2)(7)	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	µs
t_W	t_{WR}	Write cycle time	-	5	ms
t_{NS}(2)	-	Pulse width ignored (input filter on SCL and SDA)	-	80	ns

1. *There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be less than 120 ns when f_C < 1 MHz.*
2. *Evaluated by characterization - Not tested in production.*
3. *With C_L = 10 pF.*
4. *To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.*
5. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that the R_{bus} × C_{bus} time constant is within the values specified in Figure 15.*
6. *$\overline{WC}$ = 0 set up time condition to enable the execution of a write command.*
7. *$\overline{WC}$ = 0 hold time condition to enable the execution of a write command.*

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Figure 14. R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C_{bus} (f_C = 400 kHz)



The R_{bus} x C_{bus} time constant must be below the 400 ns time constant line displayed on the left

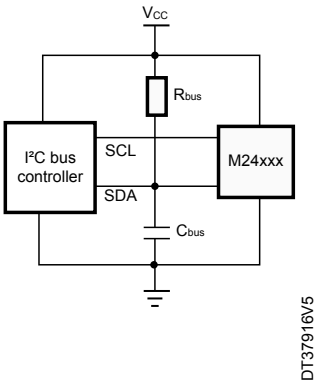
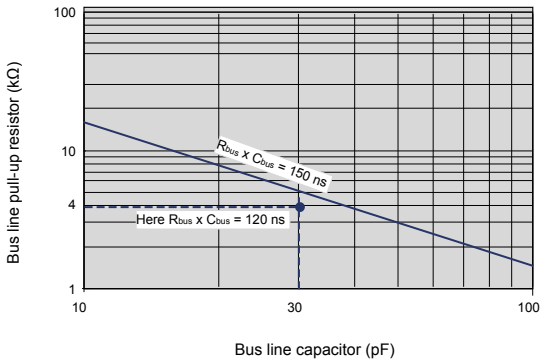
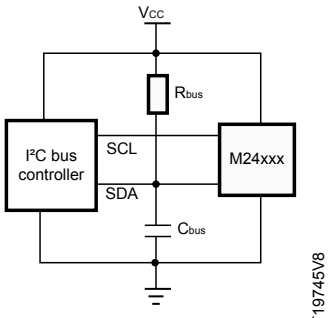


Figure 15. R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus (f_C = 1 MHz)

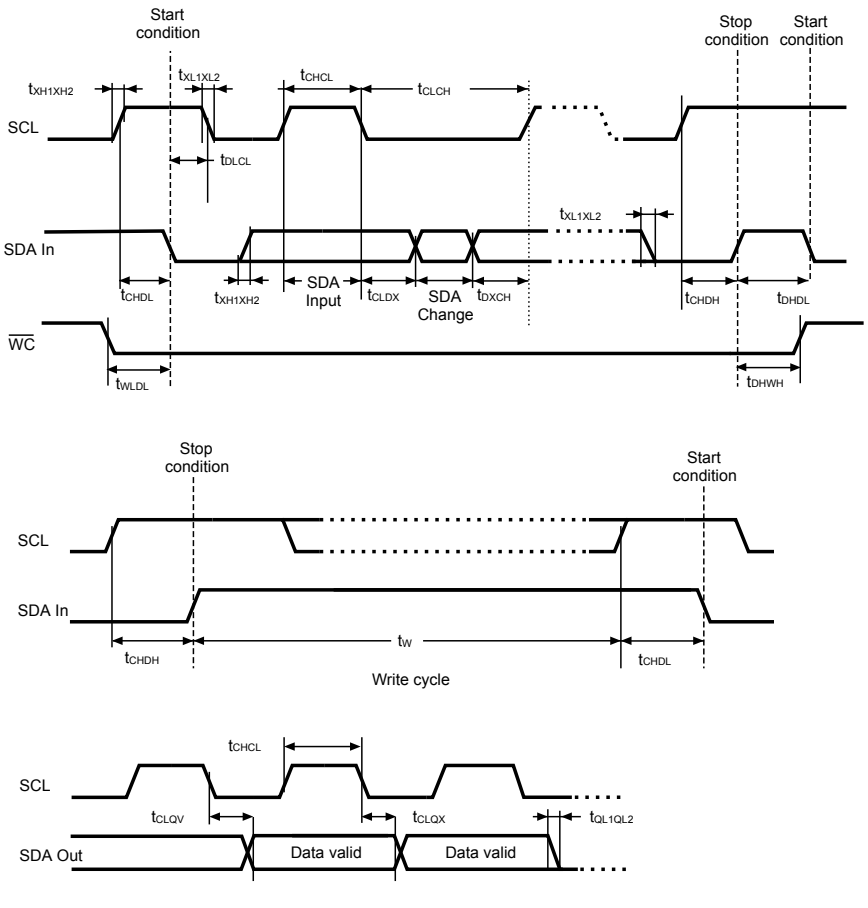


The R_{bus} x C_{bus} time constant must be below the 150 ns time constant line displayed on the left



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Figure 16. AC waveforms



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10 Package information

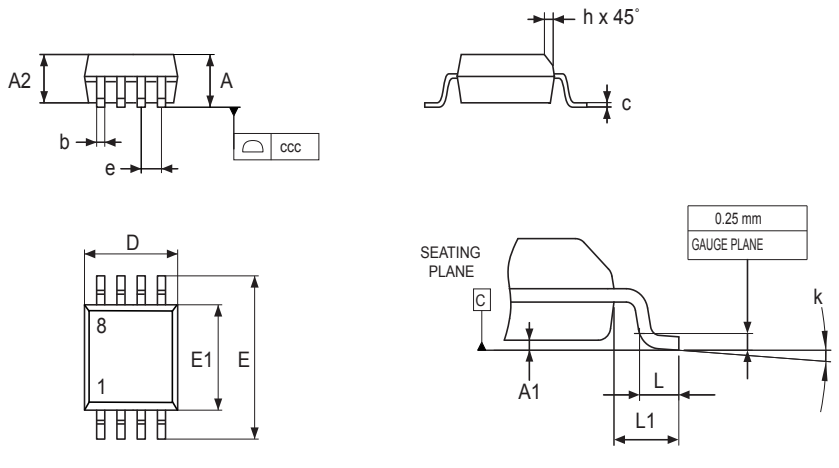
To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com.

ECOPACK is an ST trademark.

10.1 SO8N package information

This SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mil body width package.

Figure 17. SO8N - Outline



1. *Drawing is not to scale.*

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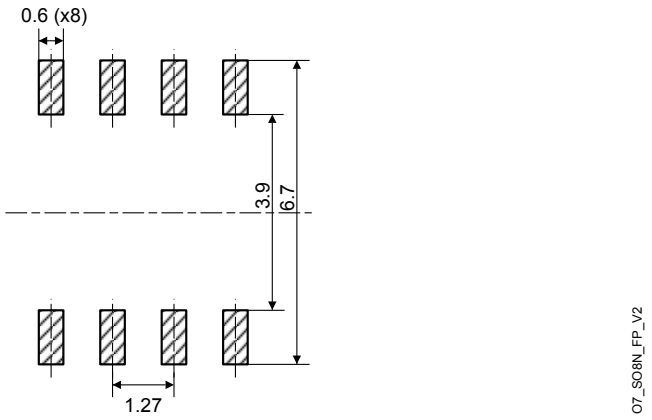
Table 17. SO8N - Mechanical data

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D[2]	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1[3]	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side*
3. *Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Note: The package top may be smaller than the package bottom. Dimensions D and E1 are determinated at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interleads flash, but including any mismatch between the top and bottom of the plastic body. The measurement side for mold flash, protusions, or gate burrs is the bottom side.

Figure 18. SO8N - Footprint example



1. *Dimensions are expressed in millimeters.*

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11 Ordering information

Table 18. Ordering information scheme

Example:	M24	C32	-U	F	MN	6	T	P	/K

Device type

M24 = I²C serial access EEPROM

Device function

C32 = 32 Kbit (4096 x 8 bit)

Device family

U = With UID

Operating voltage

F = V_{CC} = 1.7 V to 5.5 V

Package(1)

MN = SO8N (150 mil width)

Device grade

6 = Industrial: device tested with standard test flow over -40 to 85 °C

Option

T = Tape and reel packing

Blank = tube packing

Plating technology

P or G = RoHS compliant and halogen-free (ECOPACK2)

Process(2)

/K = Manufacturing technology code

1. *All packages are ECOPACK2 (RoHS-compliant and free of brominated, chlorinated and antimony-oxide flame retardants).*
2. *The process letter appears on the device package (marking) and on the shipment box. Contact your nearest ST Sales Office for further information.*

Note: For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact your nearest ST sales office.

Note: Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

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Revision history

Table 19. **Document revision history**

Date	Revision	Changes
09-Jul-2025	1	Initial release.

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Contents

1 **Description** . . . 3
2 **Signal description** . . . 4
2.1 Serial clock (SCL) . . . 4
2.2 Serial data (SDA) . . . 4
2.3 Chip enable (E2, E1, E0) . . . 4
2.4 Write control ($\overline{WC}$) . . . 4
2.5 V_{SS} (ground) . . . 4
2.6 Supply voltage (V_{CC}) . . . 4
2.6.1 Operating supply voltage (V_{CC}) . . . 4
2.6.2 Power-up conditions . . . 5
2.6.3 Device reset . . . 5
2.6.4 Power-down conditions . . . 5
3 **Memory organization** . . . 6
4 **Device features** . . . 7
4.1 Identification page . . . 7
4.2 Unique identifier (UID) . . . 7
5 **Device operation** . . . 8
5.1 Start condition . . . 8
5.2 Stop condition . . . 8
5.3 Data input . . . 9
5.4 Acknowledge bit (ACK) . . . 9
5.5 Device addressing . . . 9
6 **Instructions** . . . 10
6.1 Write operations on memory array . . . 10
6.1.1 Byte write . . . 11
6.1.2 Page write . . . 12
6.2 Write operations on the identification page . . . 13
6.3 Error correction code (ECC) and write cycling . . . 13
6.4 Minimizing write delays by polling on ACK . . . 14
6.5 Read operations on the memory array . . . 15
6.5.1 Random address read . . . 16
6.5.2 Current address read . . . 16
6.5.3 Sequential read . . . 16
6.6 Read operations on identification page . . . 17

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6.7 Read lock status on identification page 17
7 Initial delivery state 19
8 Maximum ratings 20
9 DC and AC parameters 21
10 Package information 29
10.1 SO8N package information 29
11 Ordering information 31
Revision history 32

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List of tables

Table 1. Signal names . . . 3
Table 2. UID address in the identification page . . . 7
Table 3. Device select code . . . 9
Table 4. First byte address . . . 9
Table 5. Second byte address . . . 9
Table 6. Absolute maximum ratings . . . 20
Table 7. Operating conditions . . . 21
Table 8. AC measurement conditions . . . 21
Table 9. Input parameters . . . 21
Table 10. Cycling performance by groups of four bytes . . . 22
Table 11. Memory cell data retention . . . 22
Table 12. DC characteristics (V_{CC} ≥ 1.7 V) . . . 22
Table 13. DC characteristics (V_{CC} ≥ 1.8V) . . . 23
Table 14. DC characteristics (Vcc ≥ 2.5V) . . . 24
Table 15. AC characteristics (Fast-mode) . . . 25
Table 16. AC characteristics (Fast-mode Plus) . . . 26
Table 17. SO8N - Mechanical data . . . 30
Table 18. Ordering information scheme . . . 31
Table 19. Document revision history . . . 32

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List of figures

Figure 1. Logic diagram. . . . 3
Figure 2. 8-pin package connections, top view . . . 3
Figure 3. Chip enable inputs connection . . . 4
Figure 4. Block diagram . . . 6
Figure 5. I²C bus protocol . . . 8
Figure 6. Write mode sequences with $\overline{WC}$ = 0 (data write enabled) . . . 11
Figure 7. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited). . . . 12
Figure 8. Write cycle polling flowchart using ACK . . . 14
Figure 9. Read mode sequences . . . 15
Figure 10. Random read on identification page . . . 17
Figure 11. Read lock status (identification page unlocked). . . . 18
Figure 12. Read lock status (identification page locked) . . . 18
Figure 13. AC measurement I/O waveform . . . 21
Figure 14. R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C_{bus} (f_C = 400 kHz) . . . 27
Figure 15. R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus (f_C = 1 MHz). . . . 27
Figure 16. AC waveforms . . . 28
Figure 17. SO8N - Outline . . . 29
Figure 18. SO8N - Footprint example . . . 30

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