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May 2024

FAN5069
PWM and LDO Controller Combo

Features

- General Purpose PWM Regulator and LDO Controller
- Input Voltage Range: 3V to 24V
- Output Voltage Range: 0.8V to 15V
  - V_{CC}
  - 5V
- Shunt Regulator for 12V Operation
- Support for Ceramic Cap on PWM Output
- Programmable Current Limit for PWM Output
- Programmable Switching Frequency (200KHz to 600KHz)
- $R_{DS(ON)}$ Current Sensing
- Internal Synchronous Boot Diode
- Soft-Start for both PWM and LDO
- Multi-Fault Protection with Optional Auto-resta
- 16-pin TSSOP Package

Applications

- PC/Server Motherboard Periph als
  - V_{CC_MCH} (1.5V), V- Q 1.5V, nd V_{TT_GTL} (1.25V)
- Power Supply
  - FPGA, D P, Embedu ontrollers, Graphic Card Proc sor, and C mmunication Processors
- In trial owe Supplies
- High-P ve C-to-DC Converters

Description

The FAN5069 combines a high-efficiency Pulse-Width-Modulated (PWM) controller and an LDO (Low DropOut) linear regulator controller. Synchronous rectification provides high efficiency over a wide ange f load currents. Efficiency is further enhanced y usi the low-side MOSFET's $R_{DS(ON)}$ to se e curr t.

Both the linear and P M gulato oft-sta t are con-trolled by a single e ern capac r, to limit in rush current from t supp wh the regulators are first enabled. urre limit f PWM is also programmable.

The M ulat employs a summing-current-mode ntr wit ernal compensation to achieve fast load tr sie response and provide des n optimization.

FAN 069 is offered in both industrial temperature grade (-40°C to +85°C) as well as commercial temperature grade (-10°C to +85°C).

Ordering Information

Part Number	Operating Temp. Range	Pb-Free	Package	Packing Method	Qty./Reel
FAN5069MTCX	-10°C to +85°C	Yes	16-Lead TSSOP	Tape and Reel	2500
FAN5069EMTCX	-40°C to +85°C	Yes	16-Lead TSSOP	Tape and Reel	2500

Note: Contact Fairchild sales for availability of other package options.

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Typical Application

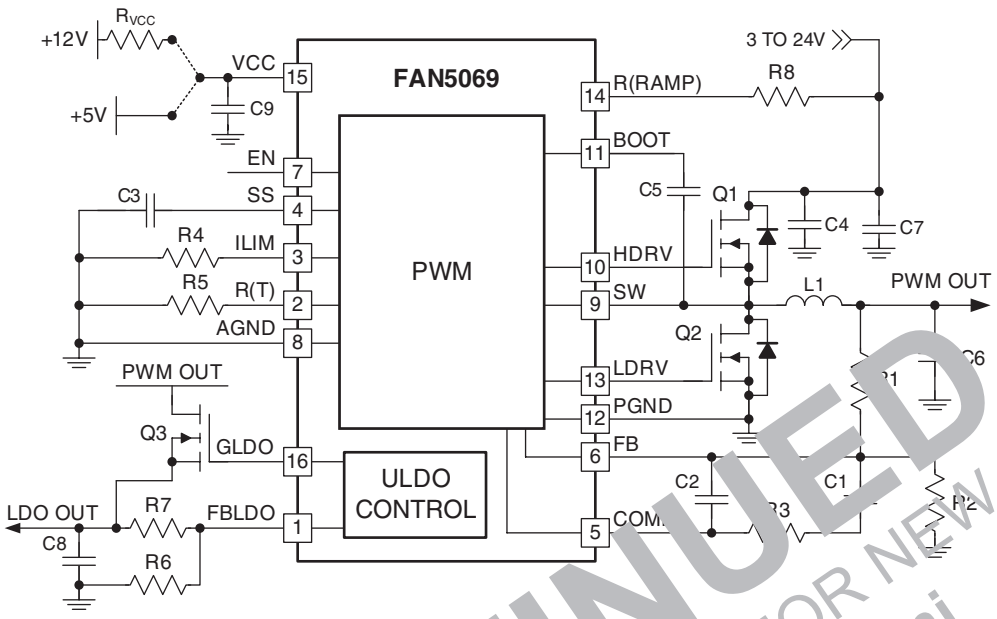

Figure 1. Typical Application Diagram

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Pin Assignment

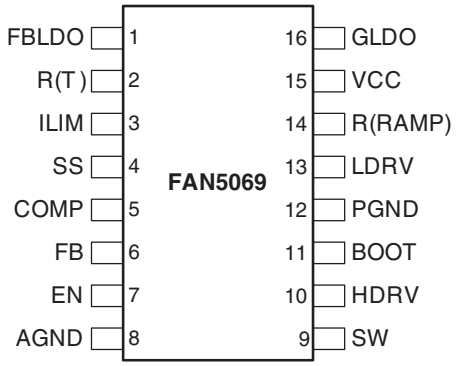

Figure 2. Pin Assignment

Pin Description

Pin #	Name	Description
1	FBLDO	**LDO Feedback**. This node is regulated to V_{REF}.
2	R(T)	**Oscillator Set Resistor.** This pin provides oscillator switching frequency adjustment. By placing a resistor (RT) from this pin to GND, the default 200kHz switching frequency is increased.
3	ILIM	**Current Limit.** A resistor from this pin to GND sets the current limit.
4	SS	**Soft-Start.** A capacitor from this pin to GND programs the slew rate of the converter and the LDO during initialization. It also sets the time by which the converter delays when restarting after a fault occurs. SS has to reach 1.2V before fault shutdown feature is enabled. The LDO is enabled when SS reaches 2V.
5	COMP	**COMP**. The output of the error amplifier drives this pin.
6	FB	**Feedback.** This pin is the inverting input of the internal error amplifier. Use this pin, in combination with the COMP pin, to compensate the feedback loop of the converter.
7	EN	**Enable.** Enables operation when pulled to logic high. Toggling EN resets the regulator after a latched fault condition. This is a CMOS input whose state is indeterminate if left open and needs to be properly biased at all times.
8	AGND	**Analog Ground.** The signal ground for IC. All internal control voltages are referred to this pin. Tie this pin to the ground island/plane through the lowest impedance connection available.
9	SW	**Switching Node.** Return for the high-side MOSFET driver and a current sense input. Connect to source of high-side MOSFET and drain of low-side MOSFET.
10	HDRV	**High-Side Gate Drive Output.** Connect to the gate of the high-side power MOSFETs. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET is turned off.
11	BOOT	**Bootstrap Supply Input.** Provides a boosted voltage to the high-side MOSFET driver. Connect to bootstrap capacitor as shown in Figure 1.
12	PGND	**Power Ground.** The return for the low-side MOSFET driver. Connect to the source of the low-side MOSFET.
13	LDRV	**Low-Side Gate Drive Output.** Connect to the gate of the low-side power MOSFETs. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET is turned off.
14	R(RAMP)	**Ramp Resistor**. A resistor from this pin to VIN sets the ramp amplitude and provides voltage feed-forward.
15	VCC	**VCC.** Provides bias power to the IC and the drive voltage for LDRV. Bypass with a ceramic capacitor as close to this pin as possible. This pin has a shunt regulator which draws current when the input voltage is above 5.6V.
16	GLDO	**Gate Drive for the LDO.** Turned off (low) until SS is greater than 2.2V.

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Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation. (1)

Parameter		Min.	Max.	Unit
V_{CC} to PGND			6.0	V
BOOT to PGND			33.0	V
SW to PGND	Continuous	-0.5	33.0	V
	Transient (t < 50nS, F < 500kHz)	-3.0	33.0	V
HDRV (V_{BOOT} – V_{SW})			6.0	V
LDRV		-0.5	6.5	V
All Other Pins		-0.3	V_{CC} + 0.3	V
Maximum Shunt Current for V_{CC}			150	mA
Electrostatic Discharge Protection (ESD) Level(2)	HBM			kV
	CDM	1.8		

Notes:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all voltages are referenced to AGND.
2. Using Mil Std. 883E, method 3015.7(Human Body Model) and EIA/JESD22C101-A (Charge Device Model).

Thermal Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{STG}	Storage Temperature	-65		150	°C
T_L	Lead Soldering Temperature, 10 Seconds			300	°C
	Vapor Phase, 60 Seconds			215	°C
	Infrared, 15 Seconds			220	°C
	Power Dissipation, T_A = 25°C			715	mW
θ_{JC}	Thermal Resistance, Junction-to-Case		37		°C/W
θ_{JA}	Thermal Resistance, Junction-to-Ambient(3)		100		°C/W

Notes:

3. Junction-to-ambient thermal resistance, θ_{JA}, is a strong function of PCB material, board thickness, thickness and number of copper planes, number of vias used, diameter of vias used, available copper surface, and attached heat sink characteristics.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	V_{CC} to GND	4.5	5.0	5.5	V
T_A	Ambient Temperature	Commercial	-10		85	°C
		Industrial	-40		85	°C
T_J	Junction Temperature				125	°C

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Electrical Characteristics

Unless otherwise noted, V_{CC} = 5V, T_A = 25°C, using circuit in Figure 1.

The '•' denotes that the specifications apply to the full ambient operating temperature range. See Notes 4 and 5.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Supply Current							
I_{VCC}	V_{CC} Current (Quiescent)	HDRV, LDRV Open	•	2.6	3.2	3.8	mA
$I_{VCC(SD)}$	V_{CC} Current (Shutdown)	EN = 0V, V_{CC} = 5.5V	•		200	400	µA
$I_{VCC(OP)}$	V_{CC} Current (Operating)	EN = 5V, V_{CC} = 5.0V, Q_{FET} = 20nC, F_{SW} = 200kHz			10	15	mA
V_{SHUNT}	V_{CC} Voltage(6)	Sinking 1mA to 100mA at V_{CC} Pin		5.5		5.9	V
Under-Voltage Lockout (UVLO)							
UVLO(H)	Rising V_{CC} UVLO Threshold		•	[illegible]	4.2	4.50	V
UVLO(L)	Falling V_{CC} UVLO Threshold		•	3.[illegible]	3.75	4.00	V
	V_{CC} UVLO Threshold Hysteresis				0.50		V
Soft-Start							
I_{SS}	Current				10		µA
$V_{LDOSTART}$	LDO Start Threshold				[illegible]		V
V_{SSOK}	PWM Protection Enable Threshold				1.2		V
Oscillator							
F_{OSC}	Frequency	R([illegible] = 56KΩ ± 1%		240	300	360	KHz
		[illegible](T) = Open		160	200	240	KHz
	Frequency [illegible]ange			160		600	KHz
ΔV_{RAMP}	Ram[illegible]Amp[illegible]ude (P[illegible]ak-to-Pea[illegible]	R(RAMP) = 330KΩ			0.4		V
	Mi[illegible]um [illegible] Time	F = 200kHz			200		nS.
R[illegible]e							
V_{REF}	R[illegible]erence Voltage (Measured at FB Pin)	T_A = 0°C to 70°C	•	790	800	810	mV
		T_A = -40°C to 85°C	•	788	800	812	mV
	Current Amplifier Reference (at SW node)				160		mV
Error Amplifier							
	DC Gain				80		dB
GBWP	Gain-BW Product				25		MHz
S/R	Slew Rate	10pF across COMP to GND			8		V/µS.
	Output Voltage Swing	No Load	•	0.5		4.0	V
I_{FB}	FB Pin Source Current				1		µA
Gate Drive							
R_{HUP}	HDRV Pull-up Resistor	Sourcing	•		1.8	3.0	Ω
R_{HDN}	HDRV Pull-down Resistor	Sinking	•		1.8	3.0	Ω
R_{LUP}	LDRV Pull-up Resistor	Sourcing	•		1.8	3.0	Ω
R_{LDN}	LDRV Pull-down Resistor	Sinking	•		1.2	2.0	Ω

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Electrical Characteristics (Continued)

Unless otherwise noted, V_{CC} = 5V, T_A = 25°C, using circuit in Figure 1.

The '•' denotes that the specifications apply to the full ambient operating temperature range. See Notes 4 and 5.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Protection/Disable							
I_{LIM}	ILIMIT Source Current			9	10	11	µA
I_{SWPD}	SW Pull-down Current	SW = 1V, EN = 0V			2		mA
V_{UV}	Under-Voltage Threshold	As % of set point; 2µS noise filter	•	65	75	80	%
V_{OV}	Over-Voltage Threshold	As % of set point; 2µS noise filter	•	110	1[illegible]	[illegible]20	%
TSD	Thermal Shutdown				[illegible]60		°C
	Enable Threshold Voltage	Enable Condition	•	[illegible]0			V
	Enable Threshold Voltage	Disable Condition				[illegible].8	V
	Enable Source Current	V_{CC} = 5V			50		µA
LDO[7]							
V_{LDOREF}	Reference Voltage (measured at FBLDO pin)	T_A = 0°C to 70°C	•	775	800	825	mV
		T_A = -40°C [illegible]°C	•	770	[illegible]0	830	mV
	Regulation	0A ≤ I_{LOA} ≤ 5A	•	1.17	1.2	1.23	V
V_{LDO_DO}	Drop out Voltage	I_{LOA} [illegible]5A and R_{DS-ON} < 50mΩ				0.3	V
	External Gate Drive	V_{C} [illegible]75V				4.5	V
		V_{C} [illegible]5.[illegible]V				5.3	V
	Gate Drive Source Current				1.2		mA
	Gate Drive Sink Current				400		µA

Notes:

4. All limits at operating temperature extremes are guaranteed by design, characterization, and statistical quality control.
5. AC specifications guaranteed by design/characterization (not production tested).
6. For a case when V_{CC} is higher than the typical 5V $V_{CC;}$ voltage observed at VCC pin when the internal shunt regulator is sinking current to keep voltage on VCC pin constant.
7. Test Conditions: V_{LDO_IN} = 1.5V and V_{LDO_OUT} = 1.2V

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Typical Performance Characteristics

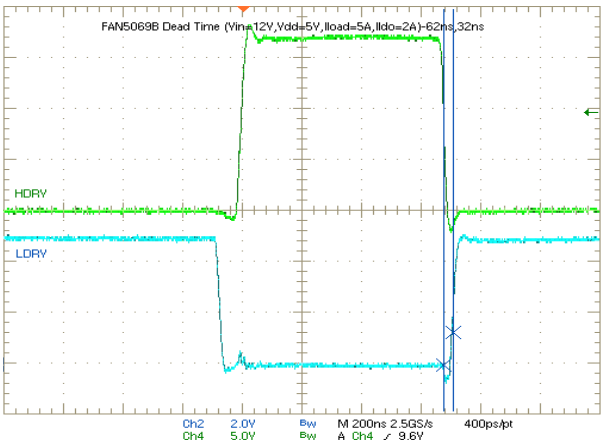

Figure 3. Dead Time Waveform

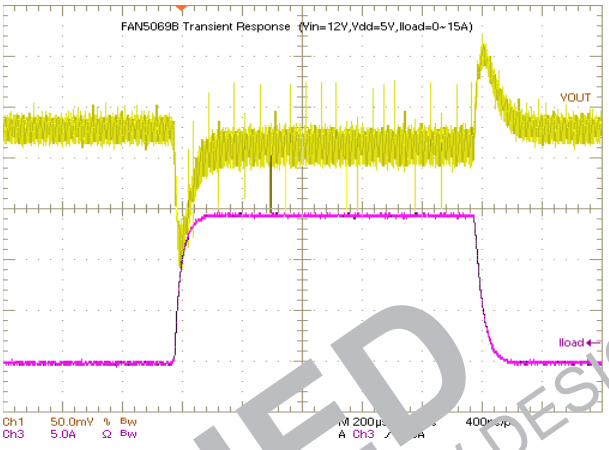

Figure 6. PWM Load Transient (0 to 15A)

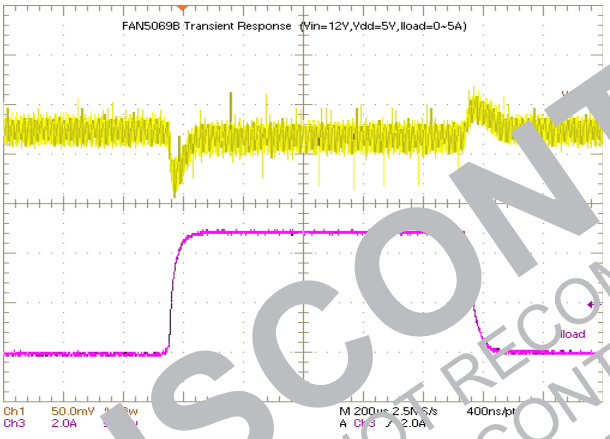

Figure 4. PWM Load Transient (0 to 5A)

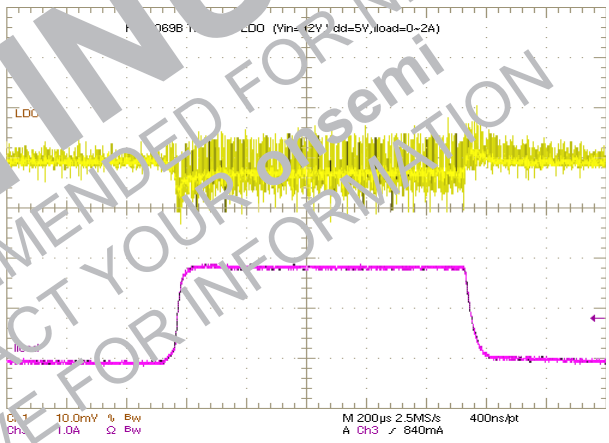

Figure 7. LDO Load Transient (0 to 2A)

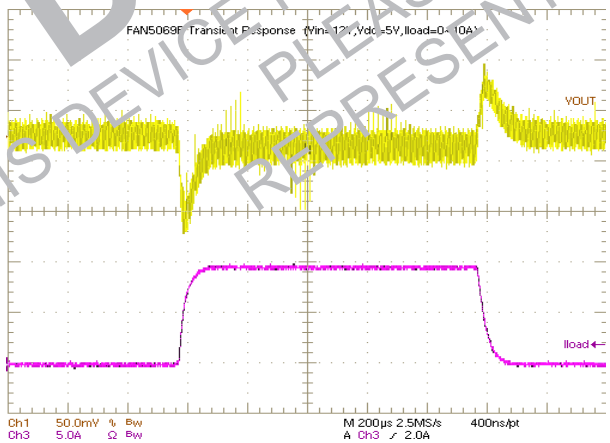

Figure 5. PWM Load Transient (0 to 10A)

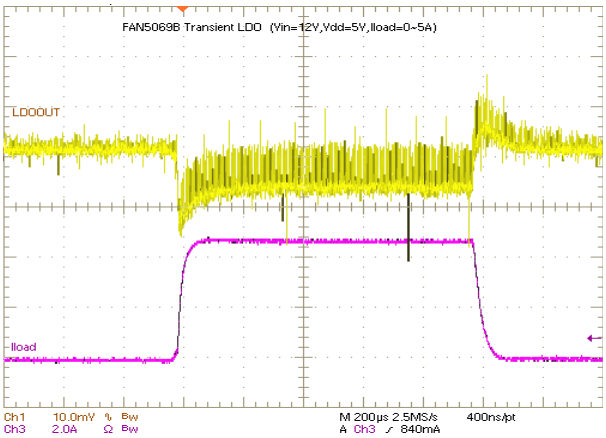

Figure 8. LDO Load Transient (0 to 5A)

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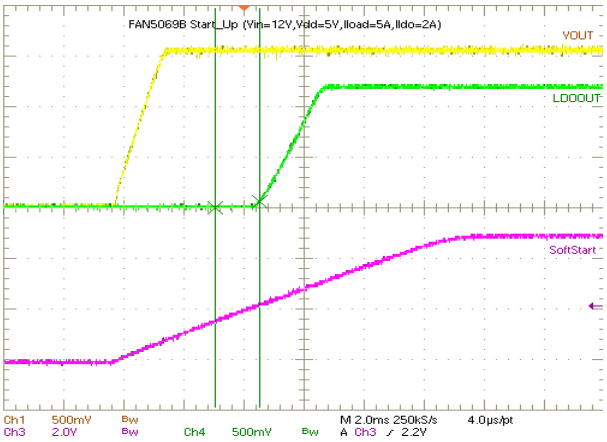

Figure 9. PWM/LDO Power Up

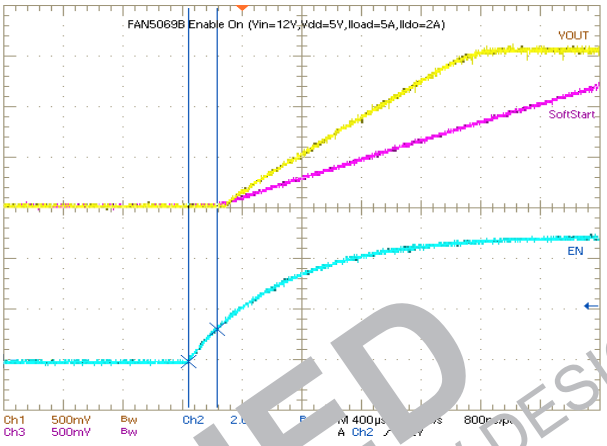

Figure 12. Enable ON (I_{PWM} = 5A)

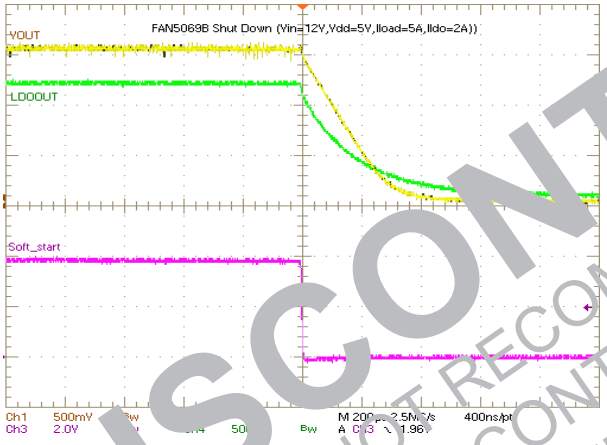

Figure 10. PWM/LDO Power Down

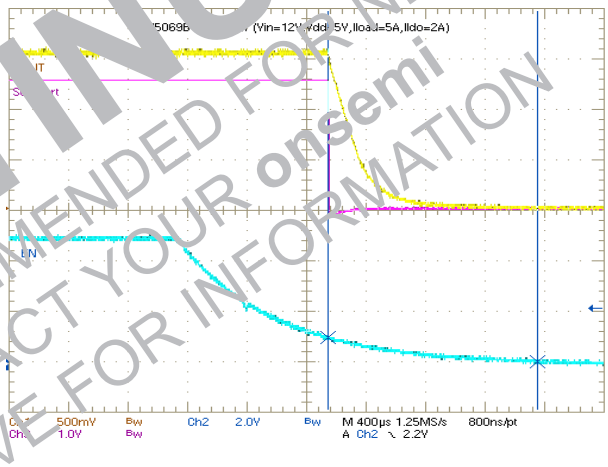

Figure 13. Enable OFF (I_{PWM} = 5A)

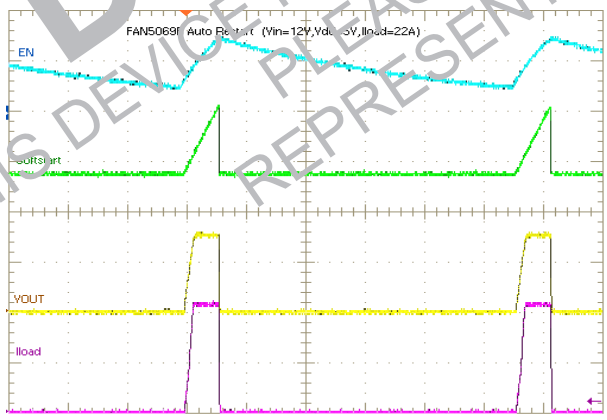

Figure 11. Auto Restart

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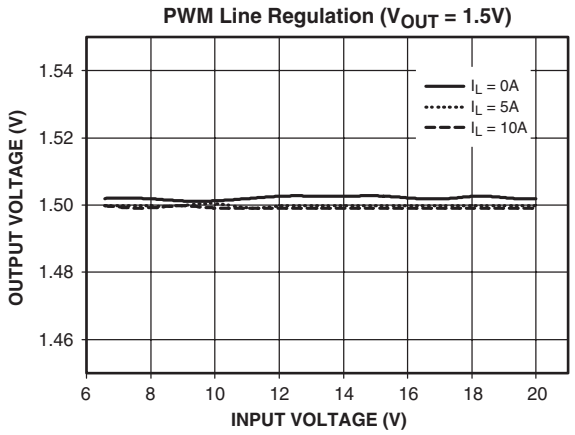

Figure 14. PWM Line Regulation

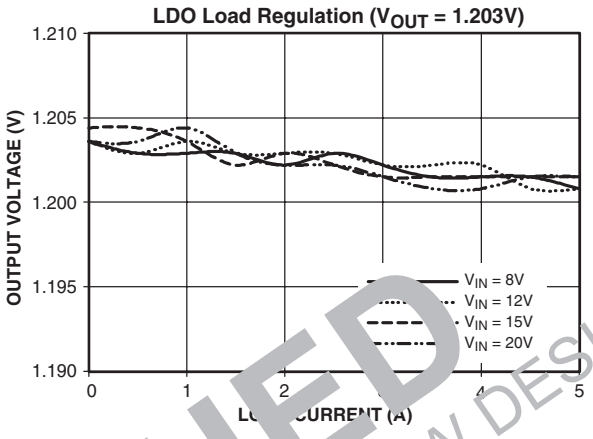

Figure 17. LDO Load Regulation

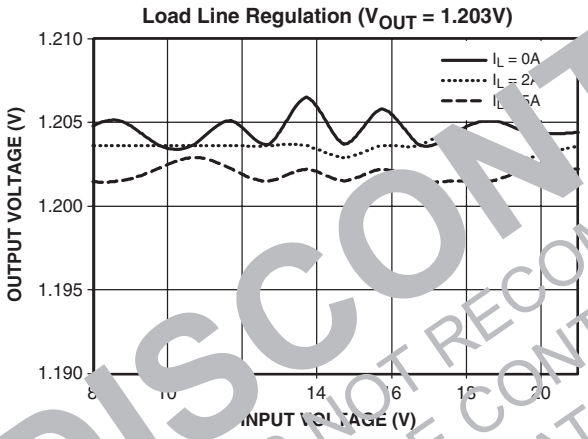

Figure 15. LDO Line Regulation

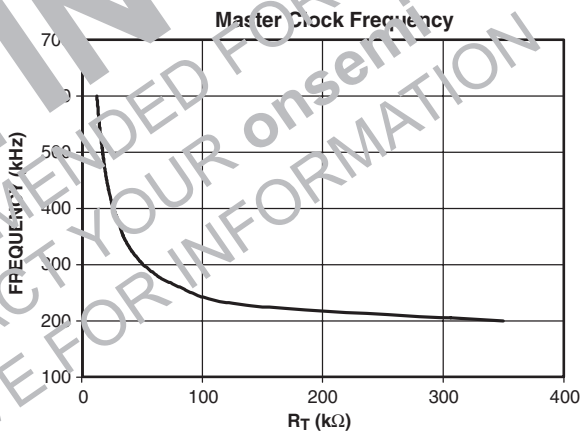

Figure 18. R_T vs. Frequency

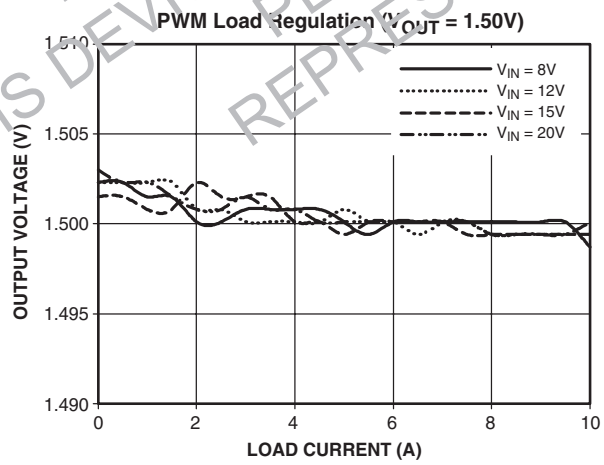

Figure 16. PWM Load Regulation

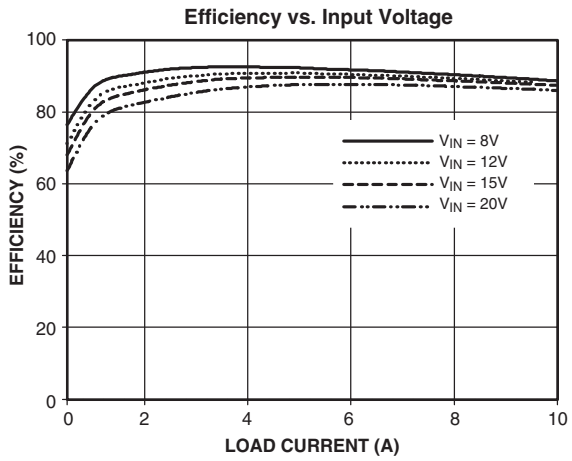

Figure 19. 1.5V PWM Efficiency

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Block Diagram

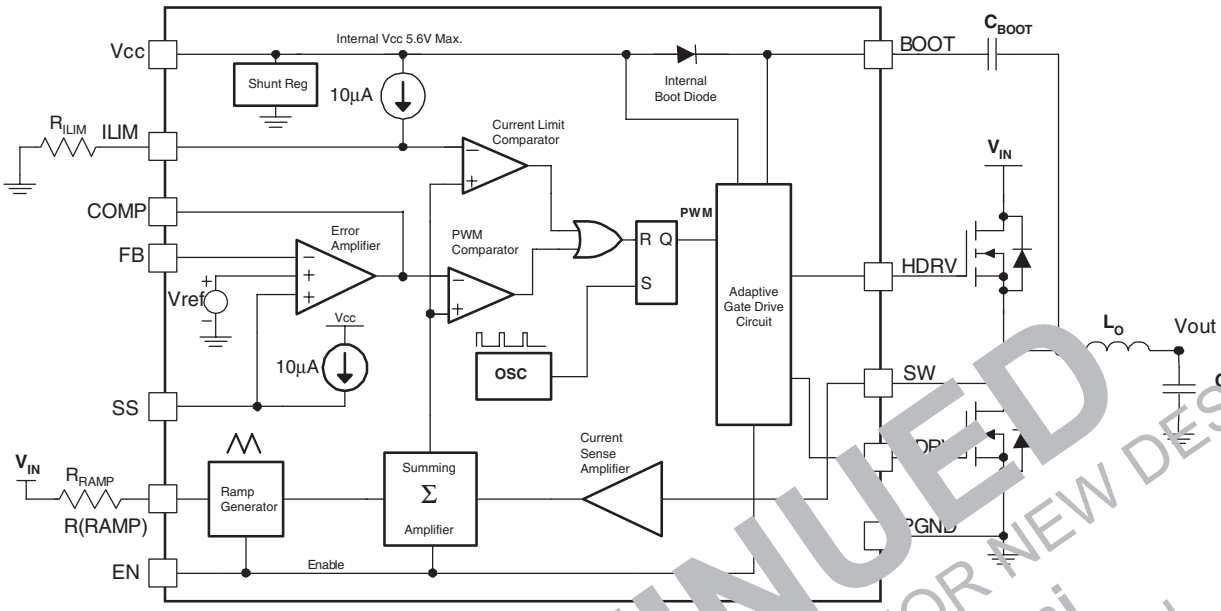

Figure 1. Block Diagram

Detailed Operation Description

FAN5069 combines a high-efficiency, fixed-frequency PWM controller designed for single-phase synchronous buck Point-Of-Load converters with an integrated LDO controller to support GTL type loads. This controller is ideally suited to deliver low-voltage, high-current power supplies needed in desktop computers, notebooks, workstations, and servers. The controller comes with an integrated boot diode which helps reduce component cost and increase space savings. With this controller, the input to the power supply can be varied from 3V to 24V and the output voltage can be set to regulate at 0.8V to 15V on the switcher output. The LDO output can be configured to regulate between 0.6V to 3V and the input to the LDO can be from 1.5V to 5V, respectively. An internal shunt regulator at the VCC pin facilitates the controller operation from either a 5V or 12V power source.

V_{CC} Bias Supply

FAN5069 can be configured to operate from 5V or 12V for V_{CC}. When 5V supply is used for V_{CC}, no resistor is required to be connected between the supply and the V_{CC}. When the 12V supply is used, a resistor R_{VCC} is connected between the 12V supply and the V_{CC}, as shown in Figure 1. The internal shunt regulator at the VCC pin is capable of sinking 150mA of current to ensure that the controller's internal V_{CC} is maintained at 5.6V maximum.

Choose a resistor such that:

- It is rated to handle the power dissipation.
- Current sunk within the controller is minimized to prevent IC temperature rise.

R_{VCC} Selection (IC)

The selection of R_{VCC} is dependent on:

- Variation of the 12V supply
- Gate charge of the top and bottom FETs (Q_{FET})
- Switching frequency (F_{SW})
- Shunt regulator minimum current (1mA)
- Quiescent current of the IC (I_Q)

Calculate R_{VCC} based on the minimum input voltage for the V_{CC}:

$$R_{VCC} = \frac{Vin_{MIN} - 5.6}{(I_Q + 1 \bullet 10^{-3} + Q_{FET} \bullet F_{SW} \bullet 1.2)} \quad \text{(EQ. 1)}$$

For a typical example, where: Vin_{MIN} = 11.5V, I_Q = 3mA, Q_{FET} = 30nC, F_{SW} = 300KHz, R_{VCC} is calculated to be 398.65Ω.

PWM Section

The FAN5069's PWM controller combines the conventional voltage mode control and current sensing through lower MOSFET R_{DS_ON} to generate the PWM signals. This method of current sensing is loss-less and cost effective. For more accurate current sense requirements, an optional external resistor can be connected with the bottom MOSFET in series.

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PWM Operation

Refer to Figure 20 for the PWM control mechanism. The FAN5069 uses the summing mode method of control to generate the PWM pulses. The amplified output of the current-sense amplifier is summed with an internally generated ramp and the combined signal is amplified and compared with the output of the error amplifier to get the pulse width to drive the high-side MOSFET. The sensed current from the previous cycle is used to modulate the output of the summing block. The output of the summing block is also compared against the voltage threshold set by the R_{LIM} resistor to limit the inductor current on a cycle-by-cycle basis. The controller facilitates external compensation for enhanced flexibility.

Initialization

When the PWM is disabled, the SW node is connected to GND through an internal 500Ω MOSFET to slowly discharge the output. As long as the PWM controller is enabled, this internal MOSFET remains OFF.

Soft-Start (PWM and LDO)

When V_{CC} exceeds the UVLO threshold and EN is high, the circuit releases SS and enables the PWM regulator. The capacitor connected to the SS pin and GND is charged by a 10µA internal current source, causing the voltage on the capacitor to rise. When this voltage exceeds 1.2V, all protection circuits are enabled. When this voltage exceeds 2.2V, the LDO output is enabled. The input to the error amplifier at the non-inverting pin is clamped by the voltage on the SS pin until it crosses the reference voltage.

The time it takes the PWM output to reach regulation (T_{Rise}) is calculated using the following equation:

$$T_{Rise} = 8 \times 10^{-2} \times C_{SS} \quad (C_{SS} \text{ is in µf}) \qquad \text{(EQ. 2)}$$

Oscillator Clock Frequency (PWM)

The clock frequency on the oscillator is set using an external resistor connected between R(T) pin and ground. The frequency follows the graph, as shown in Figure 19. The minimum clock frequency is 200KHz, which is when R(T) pin is left open. Select the value of R(T) as shown in the equation below. This equation is valid for all F_{OSC} > 200KHz.

$$R(T) = \frac{5 \times 10^{9}}{(F_{OSC} - 200 \times 10^{3})} \Omega \qquad \text{(EQ. 3)}$$

where F_{OSC} is in Hz.

For example, for F_{OSC} = 300kHz, R(T) = 50KΩ.

R_{RAMP} Selection and Feed-Forward Operation

The FAN5069 provides for input voltage feed-forward compensation through R_{RAMP}. The value of R_{RAMP} effectively changes the slope of the internal ramp, minimizing the variation of the PWM modulator gain when input voltage varies. The R_{RAMP} also has an effect on the current limit, as can be seen in the R_{LIM} equation (EQ. 5). The R_{RAMP} value can be approximated using the following equation:

$$R_{RAMP} = \frac{V_{IN} - 1.8}{6.3 \bullet 10^{-8} \bullet Fosc} K\Omega \qquad \text{(EQ. 4)}$$

where F_{OSC} is in Hz. For example, for F_{OSC} = 300kHz and V_{IN} = 12V, $R_{RAMP} \approx$ 540KΩ.

Gate Drive Section

The adaptive gate control logic translates the internal PWM control signal into the MOSFET gate drive signals and provides necessary amplification, level shifting, and shoot-through protection. It also has functions that help optimize the IC performance over a wide range of operating conditions. Since the MOSFET switching time can vary dramatically from device to device and with the input voltage, the gate control logic provides adaptive deadtime by monitoring the gate-to-source voltages of both upper and lower MOSFETs. The lower MOSFET drive is not turned on until the gate-to-source voltage of the upper MOSFET has decreased to less than approximately 1V. Similarly, the upper MOSFET is not turned on until the gate-to-source voltage of the lower MOSFET has decreased to less than approximately 1V. This allows a wide variety of upper and lower MOSFETs to be used without a concern for simultaneous conduction, or shoot-through.

A low impedance path between the driver pin and the MOSFET gate is recommended for the adaptive dead-time circuit to work properly. Any delay along this path reduces the delay generated by the adaptive dead-time circuit, thereby increasing the chances for shoot-through.

Protection

In the FAN5069, the converter is protected against extreme overload, short-circuit, over-voltage, and under-voltage conditions. All of these conditions generate an internal "fault latch" which shuts down the converter. For all fault conditions both the high-side and the low-side drives are off except in the case of OVP where the low-side MOSFET is turned on until the voltage on the FB pin goes below 0.4V. The fault latch can be reset either by toggling the EN pin or recycling V_{CC} to the chip.

Over Current Limit (PWM)

The PWM converter is protected against overloading through a cycle-by-cycle current limit set by selecting R_{ILIM} resistor. An internal 10µA current source sets the threshold voltage for the output of the summing amplifier. When the summing amplifier output exceeds this threshold level, the current limit comparator trips and the PWM starts skipping pulses. If the current limit tripping occurs for 16 continuous clock cycles, a fault latch is set and the controller shuts down the converter. This shutdown fea-

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ture is disabled during the start-up until the voltage on the SS capacitor crosses 1.2V.

To achieve current limit, the FAN5069 monitors the inductor current during the OFF time by monitoring and holding the voltage across the lower MOSFET. The voltage across the lower MOSFET is sensed between the PGND and the SW pins.

The output of the summing amplifier is a function of the inductor current, R_{DS_ON} of the bottom FET and the gain of the current sense amplifier. With the R_{DS_ON} method of current sensing, the current limit can vary widely from unit to unit. R_{DS_ON} not only varies from unit to unit, but also has a typical junction temperature coefficient of about 0.4%/°C (consult the MOSFET datasheet for actual values). The set point of the actual current limit decreases in proportion to increase in MOSFET die temperature. A factor of 1.6 in the current limit set point typically compensates for all MOSFET R_{DS_ON} variations, assuming the MOSFET's heat sinking keeps its operating die temperature below 125°C.

For more accurate current limit setting, use resistor sensing. In a resistor sensing scheme, an appropriate current sense resistor is connected between the source terminal of the bottom MOSFET and PGND.

Set the current limit by choosing R_{ILIM} as follows:

$$R_{ILIM} = \left[128 + \frac{K1 \bullet I_{MAX} \bullet R_{DSON} \bullet 10^3}{1.43} + \left(\left(1 - \frac{1.8}{Vin}\right) \bullet \frac{V_{OUT} \bullet 33.2 \bullet 10^{11}}{F_{SW} \bullet R_{RAMP}}\right)\right] \quad \text{(EQ. 5)}$$

where R_{ILIM} is in KΩ.

I_{MAX} is the maximum load current.

K1 is a constant to accommodate for the variation of MOSFET $R_{DS(ON)}$ (typically 1.6).

With K1 = 1.6, I_{MAX} = 20A, $R_{DS(ON)}$ = 7mΩ, V_{IN} = 24V, V_{OUT} = 1.2V, F_{SW} = 300 KHz, R_{RAMP} = 400 KΩ, R_{ILIM} calculates to be 323.17KΩ.

Auto Restart (PWM)

The FAN5069 supports two modes of response when the internal fault latch is set. The user can configure it to keep the power supply latched in the OFF state OR in the Auto Restart mode. When the EN pin is tied to V_{CC}, the power supply is latched OFF. When the EN pin is terminated with a 100nF to GND, the power supply is in Auto Restart mode. The table below describes the relationship between PWM restart and setting on EN pin. Do not leave the EN pin open without any capacitor.

EN Pin	PWM/Restart
Pull to GND	OFF
V_{CC}	No restart after fault
Cap to GND	Restart after TDELAY (Sec.) = 0.85 x C where C is in µF

The fault latch can also be reset by recycling the V_{CC} to the controller.

Under Voltage Protection (PWM)

The PWM converter output is monitored constantly for under voltage at the FB pin. If the voltage on the FB pin stays lower than 75% of internal Vref for 16 clock cycles, the fault latch is set and the converter shuts down. This shutdown feature is disabled during start-up until the voltage on the SS capacitor reaches 1.2V.

Over Voltage Protection (PWM)

The PWM converter output voltage is monitored constantly at the FB pin for over voltage. If the voltage on the FB pin stays higher than 115% of internal V_{REF} for two clock cycles, the controller turns OFF the upper MOSFET and turns ON the lower MOSFET. This crowbar action stops when the voltage on the FB pin reaches 0.4V to prevent the output voltage from becoming negative. This over-voltage protection (OVP) feature is active as soon as the voltage on the EN pin becomes high.

Turning ON the low-side MOSFETs on an OVP condition pulls down the output, resulting in a reverse current, which starts to build up in the inductor. If the output over-voltage is due to failure of the high-side MOSFET, this crowbar action pulls down the input supply or blows its fuse, protecting the system, which is very critical.

During soft-start, if the output overshoots beyond 115% of V_{REF}, the output voltage is brought down by the low-side MOSFET until the voltage on the FB pin goes below 0.4V. The fault latch is NOT set until the voltage on the SS pin reaches 1.2V. Once the fault latch is set, the converter shuts down.

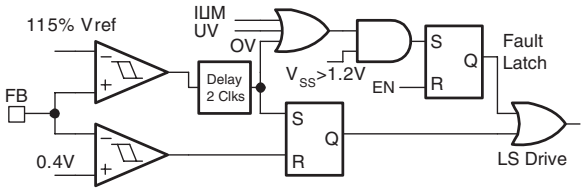

Figure 21. Over-Voltage Protection

Thermal Fault Protection

The FAN5069 features thermal protection where the IC temperature is monitored. When the IC junction temperature exceeds +160°C, the controller shuts down and when the junction temperature gets down to +125°C, the converter restarts.

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LDO Section

The LDO controller is designed to provide ultra low voltages, as low as 0.8V for GTL-type loads. The regulating loop employs a very fast response feedback loop and small capacitors can be used to keep track of the changing output voltage during transients. For stable operation, the minimum capacitance on the output needs to be 100µF and the typical ESR needs to be around 100mΩ.

The maximum voltage at the gate drive for the MOSFET can reach close to 0.5V below the V_{CC} of the controller. For example, for a 1.2V output, the minimum enhancement voltage required with 4.75V on V_{CC} is 3.05V (4.75V-0.5V-1.2V = 3.05V). The drop-out voltage for the LDO is dependent on the load current and the MOSFET chosen. It is recommended to use low enhancement voltage MOSFETs for the LDO. In applications where LDO is not needed, pull up the FBLDO pin (Pin #1) higher than 1V to disable the LDO.

The soft-start on the LDO output (ramp) is controlled by the capacitor on the SS pin to GND. The LDO output is enabled only when the voltage on the SS pin reaches 2.2V. Refer to Figure 9 for start-up waveform.

Design Section

General Design Guidelines

Establishing the input voltage range and maximum current loading on the converter before choosing the switching frequency and the inductor ripple current is highly recommended. There are trade-offs in choosing an optimum switching frequency and the ripple current.

The input voltage range should accommodate the worst-case input voltages at which the converter may ever operate. The voltage needs to account for the cable drop encountered from the source to the converter. Typically, the converter efficiency tends to be higher at lower input voltage conditions.

When selecting maximum loading conditions, consider the transient and steady-state (continuous) loading separately. The transient loading affects the selection of the inductor and the output capacitors. Steady state loading affects the selection of MOSFETs, input capacitors, and other critical heat-generating components.

The selection of switching frequency is challenging. While higher switching frequency results in smaller components, it also results in lower efficiency. Ideal selection of switching frequency takes into account the maximum operating voltage. The MOSFET switching losses are directly proportional to F_{SW} and the square function of the input voltage.

When selecting the inductor, consider the minimum and maximum load conditions. Lower inductor values produce better transient response, but result in higher ripple and lower efficiency due to high RMS currents. Optimum minimum inductance value enables the converter to operate at the boundary of continuous and discontinuous conduction modes.

Setting the Output Voltage (PWM)

The internal reference for the PWM controller is at 0.8V. The output voltage of the PWM regulator can be set in the range of 0.8V to 90% of its power input by an external resistor divider. The output is divided down by an external voltage divider to the FB pin (for example, R1 and R_{BIAS} as in Figure 24). The output voltage is given by the following equation:

$$V_{OUT} = 0.8V \times \left(1 + \frac{R1}{R_{BIAS}}\right) \quad \text{(EQ. 6)}$$

To minimize noise pickup on this node, keep the resistor to GND (R_{BIAS}) below 10kΩ.

Inductor Selection (PWM)

When the ripple current, switching frequency of the converter, and the input-output voltages are established, select the inductor using the following equation:

$$L_{MIN} = \frac{\left(V_{OUT} - \frac{V_{OUT}^2}{V_{IN}}\right)}{I_{Ripple} \times F_{SW}} \quad \text{(EQ. 7)}$$

where I_{Ripple} is the ripple current.

This number typically varies between 20% to 50% of the maximum steady-state load on the converter.

When selecting an inductor from the vendors, select the inductance value which is close to the value calculated at the rated current (including half the ripple current).

Input Capacitor Selection (PWM)

The input capacitors must have an adequate RMS current rating to withstand the temperature rise caused by the internal power dissipation. The combined RMS current rating for the input capacitor should be greater than the value calculated using the following equation:

$$I_{INPUT(RMS)} = I_{LOAD(MAX)} \times \left(\sqrt{\frac{V_{OUT}}{V_{IN}} - \left(\frac{V_{OUT}}{V_{IN}}\right)^2}\right) \quad \text{(EQ. 8)}$$

Common capacitor types used for such application include aluminum, ceramic, POS CAP, and OSCON.

Output Capacitor Selection (PWM)

The output capacitors chosen must have low enough ESR to meet the output ripple and load transient requirements. The ESR of the output capacitor should be lower than both of the values calculated below to satisfy both the transient loading and steady-state ripple conditions as given by the following equation:

$$ESR \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}} \quad \text{and} \quad ESR \le \frac{V_{Ripple}}{I_{Ripple}} \quad \text{(EQ. 9)}$$

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In the case of aluminum and polymer based capacitors, the output capacitance is typically higher than normally required to meet these requirements. While selecting the ceramic capacitors for the output; although lower ESR can be achieved easily, higher capacitance values are required to meet the $V_{OUT(MIN)}$ restrictions during a load transient. From the stability point of view, the zero caused by the ESR of the output capacitor plays an important role in the stability of the converter.

Output Capacitor Selection (LDO)

For stable operation, the minimum capacitance of 100µF with ESR around 100mΩ is recommended. For other values, contact the factory.

Power MOSFET Selection (PWM)

The FAN5069 is capable of driving N-Channel MOSFETs as circuit switch elements. For better performance, MOSFET selection must address these key parameters:

- The maximum Drain-to-Source Voltage (V_{DS}) should be at least 25% higher than worst-case input voltage.
- The MOSFETs should have low Q_G, Q_{GD}, and Q_{GS}.
- The R_{DS_ON} of the MOSFETs should be as low as possible

In typical applications for a buck converter, the duty cycles are lower than 20%. To optimize the selection of MOSFETs for both the high-side and low-side, follow different selection criteria. Select the high-side MOSFET to minimize the switching losses and the low-side MOSFET to minimize the conduction losses due to the channel and the body diode losses. Note that the gate drive losses also affect the temperature rise on the controller.

For loss calculations refer to Fairchild's Application Note AN-6005 and the associated spreadsheet.

High-Side Losses

Losses in the MOSFET can be understood by following the switching interval of the MOSFET in Figure 22. MOSFET gate drive equivalent circuit is shown in Figure 23.

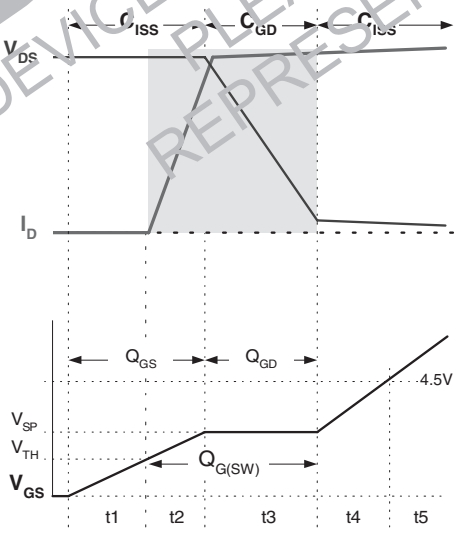

Figure 22. Switching Losses and Q_G

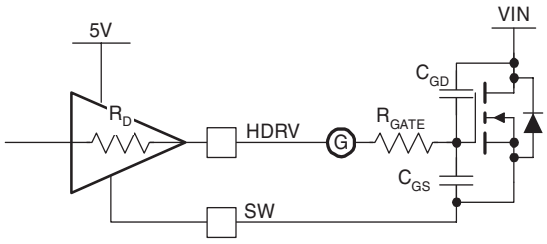

Figure 23. Drive Equivalent Circuit

The upper graph in Figure 22 represents Drain-to-Source Voltage (V_{DS}) and Drain Current (I_D) waveforms. The lower graph details Gate to Source Voltage (V_{GS}) vs. time with a constant current charging the gate. The x-axis is representative of Gate Charge (Q_G). $C_{ISS} = C_{GD} + C_{GS}$ and it controls t1, t2, and t4 timing. C_{GD} receives the current from the gate driver during t3 (as V_{DS} is falling). Obtain the gate charge (Q_G) parameters shown on the lower graph from the MOSFET datasheets.

Assume switching losses are about the same for both the rising edge and falling edge, Q1's switching losses occur during the shaded time when the MOSFET has voltage across it and current through it.

Losses are given by (EQ. 10), (EQ. 11), and (EQ. 12):

$$P_{UPPER} = P_{SW} + P_{COND} \quad \text{(EQ. 10)}$$

$$P_{SW} = \left(\frac{V_{DS} \times I_L}{2} \times 2 \times t_S\right) F_{SW} \quad \text{(EQ. 11)}$$

$$P_{COND} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT}^2 \times R_{DS(ON)} \quad \text{(EQ. 12)}$$

where P_{UPPER} is the upper MOSFET's total losses and P_{SW} and P_{COND} are the switching and conduction losses for a given MOSFET. $R_{DS(ON)}$ is at the maximum junction temperature (T_J) and t_S is the switching period (rise or fall time) and equals t2+t3 (Figure 22.).

The driver's impedance and C_{ISS} determine t2 while t3's period is controlled by the driver's impedance and Q_{GD}. Since most of t_S occurs when $V_{GS} = V_{SP}$, assume a constant current for the driver to simplify the calculation of t_S using the following equation:

$$t_S = \frac{Q_{G(SW)}}{I_{Driver}} \approx \frac{Q_{G(SW)}}{\left(\frac{V_{CC} - V_{SP}}{R_{Driver} + R_{Gate}}\right)} \quad \text{(EQ. 13)}$$

Most MOSFET vendors specify Q_{GD} and Q_{GS}. $Q_{G(SW)}$ can be determined as:

$Q_{G(SW)} = Q_{GD} + Q_{GS} - Q_{TH}$ where Q_{TH} is the gate charge required to reach the MOSFET threshold (V_{TH}).

Note that for the high-side MOSFET, V_{DS} equals V_{IN}, which can be as high as 20V in a typical portable application. Include the power delivered to the MOSFET's (P_{GATE}) in calculating the power dissipation required for the FAN5069.

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P_{GATE} is determined by the following equation:

$$P_{Gate} = Q_G \times V_{CC} \times F_{SW} \quad \text{(EQ. 14)}$$

where Q_G is the total gate charge to reach V_{CC}.

Low-Side Losses

Q2 switches on or off with its parallel schottky diode simultaneously conducting, so the $V_{DS} \approx 0.5V$. Since P_{SW} is proportional to V_{DS}, Q2's switching losses are negligible and Q2 is selected based on $R_{DS(ON)}$ alone.

Conduction losses for Q2 are given by the equation:

$$P_{COND} = (1 - D) \times I_{OUT}^2 \times R_{DS(ON)} \quad \text{(EQ. 15)}$$

where $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the MOSFET at the highest operating junction temperature and $D=V_{OUT}/V_{IN}$ is the minimum duty cycle for the converter.

Since $D_{MIN} < 20\%$ for portable computers, (1-D) ≈ 1 produces a conservative result, simplifying the calculation.

The maximum power dissipation ($P_{D(MAX)}$) is a function of the maximum allowable die temperature of the low-side MOSFET, the θ_{JA}, and the maximum allowable ambient temperature rise. $P_{D(MAX)}$ is calculated using the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}} \quad \text{(EQ. 16)}$$

θ_{JA} depends primarily on the amount of PCB area devoted to heat sinking.

Selection of MOSFET Snubber Circuit

The Switch node (SW) ringing is caused by fast switching transitions due to the energy stored in the parasitic elements. This ringing of the SW node couples to other circuits around the converter if they are not handled properly. To dampen the ringing, an R-C snubber is connected across the SW node and the source of the low-side MOSFET.

R-C components for the snubber are selected as follows:

a) Measure the SW node ringing frequency (F_{ring}) with a low capacitance scope probe.

b) Connect a capacitor (C_{SNUB}) from SW node to GND so that it reduces this ringing by half.

c) Place a resistor (R_{SNUB}) in series with this capacitor. R_{SNUB} is calculated using the following equation:

$$R_{SNUB} = \frac{2}{\pi \times F_{ring} \times C_{SNUB}} \quad \text{(EQ. 17)}$$

d) Calculate the power dissipated in the snubber resistor as shown in the following equation:

$$P_{R(SNUB)} = C_{SNUB} \times V_{IN(MAX)}^2 \times F_{SW} \quad \text{(EQ. 18)}$$

where, $V_{IN(MAX)}$ is the maximum input voltage and FSW is the converter switching frequency.

The snubber resistor chosen should be derated to handle the worst-case power dissipation. **Do not use wire-wound resistors for R_{SNUB}.**

Loop Compensation

Typically the closed loop crossover frequency (F_{cross}), where the overall gain is unity, should be selected to achieve optimal transient and steady-state response to disturbances in line and load conditions. It is recommended to keep F_{cross} below fifth of the switching frequency of the converter. Higher phase margin tends to have a more stable system with more sluggish response to load transients. Optimum phase margin is about 60°, a good compromise between steady state and transient responses. A typical design should address variations over a wide range of load conditions and over a large sample of devices.

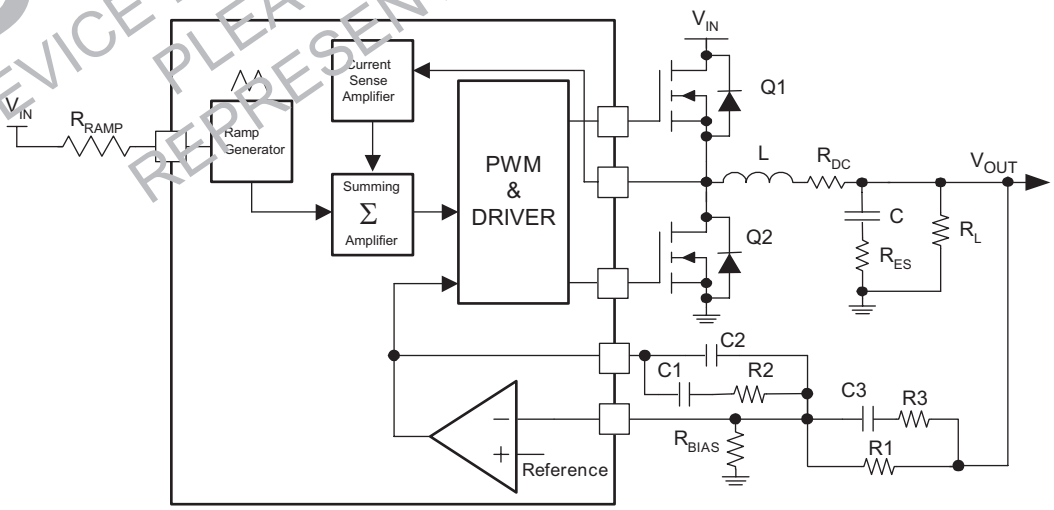

Figure 24. Closed-Loop System with Type-3 Network

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FAN5069 has a high gain error amplifier around which the loop is closed. Figure 24 shows a Type-3 compensation network. For Type-2 compensation, R3 and C3 are not used. Since the FAN5069 architecture employs summing current mode, Type-2 compensation can be used for most applications.

For further information about Type-2 compensation networks, refer to:

- *Venable, H. Dean, "The K factor: A new mathematical tool for stability analysis and synthesis," Proceedings of Powercon, March 1983.*

Note: For critical applications requiring wide loop bandwidth using very low ESR output capacitors, use Type-3 compensation.

Type 3 Feedback Component Calculations

Use the following steps to calculate feedback components:

Notation:

C_0 = Net Output Filter capacitance

$G_p(s)$ = Net Gain of Plant = control-to-output transfer function

L = Inductor Value

R_{DSON} = ON-state Drain-to Source Resistance of Low-side MOSFET

R_{es} = Net ESR of the Output Filter Capacitors

R_L = Load Resistance

T_s = Switching Period

V_{IN} = Input Voltage

F_{SW} = Switching Frequency

Equations:

Effective current sense resistance = $R_i = 7 \times R_{DSON}$ (EQ. 19)

Current modulator DC gain = $M_i = \frac{R_L}{R_i}$ (EQ. 20)

Effective ramp amplitude = $V_m = 3.33 \times 10^{-10} \times \frac{(V_{IN} - 1.8) \times T_s}{R_{ramp}}$ (EQ. 21)

Voltage modulator DC gain = $M_v = \frac{V_{IN}}{V_m}$ (EQ. 22)

Plant DC gain = $M_o = M_v \| M_i = \frac{M_v \times M_i}{M_v + M_i}$ (EQ. 23)

Sampling gain natural frequency = $\omega_n = \frac{\pi}{T_s}$ (EQ. 24)

Sampling gain quality factor (damping) = $Q_z = \frac{-2}{\pi}$ (EQ. 25)

Effective inductance = $L_e = \frac{M_O}{M_v} \times \left(L + \frac{M_v \times R_i}{\omega_n \times Q_z}\right)$ (EQ. 26)

$R_p = \frac{M_v \times R_i \times R_L}{M_v \times R_i + R_L} = (M_v \times R_i) \| R_L$ (EQ. 27)

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Poles and Zeros of Plant Transfer Function:

Plant zero frequency = $f_z = \frac{1}{2 \times \pi \times C_o \times R_{es}}$ (EQ. 28)

Plant 1st pole frequency = $f_{p1} = \frac{1}{2 \times \pi \times \left(C_o \times R_p + \frac{L_e}{R_L}\right)}$ (EQ. 29)

Plant 2nd pole frequency = $f_{p2} = \frac{1}{2 \times \pi} \times \left(\frac{1}{C_o \times R_L} + \frac{R_p}{L_e}\right)$ (EQ. 30)

Plant 3rd pole frequency = $f_{p3} = \frac{\omega_n^2 \times L_e}{2 \times \pi \times R_p}$ (EQ. 31)

Plant gain (magnitude) response:

$$|G_p|(f) = 20 \times \log M_0 + 10 \times \log\left[\frac{1 + \left(\frac{f}{f_z}\right)^2}{\left[1 + \left(\frac{f}{f_{p1}}\right)^2\right] \times \left[1 + \left(\frac{f}{f_{p2}}\right)^2\right] \times \left[1 + \left(\frac{f}{f_{p3}}\right)^2\right]}\right] \quad \text{(EQ. 32)}$$

Plant phase response:

$$\angle G_P(f) = \tan^{-1}\left(\frac{f}{f_z}\right) - \tan^{-1}\left(\frac{f}{f_{p1}}\right) - \tan^{-1}\left(\frac{f}{f_{p2}}\right) - \text{–tan}^{-1}\left(\frac{f}{f_{p3}}\right) \quad \text{(EQ. 33)}$$

Choose R1, R_{BIAS} to set the output voltage ... 0.6. Choose the zero crossover frequency F_{cross} of the overall loop. Typically F_{cross} should be less ... fifth ... F_{sw}. Choose the desired phase margin, typically between 60° to 90°.

Calculate plant gain at F_{cross} using EQ.34 ... substituting F_{cross} in place of *f*. The gain that the amplifier needs to provide to get the required cr... over ... given ...:

$$G_{AMP} = \frac{1}{|G_p|(F_{\quad})} \quad \text{(EQ. 34)}$$

The phase boost required is calculated as given in (EQ. 35)

$$\text{Phase boost} = M - \angle G_P(F_{cross}) - 90° \quad \text{(EQ. 35)}$$

where M is the desired phase margin in degrees.

The feedback component values are calculated as given in equations below:

$$K = \left\{\text{Tan}\left[\left(\frac{\text{Boost}}{4}\right) + 45°\right]\right\}^2 \quad \text{(EQ. 36)}$$

$$C2 = \frac{1}{2 \times \pi \times F_{cross} \times G_{AMP} \times R1} \quad \text{(EQ. 37)}$$

$$C1 = C2 \times (K - 1) \quad \text{(EQ. 38)}$$

$$C3 = \frac{1}{2 \times \pi \times F_{cross} \times \sqrt{K} \times R3} \quad \text{(EQ. 39)}$$

$$R2 = \frac{\sqrt{K}}{2 \times \pi \times F_{cross} \times C1} \quad \text{(EQ. 40)}$$

$$R3 = \frac{R1}{(K - 1)} \quad \text{(EQ. 41)}$$

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Design Tools

Fairchild application note **AN-6010** provides a PSPICE model and spreadsheet calculator for the PWM regulator, simplifying external component selections and verifying loop stability. The topics covered provide an understanding of the calculations in the spreadsheet.

The spreadsheet calculator, which is part of **AN-6010,** can be used to calculate all external component values for designing around FAN5069. The spreadsheet provides optimized compensation components and generates a Bode Plot to ensure loop stability.

Based on the input values entered, **AN-6010**'s PSPICE model can be used to simulate Bode Plots (for loop stability) as well as transient analysis to help customize the design for a wide range of applications.

Use Fairchild Application Note **AN-6005** for prediction of the losses and die temperatures for the power semiconductors used in the circuit.

AN-6010 and **AN-6005** can be downloaded from www.fairchildsemi.com/apnotes/.

Layout Considerations

The switching power converter layout needs careful attention and is critical to achieving low losses and clean and stable operation. Below are specific recommendations for good board layout:

- Keep the high-current traces and load connections as short as possible.
- Use thick copper boards whenever possible to achieve higher efficiency.
- Keep the loop area between the SW node, low-side MOSFET, inductor, and the output capacitor as small as possible.
- Route high dV/dt signals, such as SW node, away from the error amplifier input/output pin. Keep components connected to these pins close to the pins.
- Place ceramic de-coupling capacitor very close to the VCC pin.
- All input signals are referenced with respect to AGND pin. Dedicate one layer of the PCB for a GND plane. Use at least four layers for the PCB.
- Minimize GND loops in the layout to avoid EMI-related issues.
- Use wide traces for the lower gate drive to keep the drive impedances low.
- Connect PGND directly to the lower MOSFET source pin.
- Use wide land areas with appropriate thermal vias to effectively remove heat from the MOSFETs.
- Use snubber circuits to minimize high-frequency ringing at the SW nodes.
- Place the output capacitor for the LDO close to the source of the LDO MOSFET.

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Application Board Schematic

V_{IN} = 3 to 24V; V_{OUT} =1.5V at 20A.

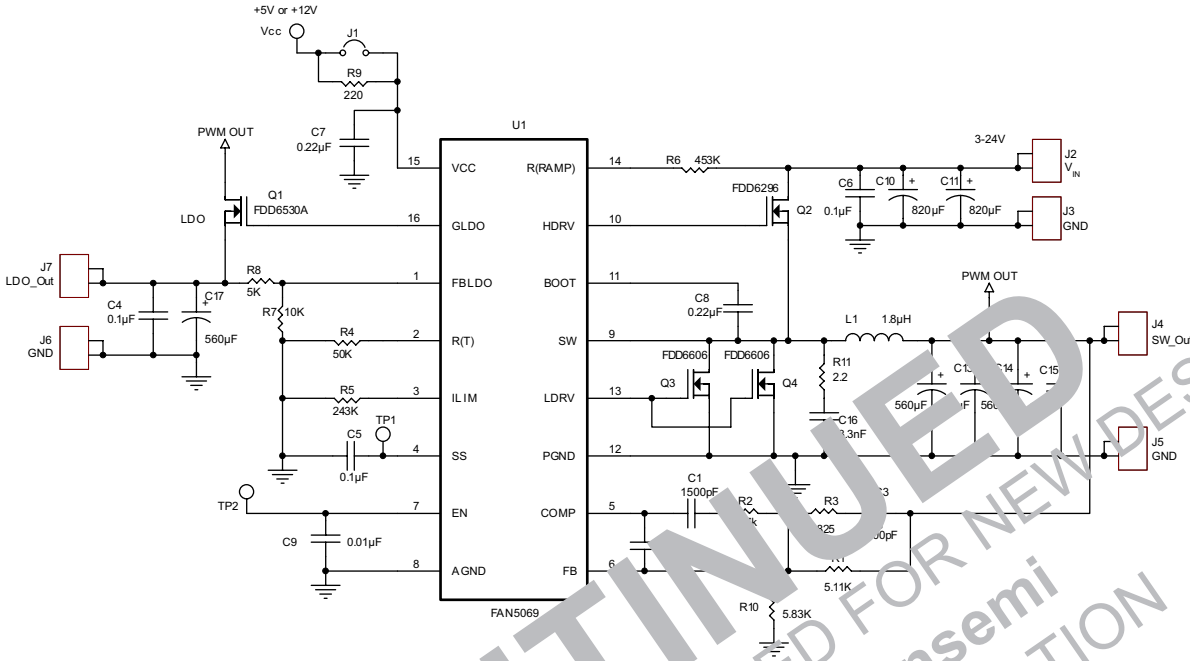

Figure 25. Application Board Schematic

Bill of Materials

Part Description	Quantity	Designator	Vendor	Vendor Part #
Capacitor, 1500pF, 20%, 25V, 0603,X7R	1	C1	Panasonic	PCC1774CT-ND
Capacitor, 220pF, 5%, 50V, 0603,NPO	1	C2	Panasonic	PCC221ACVCT-ND
Capacitor, 3300pF, 10%, 50V, 0603,X7R	1	C3	Panasonic	PCC1778CT-ND
Capacitor, 0.1µF, 10%, 25V, 0603,X7R	4	C4, C5, C6, C15	Panasonic	PCC2277CT-ND
Capacitor, 0.22µF, 10%, 50V, 0603,X7R	2	C7, C8	Panasonic	PCC1767CT-ND
Capacitor, 0.01µF, 10%, 50V, 0603,X7R	1	C9	Panasonic	PCC1784CT-ND
Capacitor, 820µF, 20%, 2.5V, 25V,20mOhm,1.96A	2	C10, C11	Nippon-Chemicon	KZH25VB820MHJ20
Capacitor, 820µF, 20%, 8X8, 2.5V,7mOhm,6.1A	1	C17	Nippon-Chemicon	PSC2.5VB820MH08
Capacitor, 560µF, 20%, 8X11.5, 4V,7mOhm,5.58A	3	C12, C13, C14	Nippon-Chemicon	PSA4VB560MH11
Capacitor, 1500pF, 10%, 50V, 0603,X7R	1	C16	Panasonic	PCC332BNCT-ND
Connector Header 0.100 Vertical, Tin - 2 Pin	1	J1	Molex	WM6436-ND
Terminal Quickfit Male .052"Dia.187" Tab	6	J2 - J7	Keystone	1212K-ND
Inductor, 1.8µH, 20%, 26Amps Max, 3.24mOhm	1	L1	Inter-Technical	SC5018-1R8M
MOSFET N-CH, 32 mΩ, 20V, 21A, D-PAK, FSID: FDD6530A	1	Q1	Fairchild Semiconductor	FDD6530A
MOSFET N-CH, 8.8 mΩ, 30V, 50A, D-PAK, FSID: FDD6296	1	Q2	Fairchild Semiconductor	FDD6296
MOSFET N-CH, 6 mΩ, 30V, 75A, D-PAK, FSID: FDD6606	2	Q3, Q4	Fairchild Semiconductor	FDD6606
Resistor, 5.11K, 1%, 1/16W	1	R1	Panasonic	P5.11KHCT-ND
Resistor, 12.7K, 1%, 1/16W	1	R2	Panasonic	P12.7KHCT-ND
Resistor, 825Ω, 1%, 1/16W	1	R3	Panasonic	P825HCT-ND
Resistor, 49.9K, 1%, 1/16W	1	R4	Panasonic	P49.9KHCT-ND
Resistor, 243K, 1%, 1/16W	1	R5	Panasonic	P243KHCT-ND
Resistor,453K, 1%, 1/16W	1	R6	Panasonic	P453KHCT-ND
Resistor,10K, 1%, 1/16W	1	R7	Panasonic	P10.0KHCT-ND
Resistor, 4.99K, 1%, 1/16W	1	R8	Panasonic	P4.99KHCT-ND
Resistor, 220Ω, 1%, 1/4W	1	R9	Panasonic	P200FCT-ND
Resistor, 5.90K, 1%, 1/16W	1	R10	Panasonic	P5.90KHCT-ND
Resistor, 2.2Ω, 1%, 1/4W	1	R11	Panasonic	P2.2ECT-ND
Connector Header 0.100 Vertical, Tin - 1 Pin	3	TP1,TP2, Vcc	Molex	WM6436-ND
IC, System Regulator, TSSOP16, FSID: FAN5069	1	U1	Fairchild Semiconductor	FAIRCHILD

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Typical Application Board Layout

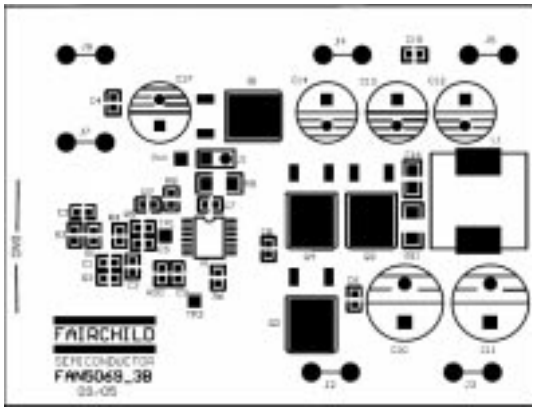

Figure 26. Assembly Diagram

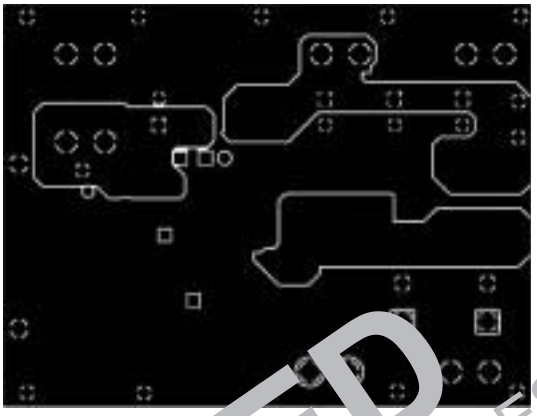

Figure 29. Mid Layer 2

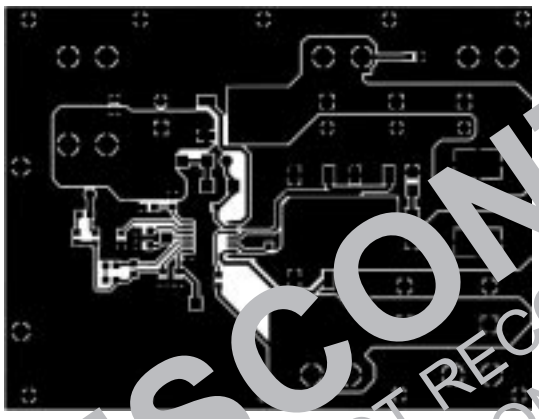

Figure 27. Top Layer



Figure 30. Bottom Layer

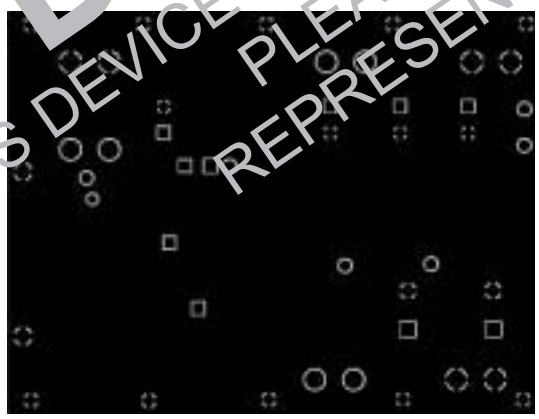

Figure 28. Mid Layer 1

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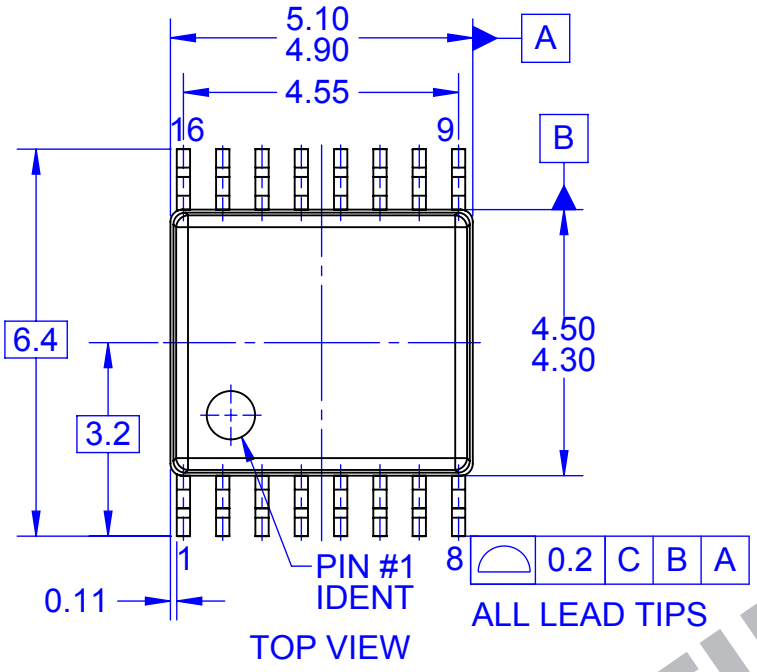

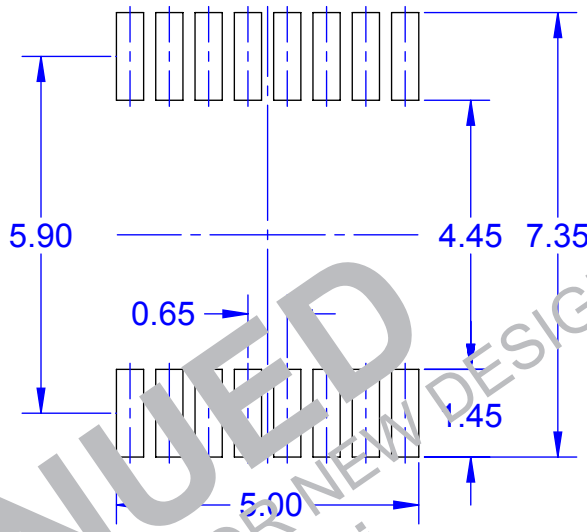

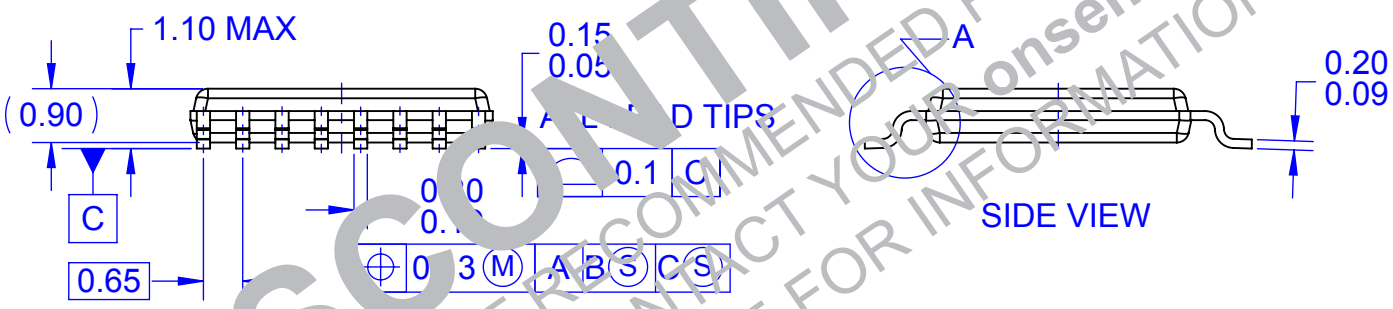

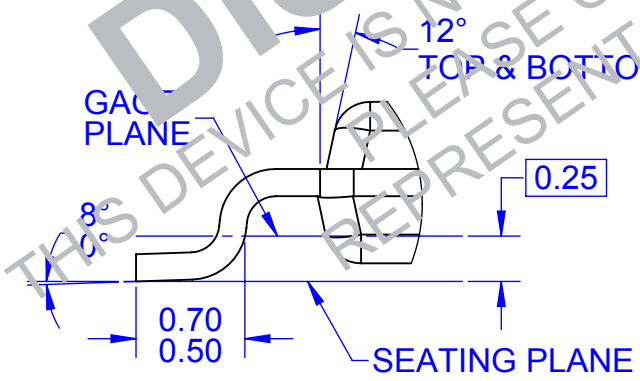

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