SM803XXX

Flexible Ultra-Low Jitter Clock Synthesizer

Features

- Generates up to 12 Differential or Single-Ended Outputs: Frequencies up to 850 MHz
- 75 fs Phase Jitter @ 156.25 MHz (1.875 MHz to 20 MHz)
- 180 fs Phase Jitter @ 156.25 MHz (12 kHz to 20 MHz)
- On-Chip Power Supply Regulation for Excellent Power Supply Noise Immunity
- Two High-performance PLL Synthesizers to Generate Multiple Frequencies
- Independently Programmable Output Logic and Frequency:
  - Output Logic: LVPECL, LVDS, HCSL, LVCMOS
- Selectable Input:
  - Crystal: 12 MHz to 62.5 MHz
  - Reference Input: 12 MHz to 850 MHz
- SPI Programmable (See Flex SPI Documentation)
- No External Crystal Oscillator Capacitors Required
- 2.5V to 3.3V Operating Power Supply
- Separate Output Power Supplies:
  - Each Bank can be at Different Power Supply Voltage Levels (4 Banks of 3 Outputs Each)
- Feedback Input Pins for use as Zero Delay Buffer
- Industrial Temperature Range, –40°C to +85°C
- Green, RoHS, and PFOS Compliant QFN Packages:
  - 48-pin 7 mm × 7 mm (10 Differential or Single Ended Outputs)
  - 76-pin, 9 mm × 9 mm (12 Differential or Single-Ended Outputs)
  - 84-pin, 7 mm × 7 mm (12 Differential or Single-Ended Outputs)

Applications

- 1/10/40/100 Gigabit Ethernet – (GbE)
- SONET/SDH
- PCI-Express Gen 1/2/3/4
- CPRI/OBSAI – Wireless Base Station
- Fibre Channel
- SAS/SATA
- DIMM (DDR2/DDR3/AMB)

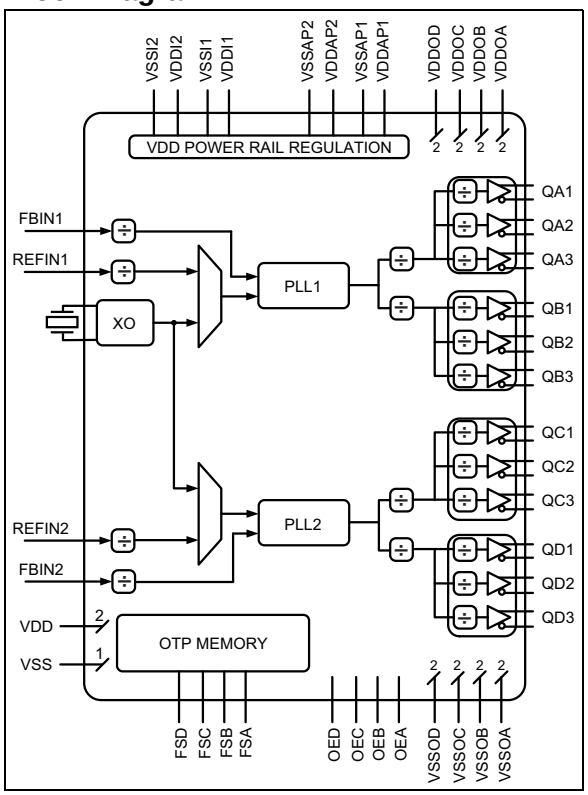
General Description

The SM803xxx is a dual-PLL clock generator that achieves ultra-low phase jitter (75 fs_{RMS}). With 12 total outputs and dividers on each output, this device can generate 12 different frequencies up to 850 MHz, from a low-cost quartz crystal or a reference clock input.

Each of 12 outputs can be independently programmed to LVPECL, LVDS, HCSL, or LVCMOS logic. For LVCMOS, only the true side of the channel is used.

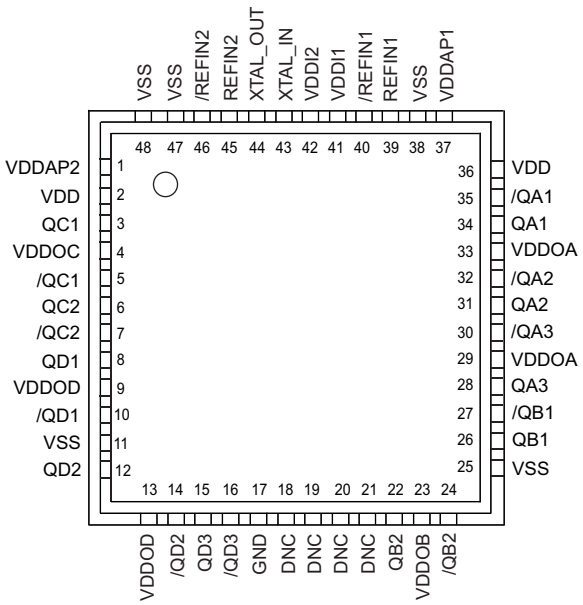
The SM803xxx is packaged in a 48-pin QFN with up to 10 outputs, a 76-pin QFN, or 84-pin QFN with 12 outputs.

Block Diagram

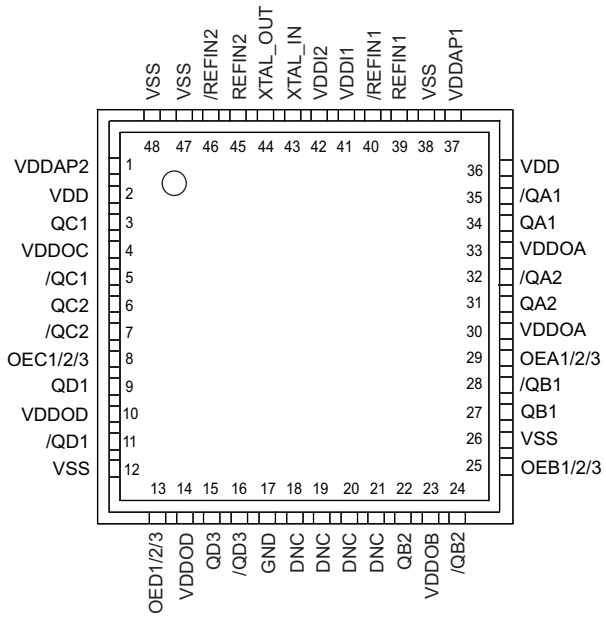


Package Types

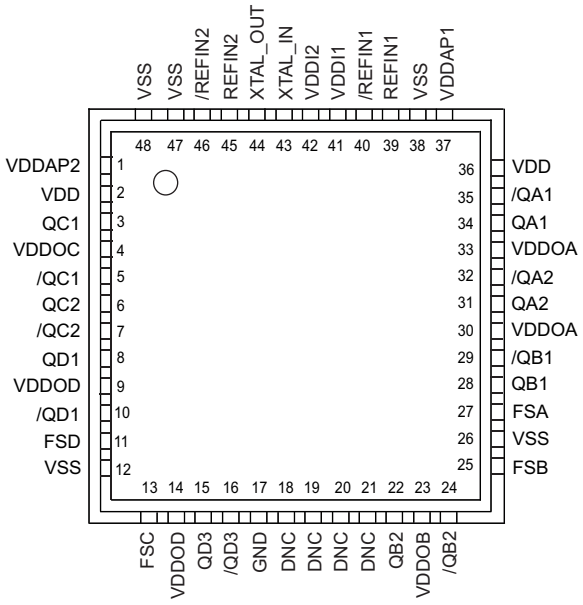
SM803XXX
Option 1: 10 outputs
48-Pin
7 mm x 7 mm QFN
Top View



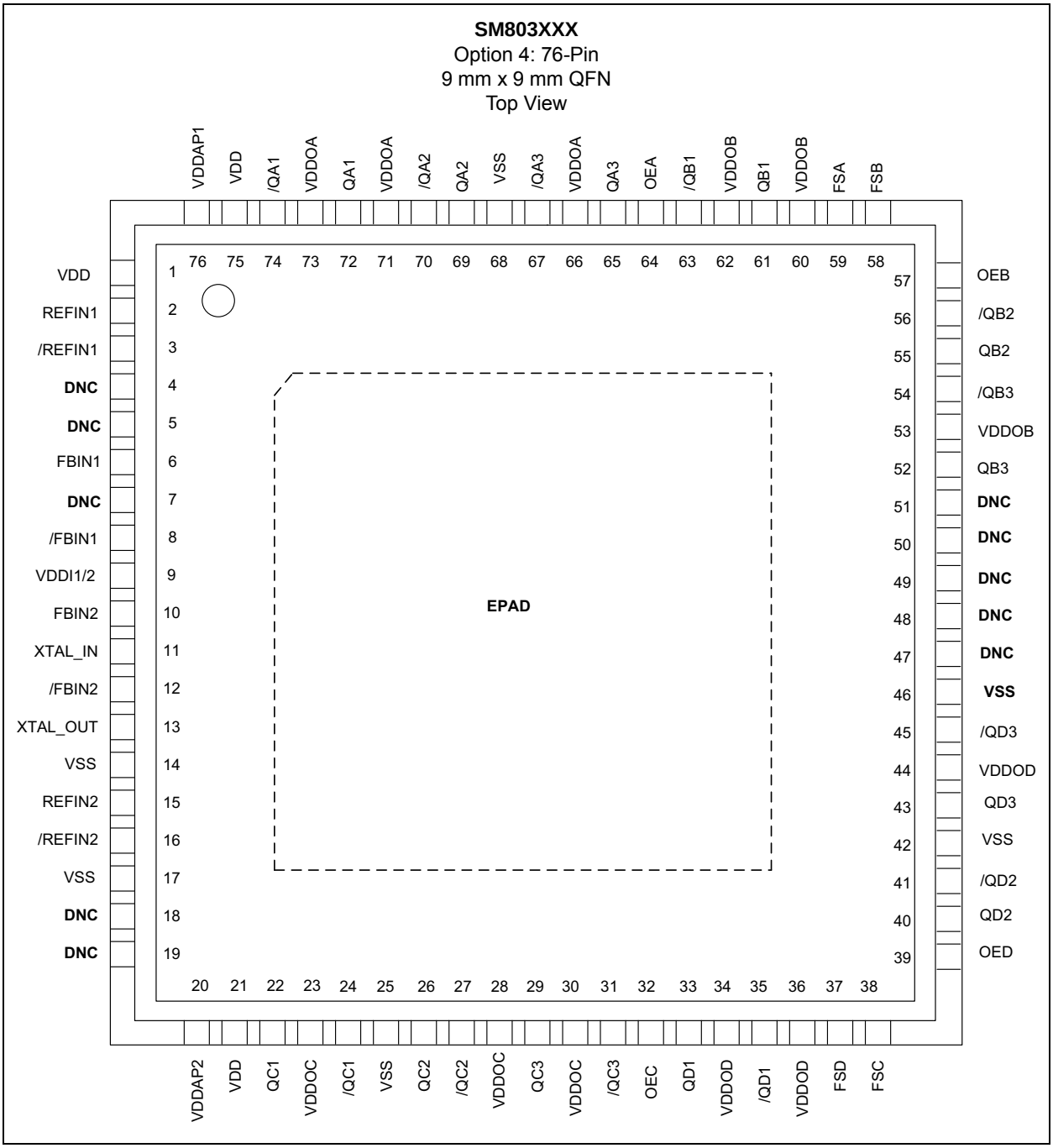
SM803XXX
Option 2: 8 outputs
with OE 48-Pin
7 mm x 7 mm QFN
Top View



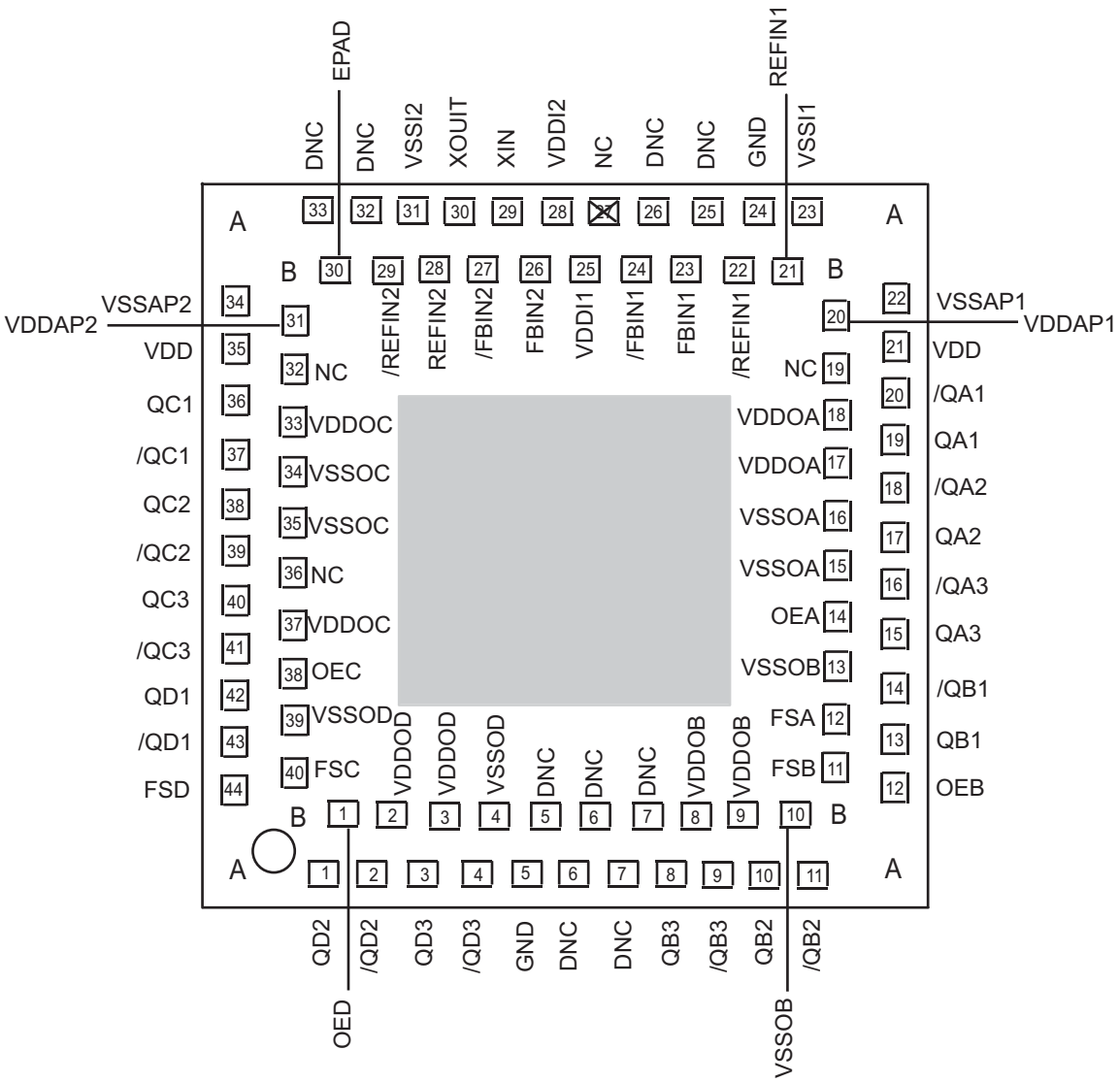
SM803XXX
Option 3: 8 outputs
with FSEL 48-Pin
7 mm x 7 mm QFN
Top View



SM803XXX
Option 4: 76-Pin
9 mm x 9 mm QFN
Top View



SM803XXX
Option 5: 84-Pin
7 mm x 7 mm QFN
Top View



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}, V_{DDA}, V_{DDI}, V_{DDO}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.50V to +4.6V
ESD Machine Model 200V
ESD Human Body Model 2000V

Operating Ratings ††

Supply Voltage (V_{DD}, V_{DDO}) ..... +2.375V to +3.465V

† **Notice:** Exceeding the absolute maximum ratings may damage the device.

†† **Notice:** The device is not guaranteed to function outside its operating ratings.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, typical values are for T_A = +25°C. The min. and max. values are for –40°C ≤ T_A ≤ +85°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}, V_{DDO}	2.375	2.5	2.625	V	2.5V Operation
		3.135	3.3	3.465		3.3V Operation
Analog Supply Voltage	V_{DDI1}, V_{DDI2}	2.375	—	3.465	V	—
PLL Core Voltage	V_{DDA}	2.375	—	3.465	V	—
PLL Core Current Consumption	I_{DDA}	—	—	60	mA	Per active PLL
Analog Current Consumption	I_{DDI}	—	—	10	mA	—
Output Stage Current Consumption	I_{DDO}	—	—	70	mA	Per output bank, unloaded
SPI and Miscellaneous Logic	I_{DD}	—	—	8	mA	—

LVPECL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{DDO} – 2V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	V_{DDO} – 1.35	V_{DDO} – 1.01	V_{DDO} – 0.8	V	50Ω to V_{DDO} – 2V
Output Low Voltage	V_{OL}	V_{DDO} – 2	V_{DDO} – 1.78	V_{DDO} – 1.6	V	50Ω to V_{DDO} – 2V
Peak-to-Peak Output Voltage	V_{SWING}	0.65	0.77	0.95	V	Figure 5-3

LVDS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 100Ω between Q and /Q.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Differential Output Voltage	V_{OD}	245	350	454	mV	Figure 5-3
Common Mode Voltage	V_{CM}	1.125	1.2	1.375	V	—
Output High Voltage	V_{OH}	1.248	1.375	1.602	V	—
Output Low Voltage	V_{OL}	0.898	1.025	1.252	V	—

HCSL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{SS}.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	660	700	850	mV	—
Output Low Voltage	V_{OL}	–150	0	27	mV	—
Crossing Point Voltage	V_{CROSS}	—	350	—	V	—

LVCMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{DDO}/2.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	V_{DD} – 0.8	—	—	V	Highest Drive (Default)
Output Low Voltage	V_{OL}	—	—	0.5	V	—
Input High Voltage	V_{IH}	V_{DD} – 0.7	—	V_{DD} + 0.3	V	—
Input Low Voltage	V_{IL}	V_{SS} – 0.3	—	0.3 × V_{DD}	V	—
Input High Current	I_{IH}	—	—	5	µA	V_{DD} = V_{IN} = 3.465V
Input Low Current	I_{IL}	–150	—	—	µA	V_{DD} = 3.465V, V_{IN} = 0V

REF_IN DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 3.3V ±5% to 2.5V ±5%, T_A = –40°C to +85°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Common Mode Voltage	V_{CMR}	0.3	—	V_{DD} – 0.3	V	—
Input Voltage Swing	V_{SWING}	0.2	—	—	V_{PP}	—

CRYSTAL CHARACTERISTICS

Parameters	Min.	Typ.	Max.	Units	Conditions
Mode of Oscillation	Fundamental, Parallel Resonant				12 pF load typical
Frequency	12	—	62.5	MHz	—
Equivalent Series Resistance (ESR)	—	—	60	Ω	—
Load Capacitance, C_L	—	12	±0.5	pF	—
Shunt Capacitor, C0	—	1	2.5	pF	—
Correlation Drive Level	—	10	100	µW	—

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%; V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Frequency	F_{IN}	12	—	62.5	MHz	XO
		12	—	850	MHz	Reference input
Output Frequency	F_{OUT}	12	—	850	MHz	LVPECL, LVDS, HCSL
		12	—	250	MHz	LVCMOS
Output Rise/Fall Time (Note 1)	T_R/T_F	85	135	350	ps	LVPECL output
		85	140	300	ps	LVDS output
		175	200	400	ps	HCSL output
		100	200	400	ps	LVCMOS output (default drive)
Output Duty Cycle	ODC	45	50	55	%	All output frequencies
		48	50	52	%	< 350 MHz output frequencies
Input to Output Propagation Delay	T_{pd}	–100	—	100	ps	ZDB mode
		—	4	—	ns	Synthesizer/Bypass mode
Output-to-Output Skew (Note 2)	T_{SKEW}	—	—	50	ps	Note 3, same output bank
PLL Lock Time	T_{LOCK}	—	5	20	ms	—
RMS Phase Jitter (Note 4, 5)	$T_{jit}(\varnothing)$	—	182	—	fs	Integration range (12 kHz - 20 MHz)
		—	74	—		Integration range (1.875 MHz - 20 MHz)

Note 1: See Figure 5-4.

2: Output-to-output skew is defined as skew between outputs at the same supply voltage and with equal load conditions. It is measured at the output differential crossing points.

3: Output-to-output skew is only defined for outputs in the same PLL bank [A:B, C:D] with the same output logic type setting.

4: All phase noise measurements were taken with an Agilent 5052B phase noise system.

5: Measured using a 50 MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1 MHz.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Lead Temperature	—	—	+260	—	°C	Soldering, 20s
Case Temperature	—	—	+115	—	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances						
Junction Thermal Resistance, 7 x 7 QFN-84Ld	θ_{JA}	—	23.4	—	°C/W	—
Junction Thermal Resistance, 7 x 7 QFN Still Air QFN-48Ld	θ_{JA}	—	24.22	—	°C/W	—
Junction Thermal Resistance, 9 x 9 QFN Still Air QFN-76Ld	θ_{JA}	—	25	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +85°C rating. Sustained junction temperatures above +85°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Numbers by Package Option					Pin Name	Pin Type	Pin Level	Pin Function
#1 48-pin	#2 48-pin	#3 48-pin	#4 76-pin	#5 84-pin				
34	34	34	72	A19	QA1	O, (DIF/SE)	LVPECL LVDS HCSL LVCMOS (Q only)	Differential / SE Clock Output (LVCMOS)
35	35	35	74	A20	/QA1			
31	31	31	69	A17	QA2			
32	32	32	70	A18	/QA2			
28	—	—	65	A15	QA3			
30	—	—	67	A16	/QA3			
26	27	28	61	A13	QB1			
27	28	29	63	A14	/QB1			
22	22	22	55	A10	QB2			
24	24	24	56	A11	/QB2			
—	—	—	52	A8	QB3			
—	—	—	54	A9	/QB3			
3	3	3	22	A36	QC1			
5	5	5	24	A37	/QC1			
6	6	6	26	A38	QC2			
7	7	7	27	A39	/QC2			
—	—	—	29	A40	QC3			
—	—	—	31	A41	/QC3			
8	9	8	33	A42	QD1			
10	11	10	35	A43	/QD1			
12	—	—	40	A1	QD2			
14	—	—	41	A2	/QD2			
15	15	15	43	A3	QD3			
16	16	16	45	A4	/QD3			
—	—	27	59	B12	FSA	I, (SE)	LVCMOS	Frequency Select, on-chip 75 kΩ pull-up 1 = Primary Selection 0 = Secondary Selection
—	—	25	58	B11	FSB			
—	—	13	38	B40	FSC			
—	—	11	37	A44	FSD			
2	2	2	1, 21	A21	V_{DD}	PWR	—	Power Supply
36	36	36	75	A35				
29	30	29	66, 71	B18	V_{DDOA}	PWR	—	Power Supply for Outputs QA1–3
33	33	33	73	B17				
23	23	23	53, 60	B8	V_{DDOB}	PWR	—	Power Supply for Outputs QB1–3
—	—	—	62	B9				
4	4	4	23	B33	V_{DDOC}	PWR	—	Power Supply for Outputs QC1–3
—	—	—	28, 30	B37				
9	10	9	34	B2	V_{DDOD}	PWR	—	Power Supply for Outputs QD1–3
13	14	14	36, 44	B3				
37	37	37	76	B20	V_{DDAP1}	PWR	—	Power Supply for PLL1
1	1	1	20	B31	V_{DDAP2}	PWR	—	Power Supply for PLL2

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Numbers by Package Option					Pin Name	Pin Type	Pin Level	Pin Function
#1 48-pin	#2 48-pin	#3 48-pin	#4 76-pin	#5 84-pin				
41	41	41	9	B25	V_{DDI1}	PWR	3.3V only	Power Supply for Input circuits
42	42	42	9	A28	V_{DDI2}	PWR	3.3V only	Power Supply for Input circuits
11	12	12	14	A22	V_{SS} (Exposed Pad)	PWR	—	Power Supply Ground. The exposed pad must be connected to the V_{SS} ground plane.
25	26	26	17	A23				
38	38	38	25	A31				
47	47	47	42	A34				
48	48	48	68	B4				
EPAD	EPAD	EPAD	EPAD	B10				
—	—	—	—	B13				
—	—	—	—	B15				
—	—	—	—	B16				
—	—	—	—	B30				
—	—	—	—	B34				
—	—	—	—	B35				
—	—	—	—	B39				
—	—	—	—	EPAD				
—	29	—	64	B14	OEA1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs QA1/2/3 disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75 kΩ pull-up
—	25	—	57	A12	OEB1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs QB1/2/3 disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75 kΩ pull-up
—	8	—	32	B38	OEC1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs QC1/2/3 disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75 kΩ pull-up
—	13	—	39	B1	OED1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs QD1/2/3 disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75kΩ pull-up
39	39	39	2	B21	REFIN1 /REFIN1	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Reference Clock Input 1
40	40	40	3	B22				
45	45	45	15	B28	REFIN2 /REFIN2	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Reference Clock Input2
46	46	46	16	B29				
—	—	—	6	B23	FBIN1 /FBIN1	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Feedback Clock Input 1 For Zero Delay Buffer function
—	—	—	8	B24				

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Numbers by Package Option					Pin Name	Pin Type	Pin Level	Pin Function
#1 48-pin	#2 48-pin	#3 48-pin	#4 76-pin	#5 84-pin				
—	—	—	10	B26	FBIN2 /FBIN2	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Feedback Clock Input 2 For Zero Delay Buffer function
—	—	—	12	B27				
43	43	43	11	A29	XTAL_IN	I, (SE)	12 pF crystal	Crystal Reference Input, no external load caps needed
44	44	44	13	A30	XTAL_OUT	O, (SE)	12 pF crystal	Crystal Reference Output, no external load caps needed
—	—	—	4	A25	DNC	—	—	Leave open, do not connect to anything
—	—	—	5	A26				
—	—	—	7	A32				
—	—	—	18, 19	A33				
—	—	—	—	A27	NC	—	—	Leave open or connect to V_{SS}.
—	—	—	—	B19				
—	—	—	—	B32				
—	—	—	—	B36				
18	18	18	47	A6	SPI	I/O, (SE)	LVCMOS	SPI bus pins for programming. Leave open; for normal operation, do not connect to anything. See FLEX SPI documentation for programming features.
19	19	19	48	A7				
20	20	20	59	B5				
21	21	21	50	B6				
—	—	—	51	B7				
17	17	17	46	A5	GND	I	—	These pins are not Power Supply grounds but must be tied to V_{SS} for proper operation.
—	—	—	—	A24				

2.1 Truth Tables

TABLE 2-2: OUTPUT ENABLE

OEA	OEB	OEC	OED	OUTPUT
0	1	1	1	3 QA outputs tri-state
1	0	1	1	3 QB outputs tri-state
1	1	0	1	3 QC outputs tri-state
1	1	1	0	3 QD outputs tri-state

TABLE 2-3: SWITCHING FREQUENCY

FSA	FSB	FSC	FSD	OUTPUT FREQUENCY
0	1	1	1	3 QA outputs: Secondary output dividers Other outputs: Primary output dividers
1	0	1	1	3 QB outputs: Secondary output dividers Other outputs: Primary output dividers
1	1	0	1	3 QC outputs: Secondary output dividers Other outputs: Primary output dividers
1	1	1	0	3 QD outputs: Secondary output dividers Other outputs: Primary output dividers

3.0 KEY PROGRAMMABLE PARAMETERS

3.1 Frequency Settings for One PLL and One Output Bank

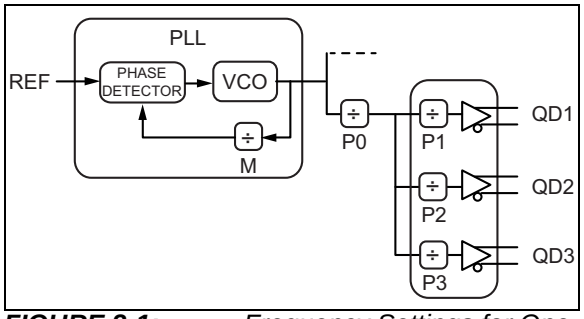


FIGURE 3-1: *Frequency Settings for One PLL and One Output Bank.*

The REF input frequency can be from a crystal or from a reference clock input. If a crystal is used, the REF input frequency range is 12 MHz to 62.5 MHz.

The VCO in the PLL has a range of 2875 MHz to 3510 MHz.

Counters M and P0 have a range of 4 to 259.

Counters P1, P2 and P3 have a range of 1 to 16.

EQUATION 3-1:

$$F_{VCO} = REF \times M$$

EQUATION 3-2:

$$QD1 = F_{VCO} \div (P0 \times P1)$$

EQUATION 3-3:

$$QD2 = F_{VCO} \div (P0 \times P2)$$

EQUATION 3-4:

$$QD3 = F_{VCO} \div (P0 \times P3)$$

3.2 Output Logic Programming

Available output logic types are LVPECL, LVDS, HCSL, and LVCMOS.

Each output can be programmed individually to one of the four logic types.

All logic types are differential except LVCMOS. For LVCMOS, only the true channel of the output pair is enabled and the complementary channel is disabled. With LVCMOS there is also an output drive setting. There is one setting for all LVCMOS outputs, so all LVCMOS outputs will have the same drive strength. Unused outputs are disabled to high impedance.

3.3 Input Selection

The reference input for the PLLs can be programmed to be either a crystal or a reference clock.

The crystal oscillator circuit has capacitors on the IC so external capacitors are not required.

There are two reference clock inputs, one for each PLL. Make sure they are connected to the same reference input source. The reference inputs can be differential or single-ended and require only a small amplitude. See Figure 3-2 and Figure 3-3.

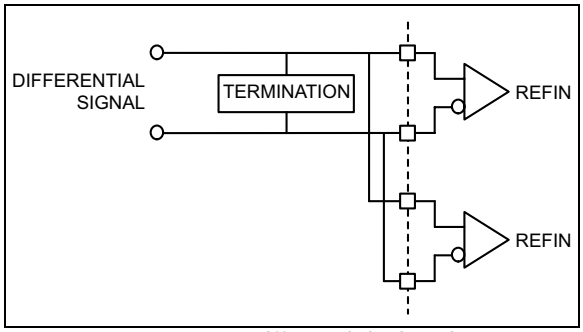


FIGURE 3-2: *Differential Signal.*

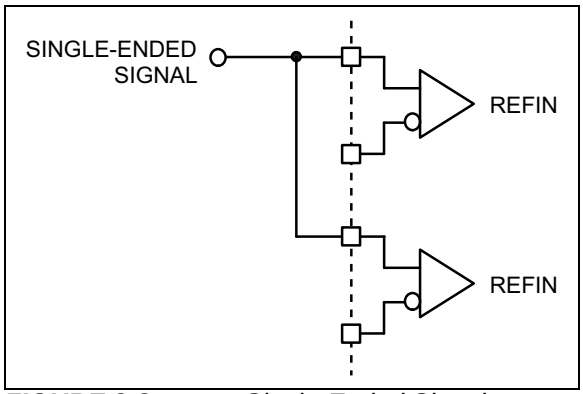


FIGURE 3-3: *Single-Ended Signal.*

The single-ended signal input can be LVCMOS, but smaller amplitudes like >800 mV_{PP} clipped sine wave from a TCXO will also work.

3.4 Frequency Select Programming

Each of the four output banks has a frequency select pin. For each bank, two P0, P1, P2 and P3 counter values can be programmed, a primary and a secondary value. The frequency select pin toggles between the two values assigned to each counter, changing the output frequencies.

4.0 APPLICATION INFORMATION

4.1 Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

4.2 Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die, so no external capacitance is needed. See the ANTC207 application note for further details.

4.3 Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30Ω resistor in series with the output, as close as possible to the output pin and start a 50Ω trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50Ω traces. For EMI reasons, it is better to use a balanced differential design.

LVDS can be AC-coupled or DC-coupled to its termination.

5.0 POWER SUPPLY FILTERING RECOMMENDATIONS

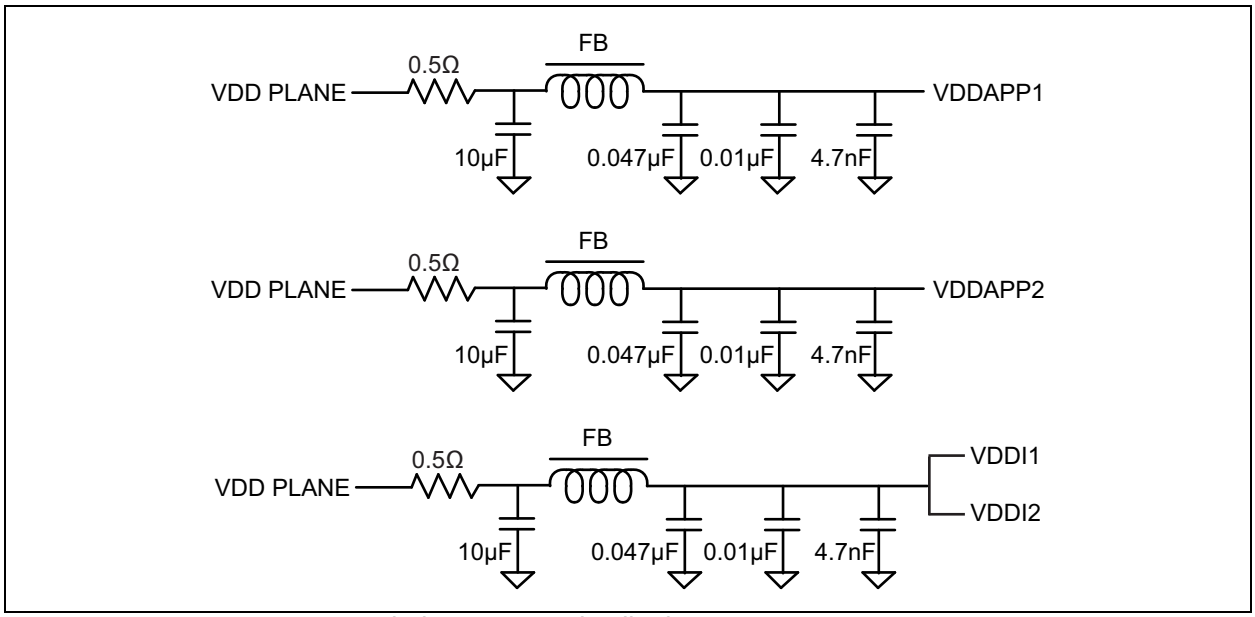


FIGURE 5-1: *Recommended Power Supply Filtering.*

- Use the power supply filtering shown in Figure 5-1 for V_{DDAP1}, V_{DDAP2}, V_{DDI1} and V_{DDI2}.
- Connect the V_{DDO} and V_{DD} pins directly to the V_{DD} power plane.
- Connect all V_{SS} pins directly to the ground power plane.
- Recommended ferrite bead properties are 80Ω to 240Ω impedance and >250 mA saturation current.
- To improve power supply filtering beyond what a ferrite bead can provide, the Ripple Blocker™ provides a solution. MIC94300 or MIC94310 are recommended parts. The filter circuit with Ripple Blocker is shown in Figure 5-2 and can be used for any of the above V_{DD} sections.

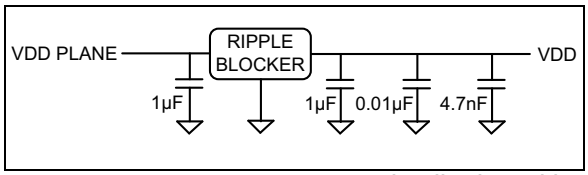


FIGURE 5-2: *Power Supply Filtering with Ripple Blocker.*

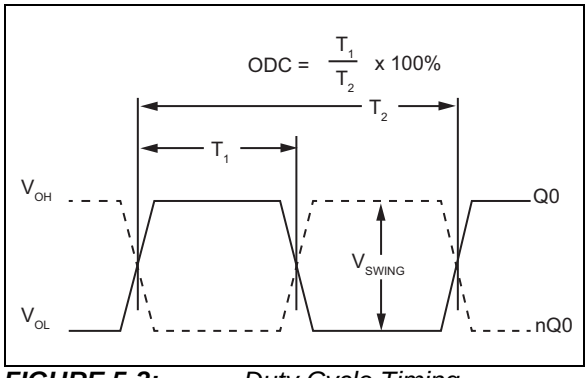


FIGURE 5-3: *Duty Cycle Timing.*

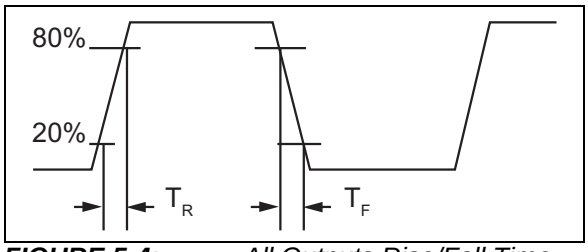


FIGURE 5-4: *All Outputs Rise/Fall Time.*

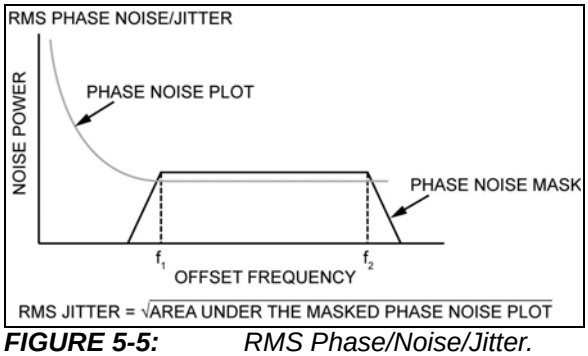


FIGURE 5-5: *RMS Phase/Noise/Jitter.*

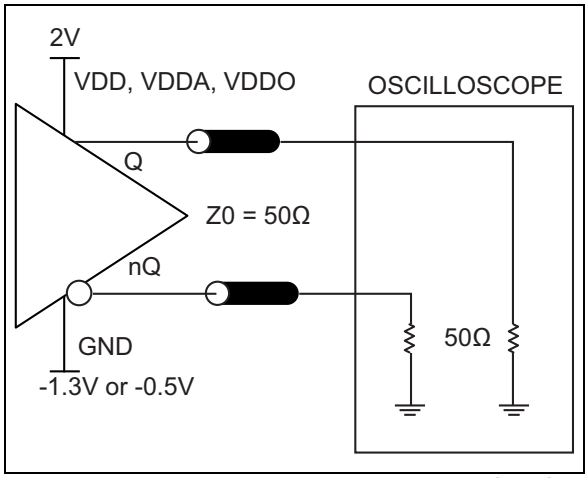


FIGURE 5-6: *LVPECL Output Load and Test Circuit.*

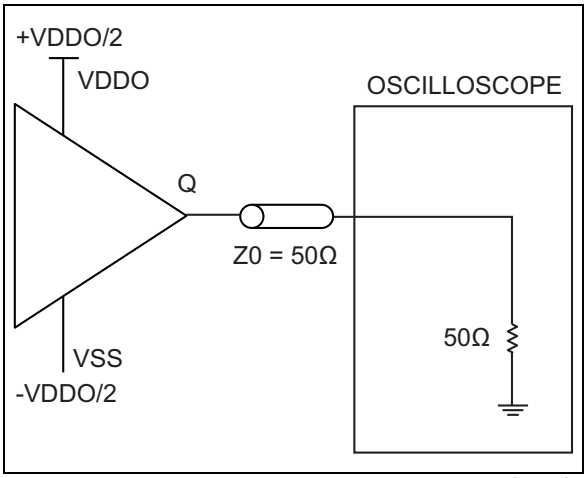


FIGURE 5-9: *LVCMOS Output Load and Test Circuit.*

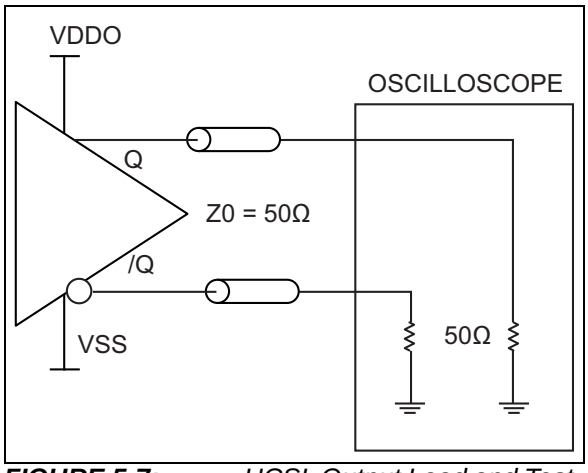


FIGURE 5-7: *HCSL Output Load and Test Circuit.*

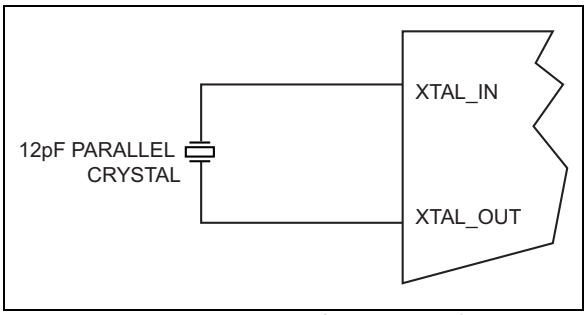


FIGURE 5-10: *Crystal Input Interface.*

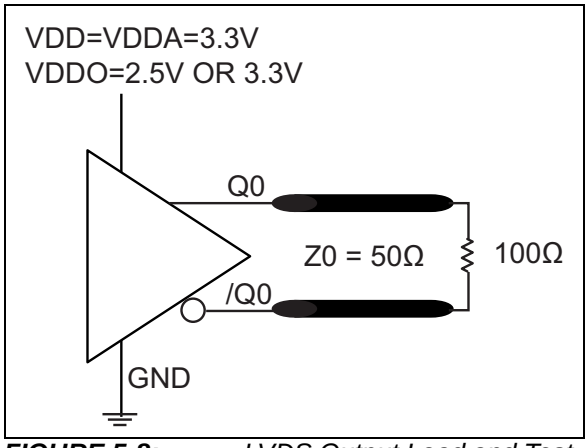


FIGURE 5-8: *LVDS Output Load and Test Circuit.*

6.0 PHASE NOISE PERFORMANCE

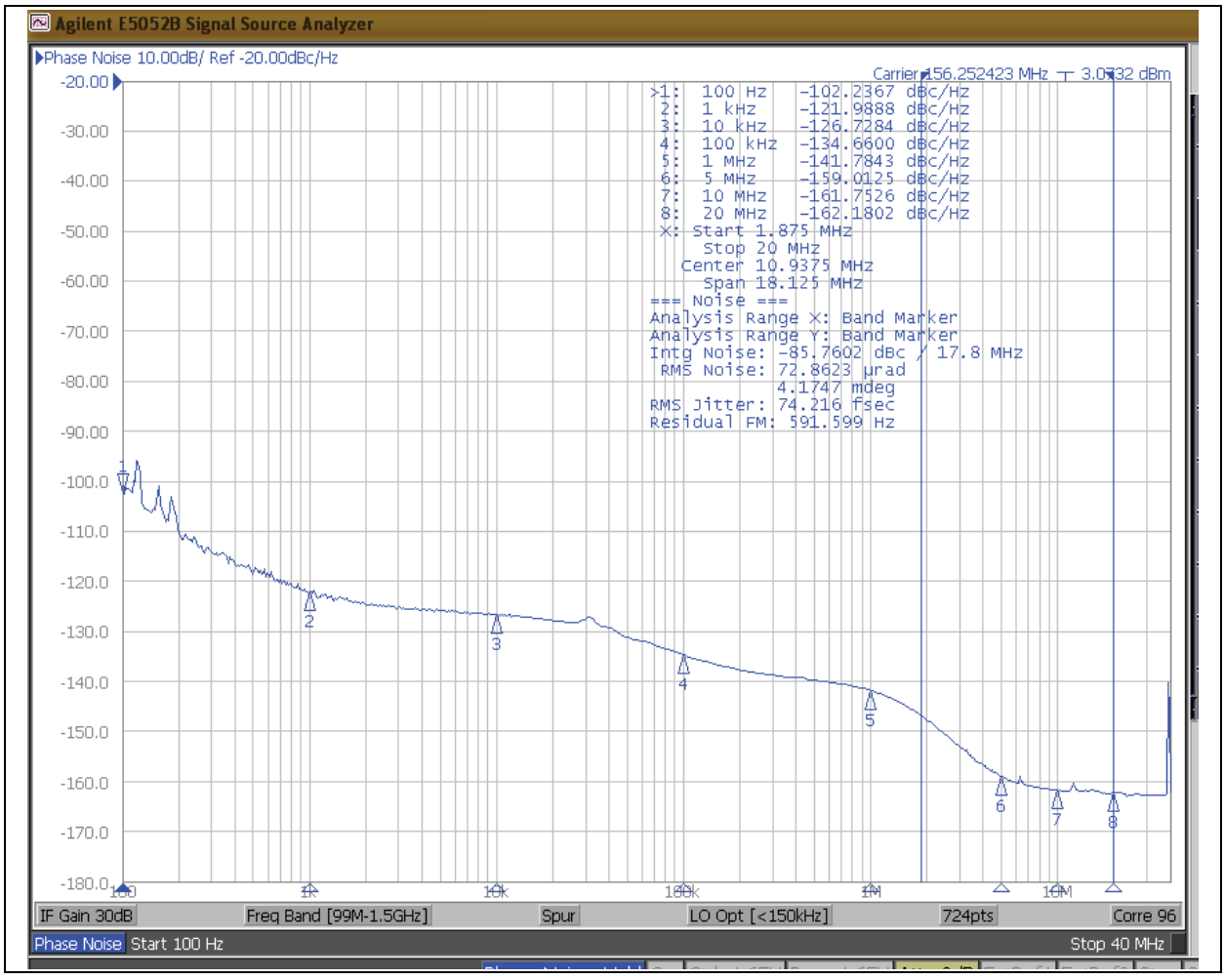


FIGURE 6-1: *156.25 MHz, Integration Range 1.875 MHz to 20 MHz: 74.2 fs_{RMS}.*

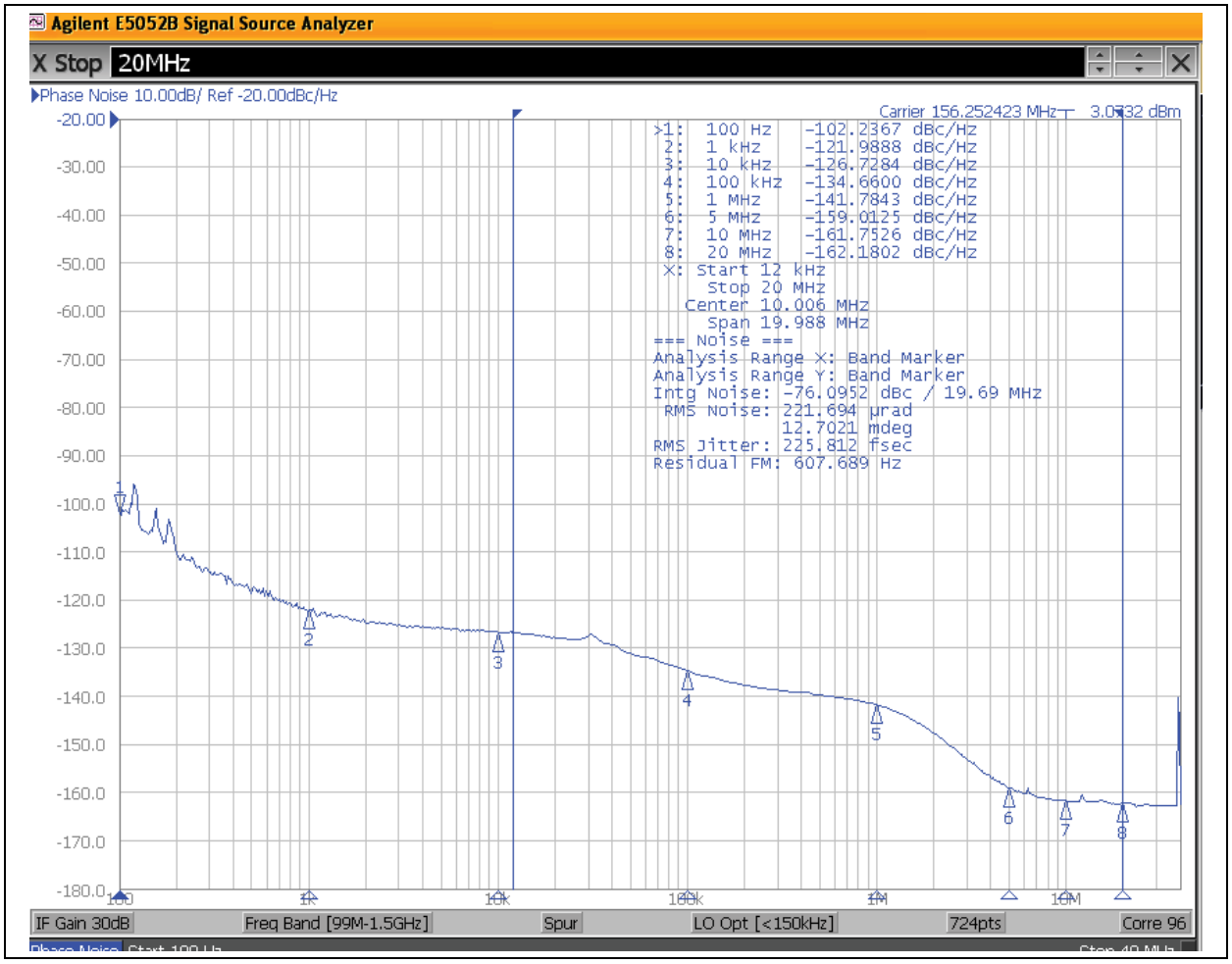


FIGURE 6-2: *156.25 MHz, Integration Range 12 kHz to 20 MHz: 225.8 fs_{RMS}.*

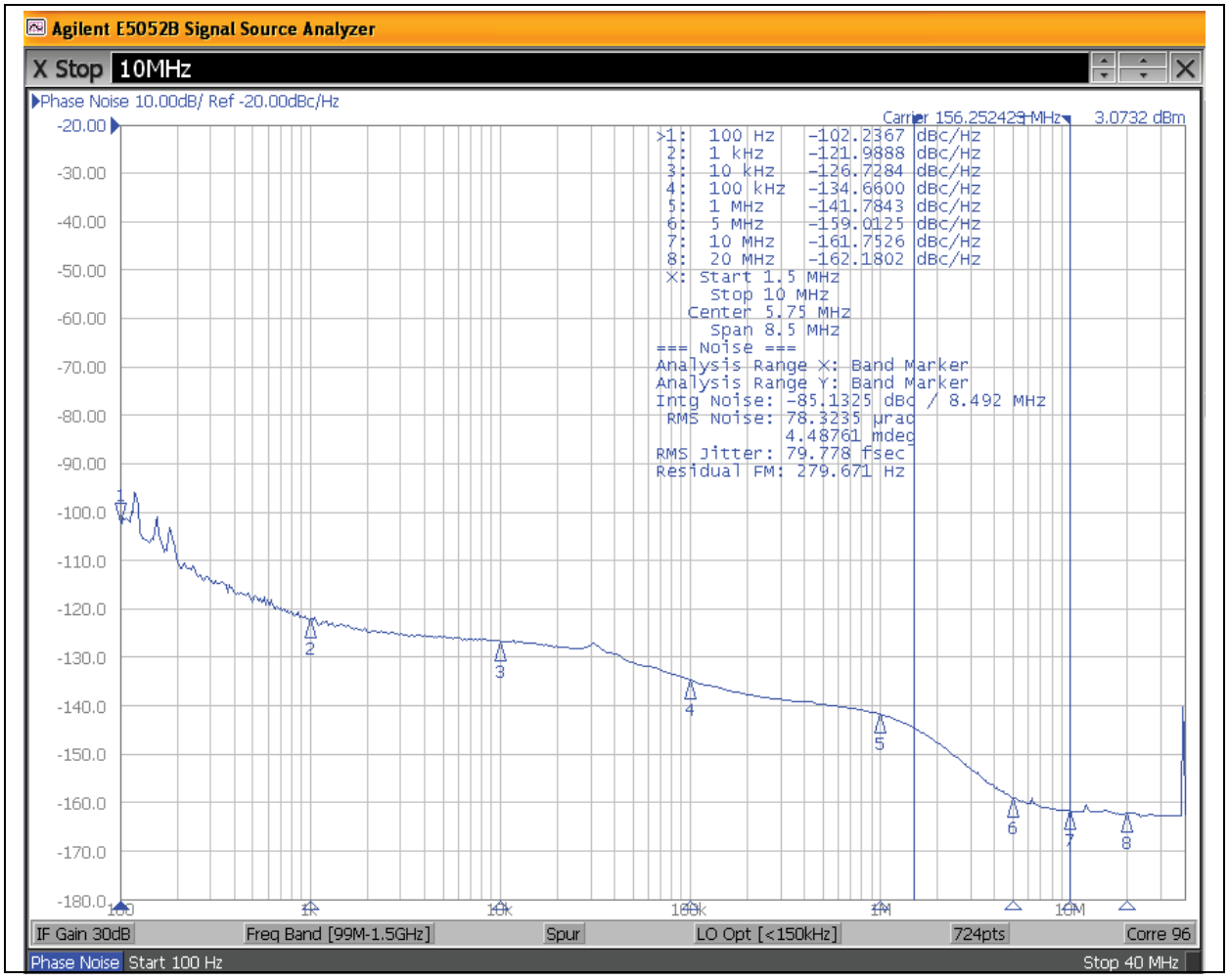


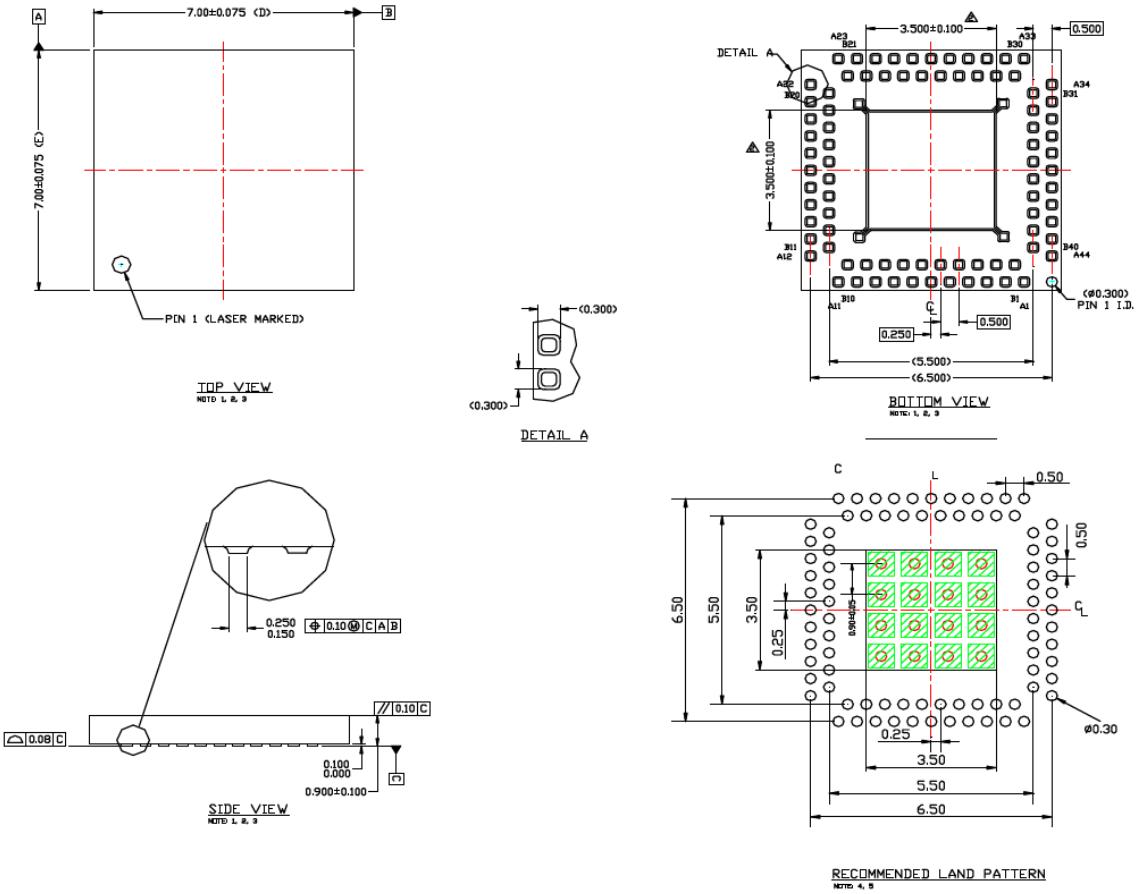
FIGURE 6-3: *156.25 MHz, Integration Range 1.5 MHz to 10 MHz: 79.8 fs_{RMS}.*

7.0 PACKAGING INFORMATION

84-Lead QFN 7 mm x 7 mm Package Outline and Recommended Land Pattern

TITLE
84 LEAD QFN 7x7mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN77-84LD-PL-1	**UNIT**	MM
Lead Frame	Substrate	**Lead Finish**	Matte Tin



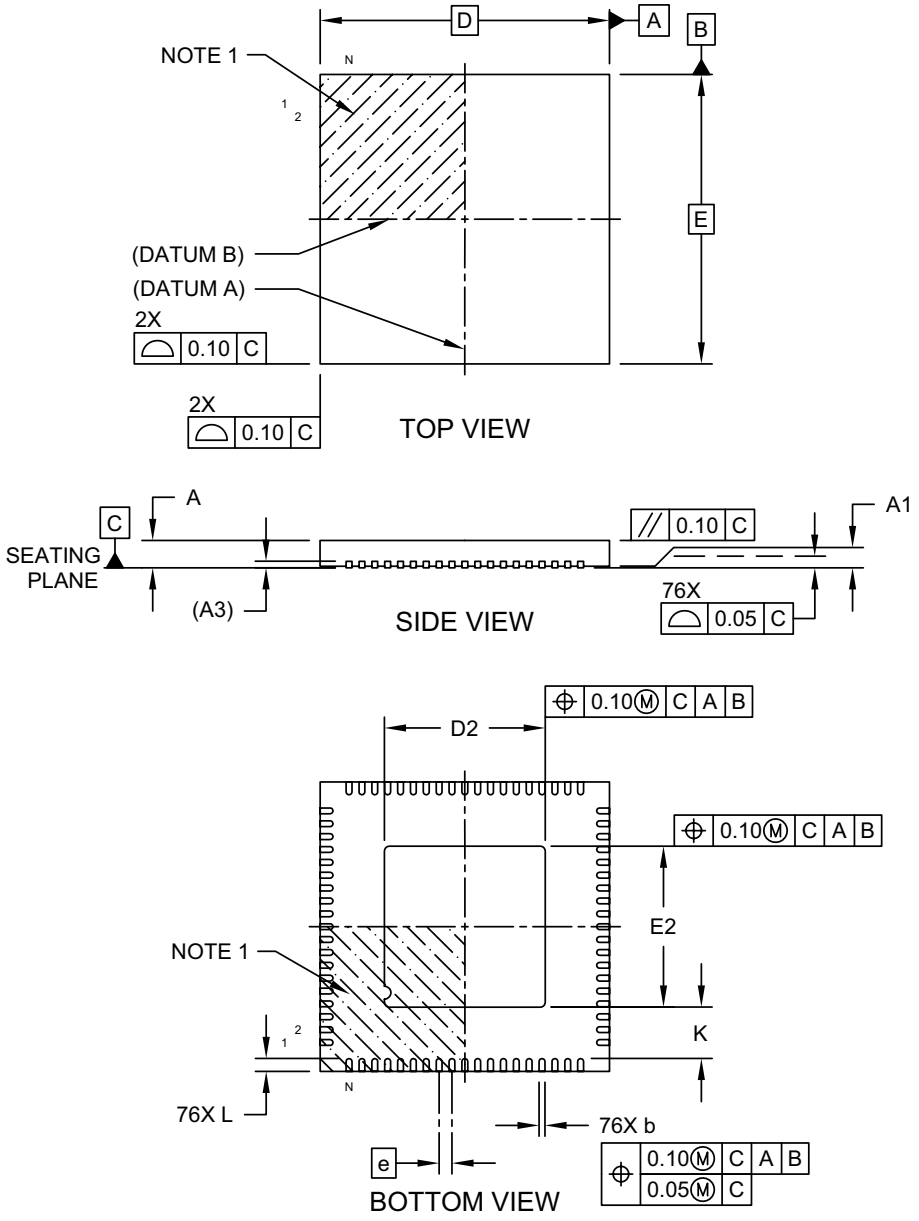
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAXIMUM THERMAL PERFORMANCE. PITCH IS 0.90mm.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 0.70x0.70 mm, PITCH IS 0.90 mm.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

76-Lead VQFN Package Outline and Recommended Land Pattern

76-Lead Very Thin Plastic Quad Flat, No Lead Package (QBA) - 9x9 mm Body [VQFN] With 5x5 mm Exposed Pad

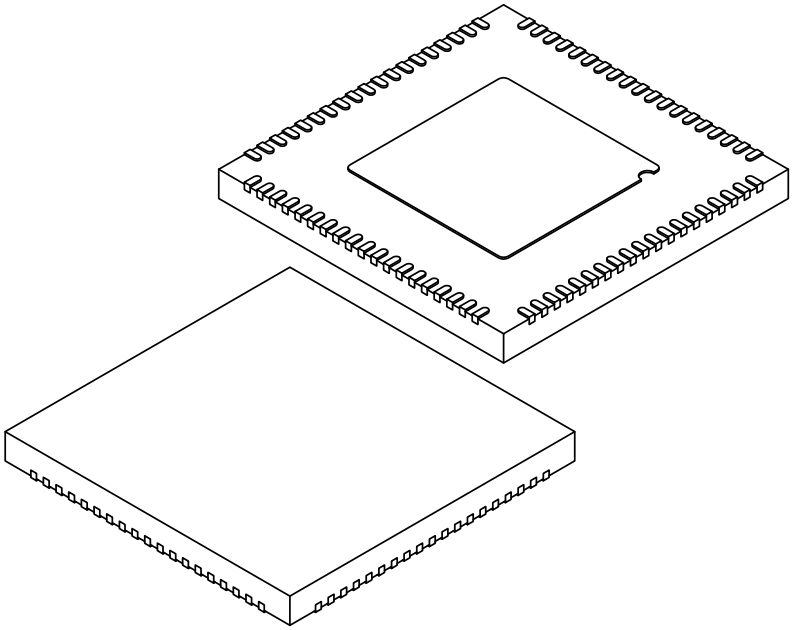
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1195A Sheet 1 of 2

76-Lead Very Thin Plastic Quad Flat, No Lead Package (QBA) - 9x9 mm Body [VQFN] With 5x5 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		76	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.9
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	4.90	5.00	5.10
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	4.90	5.00	5.10
Terminal Width	b	0.13	0.18	0.23
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

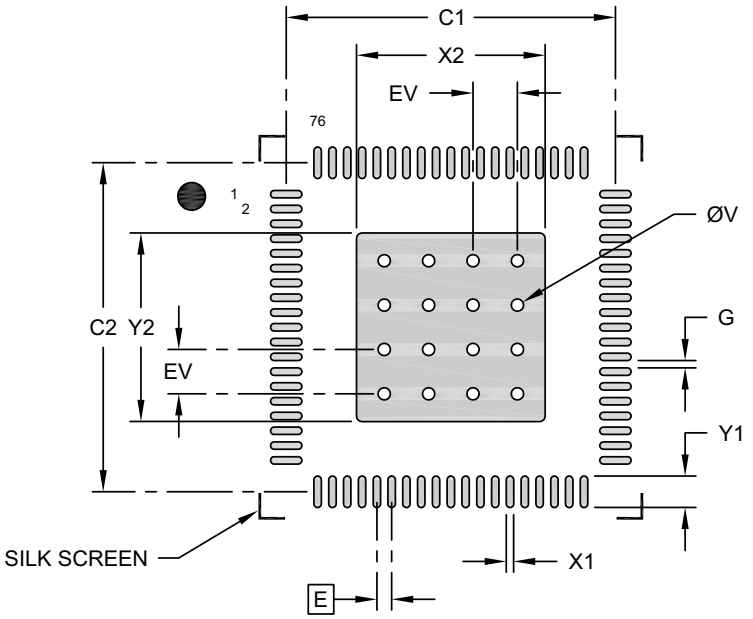
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1195A Sheet 2 of 2

76-Lead Very Thin Plastic Quad Flat, No Lead Package (QBA) - 9x9 mm Body [VQFN] With 5x5 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			5.10
Optional Center Pad Length	Y2			5.10
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X76)	X1			0.20
Contact Pad Length (X76)	Y1			0.85
Contact Pad to Contact Pad (X72)	G	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

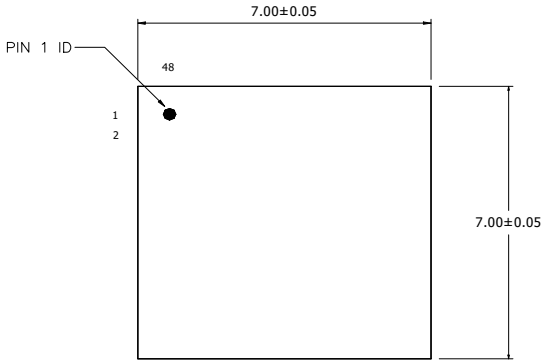
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3195A

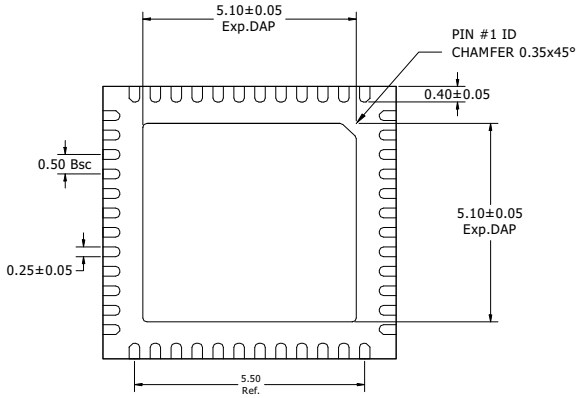
48-Lead QFN 7 mm x 7 mm Package Outline and Recommended Land Pattern

TITLE
48 LEAD QFN 7x7mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

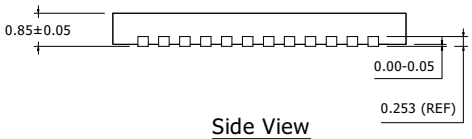
DRAWING #	QFN77-48LD-PL-1	**UNIT**	MM



Top View
NOTE: 1, 2, 3



Bottom View
NOTE: 1, 2, 3

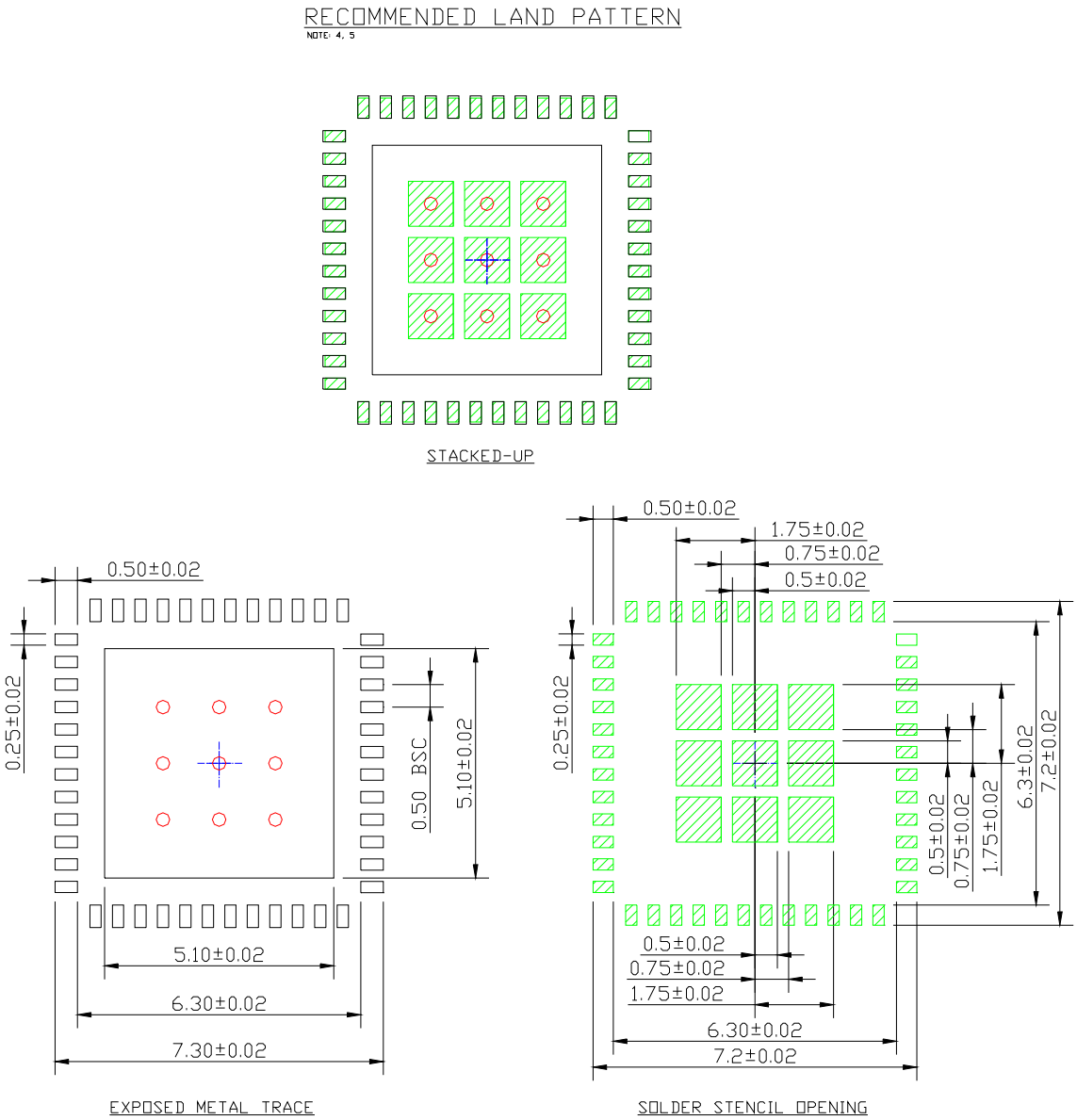


Side View
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. PITCH is 1.00mm.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 1.00x1.00mm, SPACING IS 0.25mm.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

POD-Land Pattern drawing #: QFN77-48LD-PL-1-C



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (January 2018)

- Converted Micrel document SM803XXX to Microchip data sheet template DS20005667A.
- Additional 76-Lead VQFN package included in Package Types, Pin Descriptions, and Packaging Information sections.
- Minor grammatical text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	X
Device	Voltage Option	Package Type	Temperature	Special Processing

Device:	SM803XXX:	Flexible Ultra-Low Jitter Clock Synthesizer	
Voltage Option:	U	=	2.5V/3.3V
Package Type:	M	=	48-Pin QFN, 76-Pin QFN, or 84-Pin QFN
Temperature:	G	=	–40°C to +85°C (NiPdAu Lead Free)
	Y	=	–40°C to +85°C (Matte-Sn Lead Free)
Special Processing:	Blank	=	Tray
	R	=	Tape and Reel

Package Option (Note 1)	QFN Package	# of Outputs	OE Control	FSEL Control
1	48-pin, 7 mm × 7 mm	10	No	No
2	48-pin, 7 mm × 7 mm	8	Yes	No
3	48-pin, 7 mm × 7 mm	8	No	Yes
4	76-pin, 9 mm × 9 mm	12	Yes	Yes
5	84-pin, 7 mm × 7 mm	12	Yes	Yes

Note 1: Use the web tool at http://clockworks.microchip.com/timing/ to determine the desired configuration.

Examples:

a) SM803XXXUMG: Flexible Ultra-Low Jitter Clock Synthesizer, 2.5/3.3V Voltage, 48-Pin, 76-Pin, or 84-Pin QFN, –40°C to +85°C (NiPdAu Lead Free), Tray

b) SM803XXXUMGR: Flexible Ultra-Low Jitter Clock Synthesizer, 2.5/3.3V Voltage, 48-Pin, 76-Pin, or 84-Pin QFN, –40°C to +85°C (NiPdAu Lead Free), Tape and Reel

c) SM803XXXUMY: Flexible Ultra-Low Jitter Clock Synthesizer, 2.5/3.3V Voltage, 48-Pin, 76-Pin, or 84-Pin QFN, –40°C to +85°C (Matte-Sn Lead Free), Tray

d) SM803XXXUMYR: Flexible Ultra-Low Jitter Clock Synthesizer, 2.5/3.3V Voltage, 48-Pin, 76-Pin, or 84-Pin QFN, –40°C to +85°C (Matte-Sn Lead Free), Tape and Reel.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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