TEXAS INSTRUMENTS

OPA314, OPA2314, OPA4314

SBOS563G – MAY 2011 – REVISED JUNE 2015

OPAx314 3-MHz, Low-Power, Low-Noise, RRIO, 1.8-V CMOS Operational Amplifier

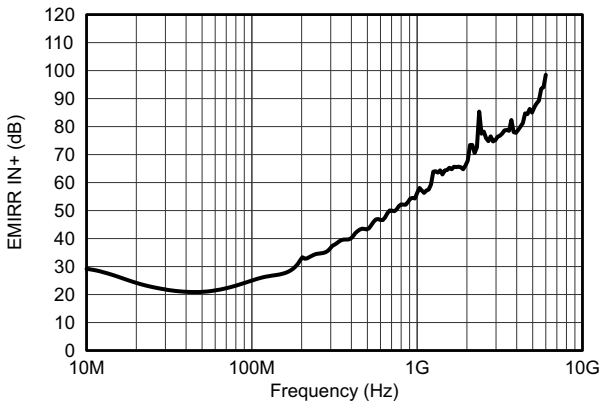
1 Features

- Low I_Q: 150 µA/ch
- Wide Supply Range: 1.8 V to 5.5 V
- Low Noise: 14 nV/√Hz at 1 kHz
- Gain Bandwidth: 3 MHz
- Low Input Bias Current: 0.2 pA
- Low Offset Voltage: 0.5 mV
- Unity-Gain Stable
- Internal RF/EMI Filter
- Extended Temperature Range: –40°C to 125°C

2 Applications

- Battery-Powered Instruments:
  - Consumer, Industrial, Medical
  - Notebooks, Portable Media Players
- Photodiode Amplifiers
- Active Filters
- Remote Sensing
- Wireless Metering
- Handheld Test Equipment

EMIRR vs Frequency



3 Description

The OPA314 family of single-, dual-, and quad-channel operational amplifiers represents a new generation of low-power, general-purpose CMOS amplifiers. Rail-to-rail input and output swings, low quiescent current (150 µA typically at 5 V_S) combined with a wide bandwidth of 3 MHz, and very low noise (14 nV/√Hz at 1 kHz) make this family very attractive for a variety of battery-powered applications that require a good balance between cost and performance. The low input bias current supports applications with MΩ source impedances.

The robust design of the OPA314 devices provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 300 pF, an integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4-kV HBM).

These devices are optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V), and are specified over the full extended temperature range of –40°C to 125°C.

The OPA314 (single) is available in both SC70-5 and SOT23-5 packages. The OPA2314 (dual) is offered in SO-8, MSOP-8, and DFN-8 packages. The quad-channel OPA4314 is offered in a TSSOP-14 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA314	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
OPA2314	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm
	VSON (8)	3.00 mm × 3.00 mm
OPA4314	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (April 2013) to Revision G — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Moved revision history to the second page ... 1

Changes from Revision E (September 2012) to Revision F — **Page**

- Changed document title (removed "Value Line Series") ... 1

Changes from Revision D (March 2012) to Revision E — **Page**

- Added "Value Line Series" to title ... 1

Changes from Revision C (February 2012) to Revision D — **Page**

- Changed product status from mixed status to production data ... 1
- Deleted shading and footnote 2 from Package Information table ... 1

Changes from Revision B (December 2011) to Revision C — **Page**

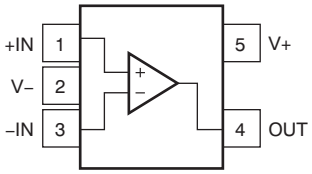
- Changed first Features bullet ... 1
- Deleted shading from OPA314 SOT23-5 row (DBV package) in Package Information table ... 1
- Added OPA2314, OPA4314 to first two Power Supply, *Quiescent current per amplifier* parameter rows in Electrical Characteristics table ... 8
- Added OPA314 Power Supply, *Quiescent current per amplifier* parameter row to Electrical Characteristics table ... 8

Changes from Revision A (August 2011) to Revision B **Page**

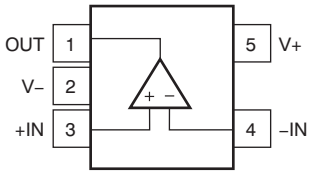
- Deleted shading from OPA2314 MSOP-8 row in Package Information table 1

5 Pin Configuration and Functions

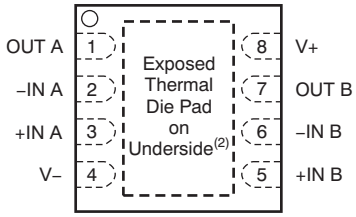
DCK Package
5-Pin SC70
Top View



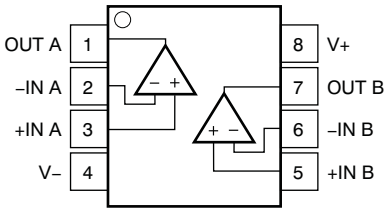
DBV Package
5-Pin SOT23
Top View



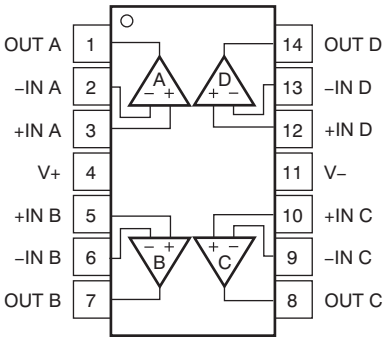
DRB Package(1)
8-Pin DFN
Top View



D or DGK Package
8-Pin SOIC or VSSOP
Top View



PW Package
14-Pin TSSOP
Top View



(1) Pitch: 0.65 mm.

(2) Connect thermal pad to V–. Pad size: 1.8 mm × 1.5 mm.

Pin Functions: OPA314

PIN			I/O	DESCRIPTION
NAME	DBV	DCK		
+IN	3	1	I	Noninverting input
–IN	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) supply
V–	2	2	—	Negative (lowest) supply

Pin Functions: OPA2314

PIN				I/O	DESCRIPTION
NAME	DRB	DGK	D		
+IN A	3	3	3	I	Noninverting input
+IN B	5	5	5	I	Noninverting input
–IN A	2	2	2	I	Inverting input
–IN B	6	6	6	I	Inverting input
OUT A	1	1	1	O	Output
OUT B	7	7	7	O	Output
V+	8	8	8	—	Positive (highest) supply
V–	4	4	4	—	Negative (lowest) supply

Pin Functions: OPA4314

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input
+IN B	5	I	Noninverting input
+IN C	10	I	Noninverting input
+IN D	12	I	Noninverting input
–IN A	2	I	Inverting input
–IN B	6	I	Inverting input
–IN C	9	I	Inverting input
–IN D	13	I	Inverting input
OUT A	1	O	Output
OUT B	7	O	Output
OUT C	8	O	Output
OUT D	14	O	Output
V+	4	—	Positive (highest) supply
V–	11	—	Negative (lowest) supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Supply voltage			7	V
Signal input terminals	Voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Current(2)	–10	10	mA
Output short-circuit(3)		Continuous		mA
Operating temperature, T_A		–40	150	°C
Junction temperature, T_J				°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	1.8 (±0.9)		5.5 (±2.75)	V
T_A	Ambient operating temperature	–40		125	°C

6.4 Thermal Information: OPA314

THERMAL METRIC(1)		OPA314			UNIT
		DBV (SOT23)	DCK (SC70)	DRL (SOT553)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.5	281.4	208.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	99.1	91.6	0.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.6	59.6	42.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.7	1.5	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	58.8	42.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: OPA2314

THERMAL METRIC[1]		OPA2314			UNIT
		D (SO)	DGK (MSOP)	DRB (DFN)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.4	191.2	53.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	89.5	61.9	69.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	111.9	20.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.9	5.1	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.1	110.2	11.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Thermal Information: OPA4314

THERMAL METRIC[1]		OPA4314		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	121	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	51.8	49.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	5.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	62.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.7 Electrical Characteristics

V_S = 1.8 V to 5.5 V; At T_A = 25 °C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.[1]

PARAMETER		TEST CONDITIONS	T_A = 25 °C			T_A = –40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE									
V_{OS}	Input offset voltage	$V_{CM} = (V_S+) – 1.3$ V		0.5	2.5				mV
dV_{OS}/dT	vs Temperature						1		µV/°C
PSRR	vs power supply	$V_{CM} = (V_S+) – 1.3$ V	78	92					dB
	Over temperature					74			dB
	Channel separation, DC	At DC		10					µV/V
INPUT VOLTAGE RANGE									
V_{CM}	Common-mode voltage range		(V–) – 0.2		(V+) + 0.2				V
CMRR	Common-mode rejection ratio	V_S = 1.8 V to 5.5 V, $(V_S–) – 0.2$ V < V_{CM} < $(V_S+) – 1.3$ V	75	96					dB
		V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V[2]	66	80					dB
	Over temperature	V_S = 1.8 V, $(V_S–) – 0.2$ V < V_{CM} < $(V_S+) – 1.3$ V				70	86		dB
		V_S = 5.5 V, $(V_S–) – 0.2$ V < V_{CM} < $(V_S+) – 1.3$ V				73	90		dB
		V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V[2]				60			dB
INPUT BIAS CURRENT									
I_B	Input bias current			±0.2	±10				pA
	Over temperature							±600	pA
I_{OS}	Input offset current			±0.2	±10				pA
	Over temperature							±600	pA
NOISE									
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz		5					μV_{PP}

(1) Parameters with minimum or maximum specification limits are 100% production tested at +25ºC, unless otherwise noted. Over temperature limits are based on characterization and statistical analysis.
(2) Specified by design and characterization; not production tested.

Electrical Characteristics (continued)

V_S = 1.8 V to 5.5 V; At T_A = 25 °C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	T_A = 25 °C			T_A = –40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
e_n	Input voltage noise density	f = 10 kHz		13					nV/√Hz
		f = 1 kHz		14					nV/√Hz
i_n	Input current noise density	f = 1 kHz		5					fA/√Hz
INPUT CAPACITANCE									
C_{IN}	Differential	V_S = 5 V		1					pF
	Common-mode	V_S = 5 V		5					pF
OPEN-LOOP GAIN									
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	90	115					dB
		V_S = 5.5 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	100	128					dB
		V_S = 1.8 V, 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ(2)	90	100					dB
		V_S = 5.5 V, 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ(2)	94	110					dB
	Over temperature	V_S = 5.5 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ				90	110		dB
		V_S = 5.5 V, 0.5 V < V_O < (V+) – 0.2 V, R_L = 2 kΩ					100		dB
	Phase margin	V_S = 5 V, G = 1, R_L = 10 kΩ		65					°
FREQUENCY RESPONSE									
GBW	Gain-bandwidth product	V_S = 1.8 V, R_L = 10 kΩ, C_L = 10 pF		2.7					MHz
		V_S = 5 V, R_L = 10 kΩ, C_L = 10 pF		3					MHz
SR	Slew rate(3)	V_S = 5 V, G = 1		1.5					V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = 1		2.3					µs
		To 0.01%, V_S = 5 V, 2-V step , G = 1		3.1					µs
	Overload recovery time	V_S = 5 V, V_{IN} × Gain > V_S		5.2					µs
THD+N	Total harmonic distortion + noise(4)	V_S = 5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz, R_L = 10 kΩ		0.001%					
OUTPUT									
V_O	Voltage output swing from supply rails	V_S = 1.8 V, R_L = 10 kΩ		5	15				mV
		V_S = 5.5 V, R_L = 10 kΩ		5	20				mV
		V_S = 1.8 V, R_L = 2 kΩ		15	30				mV
		V_S = 5.5 V, R_L = 2 kΩ		22	40				mV
	Over temperature	V_S = 5.5 V, R_L = 10 kΩ						30	mV
		V_S = 5.5 V, R_L = 2 kΩ					60		mV
I_{SC}	Short-circuit current	V_S = 5 V		±20					mA
R_O	Open-loop output impedance	V_S = 5.5 V, f = 100 Hz		570					Ω
POWER SUPPLY									
V_S	Specified voltage range		1.8		5.5				V
I_Q	Quiescent current per amplifier	OPA314, OPA2314, OPA4314, V_S = 1.8 V, I_O = 0 mA		130	180				µA
		OPA2314, OPA4314, V_S = 5 V, I_O = 0 mA		150	190				µA
		OPA314, V_S = 5 V, I_O = 0 mA		150	210				µA
	Over temperature	V_S = 5 V, I_O = 0 mA						220	µA
	Power-on time	V_S = 0 V to 5 V, to 90% I_Q level		44					µs
TEMPERATURE									
	Specified range		–40		125				°C
	Operating range		–40		150				°C

(3) Signifies the slower value of the positive or negative slew rate.
(4) Third-order filter; bandwidth = 80 kHz at –3 dB.

Electrical Characteristics (continued)

V_S = 1.8 V to 5.5 V; At T_A = 25 °C, R_L = 10 kΩ connected to $V_S/2$, V_{CM} = $V_S/2$, and V_{OUT} = $V_S/2$, unless otherwise noted.(1)

PARAMETER	TEST CONDITIONS	T_A = 25 °C			T_A = –40°C to 125°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Storage range		–65		150				°C

6.8 Typical Characteristics

Table 1. Characteristic Performance Measurements

TITLE	FIGURE
Open-Loop Gain and Phase vs Frequency	Figure 1
Open-Loop Gain vs Temperature	Figure 2
Quiescent Current vs Supply Voltage	Figure 3
Quiescent Current vs Temperature	Figure 4
Offset Voltage Production Distribution	Figure 5
Offset Voltage Drift Distribution	Figure 6
Offset Voltage vs Common-Mode Voltage (Maximum Supply)	Figure 7
Offset Voltage vs Temperature	Figure 8
CMRR and PSRR vs Frequency (RTI)	Figure 9
CMRR and PSRR vs Temperature	Figure 10
0.1-Hz to 10-Hz Input Voltage Noise (5.5 V)	Figure 11
Input Voltage Noise Spectral Density vs Frequency (1.8 V, 5.5 V)	Figure 12
Input Voltage Noise vs Common-Mode Voltage (5.5 V)	Figure 13
Input Bias and Offset Current vs Temperature	Figure 14
Open-Loop Output Impedance vs Frequency	Figure 15
Maximum Output Voltage vs Frequency and Supply Voltage	Figure 16
Output Voltage Swing vs Output Current (over Temperature)	Figure 17
Closed-Loop Gain vs Frequency, G = 1, –1, 10 (1.8 V)	Figure 18
Closed-Loop Gain vs Frequency, G = 1, –1, 10 (5.5 V)	Figure 19
Small-Signal Overshoot vs Load Capacitance	Figure 20
Small-Signal Step Response, Noninverting (1.8 V)	Figure 21
Small-Signal Step Response, Noninverting (5.5 V)	Figure 22
Large-Signal Step Response, Noninverting (1.8 V)	Figure 23
Large-Signal Step Response, Noninverting (5.5 V)	Figure 24
Positive Overload Recovery	Figure 25
Negative Overload Recovery	Figure 26
No Phase Reversal	Figure 27
Channel Separation vs Frequency (Dual)	Figure 28
THD+N vs Amplitude (G = 1, 2 kΩ, 10 kΩ)	Figure 29
THD+N vs Amplitude (G = –1, 2 kΩ, 10 kΩ)	Figure 30
THD+N vs Frequency (0.5 V_{RMS}, G = +1, 2 kΩ, 10 kΩ)	Figure 31
EMIRR	Figure 32

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

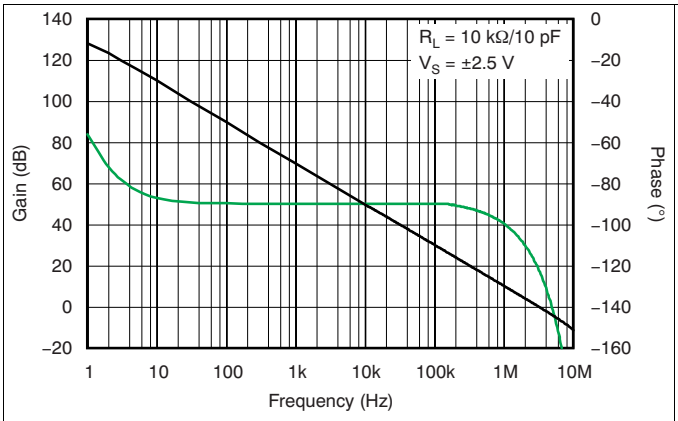


Figure 1. Open-Loop Gain and Phase vs Frequency

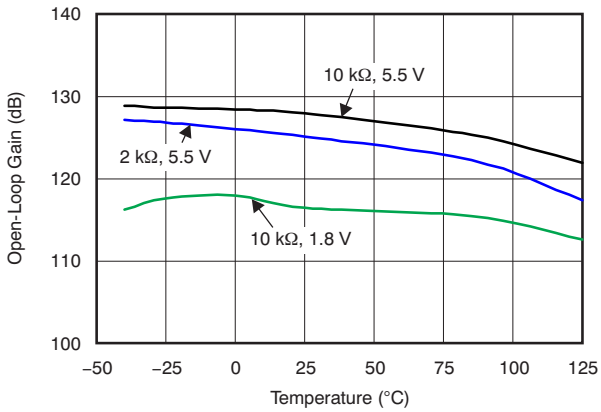


Figure 2. Open-Loop Gain vs Temperature

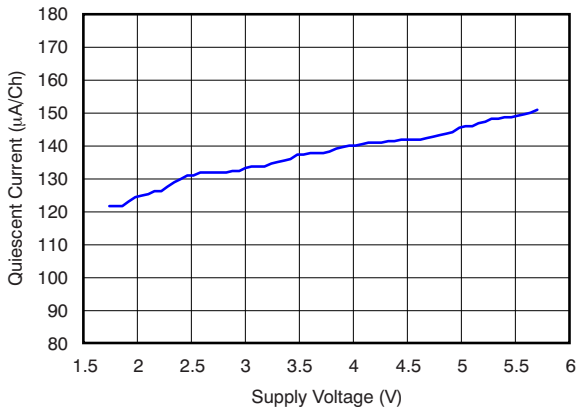


Figure 3. Quiescent Current vs Supply

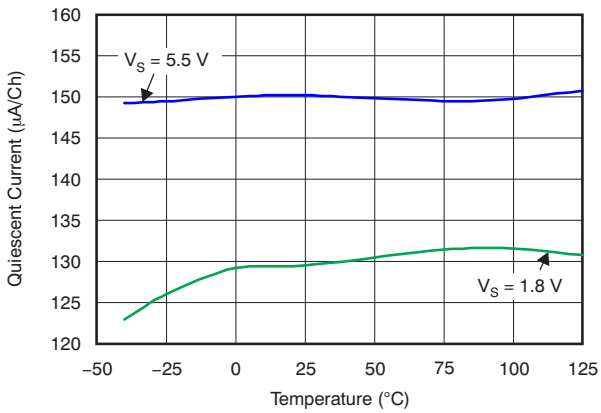


Figure 4. Quiescent Current vs Temperature

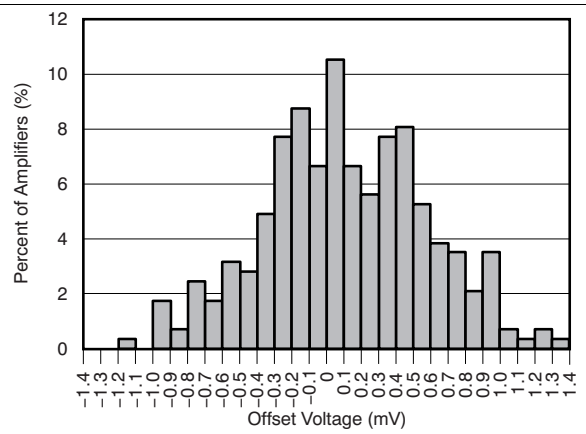


Figure 5. Offset Voltage Production Distribution

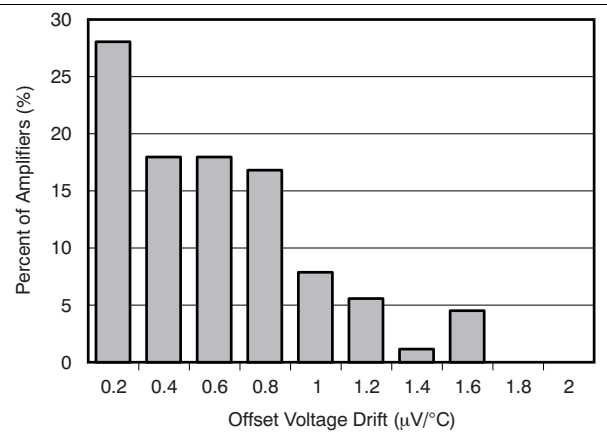


Figure 6. Offset Voltage Drift Distribution

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

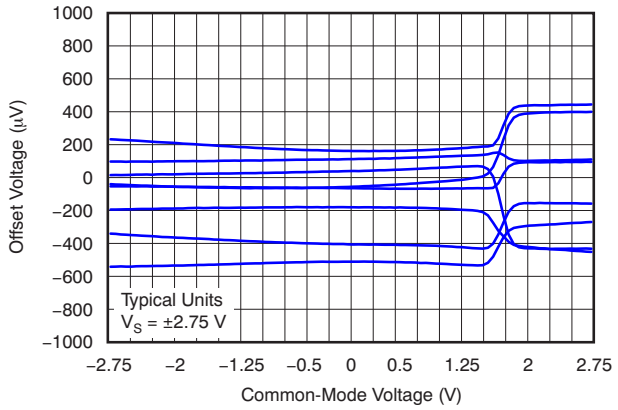


Figure 7. Offset Voltage vs Common-Mode Voltage

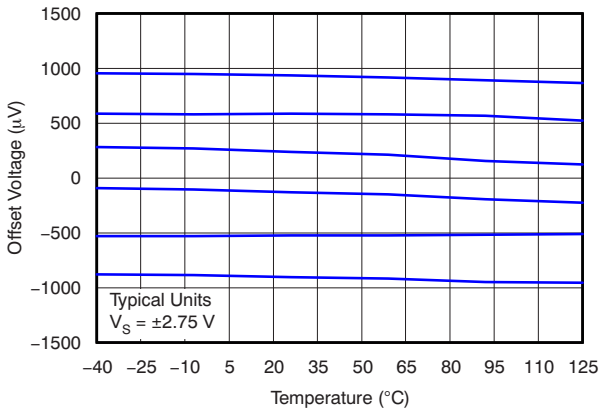


Figure 8. Offset Voltage vs Temperature

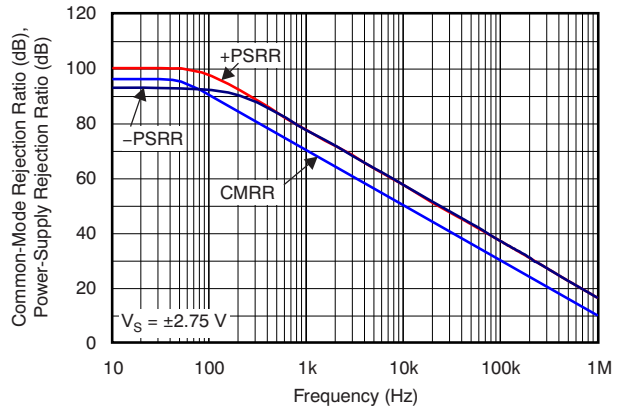


Figure 9. CMRR and PSRR vs Frequency (Referred-to-Input)

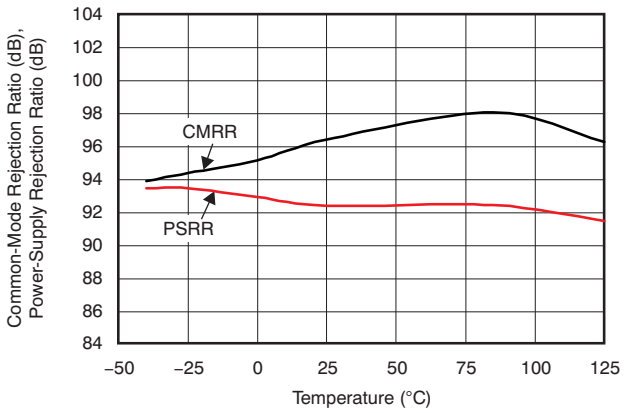


Figure 10. CMRR and PSRR vs Temperature

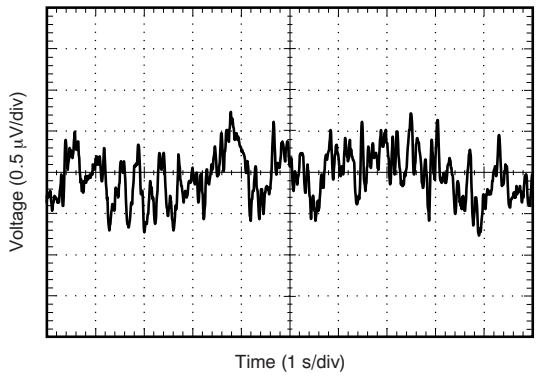


Figure 11. 0.1-Hz to 10-Hz Input Voltage Noise

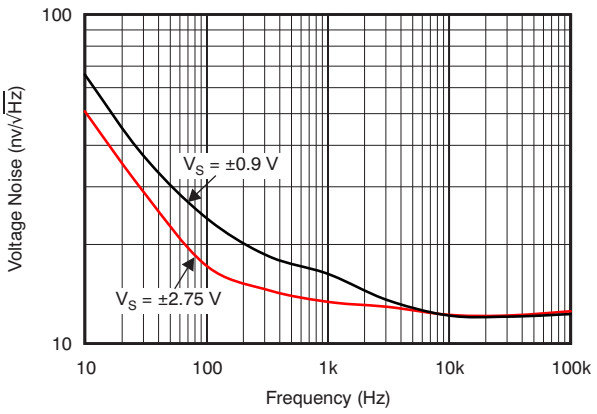


Figure 12. Input Voltage Noise Spectral Density vs Frequency

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

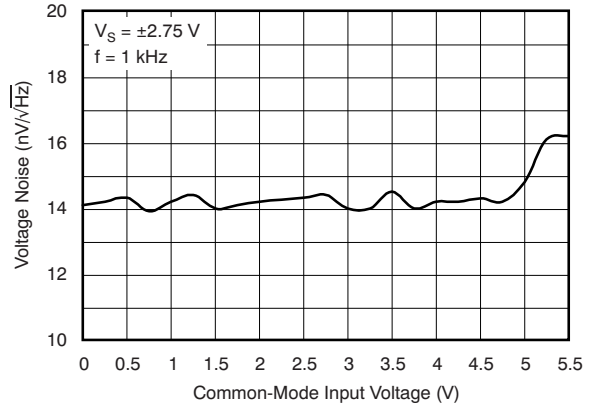


Figure 13. Voltage Noise vs Common-Mode Voltage

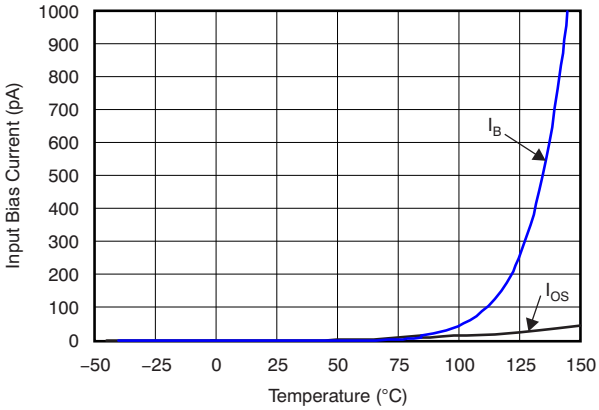


Figure 14. Input Bias and Offset Current vs Temperature

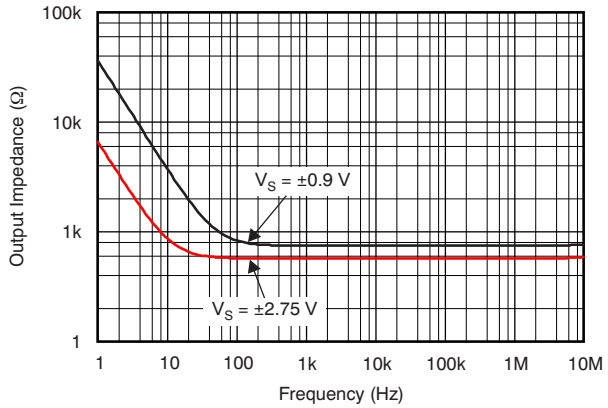


Figure 15. Open-Loop Output Impedance vs Frequency

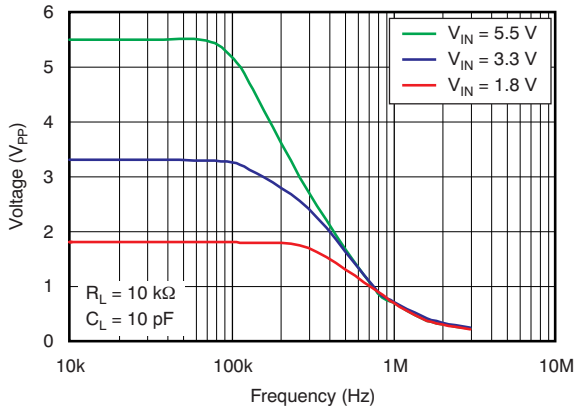


Figure 16. Maximum Output Voltage vs Frequency and Supply Voltage

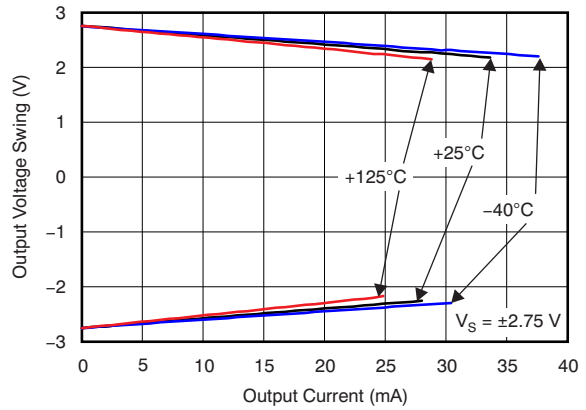


Figure 17. Output Voltage Swing vs Output Current (Over Temperature)

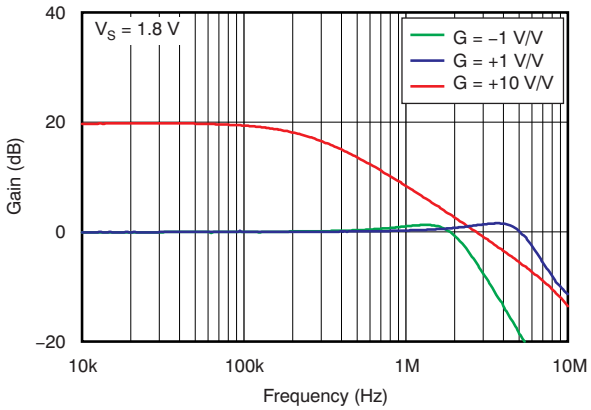


Figure 18. Closed-Loop Gain vs Frequency

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

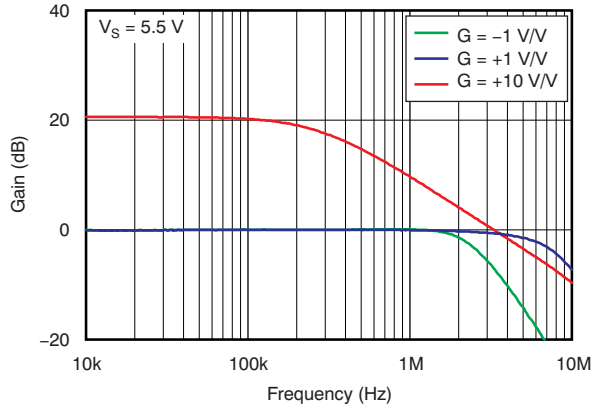


Figure 19. Closed-Loop Gain vs Frequency

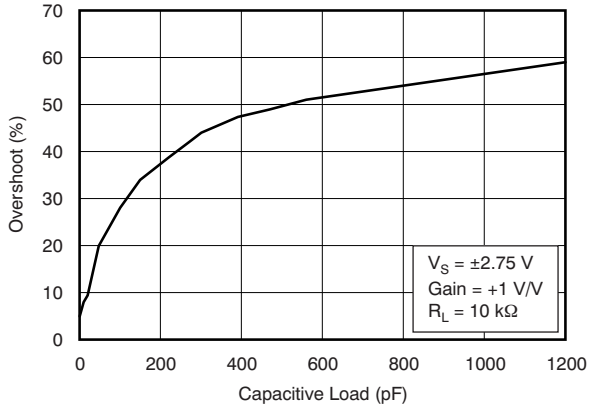


Figure 20. Small-Signal Overshoot vs Load Capacitance

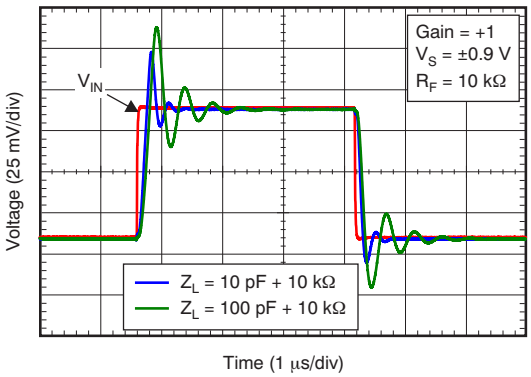


Figure 21. Small-Signal Pulse Response (Noninverting)

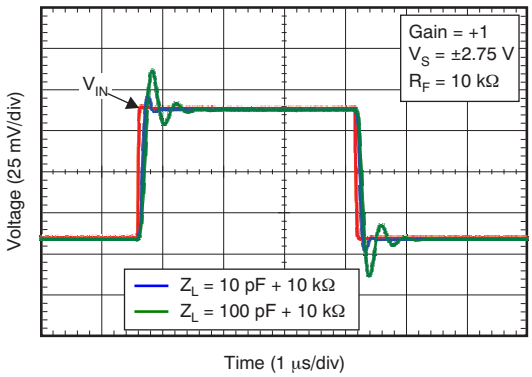


Figure 22. Small-Signal Pulse Response (Inverting)

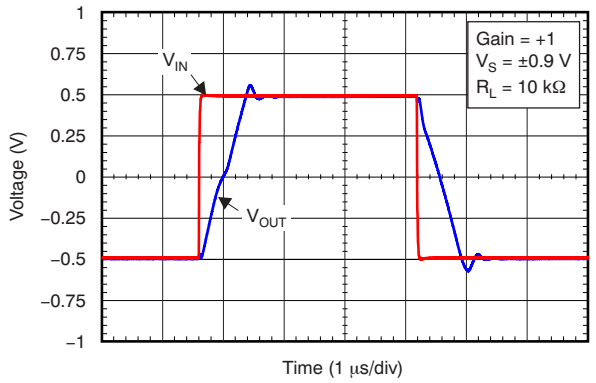


Figure 23. Large-Signal Pulse Response (Noninverting)

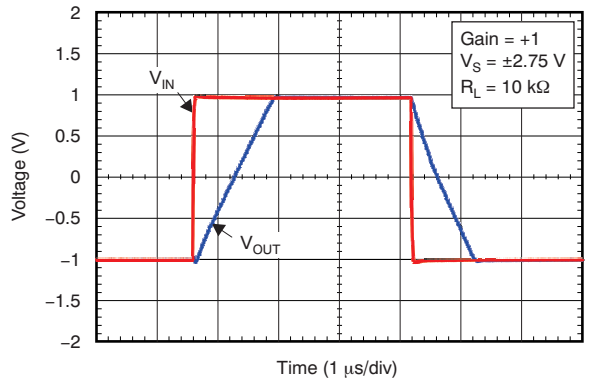


Figure 24. Large-Signal Pulse Response (Inverting)

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

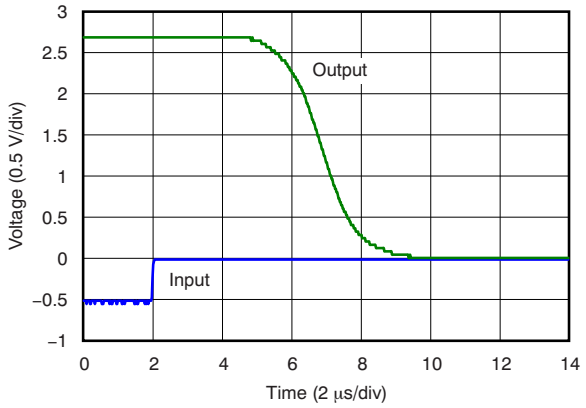


Figure 25. Positive Overload Recovery

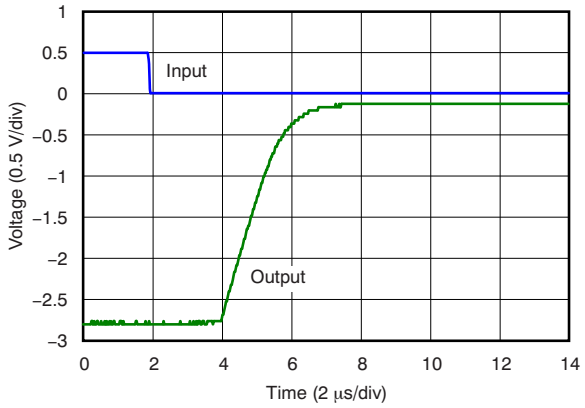


Figure 26. Negative Overload Recovery

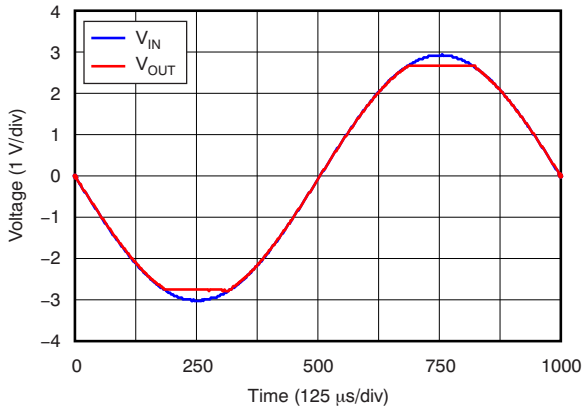


Figure 27. No Phase Reversal

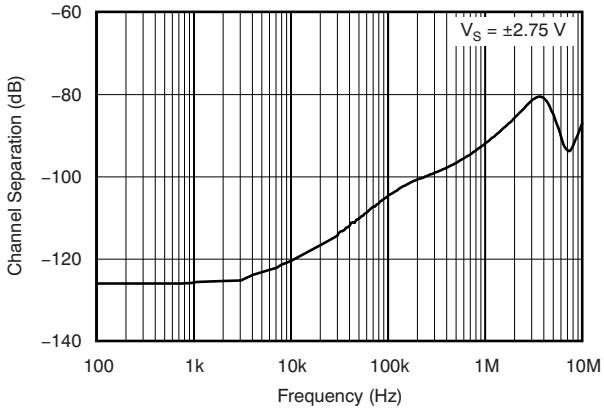


Figure 28. Channel Separation vs Frequency OPA2314

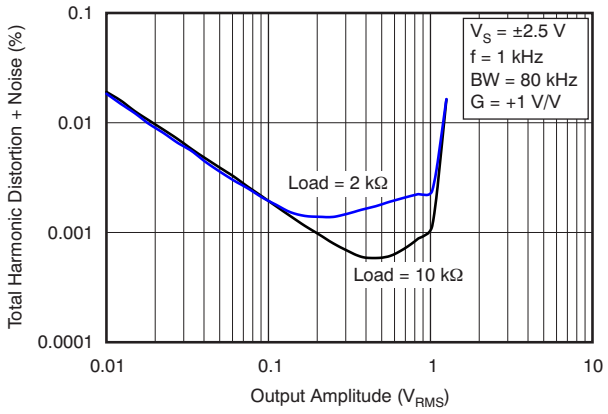


Figure 29. THD+N vs Output Amplitude (G = 1 V/V)

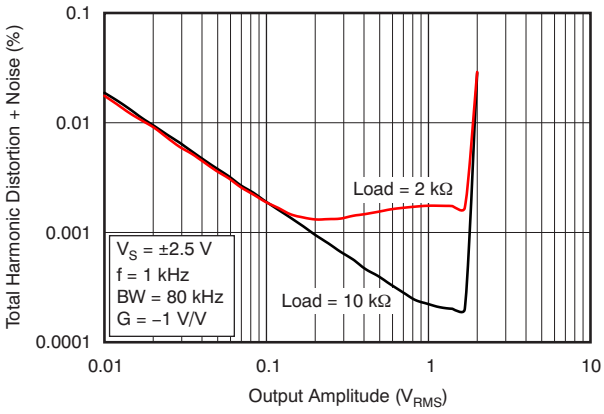


Figure 30. THD+N vs Output Amplitude (G = –1 V/V)

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

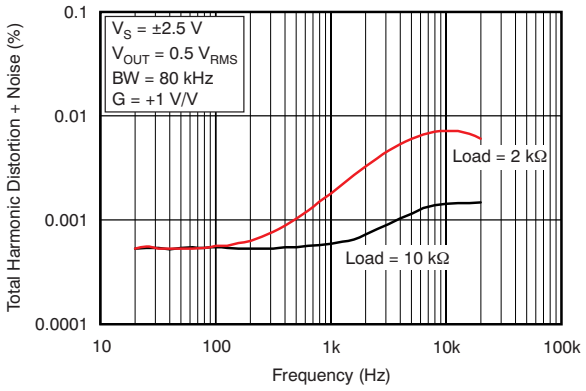


Figure 31. THD+N vs Frequency

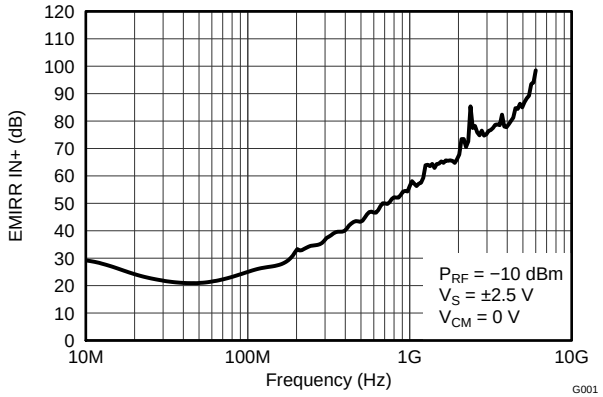


Figure 32. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR IN+) vs Frequency

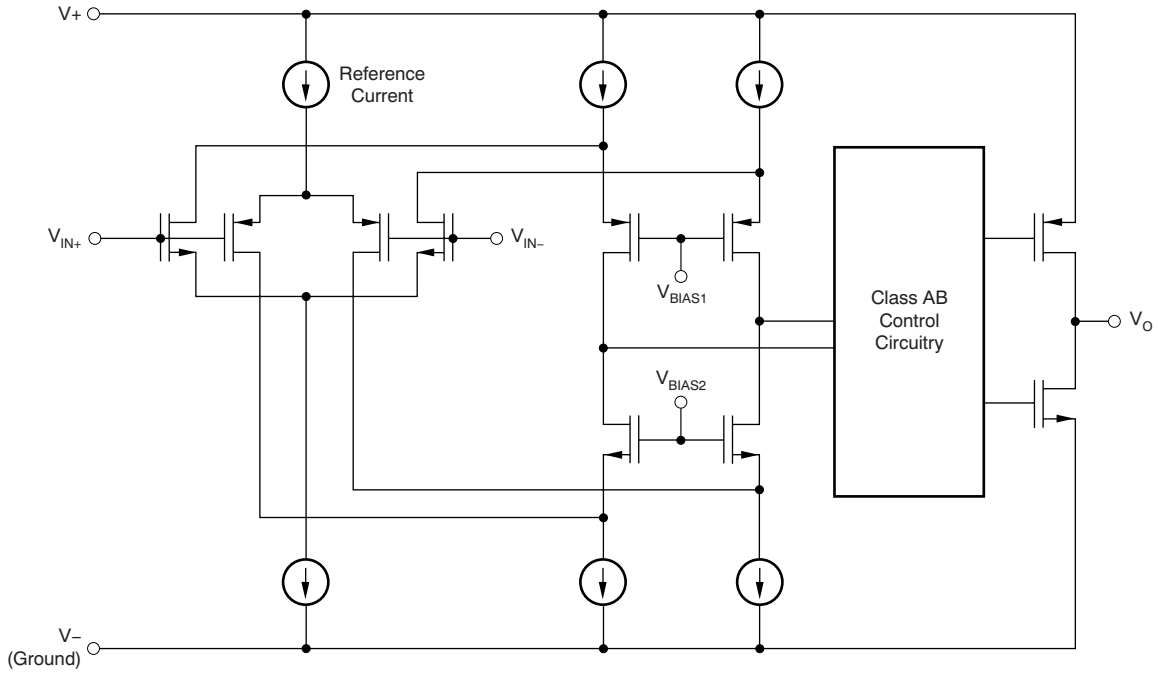
7 Detailed Description

7.1 Overview

The OPA314 is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPA314 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

The OPA314 features 3-MHz bandwidth and 1.5-V/μs slew rate with only 150-μA supply current per channel, providing good AC performance at very low power consumption. DC applications are also well served with a very low input noise voltage of 14 nV/√Hz at 1 kHz, low input bias current (0.2 pA), and an input offset voltage of 0.5 mV (typical).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA314 series operational amplifiers are fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* graphs. Power-supply pins should be bypassed with 0.01-μF ceramic capacitors.

Feature Description (continued)

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPA314 series extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 33. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3 V to 200 mV above the positive supply, while the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 1.3 V. There is a small transition region, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region can vary up to 300 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to device operation outside this region.

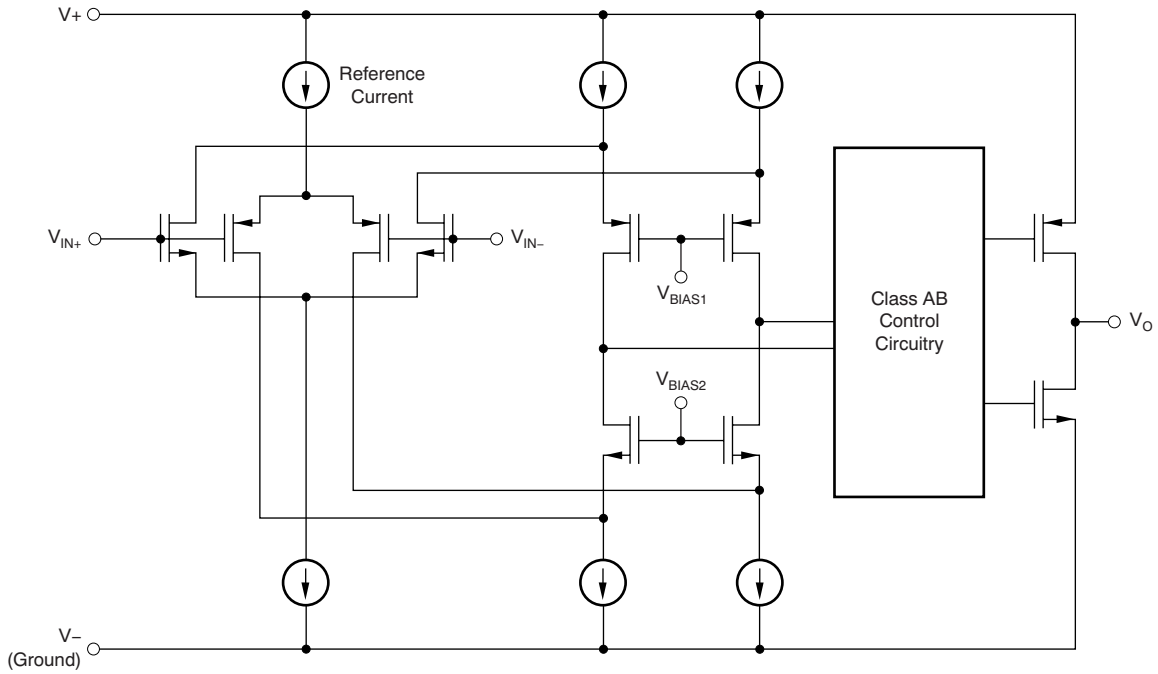


Figure 33. Simplified Schematic

7.3.3 Input and ESD Protection

The OPA314 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* . Figure 34 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

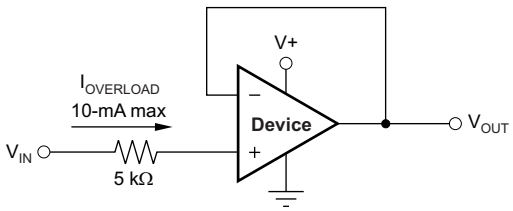


Figure 34. Input Current Protection

Feature Description (continued)

7.3.4 Common-Mode Rejection Ratio (CMRR)

CMRR for the OPA314 is specified in several ways so the best match for a given application may be used; see the *Electrical Characteristics*. First, the CMRR of the device in the common-mode range below the transition region [V_{CM} < (V+) – 1.3 V] is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at (V_{CM} = –0.2 V to 5.7 V). This last value includes the variations seen through the transition region (see Figure 7).

7.3.5 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the DC offset observed at the amplifier output may shift from its nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The OPA314 operational amplifier family incorporate an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows operational amplifiers to be directly compared by the EMI immunity. Figure 32 illustrates the results of this testing on the OPAx314. Detailed information can also be found in the application report, *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

7.3.6 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the OPA314 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 10 kΩ, the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; refer to *Figure 17*.

7.3.7 Capacitive Load and Stability

The OPA314 is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the OPA314 can become unstable. The particular operational amplifiers circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (+1-V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA314 remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See Figure 20.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor, typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 35. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

Feature Description (continued)

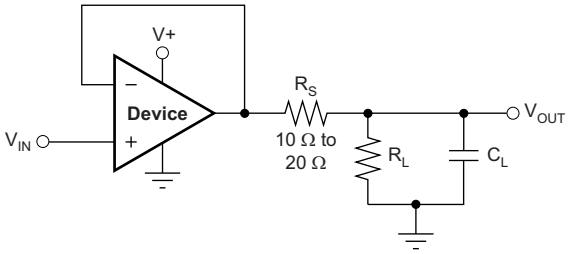


Figure 35. Improving Capacitive Load Drive

7.4 Device Functional Modes

The OPA2314 device is powered on when the supply is connected. The device can be operated as a single-supply operational amplifier or a dual-supply amplifier, depending on the application.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA2314 device is a low-power, rail-to-rail input and output operational amplifier specifically designed for portable applications. The device operates from 1.8 V to 5.5 V, is unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPA2314 device to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes the device ideal for driving sampling analog-to-digital converters (ADCs).

The OPA2314 device features a 3-MHz bandwidth and 1.5-V/μs slew rate with only 150-μA supply current per channel, providing good AC performance at very low power consumption. DC applications are also well served with a very-low input noise voltage of 14 nV/√Hz at 1 kHz, low-input bias current (0.2 pA), and an input offset voltage of 0.5 mV (typical).

8.1.1 General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as Figure 36 shows.

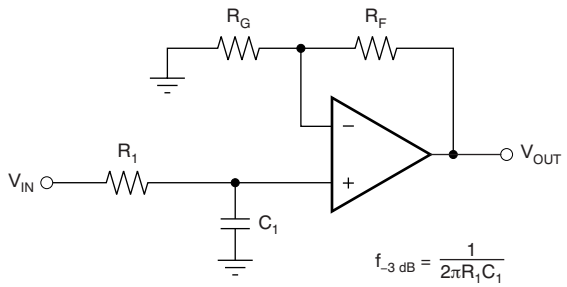


Figure 36. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task, as Figure 37 shows. For best results, the amplifier should have a bandwidth that is eight to 10 times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.

Application Information (continued)

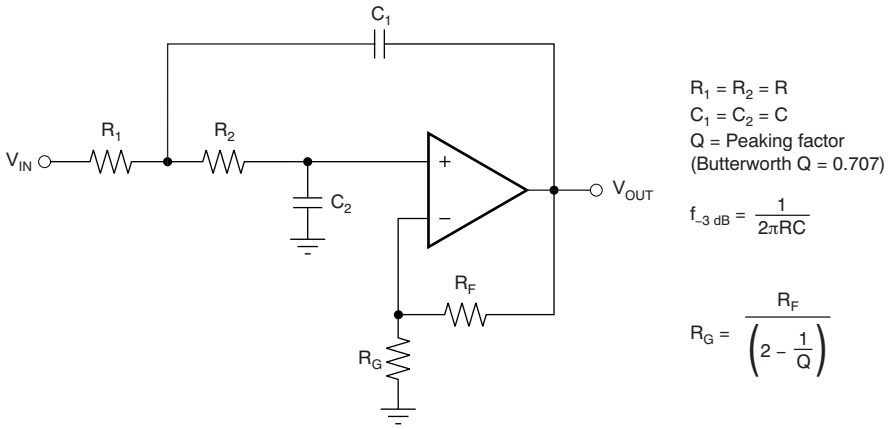


Figure 37. Two-Pole Low-Pass Sallen-Key Filter

8.1.2 Capacitive Load and Stability

The OPA2314 device is designed to be used in applications where driving a capacitive load is required. As with all op-amps, specific instances can occur where the OPA2314 device can become unstable. The particular op-amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An op-amp in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op-amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA2314 device remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See the graph, *Figure 20*.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor, typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 38. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

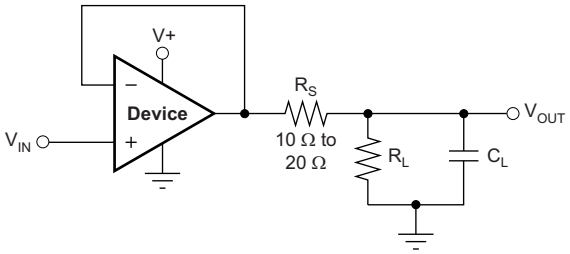


Figure 38. Improving Capacitive Load Drive

8.2 Typical Application

Some applications require differential signals. Figure 39 shows a simple circuit to convert a single-ended input of 0.1 V to 2.4 V into a differential output of ±2.3 V on a single 2.7-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier functions as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate $V_{OUT–}$. Both V_{OUT+} and $V_{OUT–}$ range from 0.1 V to 2.4 V. The difference, V_{DIFF}, is the difference between V_{OUT+} and $V_{OUT–}$. This makes the differential output voltage range 2.3 V.

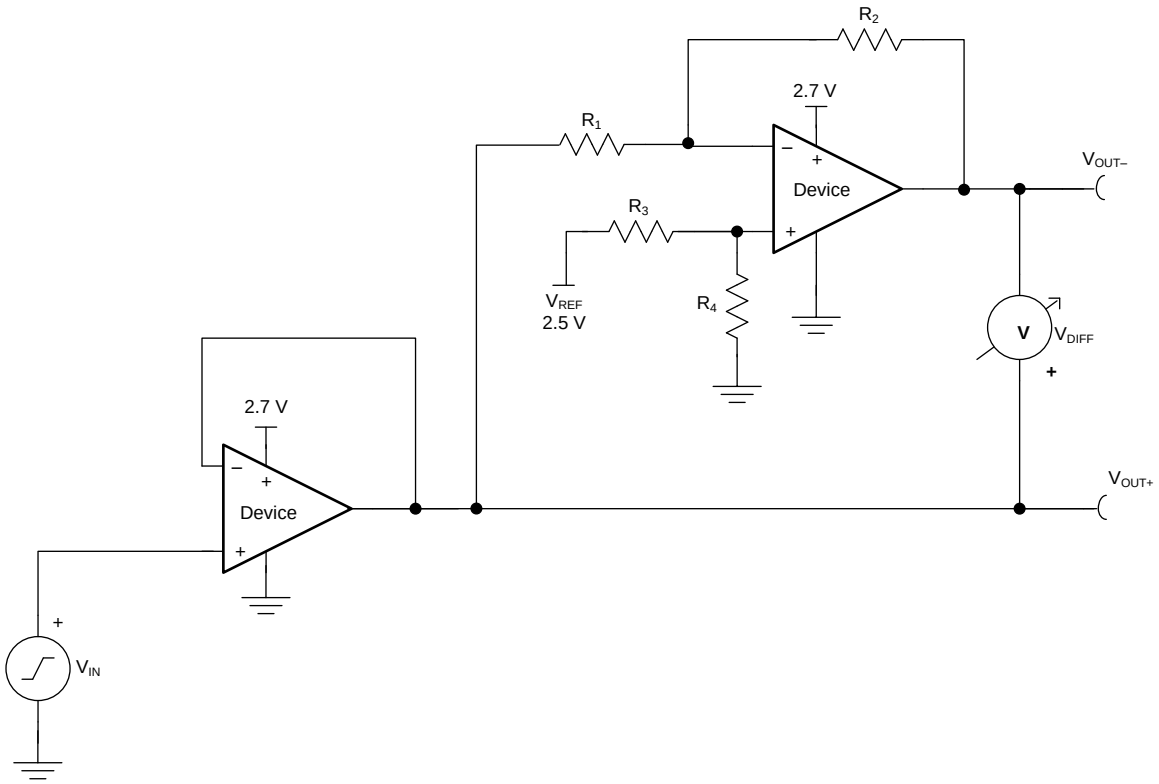


Figure 39. Schematic for a Single-Ended Input to Differential Output Conversion

8.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 2.7 V
- Reference voltage: 2.5 V
- Input: 0.1 V to 2.4 V
- Output differential: ±2.3 V
- Output common-mode voltage: 1.25 V
- Small-signal bandwidth: 1 MHz

8.2.2 Detailed Design Procedure

The circuit in Figure 39 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and $V_{OUT–}$ using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (as shown in Equation 1). $V_{OUT–}$ is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for $V_{OUT–}$ is given in Equation 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT–} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) – V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

Typical Application (continued)

The differential output signal, V_{DIFF}, is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-}. Equation 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to V_{REF}. The differential output range is 2 × V_{REF}. Furthermore, the common-mode voltage is one half of V_{REF} (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) \quad (3)$$

$$V_{OUT+} = V_{IN} \quad (4)$$

$$V_{OUT-} = V_{REF} - V_{IN} \quad (5)$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \quad (6)$$

$$V_{CM} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2} V_{REF} \quad (7)$$

8.2.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common-mode input range and output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design, so the OPA2314-Q1 device is selected because its bandwidth is greater than the target of 1 MHz. The bandwidth and power ratio makes this device power efficient and the low offset and drift ensure good accuracy for moderate precision applications.

8.2.2.2 Passive Component Selection

Because the transfer function of Vout– is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design uses resistors with resistance values of 49.9 kΩ and tolerances of 0.1%. However, if the noise of the system is a key parameter, smaller resistance values (6 kΩ or lower) can be selected to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

8.2.3 Application Curves

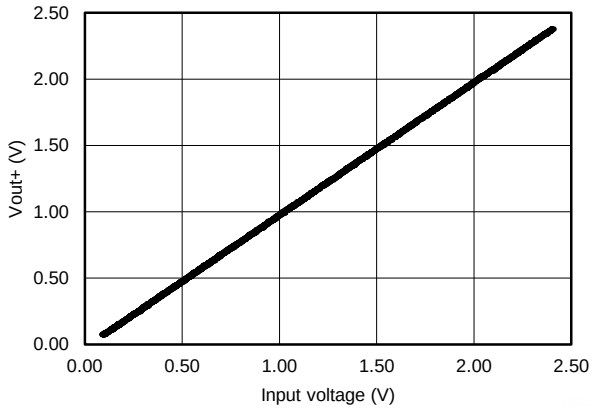


Figure 40. V_{OUT+} vs Input Voltage

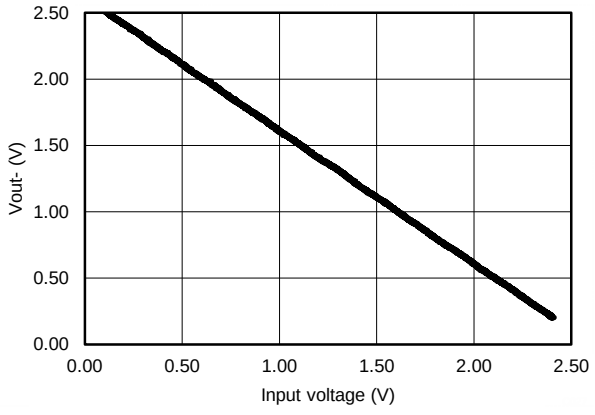


Figure 41. V_{OUT-} vs Input Voltage

Typical Application (continued)

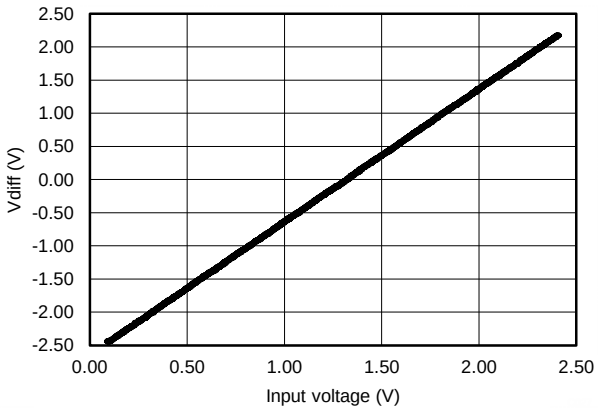


Figure 42. V_{DIFF} vs Input Voltage

9 Power Supply Recommendations

The OPA2314-Q1 device is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines* section.

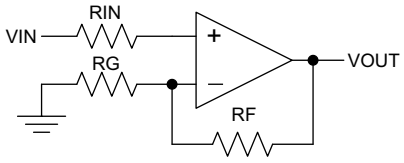
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in Figure 43.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example



(Schematic Representation)

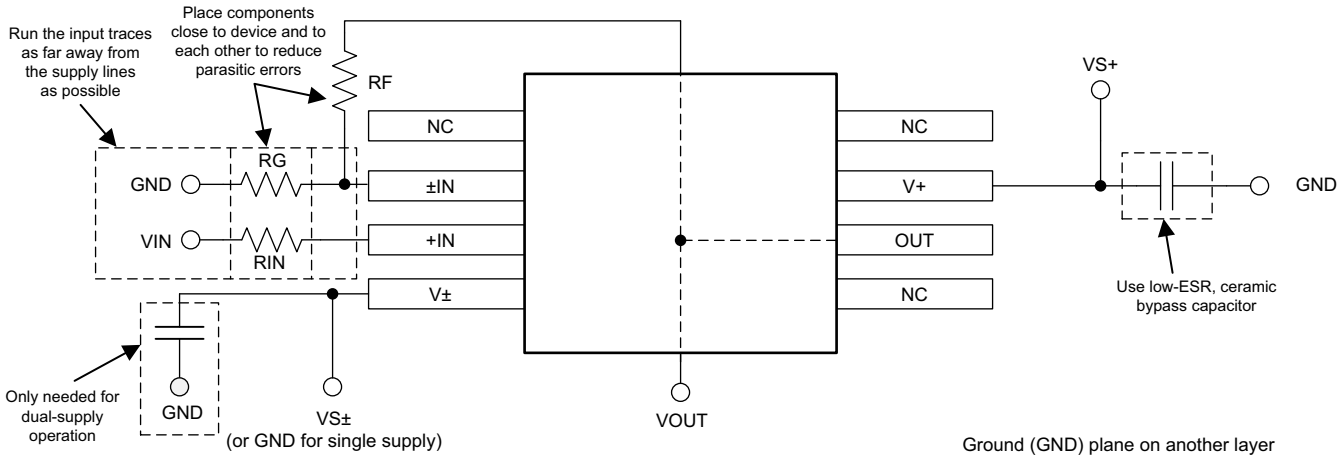


Figure 43. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

11.1.1.1 DFN Package

The OPA2314 (dual version) uses the DFN style package (also known as SON); this package is a QFN with contacts on only two sides of the package bottom. This leadless package maximizes printed circuit board (PCB) space and offers enhanced thermal and electrical characteristics through an exposed pad. One of the primary advantages of the DFN package is its low, 0.9-mm height. DFN packages are physically small, have a smaller routing area, improved thermal performance, reduced electrical parasitics, and use a pinout scheme that is consistent with other commonly-used packages, such as SO and MSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can easily be mounted using standard PCB assembly techniques. See Application Note, *QFN/SON PCB Attachment* (SLUA271) and Application Report, *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download from www.ti.com.

NOTE

The exposed leadframe die pad on the bottom of the DFN package should be connected to the most negative potential (V–).

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA314	Click here	Click here	Click here	Click here	Click here
OPA2314	Click here	Click here	Click here	Click here	Click here
OPA4314	Click here	Click here	Click here	Click here	Click here

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2314AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2314	Samples
OPA2314AIDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OCPQ	Samples
OPA2314AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OCPQ	Samples
OPA2314AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2314	Samples
OPA2314AIDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXY	Samples
OPA2314AIDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXY	Samples
OPA314AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAZ	Samples
OPA314AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAZ	Samples
OPA314AIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SAA	Samples
OPA314AIDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SAA	Samples
OPA4314AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4314	Samples
OPA4314AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4314	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA2314, OPA314, OPA4314 :

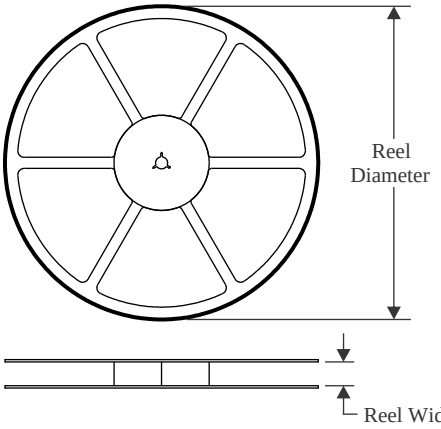
- Automotive : OPA2314-Q1, OPA314-Q1, OPA4314-Q1
- Enhanced Product : OPA2314-EP

NOTE: Qualified Version Definitions:

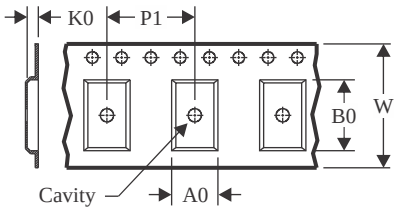
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

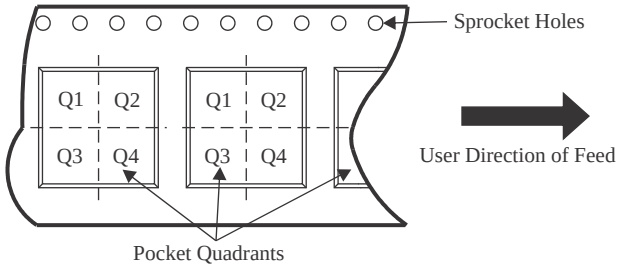


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

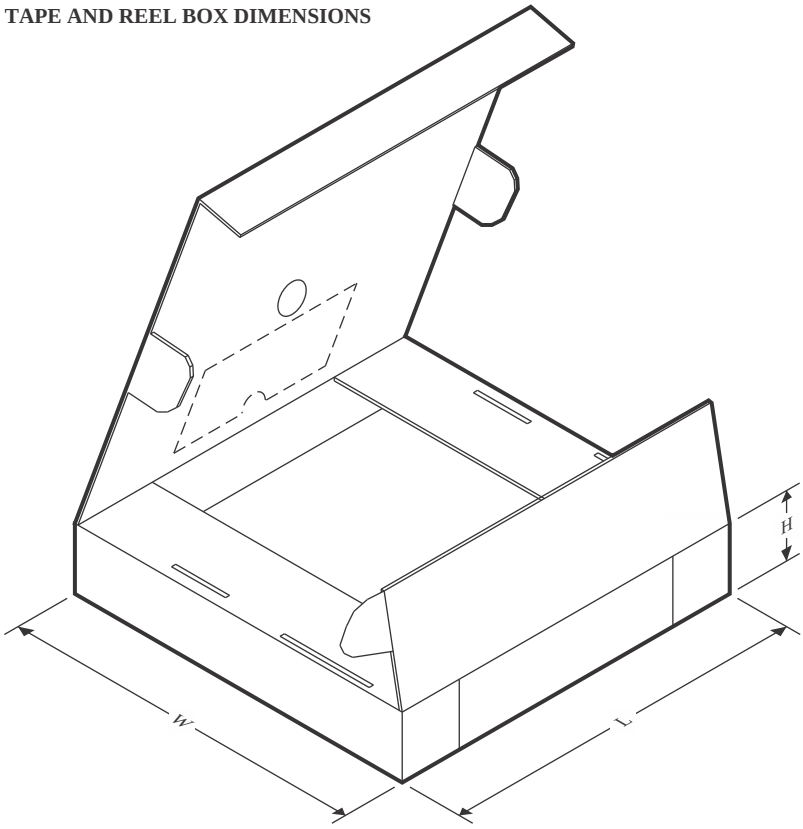
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2314AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2314AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2314AIDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2314AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA314AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA314AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA314AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA4314AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

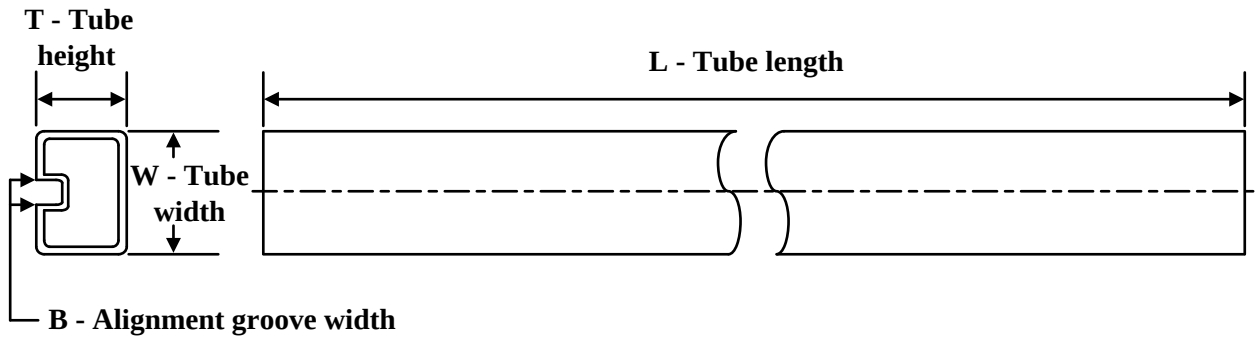
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2314AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2314AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2314AIDRBR	SON	DRB	8	3000	367.0	367.0	35.0
OPA2314AIDRBT	SON	DRB	8	250	210.0	185.0	35.0
OPA314AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA314AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA314AIDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA4314AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

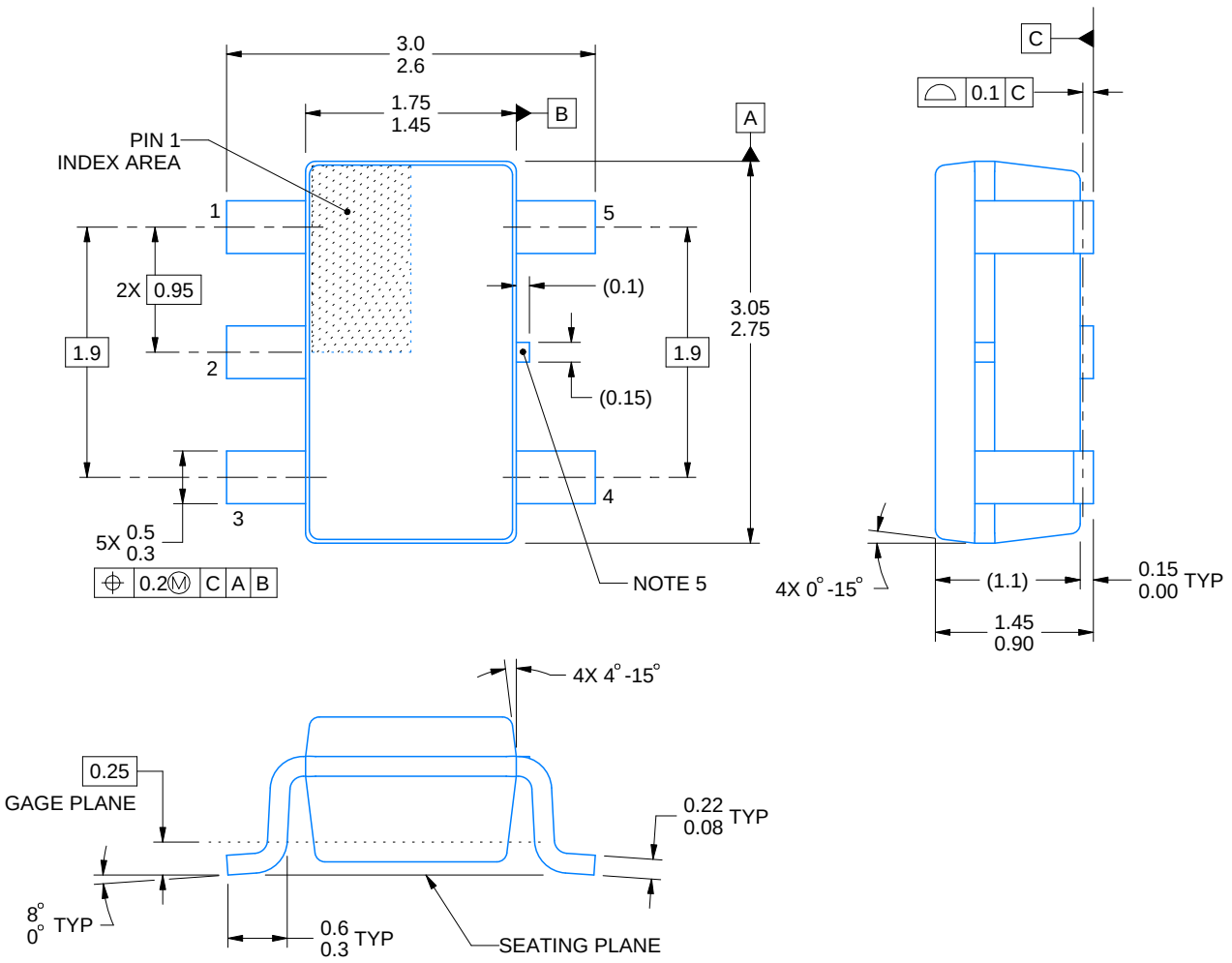
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2314AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2314AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA4314AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

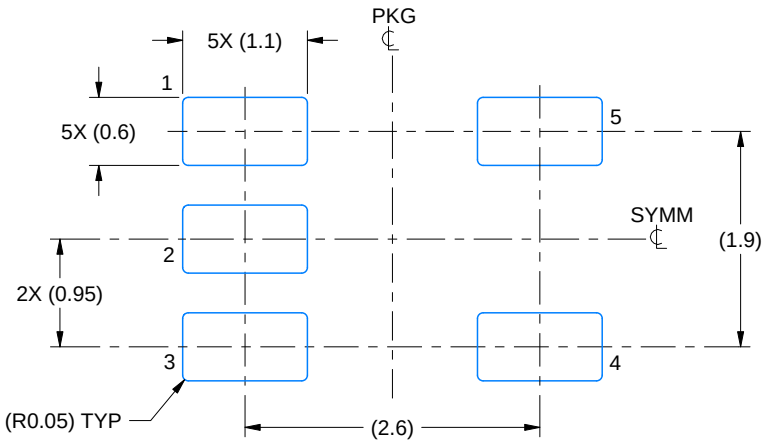
SMALL OUTLINE TRANSISTOR



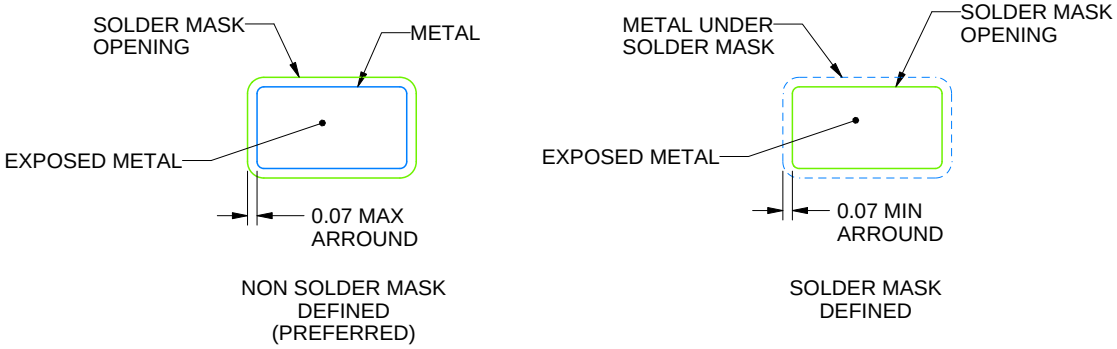
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

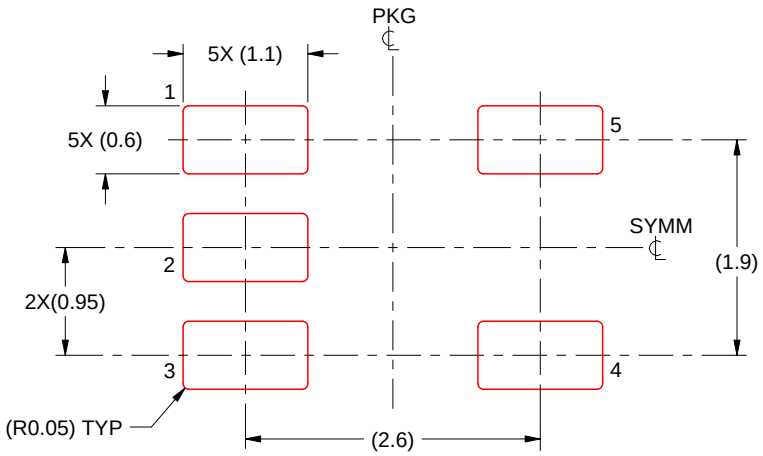


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

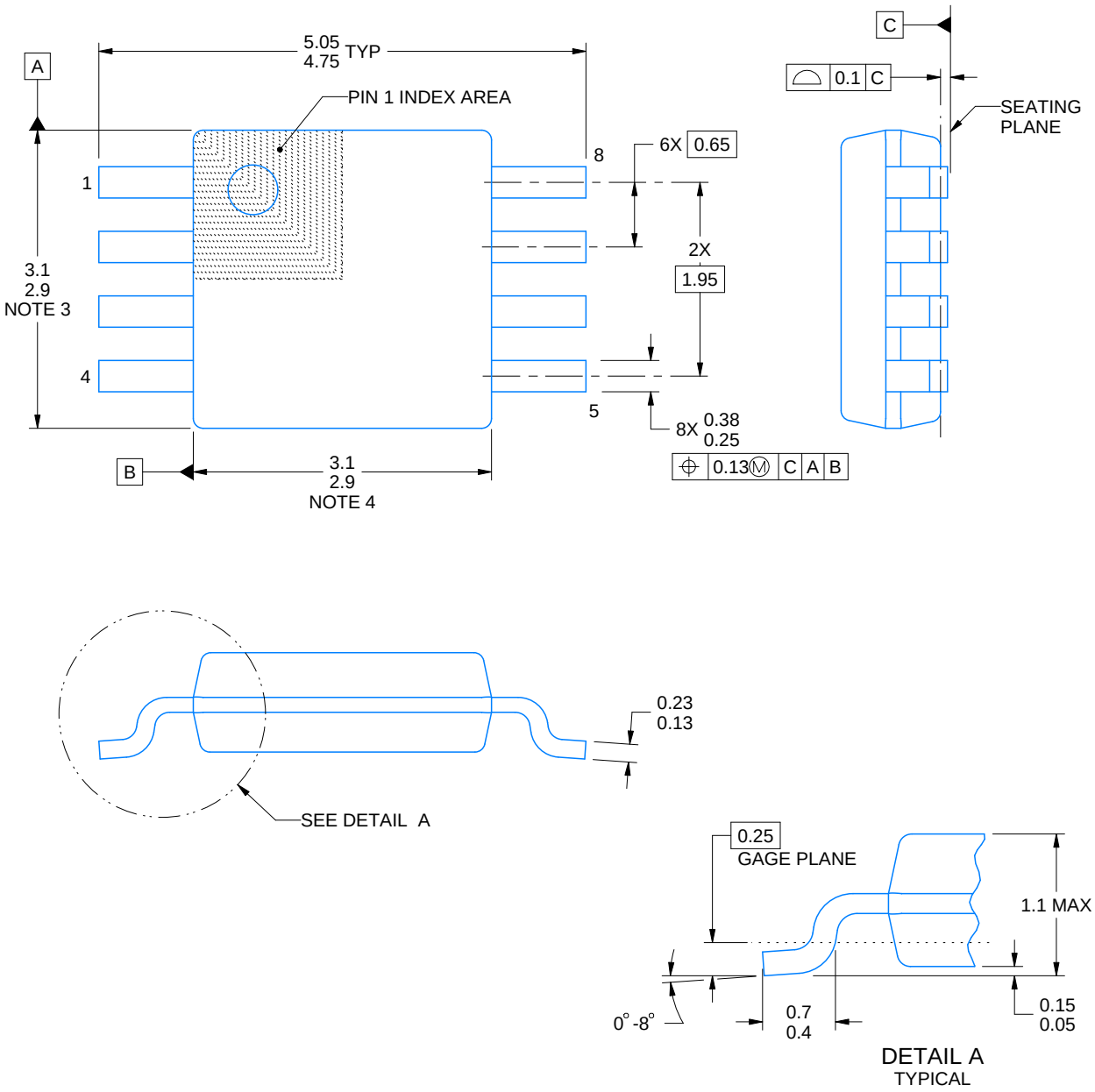
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

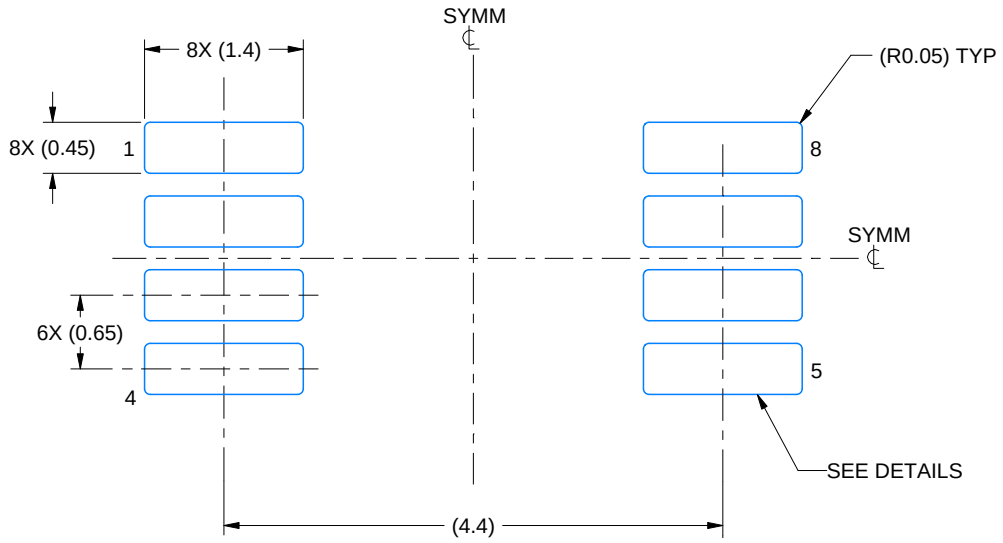


4214862/A 04/2023

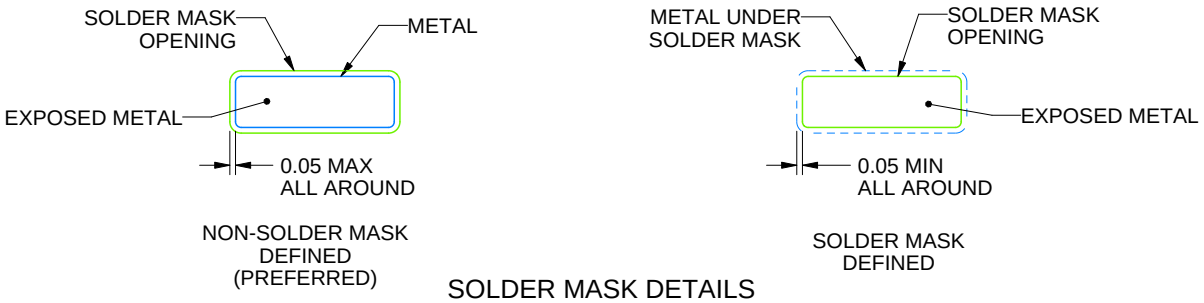
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

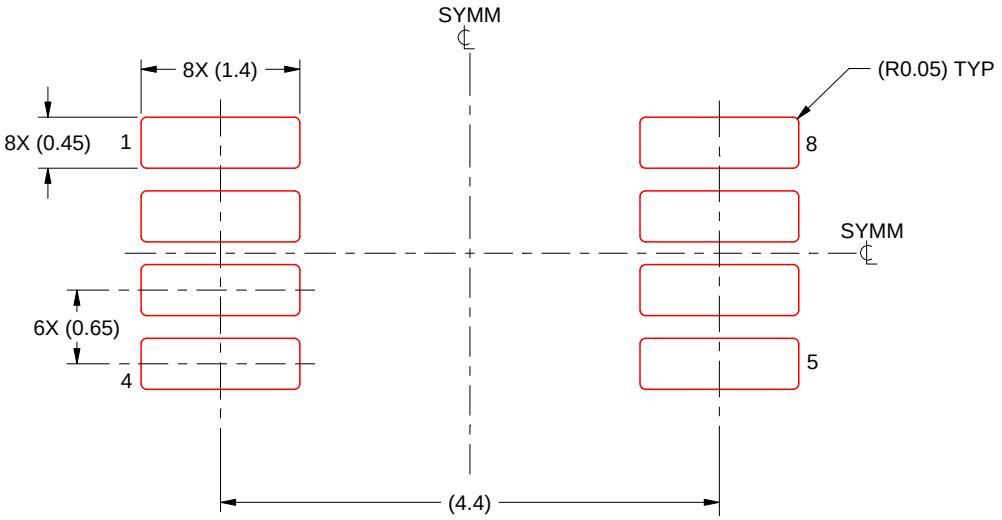


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8 VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

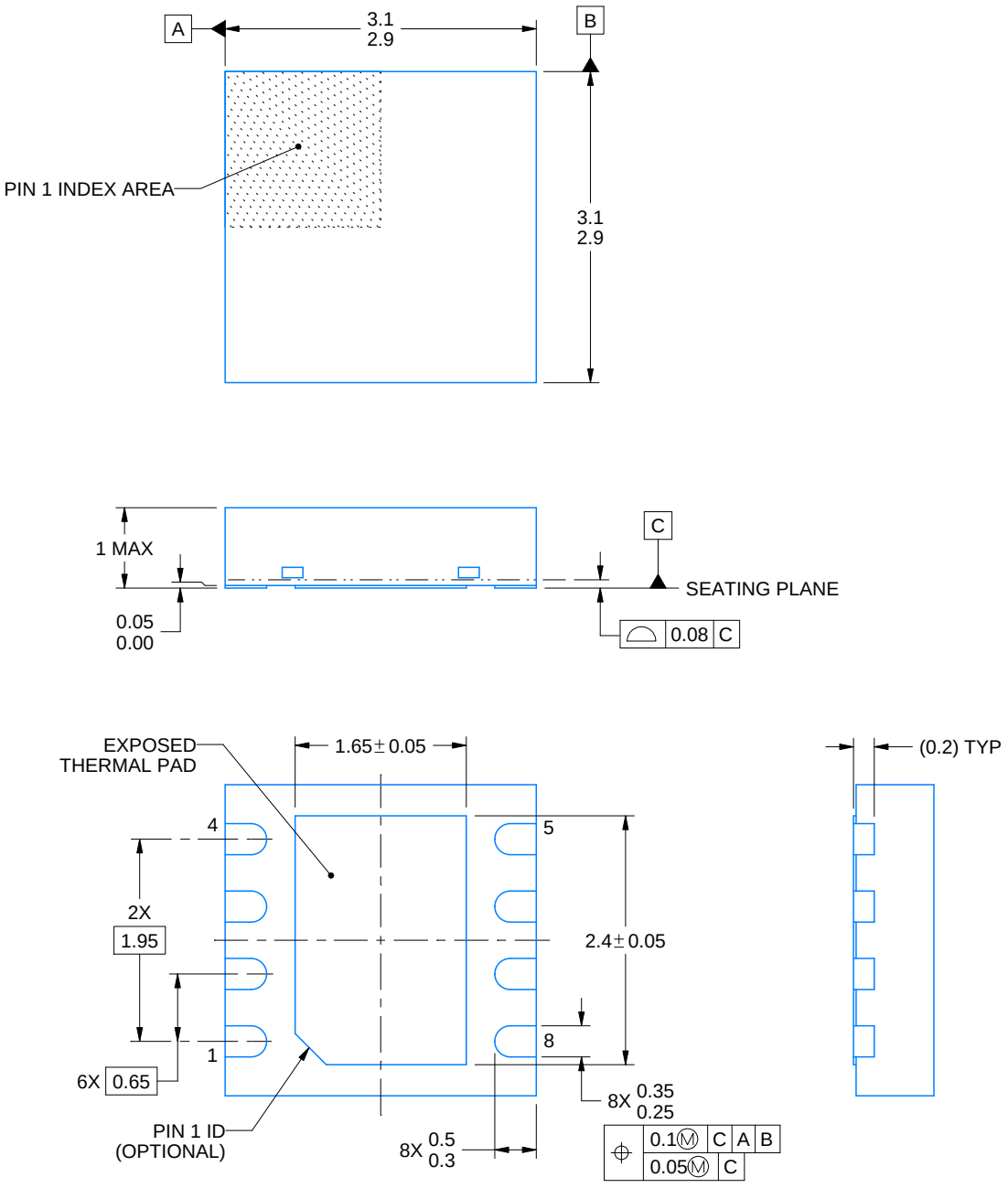
4203482/L

PACKAGE OUTLINE

DRB0008B

VSON - 1 mm max height

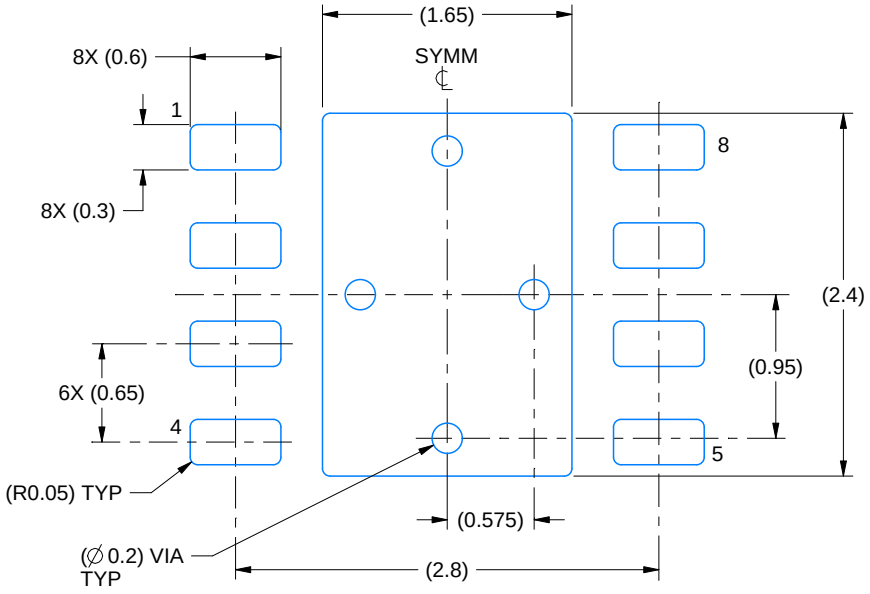
PLASTIC SMALL OUTLINE - NO LEAD



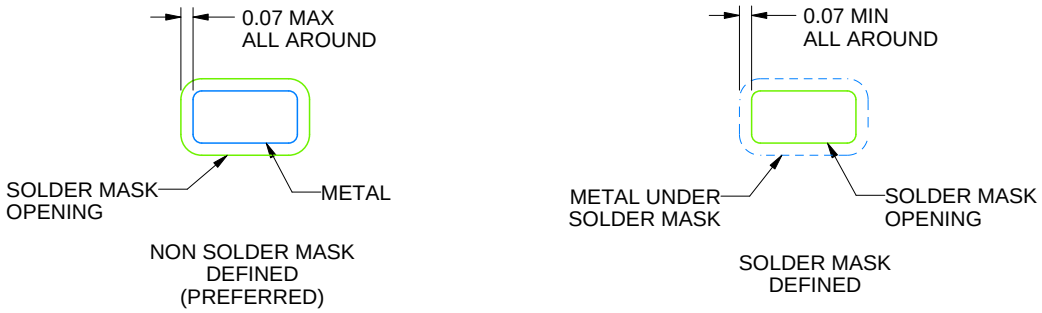
4218876/A 12/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

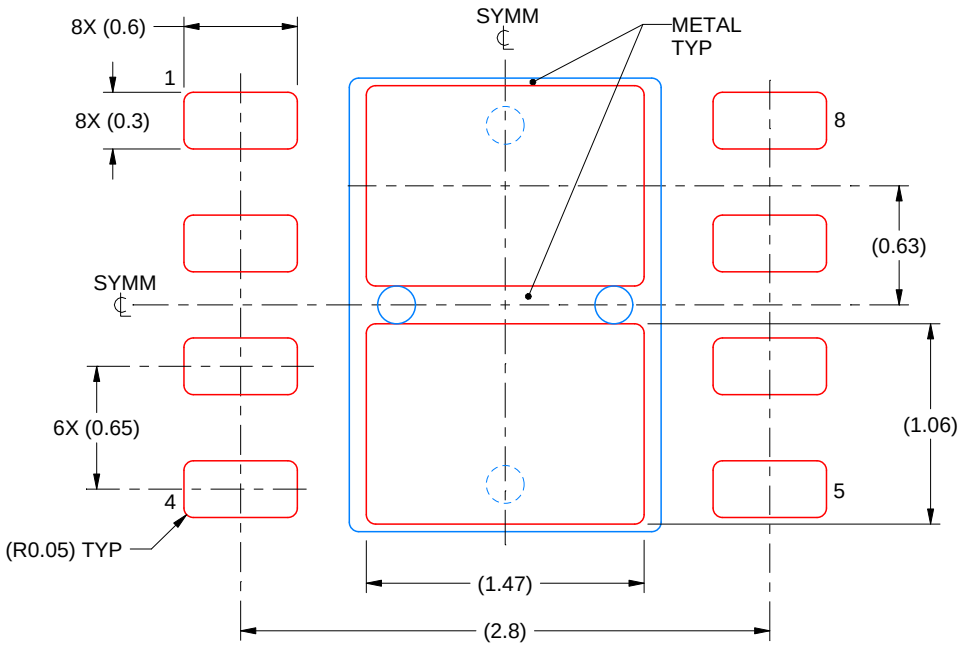


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

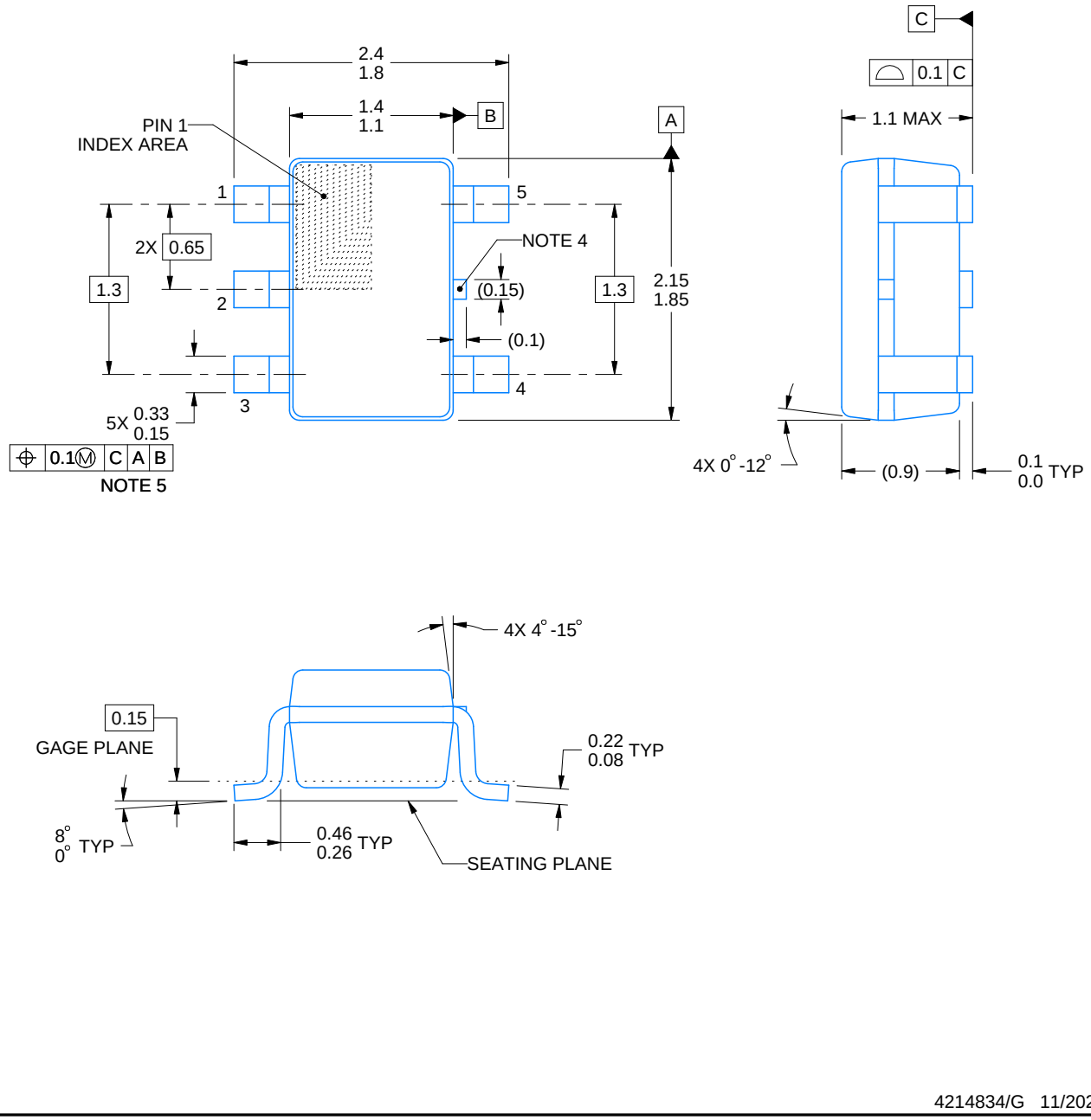
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

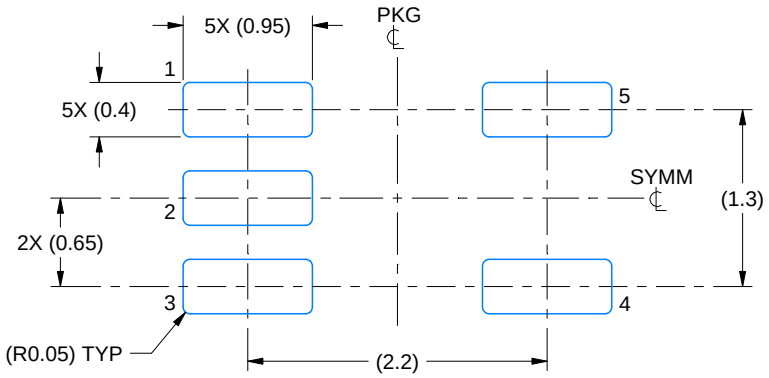
SMALL OUTLINE TRANSISTOR



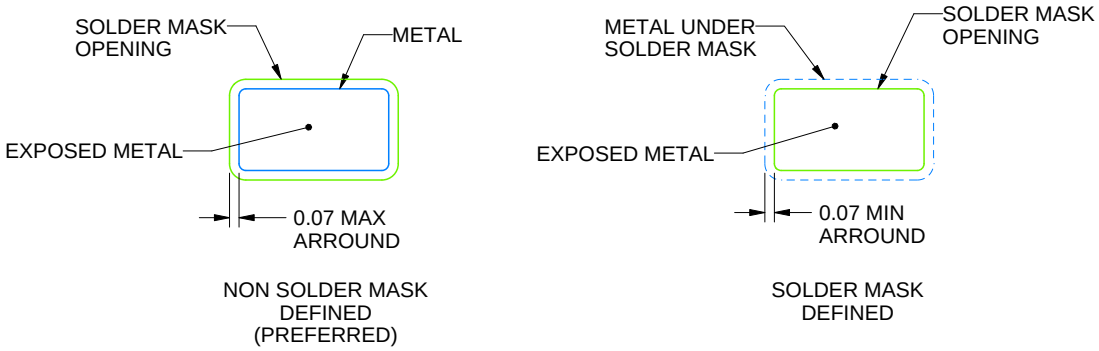
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

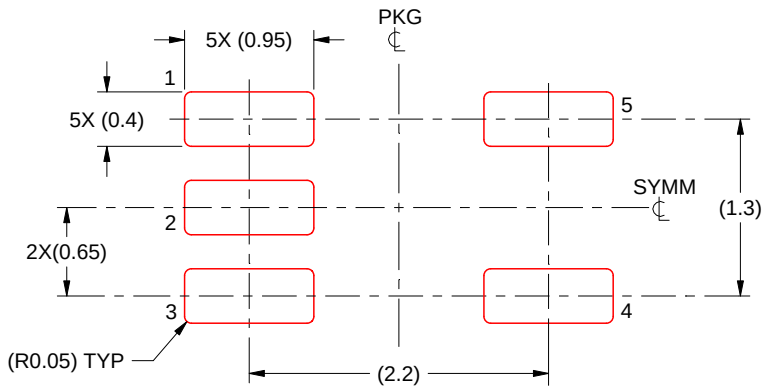


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

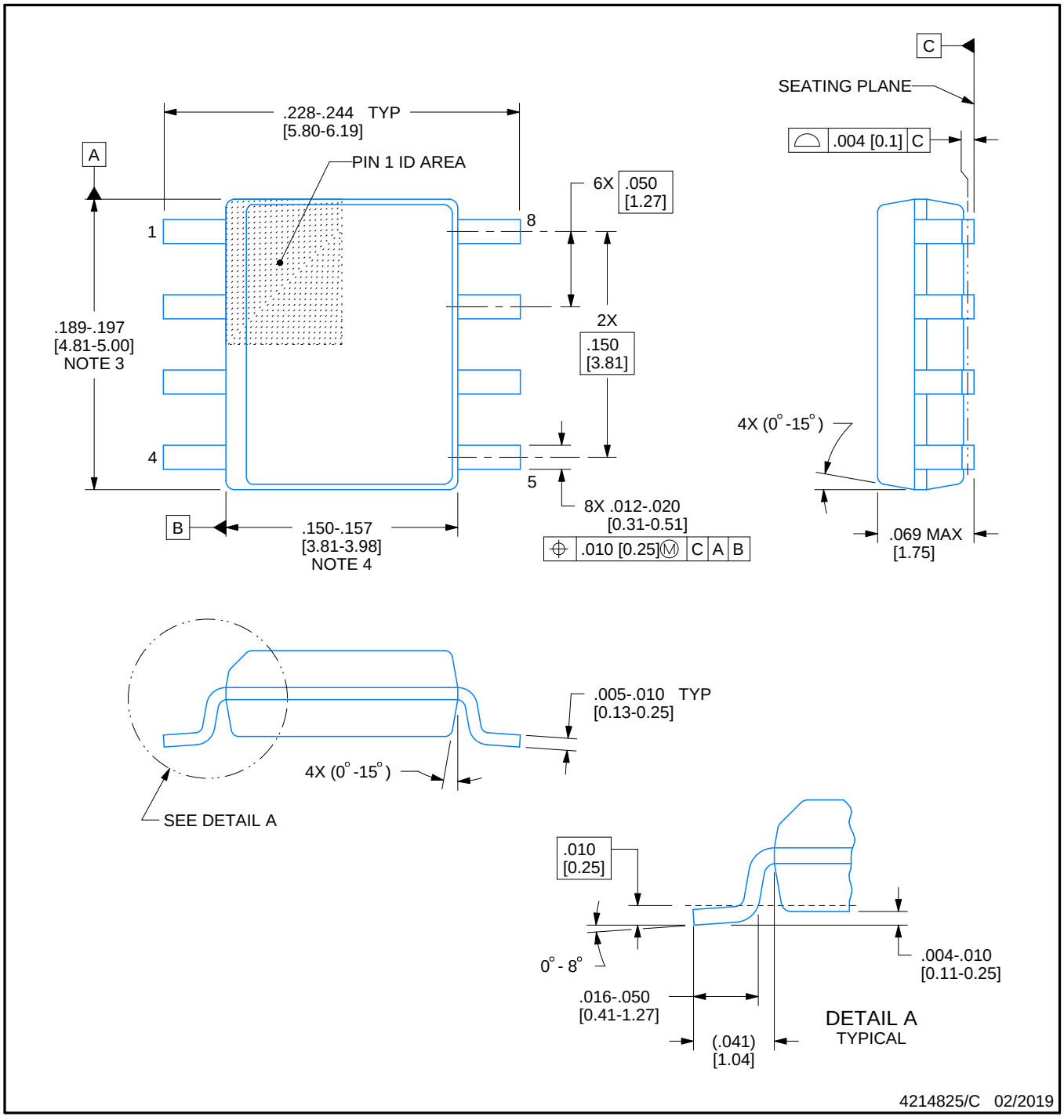
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

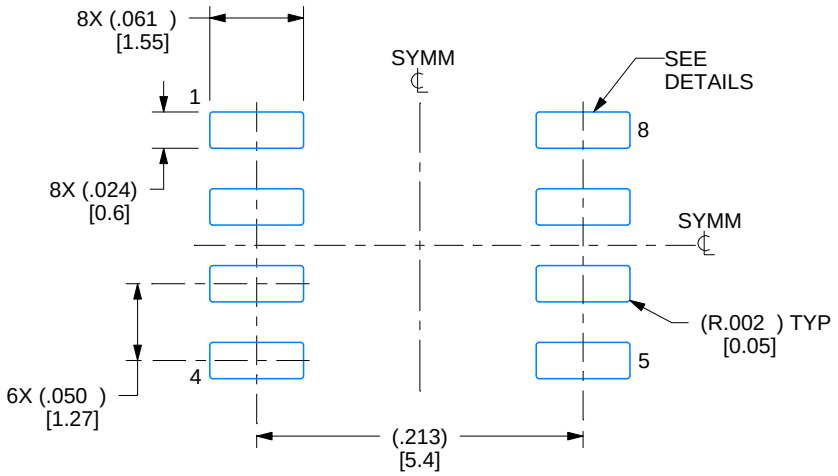
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

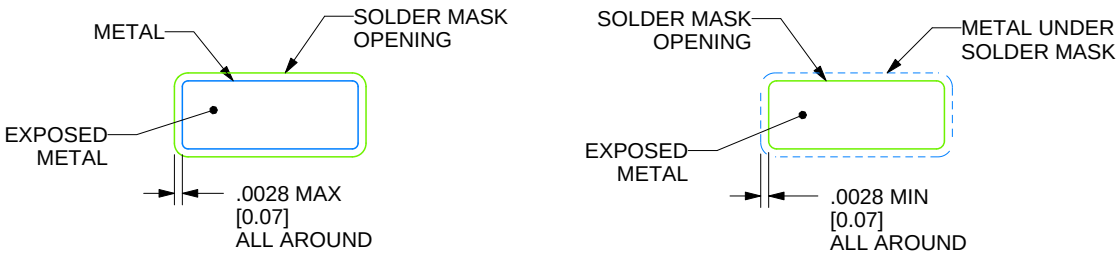
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

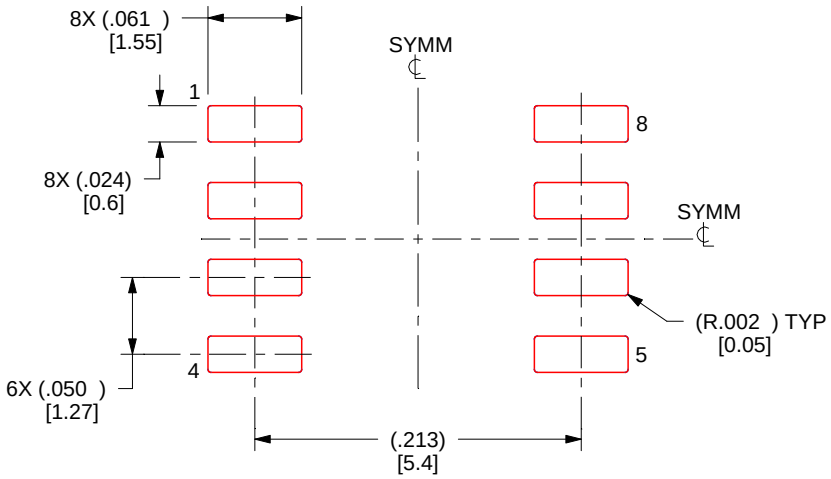
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

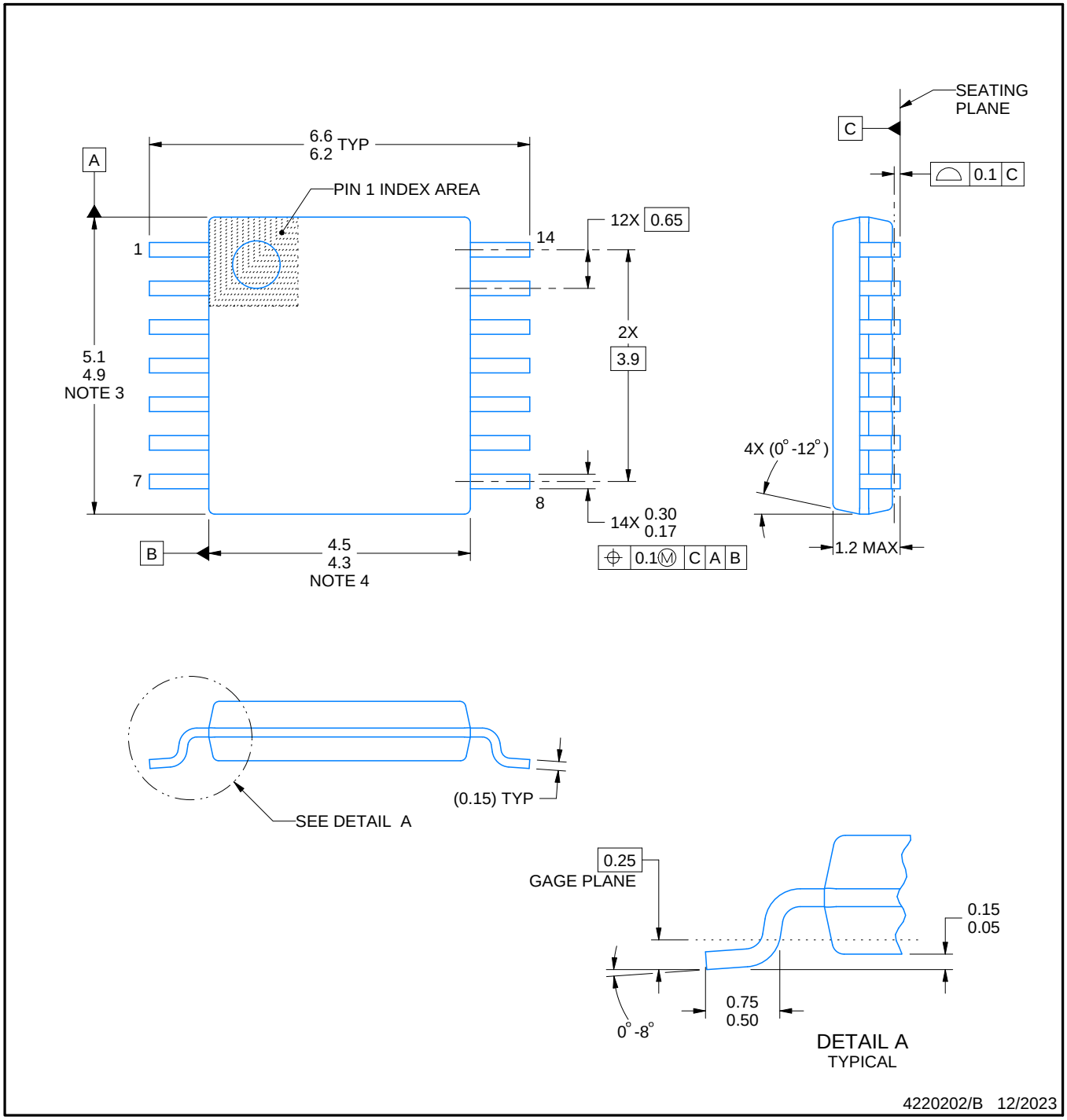
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

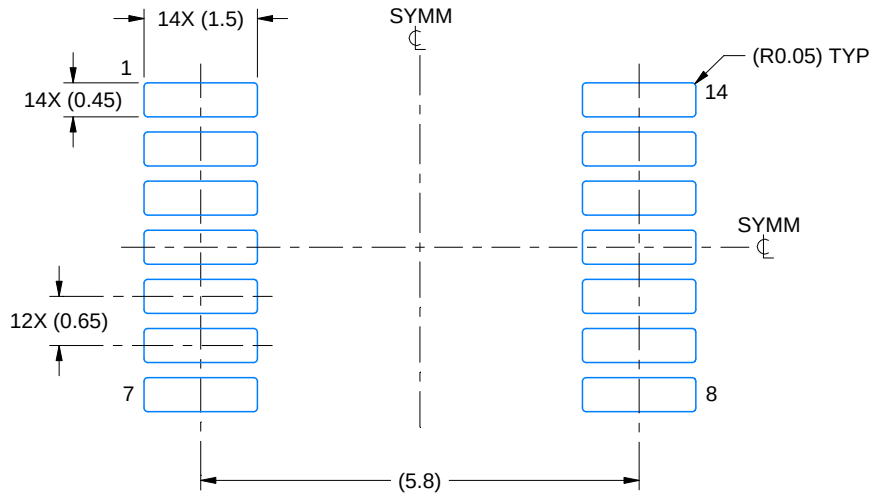
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

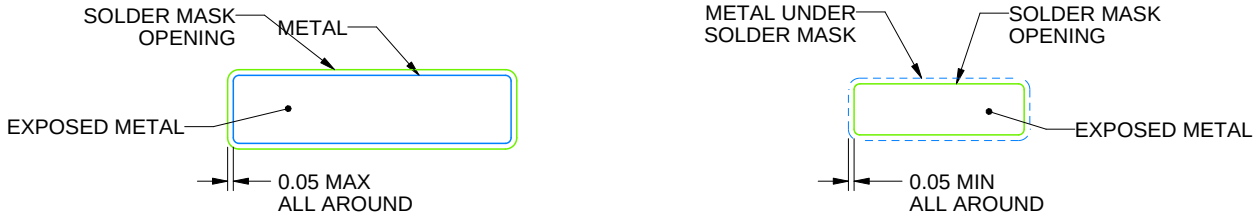


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

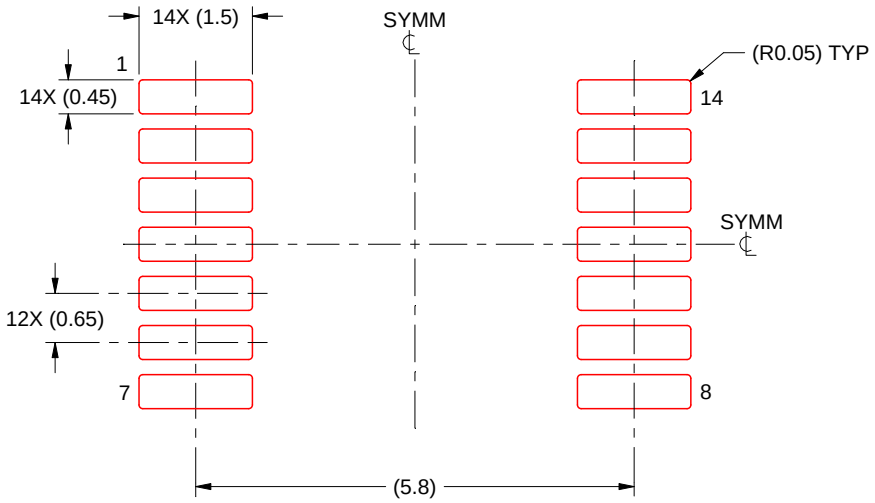


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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