1. General description

The 74HC03; 74HCT03 is a quad 2-input NAND gate with open-drain outputs. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of $V_{\rm CC}$.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- · CMOS low power dissipation
- · High noise immunity
- · Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- · Input levels:
 - For 74HC03: CMOS level
 - For 74HCT03: TTL level
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

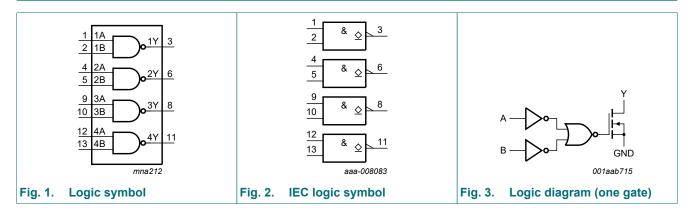
3. Ordering information

Table 1. Ordering information

Type number	Package					
	Temperature range	Name	Description	Version		
74HC03D 74HCT03D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1		
74HC03PW 74HCT03PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1		

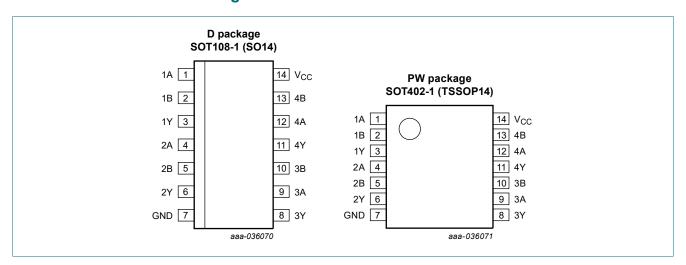


4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ Z = high-impedance \ OFF-state.$

Input	Output	
nA	nB	nY
L	L	Z
L	Н	Z
Н	L	Z
Н	Н	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7	V
Vo	output voltage		[1]	-0.5	+7	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V	[1]	-	-20	mA
Io	output current	-0.5 V < V _O		-	-25	mA
I _{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation		[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC03			74HCT03			Unit
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

^[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C. For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Тур	Max	Min	Max	Min	Max	1	
74HC03						ı	ı	ı			
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V	
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	٧	
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	٧	
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	٧	
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V	
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V	
V _{OL}	LOW-level	V _I = V _{IH} or V _{IL}									
	output voltage	$I_{O} = 20 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V	
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	٧	
		$I_O = 20 \mu A; V_{CC} = 6.0 V$	-	0	0.1	-	0.1	-	0.1	٧	
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	٧	
		I_{O} = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	٧	
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	0.1	-	-	±1	-	±1	μA	
l _{OZ}	OFF-state output current	$V_I = V_{IL}$; $V_{CC} = 6.0 \text{ V}$; $V_O = V_{CC} \text{ or GND}$	-	-	±0.5	-	±5.0	-	±10	μΑ	
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	2.0	-	-	20	-	40	μΑ	
Cı	input capacitance		-	3.5	-	-	-	-	-	pF	
74HCT0	3			1		I.	ı	ı	1		
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V	
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	8.0	V	
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$									
	output voltage	Ι _Ο = 20 μΑ	-	0	0.1	-	0.1	-	0.1	٧	
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	٧	
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ	
l _{OZ}	OFF-state output current	$V_I = V_{IL}$; $V_{CC} = 5.5 \text{ V}$; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10	μΑ	
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ	
		-	100	360	-	450	-	490	μΑ		
Cı	input capacitance		-	3.5	-	-	-	-	-	pF	

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit, see Fig. 5.

Symbol Parameter		Conditions		25 °C			-40 °C to		Unit
				Min	Тур	Max	Max	Max	
74HC03									
t _{pd}	propagation	nA, nB to nY; see Fig. 4	[1]						
	delay	V _{CC} = 2.0 V		-	28	95	120	145	ns
		V _{CC} = 4.5 V		-	10	19	24	29	ns
		V _{CC} = 5.0 V; C _L = 15 pF		-	8	-	-	-	ns
		V _{CC} = 6.0 V		-	8	16	20	25	ns
t _t	transition time	see Fig. 4	[2]						
		V _{CC} = 2.0 V		-	19	75	95	110	ns
		V _{CC} = 4.5 V		-	7	15	19	22	ns
		V _{CC} = 6.0 V		-	6	13	16	19	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC}	[3]	-	4	-	-	-	pF
74HCT0	3							ı	
t _{pd}	propagation	nA, nB to nY; see Fig. 4	[1]						
	delay	V _{CC} = 4.5 V		-	12	24	30	36	ns
		V _{CC} = 5.0 V; C _L = 15 pF		-	10	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Fig. 4</u>	[2]	-	7	15	19	22	ns
C _{PD}	power dissipation capacitance	per package; $V_I = GND$ to $V_{CC} - 1.5 V$		-	4	-	-	-	pF

^[1] t_{pd} is the same as t_{PLZ} and t_{PZL} .

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_0)$$
 where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

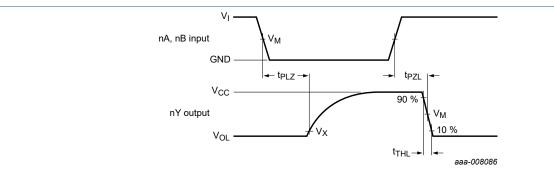
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Product data sheet

10.1. Waveforms and test circuit



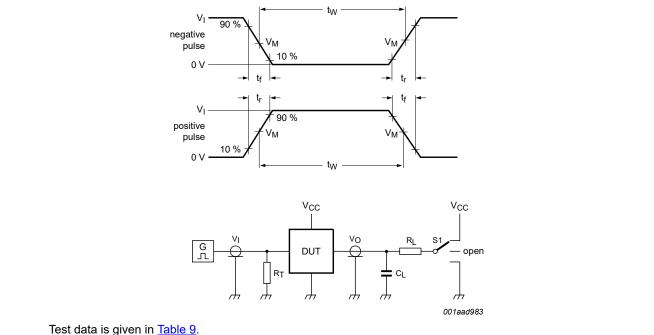
Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Input to output propagation delays Fig. 4.

Table 8. Measurement points

Туре	Input	Output		
	V _M	V _M	V _X	
74HC03	0.5 × V _{CC}	0.5 × V _{CC}	0.1 × V _{CC}	
74HCT03	1.3 V	1.3 V	0.1 × V _{CC}	



Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator;

 C_L = load capacitance including jig and probe capacitance.

Fig. 5. Test circuit for measuring switching times

Table 9. Test data

Туре	Input		Load	S1 position		
	V _I	t _r , t _f	CL	R_L	t _{PZL} , t _{PLZ}	
74HC03	V _{CC}	6 ns	15 pF, 50 pF	1 kΩ	V _{CC}	
74HCT03	3.0 V	6 ns	15 pF, 50 pF	1 kΩ	V _{CC}	

74HC_HCT03

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11. Package outline

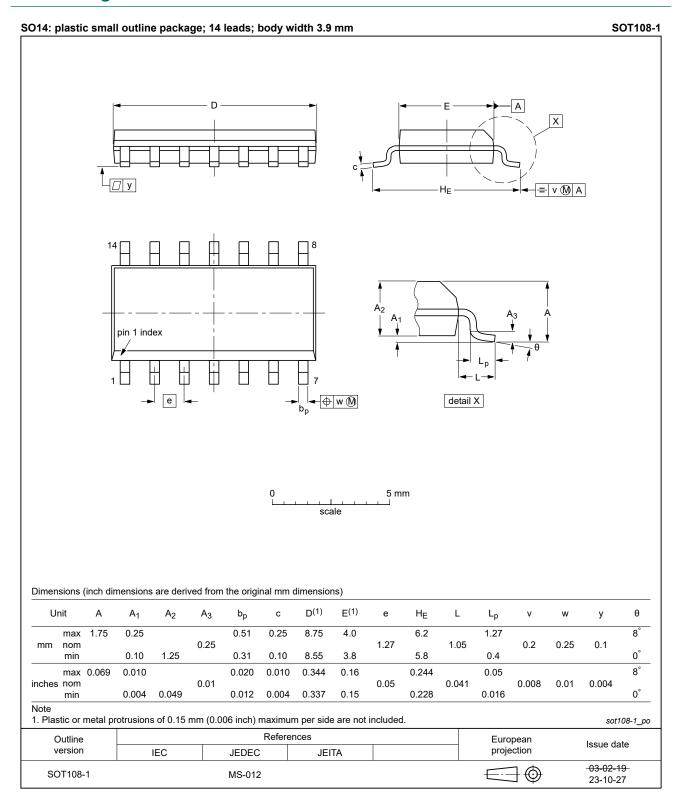


Fig. 6. Package outline SOT108-1 (SO14)

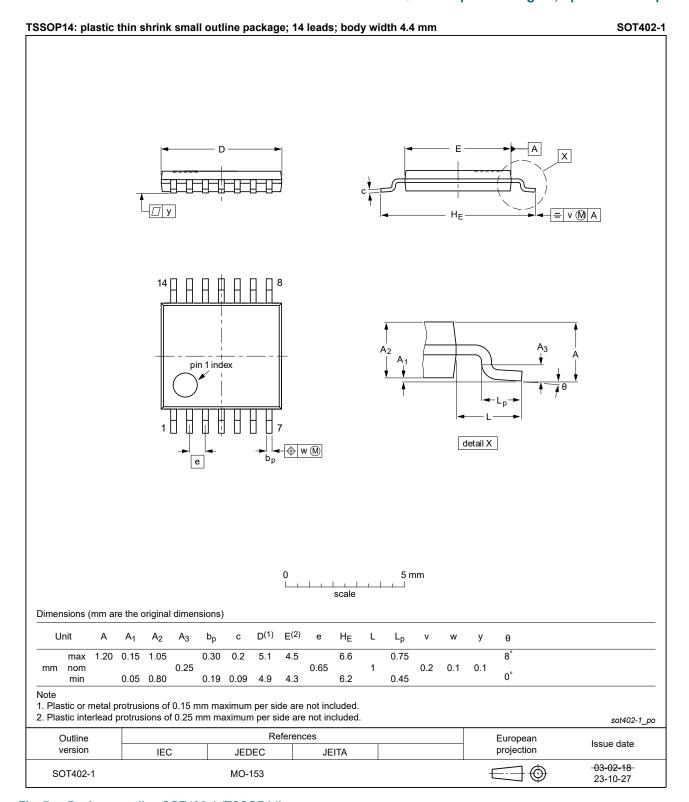


Fig. 7. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description	
CDM	Charged Device Model	
CMOS	nplementary Metal-Oxide Semiconductor	
DUT	Device Under Test	
ESD	ElectroStatic Discharge	
HBM	Human Body Model	
TTL	Transistor-Transistor Logic	

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74HC_HCT03 v.7	20240216	Product data sheet	-	74HC_HCT03 v.6		
Modifications:	 Section 2: ESD specification updated according to the latest JEDEC standard. Fig. 6, Fig. 7: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153 					
74HC_HCT03 v.6	20210810	Product data sheet	-	74HC_HCT03 v.5		
Modifications:	Section 2 up Type number	odated. er 74HC03DB (SOT337-1/9	SSOP14) removed	d.		
74HC_HCT03 v.5	20210107	Product data sheet	-	74HC_HCT03 v.4		
Modifications:	guidelines o Legal texts I Type number	of this data sheet has been if Nexperia. have been adapted to the r er 74HCT03DB (SOT337-1 Derating values for P _{tot} total	new company nan / SSOP14) remo	ne where appropriate. ved.		
74HC_HCT03 v.4	20151127	Product data sheet	-	74HC_HCT03 v.3		
Modifications:	Type number	ers 74HC03N and 74HCT0	3N (SOT27-1) rer	moved.		
74HC_HCT03 v.3	20130627	Product data sheet	-	74HC_HCT03_CNV v.2		
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 					
74HC_HCT03_CNV v.2	19970827	Product specification	-	-		

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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