# Octal Bus Buffer/Line Driver
# MC74VHC245, MC74VHCT245A

The MC74VHC245/MC74VHCT245A is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology.

It is intended for two−way asynchronous communication between data buses. The direction of data transmission is determined by the level of the DIR input. The output enable pin (OE) can be used to disable the device, so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

The MC74VHC245 inputs are compatible with standard CMOS levels while the MC74VHCT245A inputs are compatible with TTL levels. The MC74VHCT245A device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The MC74VHC245 and MC74VHCT245A inputs tolerate voltages up to 5.5 V, allowing the interface of 5 V systems to 3 V systems.

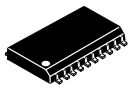
The MC74VHCT245A output structures provide protection when VCC = 0 V. These output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

### Features

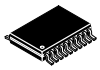
- High Speed: $t_{PD}$ = 4.0 ns (Typ) at $V_{CC}$ = 5.0 V (VHC)
  $t_{PD}$ = 4.9 ns (Typ) at $V_{CC}$ = 5.0 V (VHCT)
- Low Power Dissipation: $I_{CC}$ = 4.0 μA (Max) at $T_A$ = 25°C
- High Noise Immunity: VNIH = VNIL = 28%
- Power Down Protection Provided
- Balanced Propagation Delays
- Designed for: 2.0 V to 5.5 V (VHC)
  4.5 V to 5.5 V (VHCT)
- Low Noise: $V_{OLP}$ = 1.2 V (Max) (VHC)
  $V_{OLP}$ = 1.6 V (Max) (VHCT)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model > 2000 V;
- Chip Complexity: 308 FETs
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

### Application Notes

- Do not force a signal on an I/O pin when it is an active output, damage may occur.
- All floating (high impedance) input or I/O pins must be fixed by means of pull up or pull down resistors or bus terminator ICs.
- A parasitic diode is formed between the bus and $V_{CC}$ terminals. Therefore, the VHC245 cannot be used to interface 5 V to 3 V systems directly.

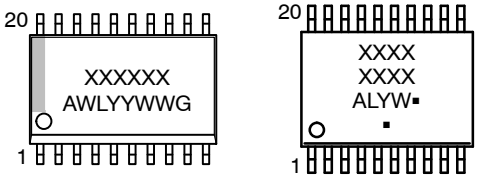


**SOIC−20**
**DW SUFFIX**
**CASE 751D**



**TSSOP−20**
**DT SUFFIX**
**CASE 948E**

### MARKING DIAGRAMS

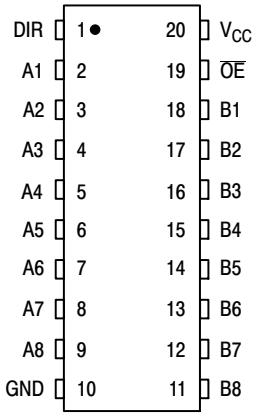



**SOIC−20** **TSSOP−20**

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

### PIN ASSIGNMENT




### ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

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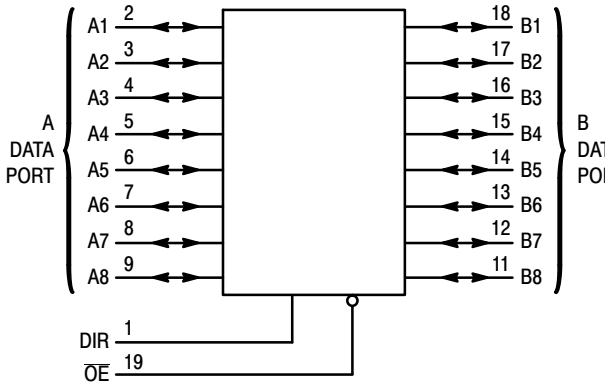



**Figure 1. Logic Diagram**

## FUNCTION TABLE

| Control Inputs | | |
|---|---|---|
| **OE** | **DIR** | **Operation** |
| L | L | Data Transmitted from Bus B to Bus A |
| L | H | Data Transmitted from Bus A to Bus B |
| H | X | Buses Isolated (High−Impedance State) |

## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +6.5 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to +6.5 | V |
| $V_{OUT}$ | DC Output Voltage (MC74VHC) | | −0.5 to $V_{CC}$+0.5 | V |
| | DC Output Voltage (MC74VHCT) | Active Mode (High or Low State)<br>Tristate Mode (Note 1)<br>Power−Off Mode ($V_{CC}$ = 0 V) | −0.5 to $V_{CC}$+0.5<br>−0.5 to +6.5<br>−0.5 to +6.5 | |
| $I_{IN}$ | DC Input Current, per Pin | | ±20 | mA |
| $I_{OUT}$ | DC Output Current, Per Pin | | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | | ±75 | mA |
| $I_{IK}$ | Input Clamp Current | | −20 | mA |
| $I_{OK}$ | Output Clamp Current | MC74VHC<br>MC74VHCT | ±20<br>−20 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 secs | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 2) | SOIC−20W<br>TSSOP−20 | 96<br>150 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 25°C | SOIC−20W<br>TSSOP−20 | 1302<br>833 | mW |
| MSL | Moisture Sensitivity | SOIC−20W<br>All Other Packages | Level 3<br>Level 1 | − |
| $F_R$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.245 in | − |
| $V_{ESD}$ | ESD Withstand Voltage (Note 3) | Human Body Model<br>Charged Device Model | 2000<br>N/A | V |
| $I_{LATCHUP}$ | Latchup Performance (Note 4) | | ±100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.



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## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| **MC74VHC** | | | | | |
| $V_{CC}$ | DC Supply Voltage | | 2.0 | 5.5 | V |
| $V_{IN}$ | DC Input Voltage (Note 5) | | 0 | 5.5 | V |
| $V_{OUT}$ | DC Output Voltage (Note 5) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature | | −40 | +85 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Rate | $V_{CC}$ = 3.0 V to 3.6 V<br>$V_{CC}$ = 4.5 V to 5.5 V | 0<br>0 | 100<br>20 | ns/V |
| **MC74VHCT** | | | | | |
| $V_{CC}$ | DC Supply Voltage | | 4.5 | 5.5 | V |
| $V_{IN}$ | DC Input Voltage (Note 5) | | 0 | 5.5 | V |
| $V_{OUT}$ | DC Output Voltage (Note 5) | Active Mode (High or Low State)<br>Tristate Mode<br>Power−Off Mode ($V_{CC}$ = 0 V) | 0<br>0<br>0 | $V_{CC}$<br>5.5<br>5.5 | V |
| $T_A$ | Operating Temperature | | −40 | +85 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Rate | $V_{CC}$ = 4.5 V to 5.5 V | 0 | 20 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (MC74VHC245)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | $T_A$ = 25°C | | | $T_A$ = − 40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | Minimum High−Level Input Voltage | | 2.0<br>3.0 to 5.5 | 1.50<br>$V_{CC}$ x 0.7 | | | 1.50<br>$V_{CC}$ x 0.7 | | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | | 2.0<br>3.0 to 5.5 | | | 0.50<br>$V_{CC}$ x 0.3 | | 0.50<br>$V_{CC}$ x 0.3 | V |
| $V_{OH}$ | Minimum High−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = −50 μA | 2.0<br>3.0<br>4.5 | 1.9<br>2.9<br>4.4 | 2.0<br>3.0<br>4.5 | | 1.9<br>2.9<br>4.4 | | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = − 4 mA<br>$I_{OH}$ = − 8 mA | 3.0<br>4.5 | 2.58<br>3.94 | | | 2.48<br>3.80 | | |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 50 μA | 2.0<br>3.0<br>4.5 | | 0.0<br>0.0<br>0.0 | 0.1<br>0.1<br>0.1 | | 0.1<br>0.1<br>0.1 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 8 mA | 3.0<br>4.5 | | | 0.36<br>0.36 | | 0.44<br>0.44 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = 5.5 V or GND (DIR, $\overline{OE}$) | 0 to 5.5 | | | ±0.1 | | ±1.0 | μA |
| $I_{OZ}$ | Maximum Three−State Leakage Current | $V_{in}$ = $V_{IL}$ or $V_{IH}$<br>$V_{out}$ = $V_{CC}$ or GND | 5.5 | | | ±0.25 | | ±2.5 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{in}$ = $V_{CC}$ or GND | 5.5 | | | 4.0 | | 40.0 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



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## AC ELECTRICAL CHARACTERISTICS (MC74VHC245)

| Symbol | Parameter | Test Conditions | $T_A$ = 25°C | | | $T_A$ = − 40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, A to B or B to A | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15 pF | | 5.8 | 8.4 | 1.0 | 10.0 | ns |
| | | $C_L$ = 50 pF | | 8.3 | 11.9 | 1.0 | 13.5 | |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 15 pF | | 4.0 | 5.5 | 1.0 | 6.5 | |
| | | $C_L$ = 50 pF | | 5.5 | 7.5 | 1.0 | 8.5 | |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time $\overline{OE}$ to A or B | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15 pF | | 8.5 | 13.2 | 1.0 | 15.5 | ns |
| | | $C_L$ = 50 pF | | 11.0 | 16.7 | 1.0 | 19.0 | |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 15 pF | | 5.8 | 8.5 | 1.0 | 10.0 | |
| | | $C_L$ = 50 pF | | 7.3 | 10.6 | 1.0 | 12.0 | |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time $\overline{OE}$ to A or B | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 50 pF | | 11.5 | 15.8 | 1.0 | 18.0 | ns |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 50 pF | | 7.0 | 9.7 | 1.0 | 11.0 | |
| $t_{OSLH}$, $t_{OSHL}$ | Output to Output Skew | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 50 pF (Note 6) | | | 1.5 | | 1.5 | ns |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 50 pF (Note 6) | | | 1.0 | | 1.0 | ns |
| $C_{in}$ | Maximum Input Capacitance DIR, $\overline{OE}$ | | | 4 | 10 | | 10 | pF |
| $C_{I/O}$ | Maximum Three−State I/O Capacitance | | | 8 | | | | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Note 7) | 21 | pF |

6. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
7. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC} / 8$ (per bit). $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

## NOISE CHARACTERISTICS (MC74VHC245)

| Symbol | Parameter | $T_A$ = 25°C | | Unit |
|---|---|---|---|---|
| | | Typ | Max | |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 0.9 | 1.2 | V |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | −0.9 | −1.2 | V |
| $V_{IHD}$ | Minimum High Level Dynamic Input Voltage | | 3.5 | V |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | | 1.5 | V |



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**DC ELECTRICAL CHARACTERISTICS** (MC74VHCT245A)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | $T_A$ = 25°C | | | $T_A$ = − 40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | Minimum High−Level Input Voltage | | 4.5 to 5.5 | 2.0 | | | 2.0 | | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | | 4.5 to 5.5 | | | 0.8 | | 0.8 | V |
| $V_{OH}$ | Minimum High−Level Output Voltage $V_{in}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = − 50 μA | 4.5 | 4.4 | 4.5 | | 4.4 | | V |
| | | $I_{OH}$ = − 8 mA | 4.5 | 3.94 | | | 3.80 | | |
| $V_{OL}$ | Maximum Low−Level Output Voltage $V_{in}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 4.5 | | 0.0 | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 8 mA | 4.5 | | | 0.36 | | 0.44 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = 5.5 V or GND | 0 to 5.5 | | | ± 0.1 | | ± 1.0 | μA |
| $I_{OZ}$ | Maximum 3−State Leakage Current | $V_{in}$ = $V_{IL}$ or $V_{IH}$<br>$V_{out}$ = $V_{CC}$ or GND | 5.5 | | | ± 0.25 | | ± 2.5 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{in}$ = $V_{CC}$ or GND | 5.5 | | | 4.0 | | 40.0 | μA |
| $I_{CCT}$ | Quiescent Supply Current | Per Input: $V_{IN}$ = 3.4 V<br>Other Input: $V_{CC}$ or GND | 5.5 | | | 1.35 | | 1.50 | mA |
| $I_{OPD}$ | Output Leakage Current | $V_{OUT}$ = 5.5 V | 0 | | | 0.5 | | 5.0 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



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## AC ELECTRICAL CHARACTERISTICS (MC74VHCT245A)

| Symbol | Parameter | Test Conditions | | $T_A$ = 25°C Min | $T_A$ = 25°C Typ | $T_A$ = 25°C Max | $T_A$ = – 40 to 85°C Min | $T_A$ = – 40 to 85°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay A to B or B to A | $V_{CC}$ = 5.0 ± 0.5 V | $C_L$ = 15 pF<br>$C_L$ = 50 pF | | 4.9<br>5.4 | 7.7<br>8.7 | 1.0<br>1.0 | 8.5<br>9.5 | ns |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time $\overline{OE}$ to A or B | $V_{CC}$ = 5.0 ± 0.5 V | $C_L$ = 15 pF<br>$C_L$ = 50 pF | | 9.4<br>9.9 | 13.8<br>14.8 | 1.0<br>1.0 | 15.0<br>16.0 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time $\overline{OE}$ to A or B | $V_{CC}$ = 5.0 ± 0.5 V | $C_L$ = 50 pF | | 10.1 | 15.4 | 1.0 | 16.5 | ns |
| $t_{OSLH}$, $t_{OSHL}$ | Output to Output Skew | $V_{CC}$ = 5.0 ± 0.5 V (Note 8) | $C_L$ = 50 pF | | | 1.0 | | 1.0 | ns |
| $C_{in}$ | Maximum Input Capacitance | | | | 4 | 10 | | 10 | pF |
| $C_{out}$ | Maximum 3–State Output Capacitance (Output in High–Impedance State) | | | | 13 | | | | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Note 9) | 16 | pF |

8. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
9. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). $C_{PD}$ is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

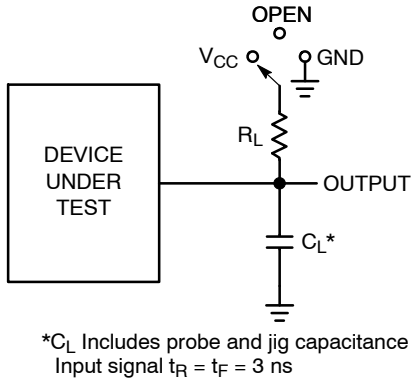
## NOISE CHARACTERISTICS (MC74VHCT245A)

| Symbol | Parameter | $T_A$ = 25°C Typ | $T_A$ = 25°C Max | Unit |
|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 1.2 | 1.6 | V |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | –1.2 | –1.6 | V |
| $V_{IHD}$ | Minimum High Level Dynamic Input Voltage | | 2.0 | V |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | | 0.8 | V |



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*$C_L$ Includes probe and jig capacitance
Input signal $t_R = t_F = 3$ ns

| Test | Switch Position | $C_L$ | $R_L$ |
|---|---|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open | See AC Characteristics Table | 1 kΩ |
| $t_{PLZ}$ / $t_{PZL}$ | $V_{CC}$ | | |
| $t_{PHZ}$ / $t_{PZH}$ | GND | | |

**Figure 2. Test Circuits**

## SWITCHING WAVEFORMS

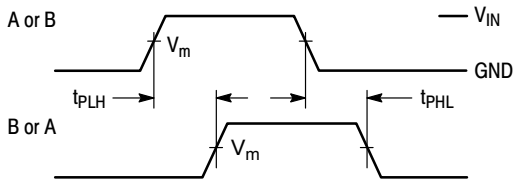



**Figure 3.**

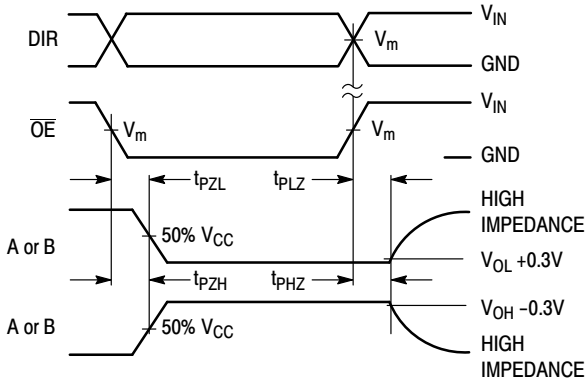



**Figure 4.**

| Device | $V_{IN}$, V | $V_m$, V |
|---|---|---|
| MC74VHC245 | $V_{CC}$ | 50% x $V_{CC}$ |
| MC74VHCT245A | 3 V | 1.5 V |



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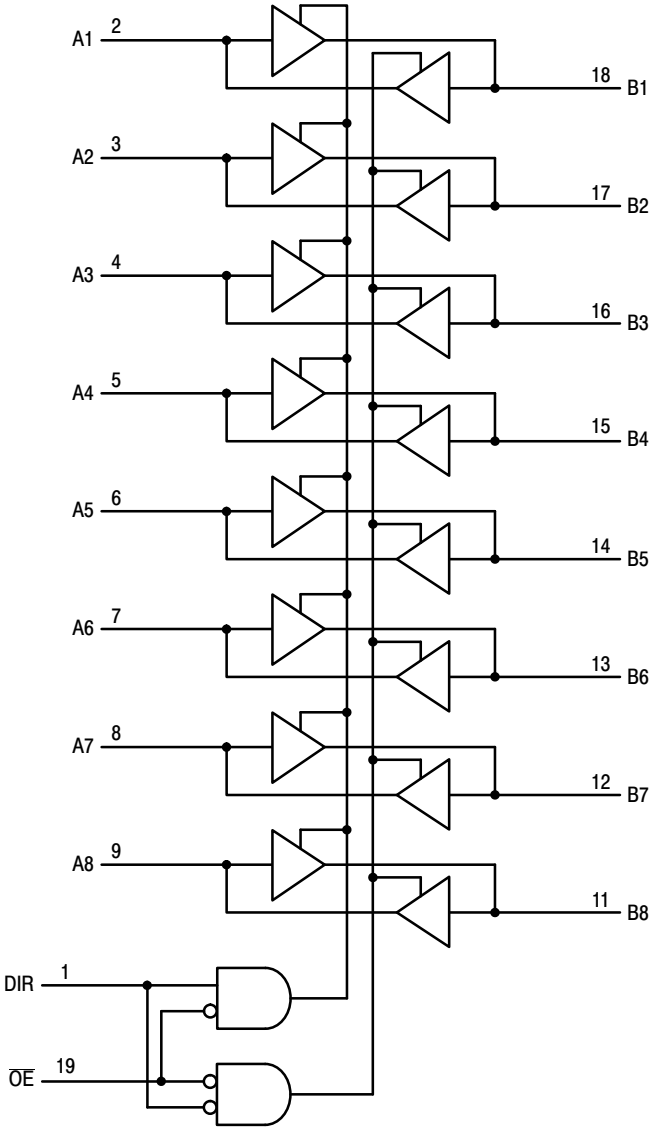



**Figure 5. Expanded Logic Diagram**

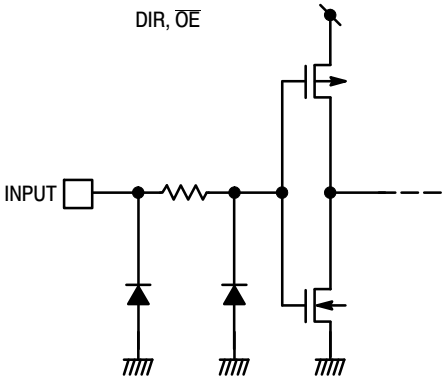



**Figure 6. Input Equivalent Circuit**

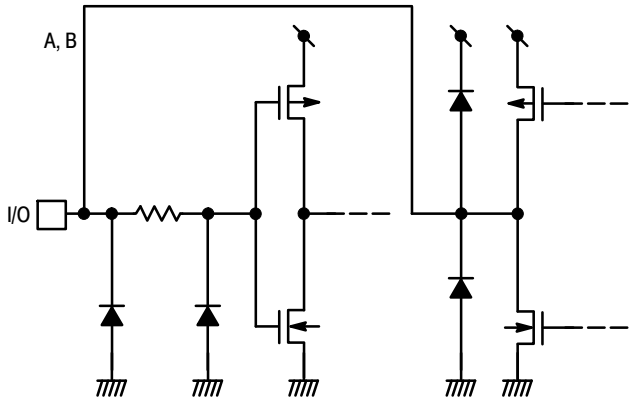



**Figure 7. Bus Terminal Equivalent Circuit**



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## ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| MC74VHC245DWG | VHC245G | SOIC−20 WB | 38 Units / Rail |
| MC74VHC245DWR2G | VHC245G | SOIC−20 WB | 2500 / Tape & Reel |
| MC74VHC245DTG | VHC<br>245 | TSSOP−20 | 75 Units / Rail |
| MC74VHC245DTR2G | VHC<br>245 | TSSOP−20 | 1000 / Tape & Reel |
| MC74VHCT245ADWG | VHCT245AG | SOIC−20 WB | 38 Units / Rail |
| MC74VHCT245ADWR2G | VHCT245AG | SOIC−20 WB | 2500 / Tape & Reel |
| MC74VHCT245ADTG | VHCT<br>245A | TSSOP−20 | 75 Units / Rail |
| MC74VHCT245ADTR2G | VHCT<br>245A | TSSOP−20 | 1000 / Tape & Reel |

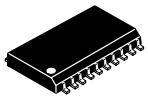
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable



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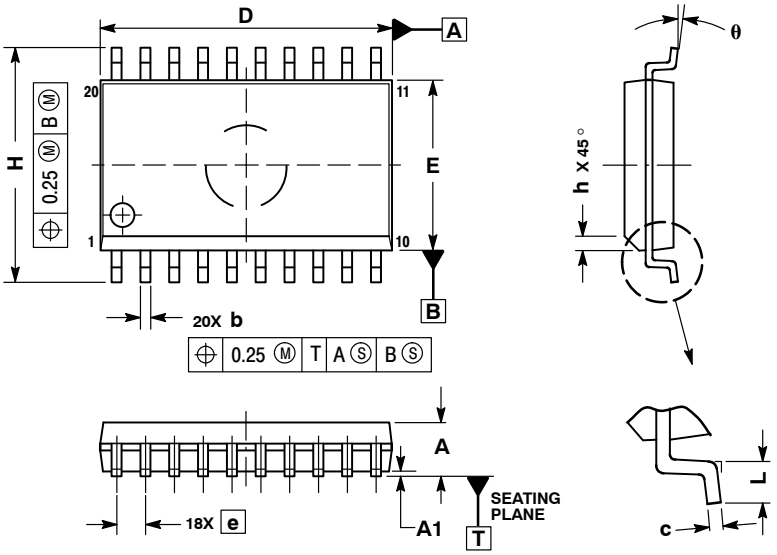
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**SOIC−20 WB**
CASE 751D−05
ISSUE H

DATE 22 APR 2015

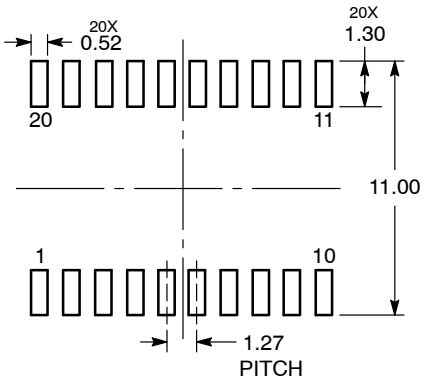
**SCALE 1:1**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

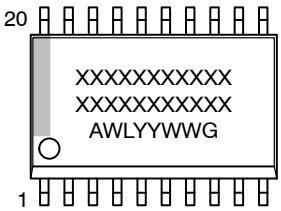
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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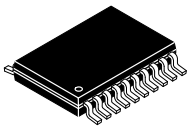
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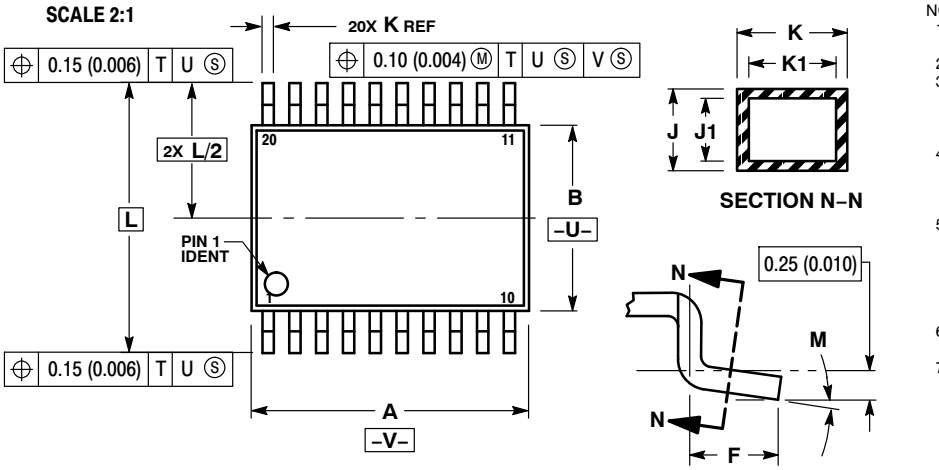
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**TSSOP−20 WB**
CASE 948E
ISSUE D

DATE 17 FEB 2016



SCALE 2:1



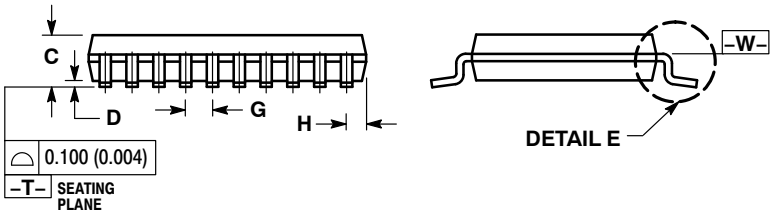




SECTION N−N




DETAIL E



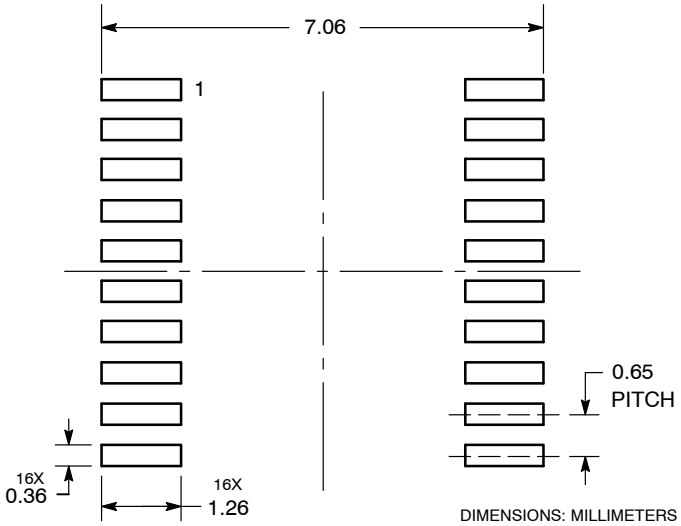




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

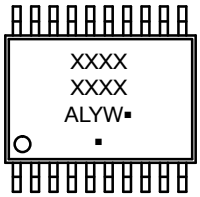
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
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