

POWER MANAGEMENT Features

- V_{IN} Range — 2.75 – 5.5V
- V_{OUT} Selectable — 1.0 - 3.3V
- Up to 2A Output Current for Each Channel
- Package with Ultra-Small Footprint : 3 x 3 x 0.6(mm)
- Switching Frequency — 2.5MHz
- Efficiency Up to 94%
- Low Output Noise in CCM
- Excellent Transient Response
- Start Up into Pre-Biased Output
- 100% Duty-Cycle Low Dropout Operation
- Shutdown Current — $<1\mu A$
- Internal Soft-Start
- Input Under-Voltage Lockout
- Output Over-Voltage, Current Limit Protection
- Over-Temperature Protection
- V_{OUT} Further Adjustable Using External Resistors
- PGOOD Feature
- Lead-free, Halogen-free, and RoHS/WEEE Compliant

Applications

- Wireless Access Point/Router/Modem
- Femtocell
- Set-Top Box
- Point-Of-Sale
- Projector

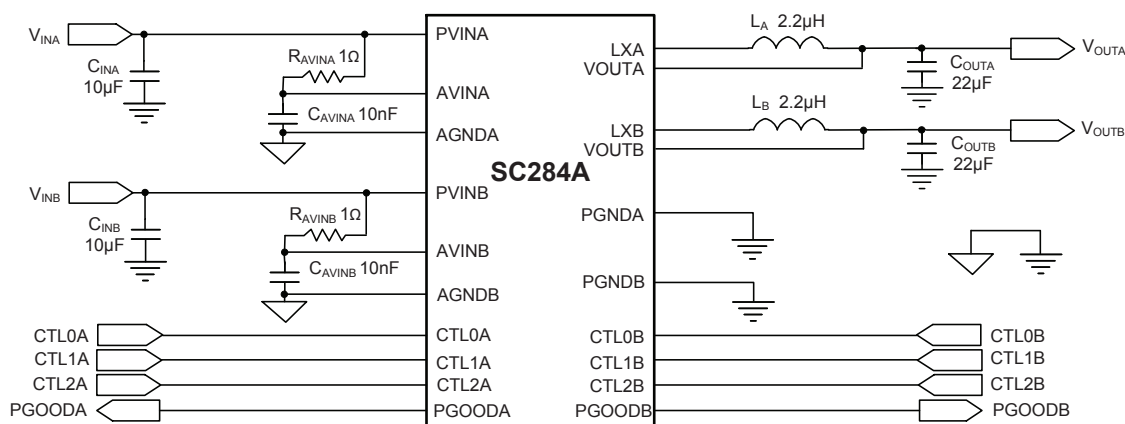
Description

The SC284A is a dual channel 2A synchronous step-down regulator designed to operate with an input voltage range of 2.75 to 5.5 Volts. Each channel offers seven pre-determined output voltages via three control pins programmable from 1.0 to 3.3 Volts. The control pins allow for on-the-fly voltage changes, enabling system designers to implement dynamic power savings. The SC284A is also capable of adjusting the output voltage via an external resistor divider.

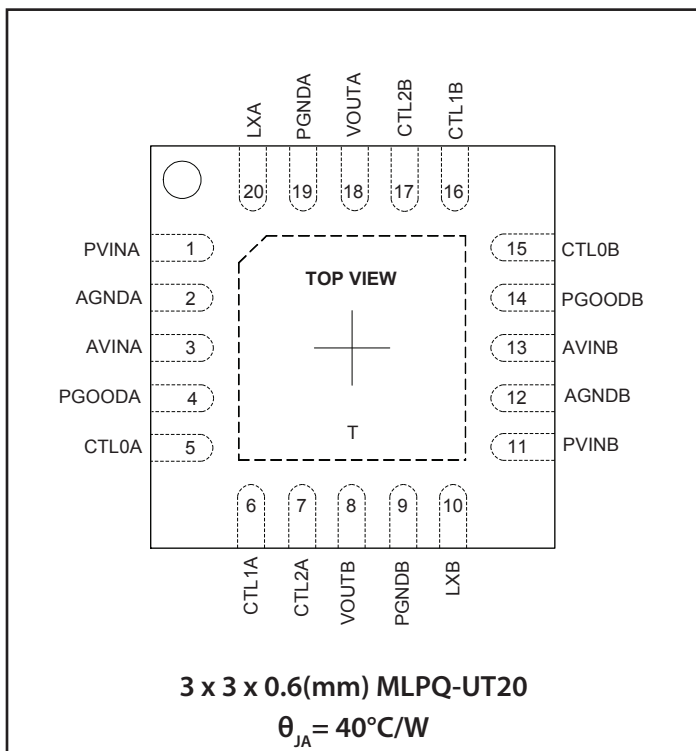
The SC284A is optimized for maximum efficiency. It operates at a fixed 2.5MHz oscillator frequency, allowing the use of small surface mount external components.

Connecting CTL0 — CTL2 to logic low forces the device into shutdown mode reducing the supply current to less than $1\mu A$. Connecting any of the control pins to logic high enables the converter and sets the output voltage according to Table 1. Other features include under-voltage lockout, soft-start to limit inrush current, and over-temperature protection.

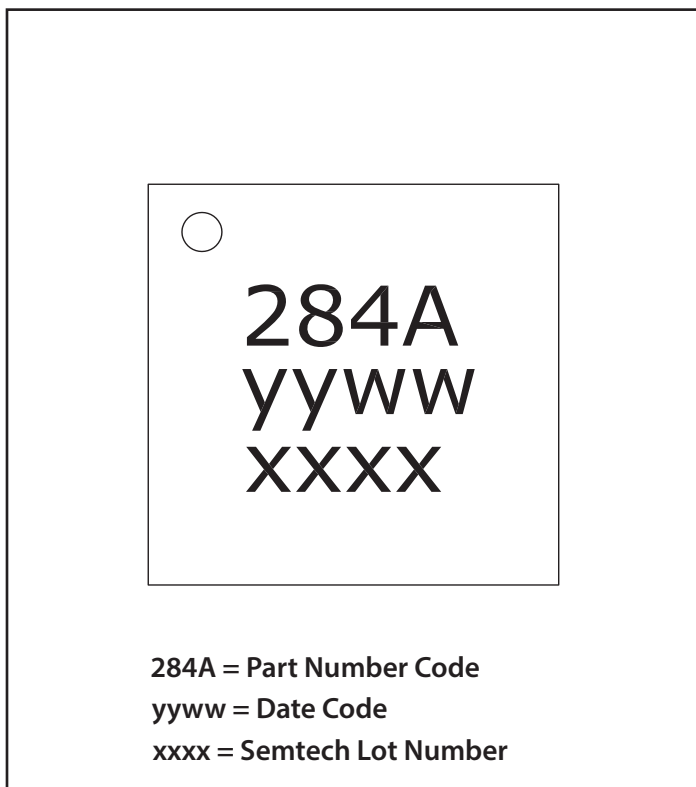
Typical Application Circuit



Pin Configuration



Marking Information



Ordering Information

Device	Package
SC284AULTRC ⁽¹⁾⁽²⁾	3 x 3 x 0.6(mm) MLPQ-UT20
SC284AEVB	Evaluation Board

Notes:

- (1) Available in tape and reel only. A reel contains 3,000 devices.
- (2) Available in lead-free package only. Device is fully WEEE and RoHS compliant and halogen-free.

Table 1 – Output Voltage Settings

CTL2[A/B]	CTL1[A/B]	CTL0[A/B]	Output Voltage
0	0	0	Disabled
0	0	1	1.0V
0	1	0	1.1V
0	1	1	1.2V
1	0	0	1.5V
1	0	1	1.8V
1	1	0	2.5V
1	1	1	3.3V

Absolute Maximum Ratings

AVINA, AVINB, PVINA, PVINB Supply (V) -0.3 to +6.0
 LXA and LXB (V) -1 to $V_{IN} + 1$, -3 (20ns Max), 6 Max
 VOUTA and VOUTB (V) -0.3 to ($V_{IN} + 0.3$)
 CTLXA/B pins (V) -0.3 to ($V_{IN} + 0.3$)
 Peak IR Reflow Temperature (°C) 260
 ESD Protection Level⁽²⁾ (kV) 3kV
 Output Short Circuit to GND. Continuous

Recommended Operating Conditions

V_{INA} and V_{INB} Supply (V) 2.75 to 5.5
 Maximum Output Current Each Channel (A) 2.0

Thermal Information

Thermal Resistance, Junction to Ambient ⁽¹⁾ (°C/W) 40
 Maximum Junction Temperature (°C) +150
 Storage Temperature Range (°C) -65 to +150

Exceeding the absolute maximum ratings may result in permanent damage to the device and/or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Notes:

- (1) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.
- (2) Tested according to JEDEC standard JESD22-A114-B.

Electrical Characteristics

Unless specified: $V_{INA} = V_{INB} = 5.0V$, $V_{OUTA} = V_{OUTB} = 1.5V$, $C_{INA} = C_{INB} = 10\mu F$, $C_{OUTA} = C_{OUTB} = 22\mu F$, $L = 2.2\mu H$, $-40^{\circ}C \leq (T_A = T_J) \leq +125^{\circ}C$. Unless otherwise noted typical values at $T_A = +25^{\circ}C$.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	$V_{INA/B}$		2.75		5.5	V
Under-Voltage Lockout	UVLO	Rising V_{INA} , V_{INB}	2.55	2.65	2.75	V
		Hysteresis		200		mV
Quiescent Current	I_Q	Channel A & B, Excluding I_{OUT} per channel		6		mA
Shutdown Current	I_{SHDN}	$CTL_{0-2} = GND$, Per channel		1	10	μA
Soft-Start Time	t_{SS}	Channel A & B; $I_{OUT} = 2A$, $V_{OUT} = 90\%$ of final value		1700		μs
Output Voltage Range	V_{OUT}		1.0		3.3	V
Output Voltage Tolerance ⁽¹⁾	ΔV_{OUT}	Channel A & B; $I_{OUT} = 400mA$	-2.0		+2.0	%
CTL Settings Regulation	$\Delta V_{CTL-REG}$	Channel A & B; Relative to V_{OUT} at $CTL = 100$, $I_{OUTA} = 400mA$; $I_{OUTB} = 400mA$		± 1		%
Line Regulation	$\Delta V_{LINE-REG}$	Channel A & B; $V_{IN} = 2.75 - 5.5V$		± 0.2		%/V
Load Regulation	$\Delta V_{LOAD-REG}$	Channel A & B; $V_{IN} = 5.0V$; $I_{OUT} = 1mA - 2A$		± 0.3		%/A
Current Limit Threshold	I_{LIMIT}	Channel A & B; Peak LX current	2.25	3.0	3.75	A
Oscillator Frequency	f_{OSC}	Channel A & B	2.0	2.5	3.0	MHz

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LX Leakage Current ⁽²⁾	$I_{L(LX)}$	Channel A & B; $V_{IN} = 5.5V$; $LX = 0V$; $CTL_{0-2} = GND$	-10	-1		μA
		Channel A & B; $V_{IN} = 5.5V$; $LX = 5.0V$; $CTL_{0-2} = GND$		1	10	
Foldback Holding Current	I_{CL_HOLD}	Average LX Current, $V_{OUT} = 1.5V$		600		mA
High Side Switch Resistance ⁽³⁾	$R_{DS(on)_P}$	Channel A & B; $I_{LX} = 100mA$, $T_J = 25^\circ C$		95		m Ω
Low Side Switch Resistance	$R_{DS(on)_N}$	Channel A & B; $I_{LX} = -100mA$, $T_J = 25^\circ C$		65		
CTLx Input Current ⁽²⁾	$I_{CTL_}$	Channel A & B; $CTL_{0-2} = VIN$ or GND	-2.0		2.0	μA
CTLx Input High Threshold	V_{CTLX_HI}	Channel A & B	1.6			V
CTLx Input Low Threshold	V_{CTLX_LO}	Channel A & B			0.4	V
Impedance of PGOOD Low	R_{PGOOD_LO}			8		Ω
PGOOD Threshold	V_{PG_TH}	V_{OUT} rising		90		%
PGOOD Delay	V_{PG_DLY}	Asserted		2		ms
		PGOOD = Low		20		μs
V_{OUT} Over Voltage Protection	V_{OVP}	Channel A & B		115		%
Thermal Shutdown Temperature ⁽⁴⁾	T_{SD}	Channel A & B		160		$^\circ C$
Thermal Shutdown Hysteresis ⁽⁴⁾	T_{SD_HYS}	Channel A & B		10		$^\circ C$

Notes:

(1) The "Output Voltage Tolerance" includes output voltage accuracy, voltage drift over temperature.

(2) A negative current means the current flows from the pin and a positive current means the current flows into the pin.

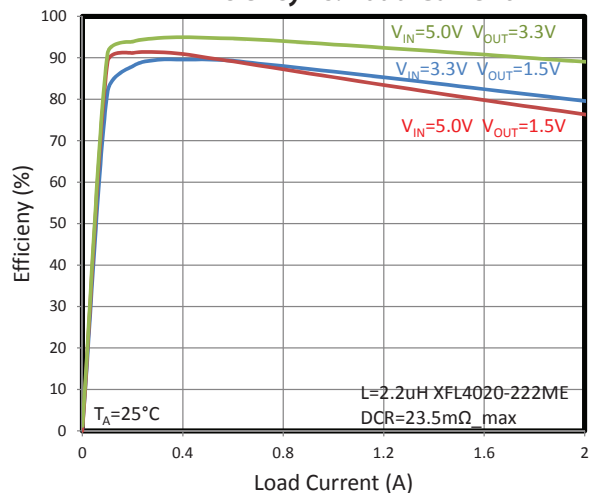
(3) Measured from $VIN_{A/B}$ to $LX_{A/B}$.

(4) Thermal shutdown protection is independent for each channel.

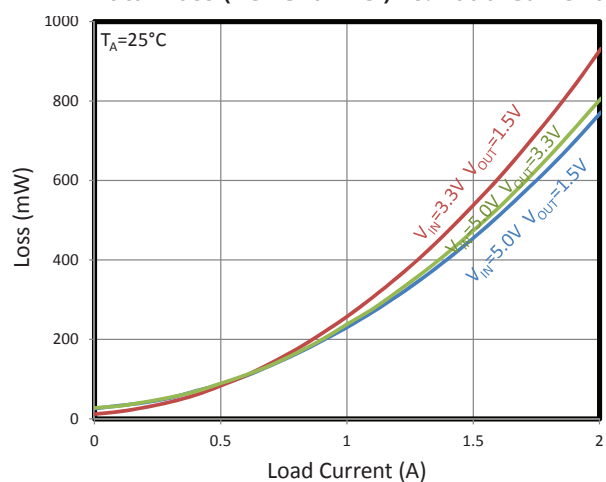
Typical Characteristics

Circuit Conditions: $C_{IN} = 10\mu F/6.3V$; $C_{OUT} = 22\mu F/6.3V$, Unless otherwise noted, $L = 2.2\mu H$ (TOKO: 1127AS-2R2M).

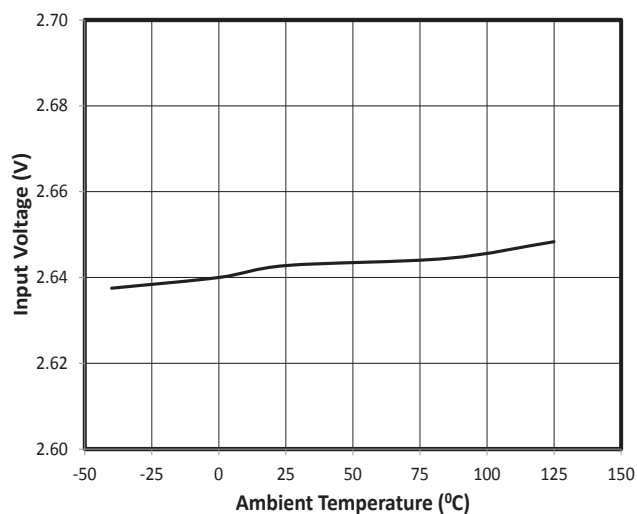
Efficiency vs. Load Current



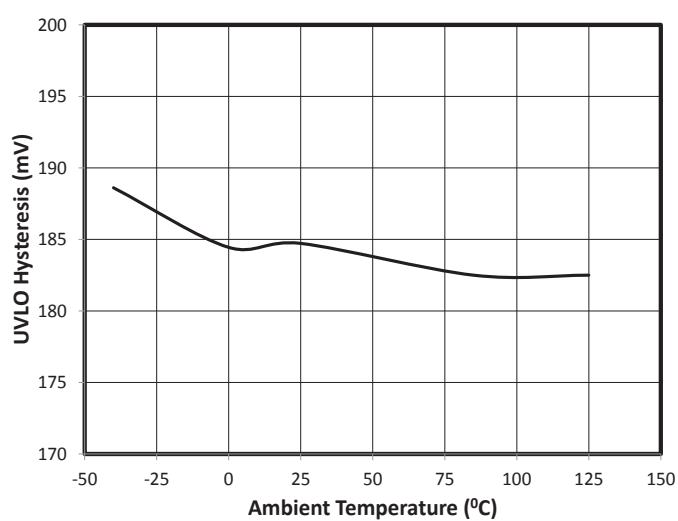
Total Loss (Per Channel) vs. Load Current



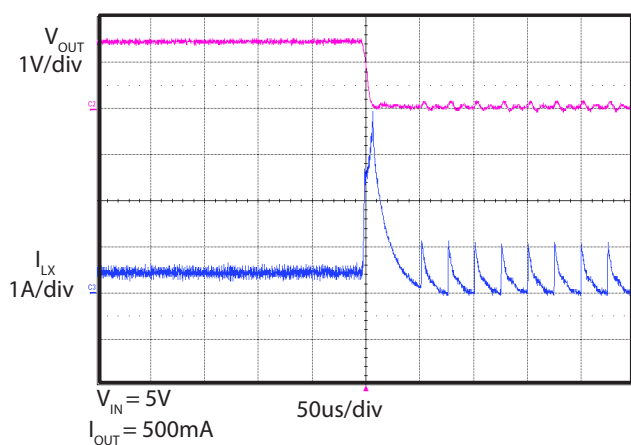
UVLO Rising Threshold



UVLO Hysteresis



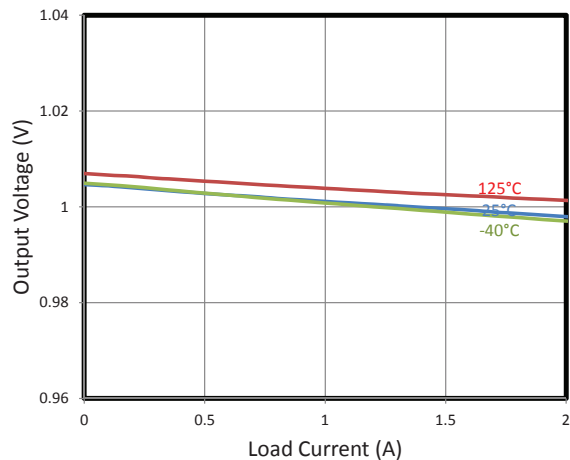
Output Hard Short ($V_{OUT} = 1.5V$)



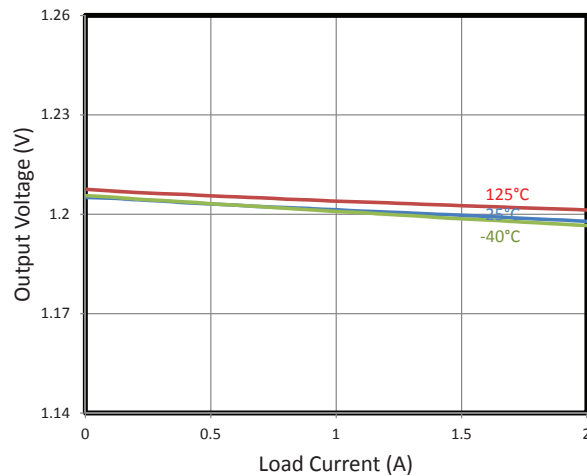
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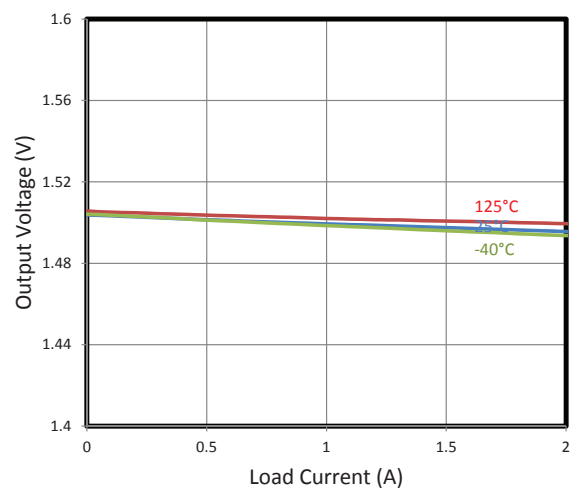
Load Regulation, $V_{out}=1.0V$



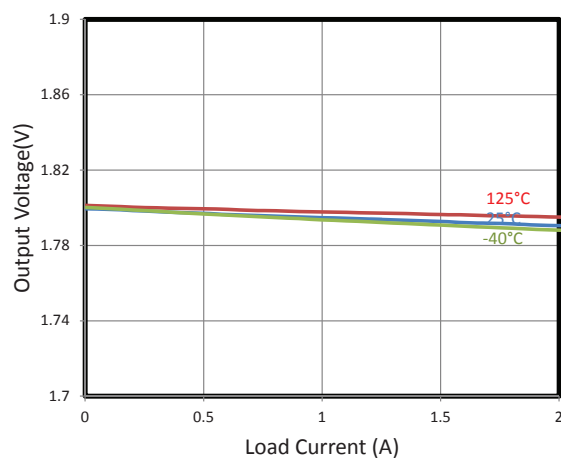
Load Regulation, $V_{out}=1.2V$



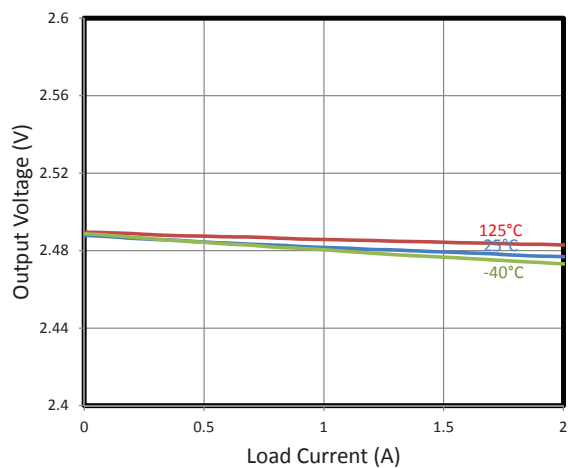
Load Regulation, $V_{out}=1.5V$



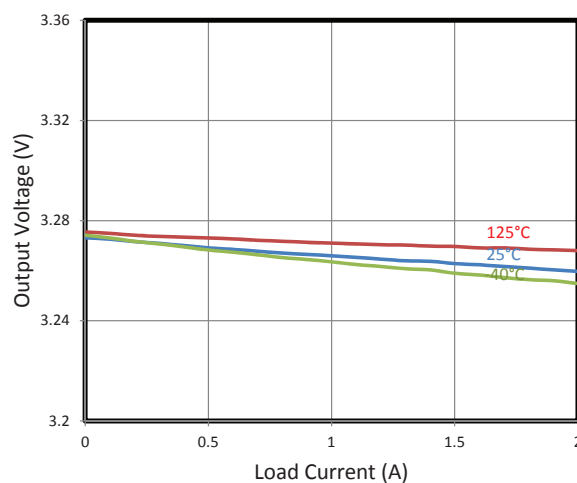
Load Regulation, $V_{out}=1.8V$



Load Regulation, $V_{out}=2.5V$



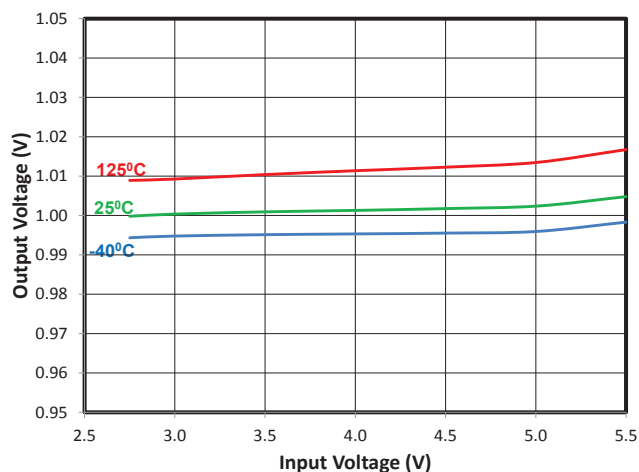
Load Regulation, $V_{out}=3.3V$



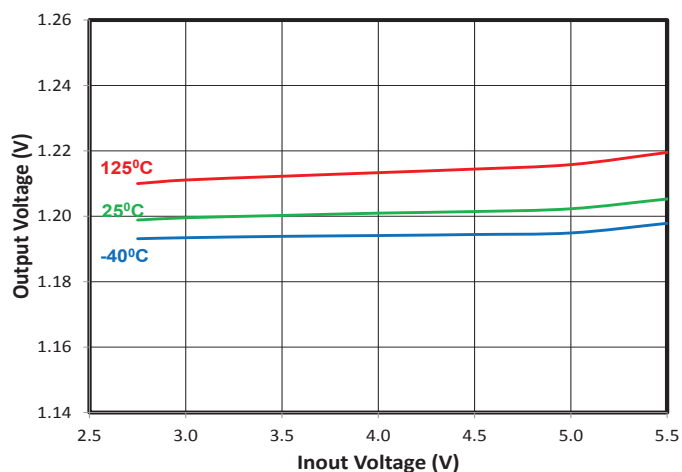
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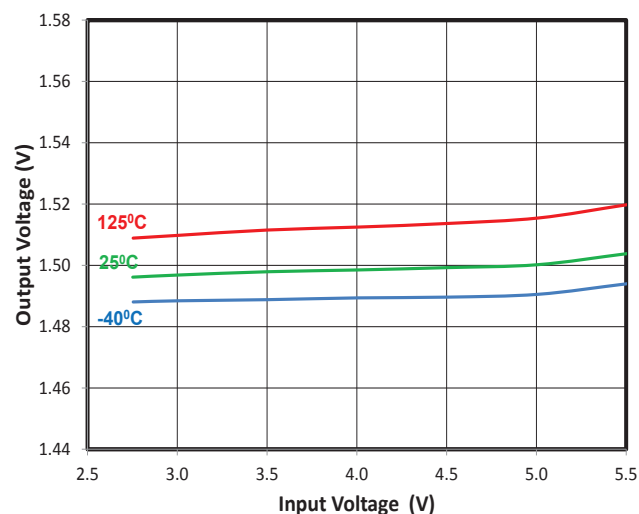
Line Regulation, $V_{out}=1.0V$, $I_{out}=500mA$



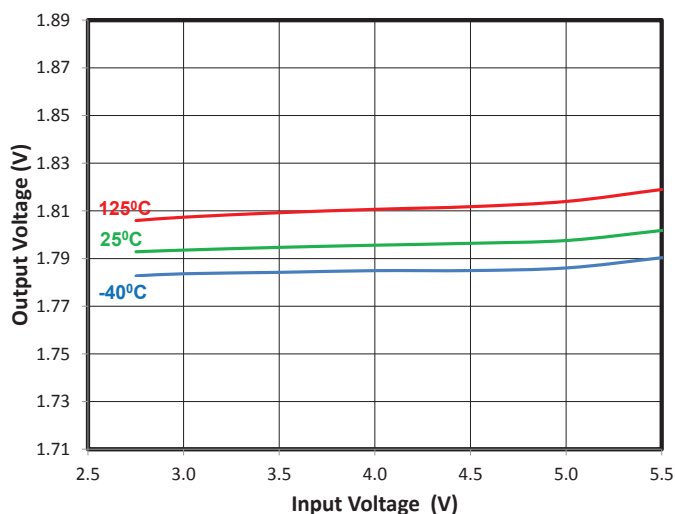
Line Regulation, $V_{out}=1.2V$, $I_{out}=500mA$



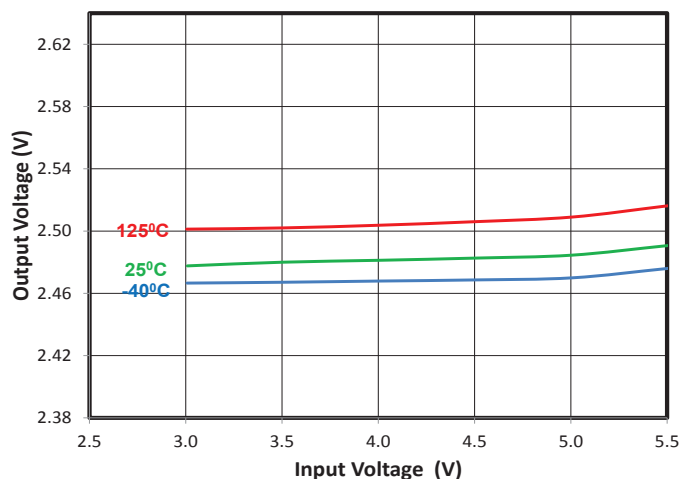
Line Regulation, $V_{out}=1.5V$, $I_{out}=500mA$



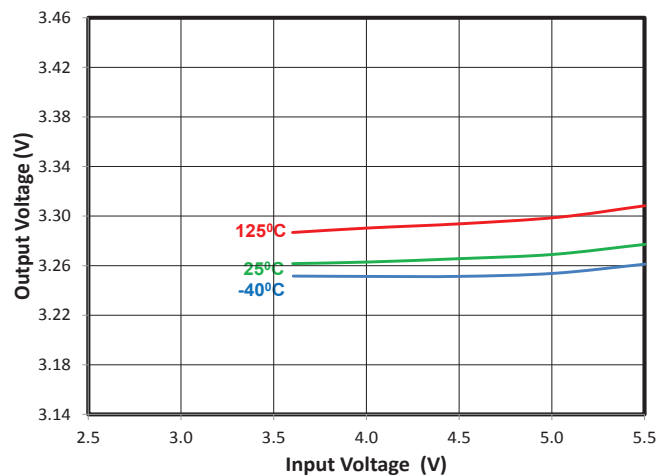
Line Regulation, $V_{out}=1.8V$, $I_{out}=500mA$



Line Regulation, $V_{out}=2.5V$, $I_{out}=500mA$



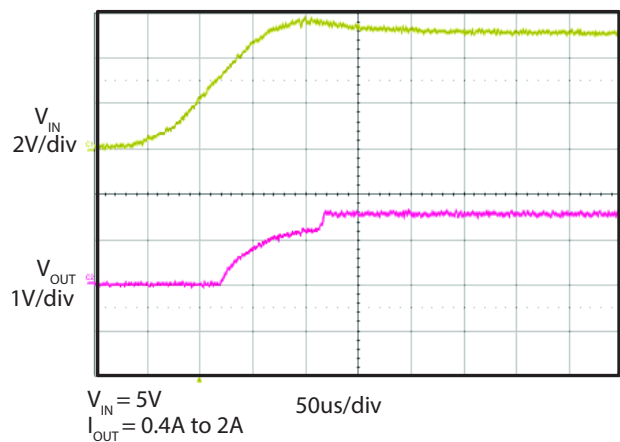
Line Regulation, $V_{out}=3.3V$, $I_{out} = 500mA$



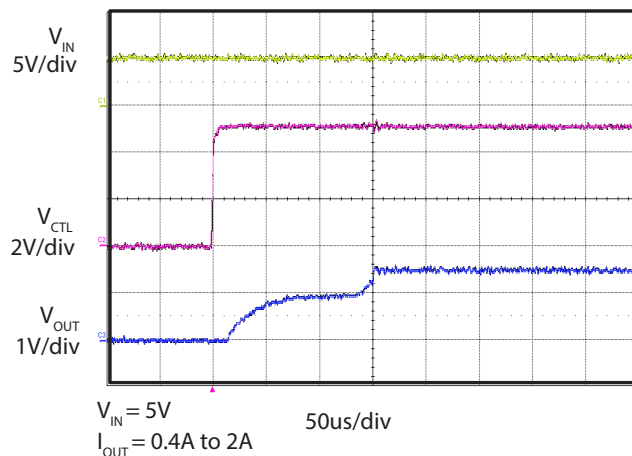
Typical Waveforms

Circuit Conditions: $C_{IN} = 10\mu F/6.3V$; $C_{OUT} = 22\mu F/6.3V$, $L = 2.2\mu H$ (TOKO: 1127AS-2R2M).

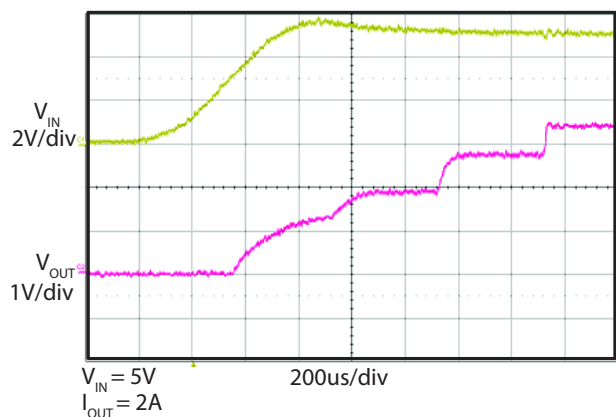
Start Up (Power up $V_{IN}=V_{CTLx}$) ($V_{OUT}=1.5V$)



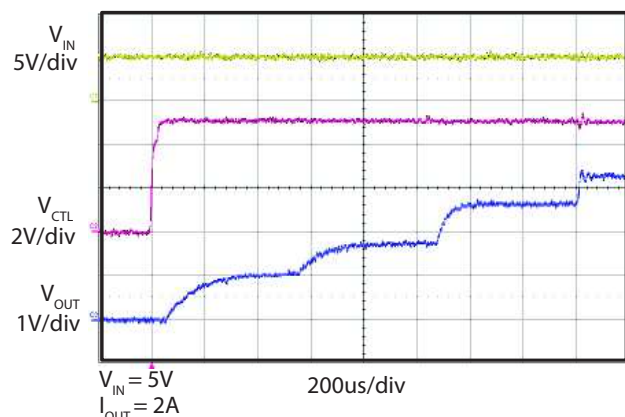
Start Up (Enable) ($V_{OUT}=1.5V$)



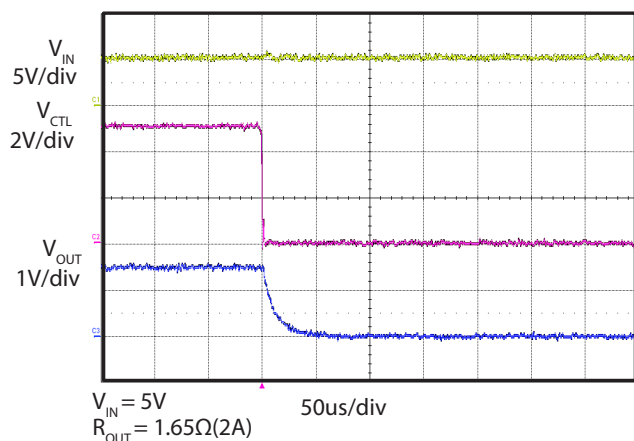
Start Up (Power up $V_{IN}=V_{CTLx}$) ($V_{OUT}=3.3V$)



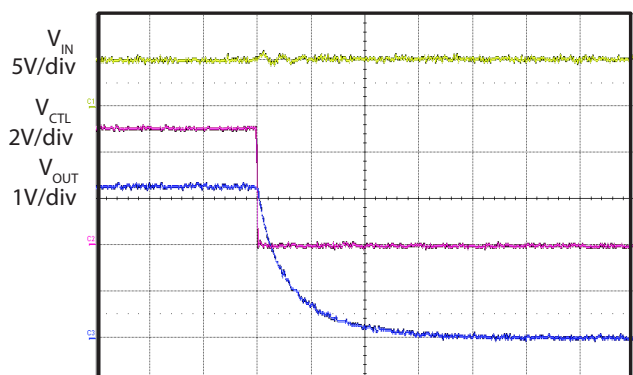
Start Up (Enable) ($V_{OUT}=3.3V$)



Shutdown (Disable) ($V_{OUT}=1.5V$)



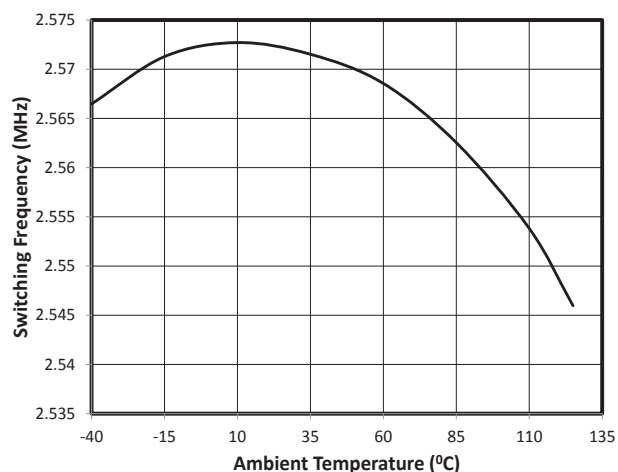
Shutdown (Disable) ($V_{OUT}=3.3V$)



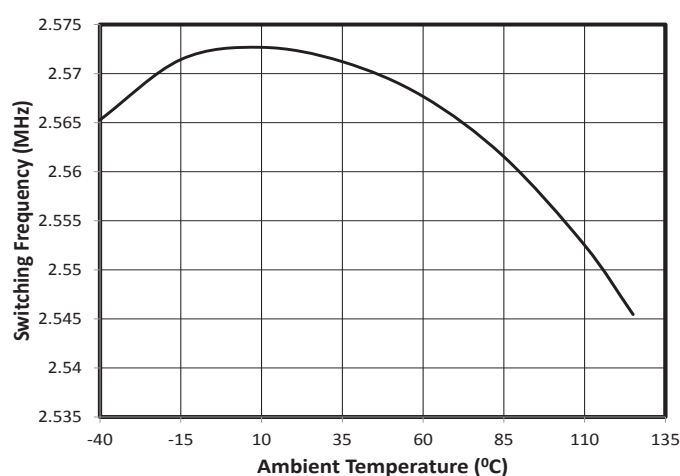
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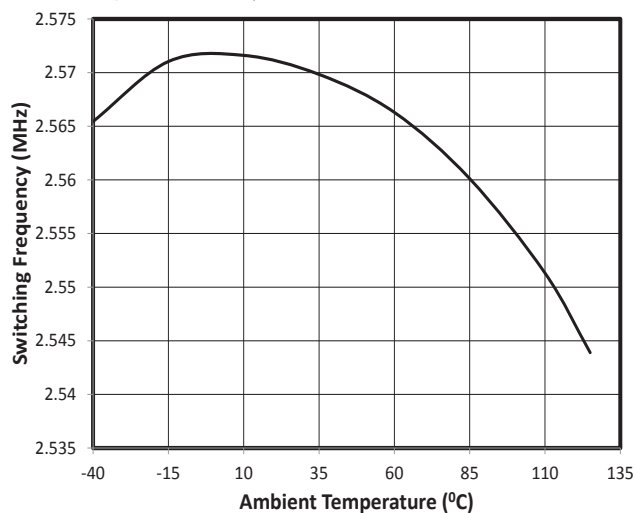
Switching Frequency Vs Temperature, $V_{out}=1.0V$



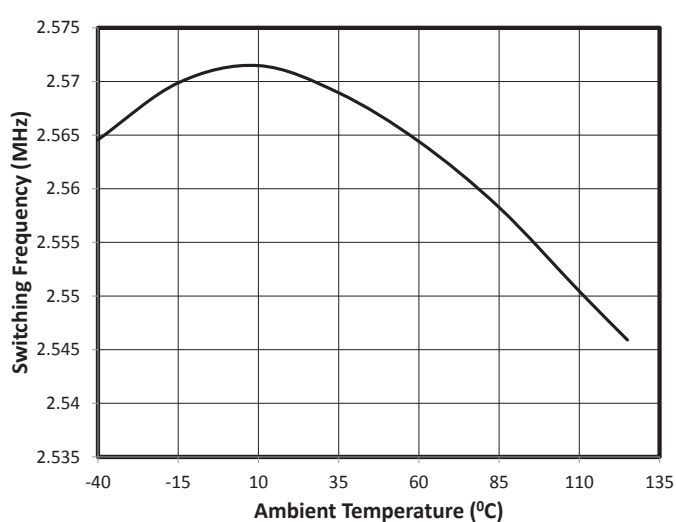
Switching Frequency Vs Temperature, $V_{out}=1.2V$



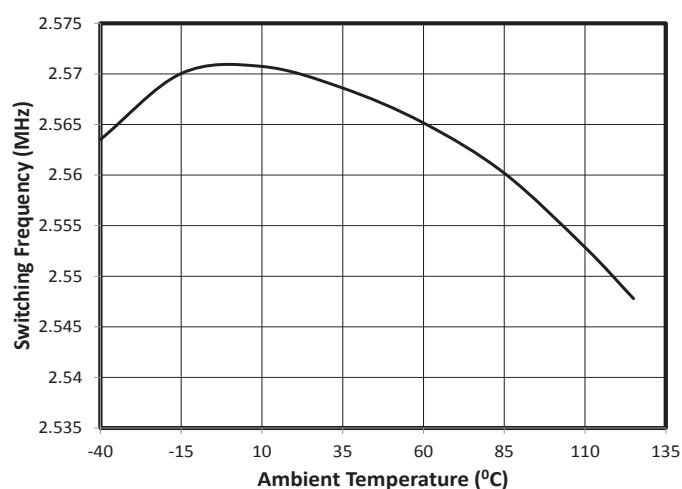
Switching Frequency Vs Temperature, $V_{out}=1.5V$



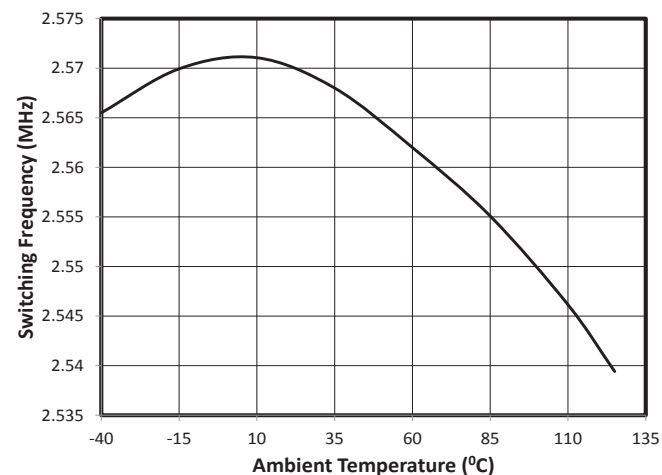
Switching Frequency Vs Temperature, $V_{out}=1.8V$



Switching Frequency Vs Temperature, $V_{out}=2.5V$



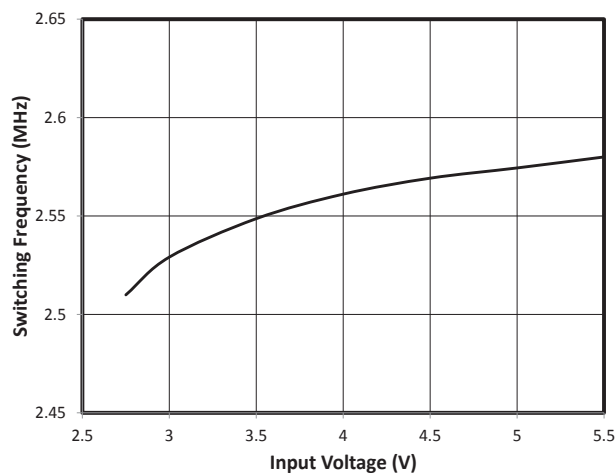
Switching Frequency vs Temperature, $V_{out}=3.3V$



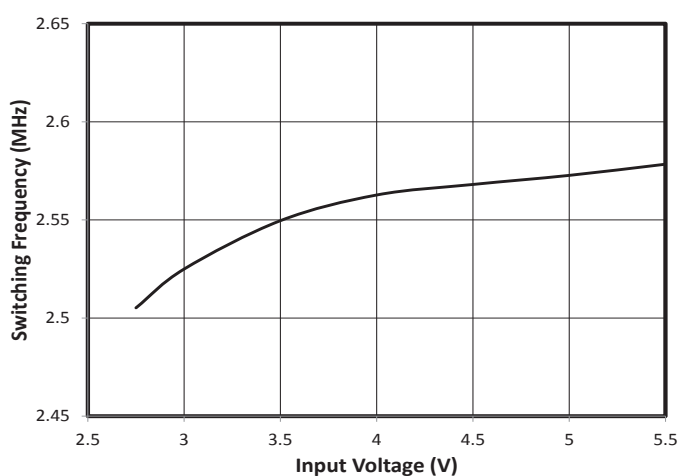
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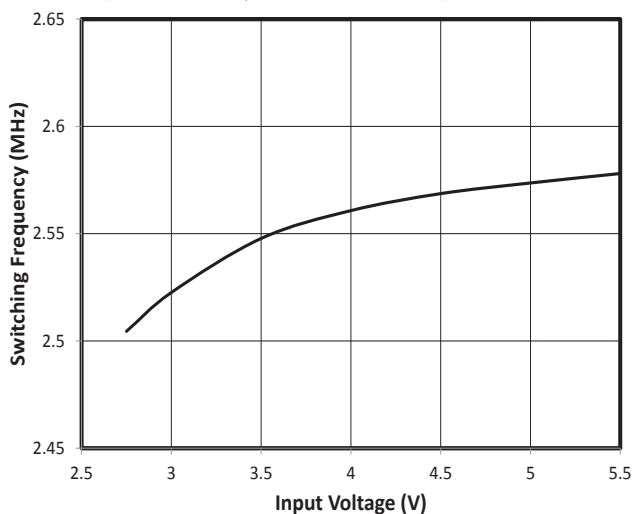
Switching Frequency Vs Input Voltage, $V_{out}=1.0V$



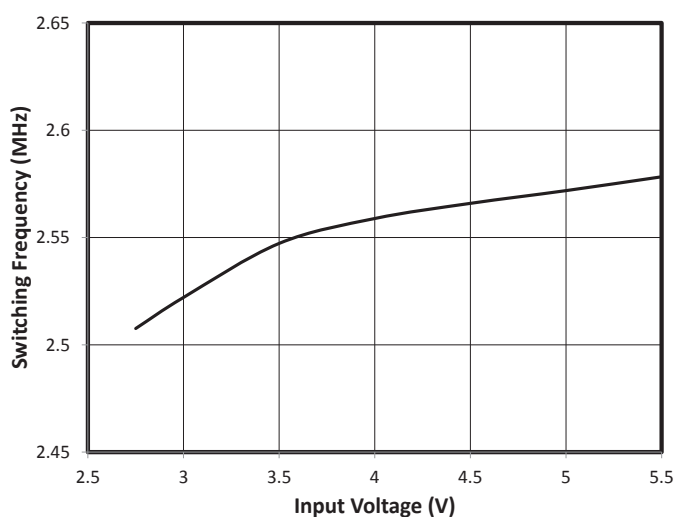
Switching Frequency Vs Input Voltage, $V_{out}=1.2V$



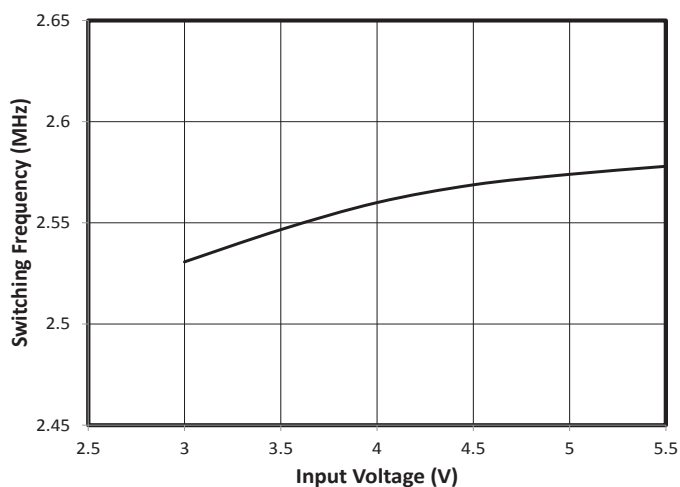
Switching Frequency Vs Input Voltage, $V_{out}=1.5V$



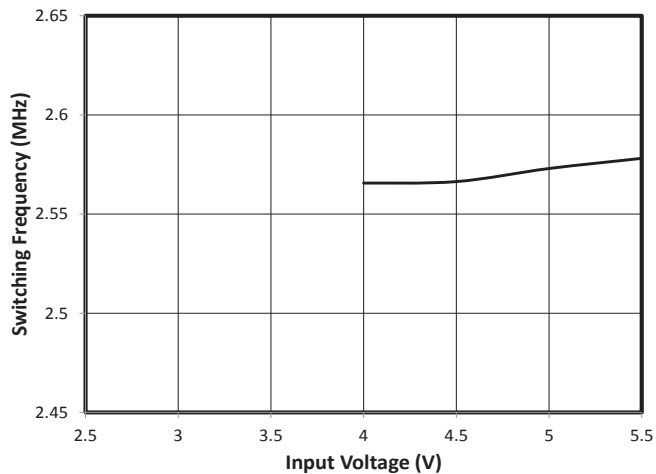
Switching Frequency Vs Input Voltage, $V_{out}=1.8V$



Switching Frequency Vs Input Voltage, $V_{out}=2.5V$



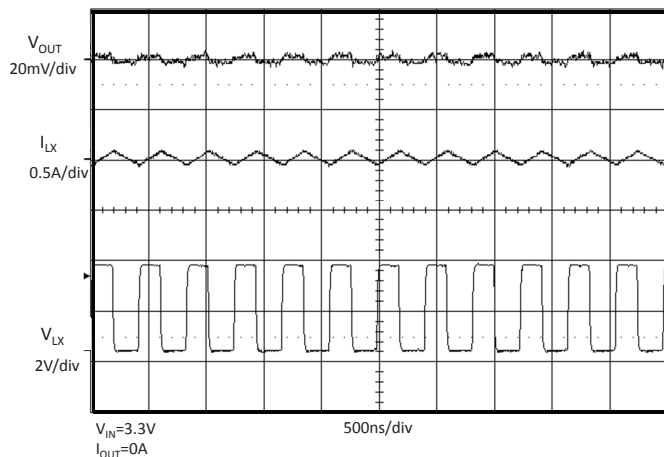
Switching Frequency vs Input Voltage, $V_{out}=3.3V$



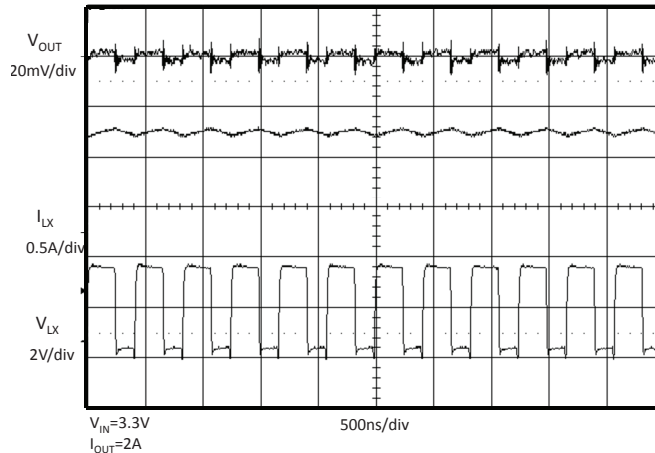
Typical Waveforms

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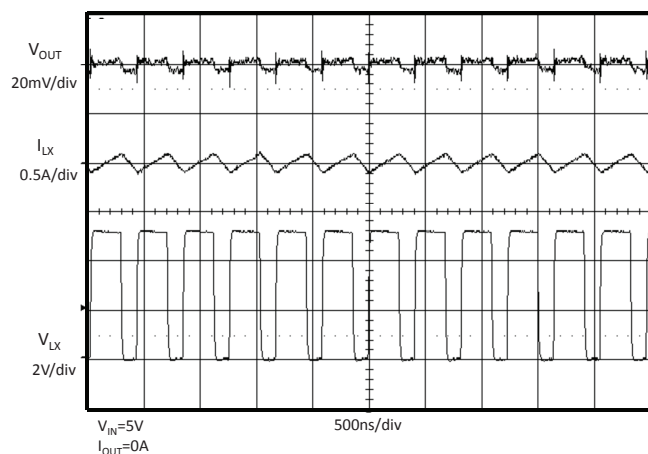
Output Voltage Ripple, ($V_{OUT} = 1.5V$)



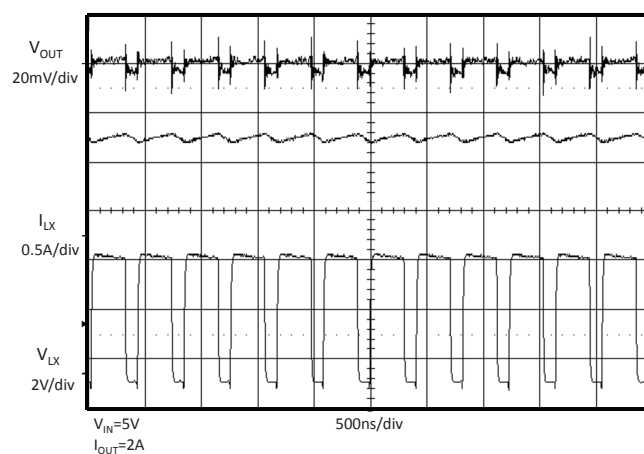
Output Voltage Ripple, ($V_{OUT} = 1.5V$)



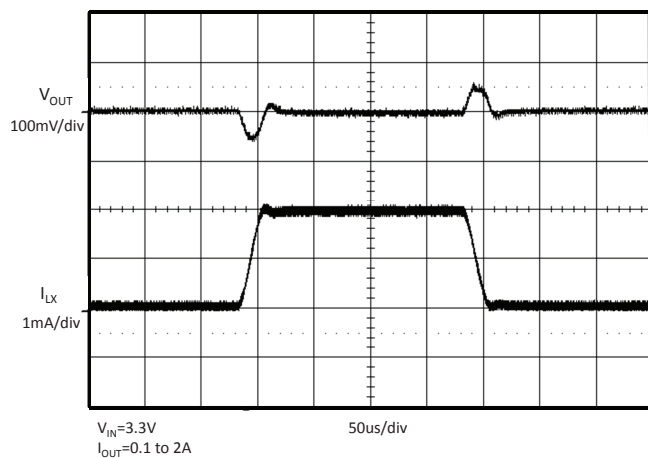
Output Voltage Ripple, ($V_{OUT} = 3.3V$)



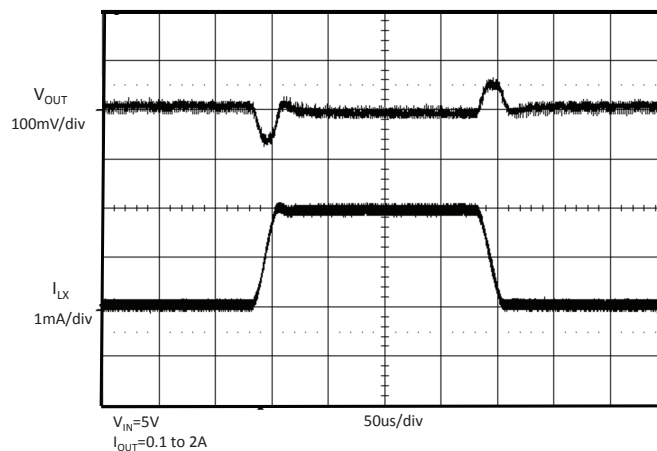
Output Voltage Ripple, ($V_{OUT} = 3.3V$)



Transient Response, ($V_{OUT} = 1.5V$; 0.1A to 2A)



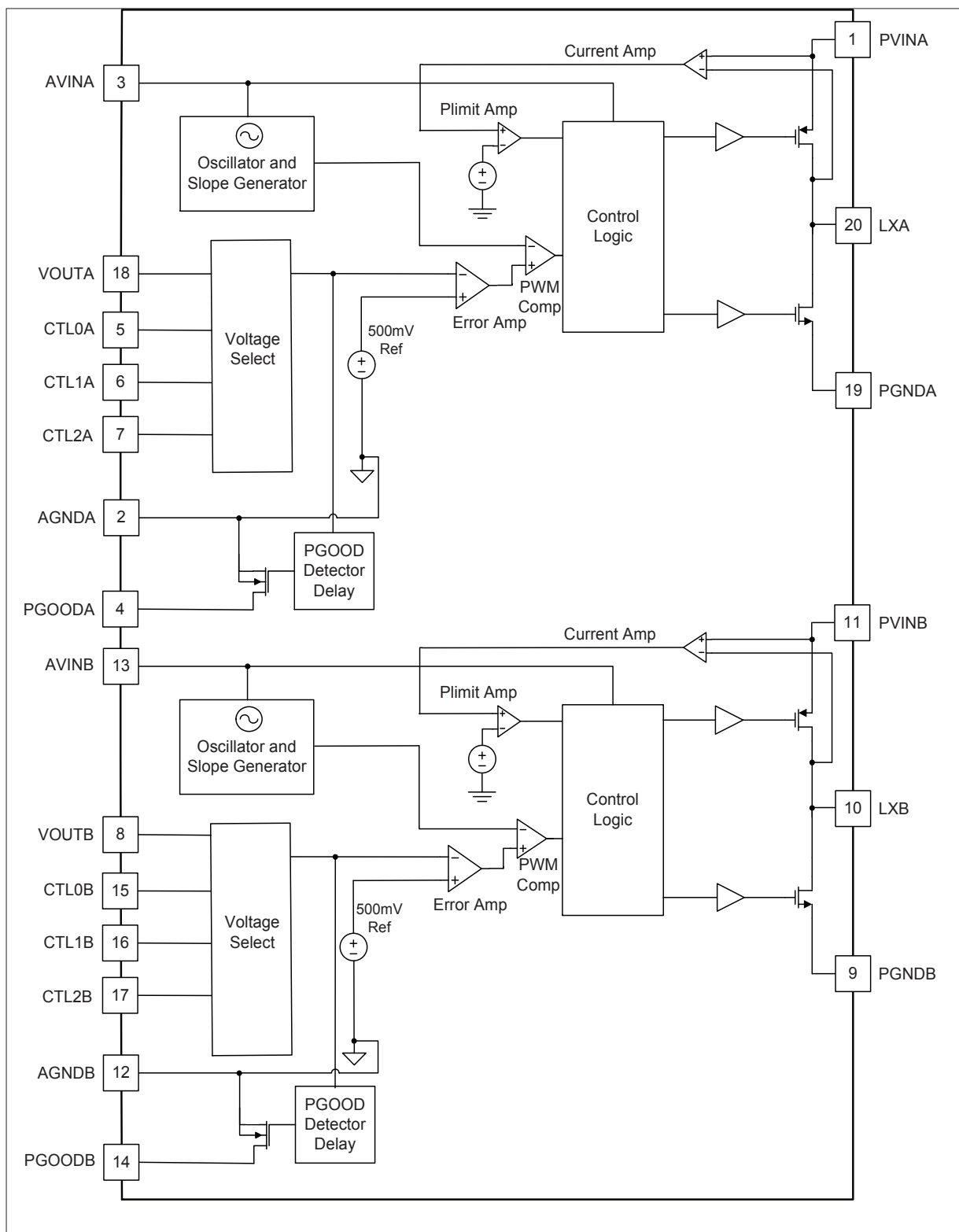
Transient Response, ($V_{OUT} = 3.3V$; 0.1A to 2A)



Pin Descriptions

Pin #	Pin Name	Pin Function
1	PVINA	Channel A — Input supply voltage for the converter power stage and internal circuitry.
2	AGNDA	Ground connection for internal circuitry — connect directly to PGNDA.
3	AVINA	Power supply for internal circuitry — must be connected to PVINA using an R-C filter of 1 Ω and 10nF.
4	PGOODA	Power Good indicator for channel A. When the output voltage reaches the PGOODA threshold, this pin will be open drain (after the PGOOD delay), otherwise it is pulled low internally.
5	CTL0A	Channel A — Control bit 0, see Table 1 for decoding. This pin has a 1 M Ω internal pull-down resistor. This resistor is switched in circuit whenever the pin voltage is below the input high threshold, or when the part is in under-voltage lockout.
6	CTL1A	Channel A — Control bit 1, see Table 1 for decoding. This pin has a 1 M Ω internal pull-down resistor. This resistor is switched in circuit whenever the pin voltage is below the input high threshold, or when the part is in under-voltage lockout.
7	CTL2A	Channel A — Control bit 2, see Table 1 for decoding. This pin has a 1 M Ω internal pull-down resistor. This resistor is switched in circuit whenever the pin voltage is below the input high threshold, or when the part is in under-voltage lockout.
8	VOUTB	Output voltage sense pin of Channel B
9	PGNDB	Channel B — Ground connection for converter power stage and internal circuitry.
10	LXB	Switching node of Channel B — connect an inductor between this pin and the output capacitor.
11	PVINB	Channel B — Input supply voltage for the converter power stage and internal circuitry.
12	AGNDB	Ground connection for internal circuitry — connect directly to PGNDB.
13	AVINB	Power supply for internal circuitry — must be connected to PVINB using an R-C filter of 1 Ω and 10nF.
14	PGOODB	Power Good indicator for channel B. When the output voltage reaches the PGOODB threshold, this pin will be open drain (after the PGOOD delay), otherwise it is pulled low internally.
15	CTL0B	Channel B — Control bit 0, see Table 1 for decoding. This pin has a 1 M Ω internal pull-down resistor. This resistor is switched in circuit whenever the pin voltage is below the input high threshold, or when the part is in under-voltage lockout.
16	CTL1B	Channel B — Control bit 1 - see Table 1 for decoding. This pin has a 1 M Ω internal pull-down resistor. This resistor is switched in circuit whenever the pin voltage is below the input high threshold, or when the part is in under-voltage lockout.
17	CTL2B	Channel B — Control bit 2, see Table 1 for decoding. This pin has a 1 M Ω internal pull-down resistor. This resistor is switched in circuit whenever the pin voltage is below the input high threshold, or when the part is in under-voltage lockout.
18	VOUTA	Output voltage sense pin of Channel A
19	PGNDA	Channel A — Ground connection for converter power stage and internal circuitry.
20	LXA	Switching node of Channel A — connect an inductor between this pin and the output capacitor.
	PAD	Thermal pad for heatsinking purposes.

Block Diagram



Applications Information (continued)

Power Good

PGOOD is an open-drain output. When the output voltage drops below nominal voltage, the PGOOD pin is pulled low after a 20 μ s delay. During start-up, PGOOD will be asserted 1.7ms (typ.) after the output voltage reaches 90% of the final regulation voltage. Over voltage, fold-back current limit and thermal shutdown will force PGOOD low after a 20 μ s delay. When recovering from a fault, PGOOD will be asserted 1.7ms (typ.) after Vout reaches 90% of the final regulation voltage.

Load Current Derating Curves

Each channel of SC284A could support up to 2A load current as long as the junction temperature is lower than the maximum allowable 125C. Since both channels are within the same package, the 125C maximum junction temperature determines the max load current of both channels at room temperature and other elevated ambient temperatures. Figure 2 shows the load current performance of both channels at 85°C for a particular EVB used in product characterization.

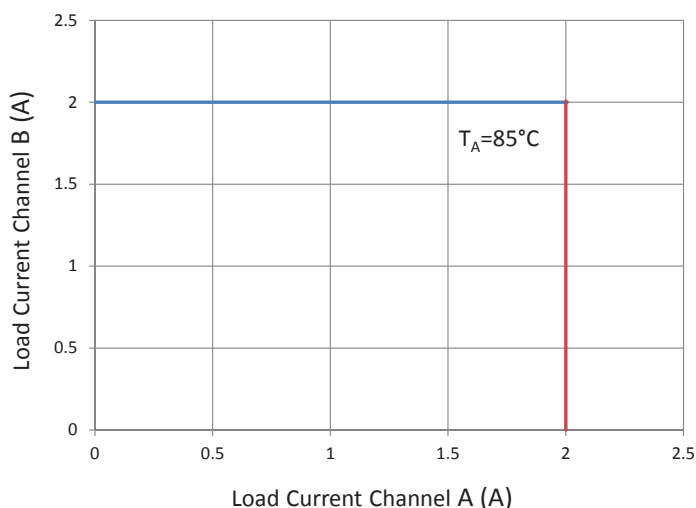


Figure 2 — Maximum allowable load current for each channel for a maximum junction temperature of 125°C

Protection Features

The SC284A provides the following protection features:

- Current Limit
- Over-Voltage Protection
- Soft-Start
- Thermal Shutdown

Current Limit

The internal PMOS power device in the switching stage is protected by a current limit feature. If the inductor current is above the PMOS current limit for 16 consecutive cycles, the part enters foldback current limit mode and the output current is limited to the current limit holding current (I_{CL_HOLD}) of a few hundred milliamperes. Under this condition, the output voltage will be the product of I_{CL_HOLD} and the load resistance. The current limit holding current will decrease when the output voltage increases. The load presented must fall below the current limit holding current for the part to exit foldback current limit mode. Figure 3 shows how the typical current limit holding current varies with output voltage. The SC284A is capable of sustaining an indefinite short circuit without damage and will resume normal operation when the fault is removed. The foldback current limit mode is disabled during soft-start.

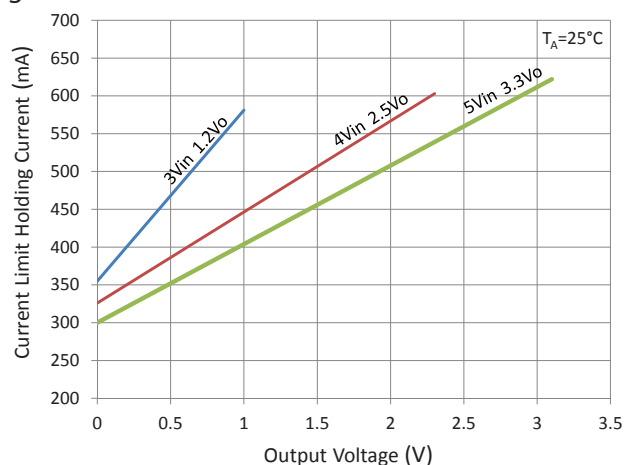


Figure 3— Typical Current Limit Holding Current vs. Output Voltage

Over-Voltage Protection

In the event of a 15% over-voltage on the output, the PWM drive is disabled leaving the LX pin floating.

Soft-Start

Soft-start is activated once VIN reaches the UVLO and one or more CTL pins are set high to enable the part. A thermal shutdown event will also activate the soft-start sequence. Soft-start controls the maximum current during startup thus limiting inrush current. The PMOS current limit is stepped through four soft-start levels of approximately 20%, 25%, 40%, & 100%. Each step is maintained for 400 μ s

Applications Information (continued)

following an internal reference start up duration of 100μs giving a total nominal startup period of 1700μs. During startup, the chip operates by controlling the inductor current swings between 0A and current limit. If at any time V_{OUT} reaches 86% of the target or at the end of the soft-start period, the SC284A will switch to PWM mode operation.

The SC284A is capable of starting up into a pre-biased output.

Shut Down

When all CTL pins of a channel are low, the corresponding channel will be disabled, drawing less than 1μA from that input power supply. The internal switches and bandgap voltage will be immediately turned off.

Thermal Shutdown

The device has a thermal shutdown feature to protect the SC284A if the junction temperature exceeds 160°C. During thermal shutdown, the on-chip power devices are disabled, tri-stating the LX output. When the temperature drops by 10°C, it will initiate a soft-start cycle to resume normal operation.

Inductor Selection

The SC284A converter has internal loop compensation. The compensation is designed to work with an output filter corner frequency of less than 40kHz for a V_{IN} of 5V and 50kHz for a V_{IN} of 3.3V over any operating condition. The corner frequency of the output filter is shown in the following equation.

$$f_c = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

Values outside this range may lead to instability, malfunction, or out-of-specification performance.

In general, the inductance is chosen by making the inductor ripple current to be less than 30% of maximum load current. When choosing an inductor, it is important to consider the change in inductance with DC bias current. The inductor saturation current is specified as the current at which the inductance drops a specific percentage from the nominal value. This is approximately 30%. Except for short-circuit or other fault conditions,

the peak current must always be less than the saturation current specified by the manufacturer. The peak current is the maximum load current plus one half of the inductor ripple current at the maximum input voltage. Load and/or line transients can cause the peak current to exceed this level for short durations. Maintaining the peak current below the inductor saturation specification keeps the inductor ripple current and the output voltage ripple at acceptable levels. Manufacturers often provide graphs of actual inductance and saturation characteristics versus applied inductor current. The saturation characteristics of the inductor can vary significantly with core temperature. Core and ambient temperatures should be considered when examining the core saturation characteristics.

When the inductance has been determined, the DC resistance (DCR) must be examined. The efficiency that can be achieved is dependent upon the DCR of the inductor. Lower values give higher efficiency. The RMS DC current rating of the inductor is associated with losses in the copper windings and the resulting temperature rise of the inductor. This is usually specified as the current which produces a 40°C temperature rise. Most copper windings are rated to accommodate this temperature rise above maximum ambient.

Magnetic fields associated with the output inductor can interfere with nearby circuitry. This can be minimized by the use of low noise shielded inductors which use the minimum gap possible to limit the distance that magnetic fields can radiate from the inductor. However shielded inductors typically have a higher DCR and are thus less efficient than a similarly sized non-shielded inductor. Final inductor selection depends upon various design considerations such as efficiency, EMI, size, and cost. Table 2 lists the manufacturers of recommended inductor options. The saturation characteristics and DC current ratings are also shown.

Applications Information (continued)

Manufacturer Part Number	L (μH)	DCR Max (Ω)	Rated Current (A)	L at Rated Current (μH)	Dimensions LxWxH (mm)
TOKO 1071AS-1R0N	1.00±30%	0.040	2.70	0.70	2.8x3.0x1.5
TOKO 1127AS-2R2M	2.20±20%	0.048	2.50	1.54	3.5x3.7x1.8
Panasonic ELLVGG1R0N	1.00±23%	0.062	2.20	0.70	3.2x3.2x1.5

Table 2 – Recommended Inductors

C_{OUT} Selection

The internal voltage loop compensation in the SC284A limits the minimum output capacitor value to 22μF if using a 2.2μH inductor or 44μF if using a 1μH inductor. This is due to its influence on the the loop crossover frequency, phase margin, and gain margin. The total output capacitance should not exceed 50μF to avoid any start-up problems. For most typical applications it is recommended to use an output capacitance of 22μF to 44μF. When choosing the output capacitor's capacitance, verify the voltage derating effect from the capacitor vendor's data sheet.

Capacitors with X7R or X5R ceramic dielectric are recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

The output voltage droop due to a load transient is determined by the capacitance of the ceramic output capacitor. The ceramic capacitor supplies the load current initially until the loop responds. Within a few switching cycles the loop will respond and the inductor current will increase to match the required load. The output voltage droop during the period prior to the loop responding can be related to the choice of output capacitor by the relationship from the following equation.

$$C_{OUT} = \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f_{OSC}}$$

The output capacitor RMS ripple current may be calculated from the following equation.

$$I_{COUT(RMS)} = \frac{1}{2\sqrt{3}} \left[\frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{L \times f_{OSC} \times V_{IN}} \right]$$

Table 3 lists the manufacturers of recommended capacitor options.

Manufacturer Part Number	Value (μF)	Type	Rated Voltage (VDC)	Value at 3.3V (μF)	Dimensions LxWxH (mm)
Murata GRM21BR60J106K	10±10%	X5R	6.3	4.74	2.0x1.25x1.25 (EIA:0805)
Murata GRM219R60J106K	10±10%	X5R	6.3	4.05	2.0x1.25x0.85 (EIA:0805)
Murata GRM21BR60J226M	22±20%	X5R	6.3	6.57	2.0x1.25x1.25 (EIA:0805)
Murata GRM31CR60J476M	47±20%	X5R	6.3	20.3	3.2x1.6x1.6 (EIA:1206)

Table 3 – Recommended Capacitors

C_{IN} Selection

The SC284A source input current is a DC supply current with a triangular ripple imposed on it. To prevent large input voltage ripple, a low ESR ceramic capacitor is required. A minimum value of 10μF should be used. It is important to consider the DC voltage coefficient characteristics when determining the actual required value. It should be noted a 10μF, 6.3V, X5R ceramic capacitor with 5V DC applied may exhibit a capacitance as low as 4.05μF. To estimate the required input capacitor, determine the acceptable input ripple voltage and calculate the minimum value required for C_{IN} as shown by the following equation.

$$I_{CIN(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

The input capacitor RMS ripple current varies with the input and output voltage. The maximum input capacitor RMS current is found from the next equation .

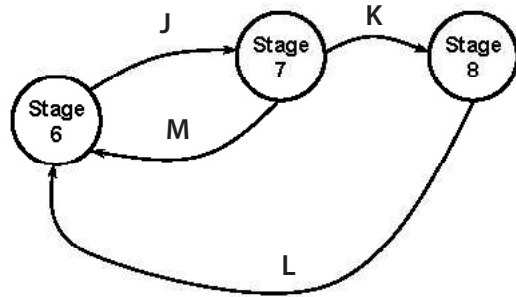
$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{\left(\frac{\Delta V}{I_{OUT}} - ESR \right) \times f_{OSC}}$$

Applications Information (continued)

The input voltage ripple and RMS current ripple are at a maximum when the input voltage is twice the output voltage or 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the PMOS switch. Low ESR/ESL X5R ceramic capacitors are recommended for this function. To minimize stray inductance, the capacitor should be placed as close as possible to the VIN and GND pins of the SC284A.

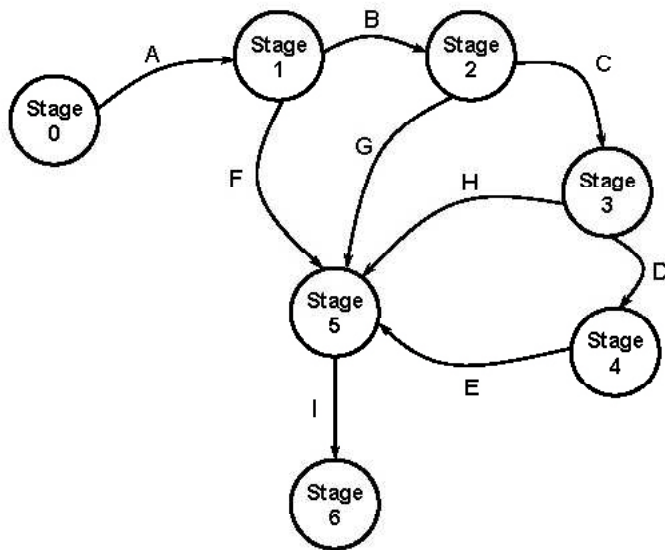
Applications Information (continued)



Stages	Operation description
6	Normal PWM operation Overload protection is enabled and peak current limit at 100% level
7	Cycle by cycle peak current limit
8	OCF protection is activated. Foldback peak current limit. PWM "ON" when inductor current of 0A PWM "OFF" when inductor current hits peak current limit of foldback mode.

Conditions	Operation description
J	Inductor current hits peak current limit
K	Peak current limit for 10 consecutive cycles
L	Vout ≥ 100% target
M	Inductor current doesn't hit peak current limit

Figure 4 — Current Limit Protection

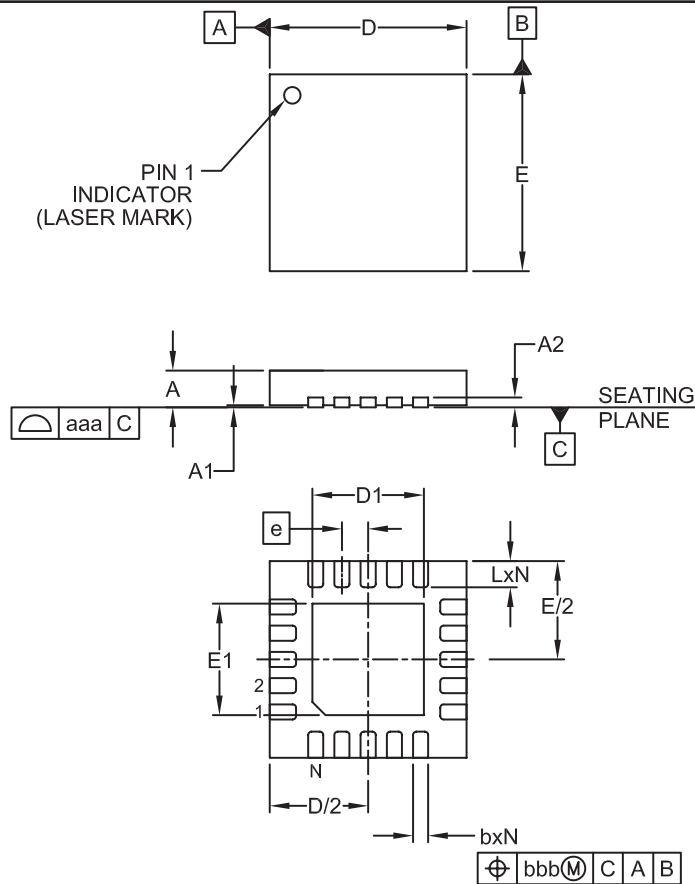


Stages	Operation description
0	Chip is OFF.
1	Peak current limit at 20% level PWM "ON" when inductor current of 0A PWM "OFF" when inductor current hits peak current limit Stage duration of 400μs
2	Peak current limit at 25% level PWM "ON" when inductor current of 0A PWM "OFF" when inductor current hits peak current limit Stage duration of 400μs
3	Peak current limit at 40% level PWM "ON" when inductor current of 500mA PWM "OFF" when inductor current hits peak current limit Stage duration of 400μs
4	Peak current limit at 100% level PWM "ON" when inductor current of 500mA PWM "OFF" when inductor current hits peak current limit Stage duration of 400μs
5	Peak current limit at 100% level Switch to closed-loop PWM operation.
6	Soft Start ends. Normal PWM operation Overload protection is enabled

Conditions	Operation description
A	VIN > UVLO Threshold AND One or more CTL pin is high. AND Internal reference is ready.
B	End of stage 1 AND Vout < 86% of target
C	End of stage 2 AND Vout < 86% of target
D	End of stage 3 AND Vout < 86% of target
E	End of stage 4 AND Vout < 86% of target
F	Vout > 86% of target
G	Vout > 86% of target
H	Vout > 86% of target
I	End of soft start time of 1700μs

Figure 5 — Soft Start Operation

Outline Drawing – 3x3 MLPQ-UT20

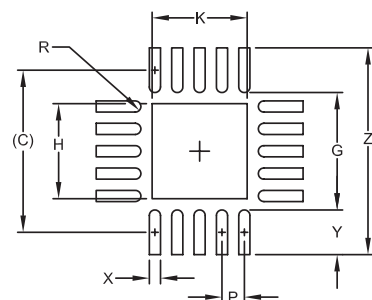


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2	(.006)			(0.152)		
b	.006	.008	.010	0.15	0.20	0.25
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e	.016 BSC			0.40 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	20			20		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

Land Pattern – 3x3 MLPQ-UT20



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

www.semtech.com