Datasheet

LCD Segment Drivers

Multi-function LCD Segment Drivers

BU97520AKV-M **MAX 276 Segment(69SEG x 4COM)**

General Description

The BU97520AKV-M is 1/4 or 1/3 Duty General-purpose LCD driver. The BU97520AKV-M can drive up to 276 LCD Segments directly. The BU97520AKV-M can also control up to 6 General-purpose output pins / 6 PWM output pins. These products also incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring.

Features

- AEC-Q100 Qualified *(Note 1)*
- Key Input Function for up to 30 Keys. (A key scan is performed only when a key is pressed.)
- Either 1/4 or 1/3 Duty can be Selected with the Serial Control Data.
  1/4 Duty Drive: up to 276 Segments
  1/3 Duty Drive: up to 207 Segments
- Selectable Display Frame Frequency for Common and Segment Output Waveforms.
- Configurable Output Pin to Segment Output / PWM Output / General-purpose Output.(Max 6 Pins)
- Built-in OSC Circuit
- The INHb Pin can Force the Display to the off State.
- Integrated Voltage Detect Type Power on Reset (VDET) Circuit
- No External Component
- Low Power Consumption Design
- Supports Line and Frame Inversion

(Note 1) Grade 3

Applications

- Car Audio, Home Electrical Appliance, Meter Equipment etc.

Key Specifications

- Supply Voltage Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 276 Segments
- Display Duty: 1/3, 1/4 Selectable
- Bias: 1/2, 1/3 Bias
- Interface: 3wire Serial Interface

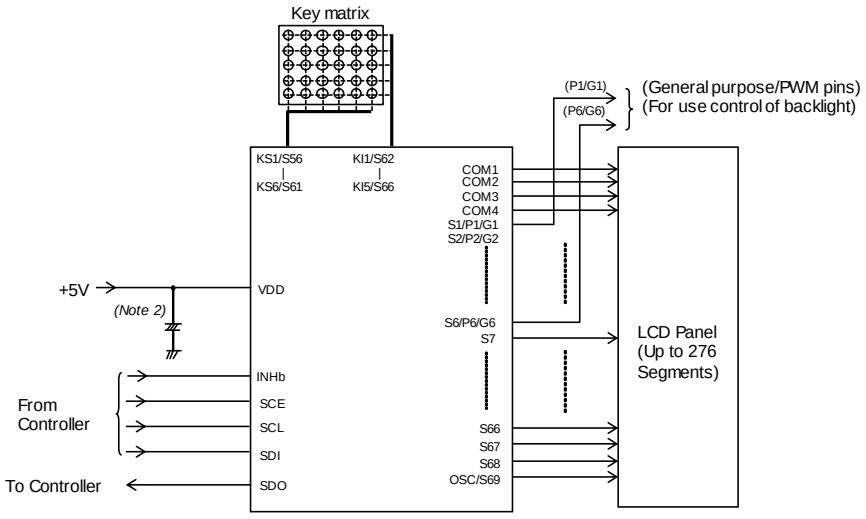
Package

W(Typ) × D(Typ) × H(Max)



VQFP80
14.00mm x 14.00mm x 1.60mm

Typical Application Circuit



(Note 2) Insert capacitors between VDD and VSS C ≥ 0.1µF.

Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

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Block Diagram

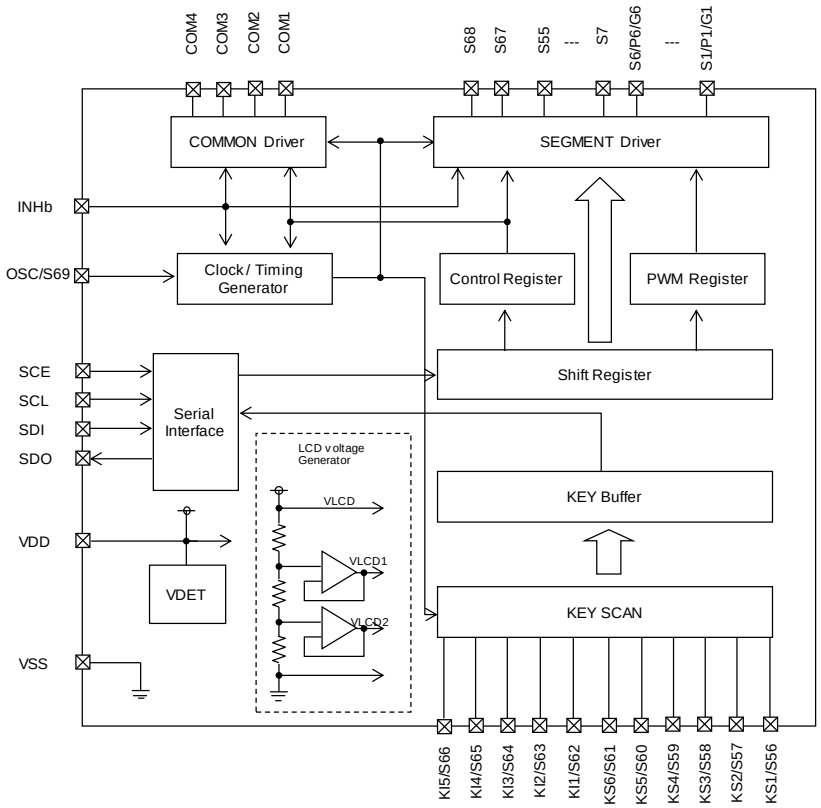


Figure 2. Block Diagram

Pin Configuration

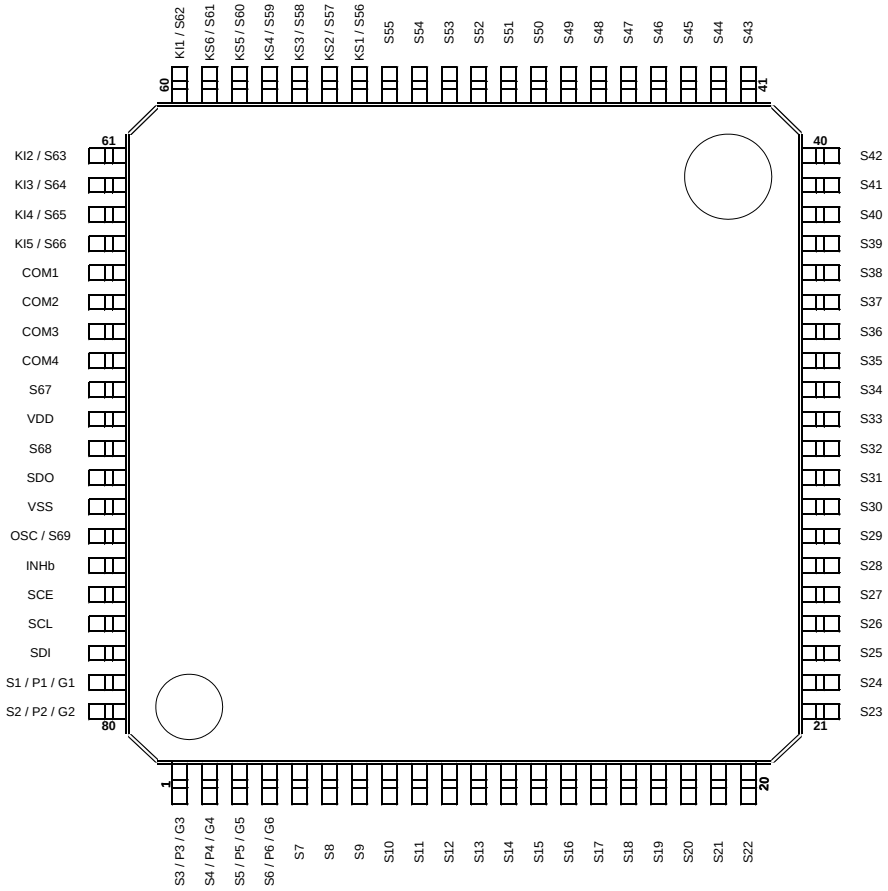


Figure 3. Pin Configuration (TOP VIEW)

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Absolute Maximum Ratings (VSS = 0.0V)

Parameter	Symbol	Conditions	Rating	Unit
Maximum Supply Voltage	VDD	VDD	-0.3 to +7.0	V
Input Voltage	V_{IN1}	SCE, SCL, SDI, INHb, OSC	-0.3 to +7.0	V
	V_{IN2}	KI1 to KI5	-0.3 to +7.0	V
Allowable Loss	Pd	-	1.20*(Note)*	W
Operating Temperature	Topr	-	-40 to +85	°C
Storage Temperature	Tstg	-	-55 to +125	°C

(Note) Derate by 12.0mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board).
(Board size: 70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only)

Caution1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings

Caution2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Recommended Operating Conditions (Ta = -40°C to +85°C, VSS = 0V)

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Supply Voltage	VDD	-	2.7	5.0	6.0	V

Electrical Characteristics (Ta = -40°C to +85°C, VDD = 2.7V to 6.0V, VSS = 0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Hysteresis	V_{H1}	SCE, SCL, SDI, INHb, OSC	-	-	0.03VDD	-	V
	V_{H2}	KI1 to KI5	-	-	0.1VDD	-	V
Power-on Detection Voltage	V_{DET}	VDD	-	1.4	1.8	2.2	V
"H" Level Input Voltage	V_{IH1}	SCE, SCL, SDI, INHb, OSC	4.0V ≤ VDD ≤ 6.0V	0.4VDD	-	VDD	V
	V_{IH2}	SCE, SCL, SDI, INHb, OSC	2.7V ≤ VDD < 4.0V	0.8VDD	-	VDD	V
	V_{IH3}	KI1 to KI5	-	0.7VDD	-	VDD	V
"L" Level Input Voltage	V_{IL1}	SCE, SCL, SDI, INHb OSC, KI1 to KI5	-	0	-	0.2VDD	V
Input Floating Voltage	V_{IF}	KI1 to KI5	-	-	-	0.05VDD	V
Pull-down Resistance	R_{PD}	KI1 to KI5	VDD = 5.0V	50	100	250	kΩ
Output Off Leakage Current	I_{OFFH}	SDO	V_O = 6.0V	-	-	6.0	μA
"H" Level Input Current	I_{IH1}	SCE, SCL,SDI, INHb, OSC	V_I = 5.5V	-	-	5.0	μA
"L" Level Input Current	I_{IL1}	SCE, SCL,SDI, INHb, OSC	V_I = 0V	-5.0	-	-	μA
"H" Level Output Voltage	V_{OH1}	S1 to S69	I_O = -20μA	VDD-0.9	-	-	V
	V_{OH2}	COM1 to COM4	I_O = -100μA	VDD-0.9	-	-	
	V_{OH3}	P1/G1 to P6/G6	I_O = -1mA	VDD-0.9	-	-	
	V_{OH4}	KS1 to KS6	I_O = -500μA	VDD-1.0	VDD-0.5	VDD-0.2	
"L" Level Output Voltage	V_{OL1}	S1 to S69	I_O = 20μA	-	-	0.9	V
	V_{OL2}	COM1 to COM4	I_O = 100μA	-	-	0.9	
	V_{OL3}	P1/G1 to P6/G6	I_O = 1mA	-	-	0.9	
	V_{OL4}	KS1 to KS6	I_O = 25μA	0.2	0.5	1.5	
	V_{OL5}	SDO	I_O = 1mA	-	0.1	0.5	
Middle Level Output Voltage	V_{MID1}	S1 to S69	1/2 Bias I_O = ±20μA	1/2VDD -0.9	-	1/2VDD +0.9	V
	V_{MID2}	COM1 to COM4	1/2 Bias I_O = ±100μA	1/2VDD -0.9	-	1/2VDD +0.9	
	V_{MID3}	S1 to S69	1/3 Bias I_O = ±20μA	2/3VDD -0.9	-	2/3VDD +0.9	
	V_{MID4}	S1 to S69	1/3 Bias I_O = ±20μA	1/3VDD -0.9	-	1/3VDD +0.9	
	V_{MID5}	COM1 to COM4	1/3 Bias I_O = ±100μA	2/3VDD -0.9	-	2/3VDD +0.9	
	V_{MID6}	COM1 to COM4	1/3 Bias I_O = ±100μA	1/3VDD -0.9	-	1/3VDD +0.9	
Current Consumption	I_{DD1}	VDD	Power-saving mode	-	-	15	μA
	I_{DD2}	VDD	VDD = 5.0V Output open ,1/2 Bias Frame frequency = 80Hz	-	85	170	
	I_{DD3}	VDD	VDD = 5.0V Output open ,1/3 Bias Frame frequency = 80Hz	-	110	210	

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Oscillation Characteristics(Ta = -40°C to +85°C, VDD = 2.7V to 6.0V , VSS = 0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Oscillator Frequency 1	$f_{OSC\,1}$	-	VDD = 2.7V to 6.0V	300	-	720	kHz
Oscillator Frequency 2	$f_{OSC\,2}$	-	VDD = 5V	510	600	690	kHz
External Clock Frequency*(Note 1)*	$f_{OSC\,3}$	OSC	External clock mode (OC=1)	30	-	1000	kHz
External Clock Rise Time	tr			-	160	-	ns
External Clock Fall Time	tf			-	160	-	ns
External Clock Duty	t_{DTY}			30	50	70	%

(Note 1) Frame frequency is decided by external clock and dividing ratio of FC0, FC1, FC2 setting.

[Reference Data]

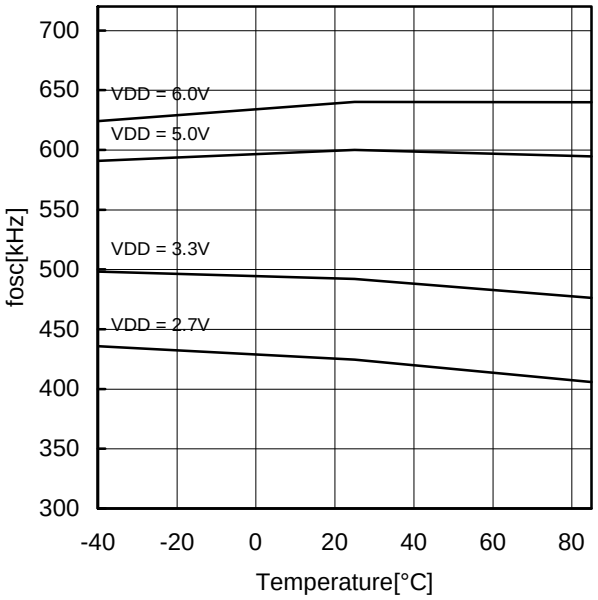
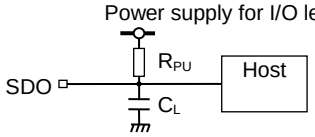


Figure 4. Oscillator Frequency Typical Temperature Characteristics

MPU Interface Characteristics (Ta = -40°C to +85°C, VDD = 2.7V to 6.0V, VSS = 0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Data Setup Time	t_{DS}	SCL, SDI	-	120	-	-	ns
Data Hold Time	t_{DH}	SCL, SDI	-	120	-	-	ns
SCE Wait Time	t_{CP}	SCE, SCL	-	120	-	-	ns
SCE Setup Time	t_{CS}	SCE, SCL	-	120	-	-	ns
SCE Hold Time	t_{CH}	SCE, SCL	-	120	-	-	ns
Clock Cycle Time	t_{CCYC}	SCL	-	320	-	-	ns
High-level Clock Pulse Width	t_{CHW}	SCL	-	120	-	-	ns
Low-Level Clock Pulse Width (Write)	t_{CLWW}	SCL	-	120	-	-	ns
Low-Level Clock Pulse Width (Read)	t_{CLWR}	SCL	R_{PU}=4.7kΩ, C_L=10pF*(Note 2)*	1.6	-	-	µs
Rise Time	tr	SCE, SCL, SDI	-	-	160	-	ns
Fall Time	tf	SCE, SCL, SDI	-	-	160	-	ns
INHb Switching Time	t_C	INHb, SCE	-	10	-	-	µs
SDO Output Delay Time	t_{DC}	SDO	R_{PU}=4.7KΩ, C_L=10pF*(Note 2)*	-	-	1.5	µs
SDO Rise Time	t_{DR}	SDO	R_{PU}=4.7KΩ, C_L=10pF*(Note 2)*	-	-	1.5	µs

(Note 2) Since SDO is an open-drain output, "t_{DC}" and "t_{DR}" depend on the resistance of the pull-up resistor R_{PU} and the load capacitance C_L.
R_{PU}: 1kΩ≤R_{PU}≤10kΩ is recommended.
C_L: A parasitic capacitance to VSS in an application circuit. Any component is not necessary to be attached.

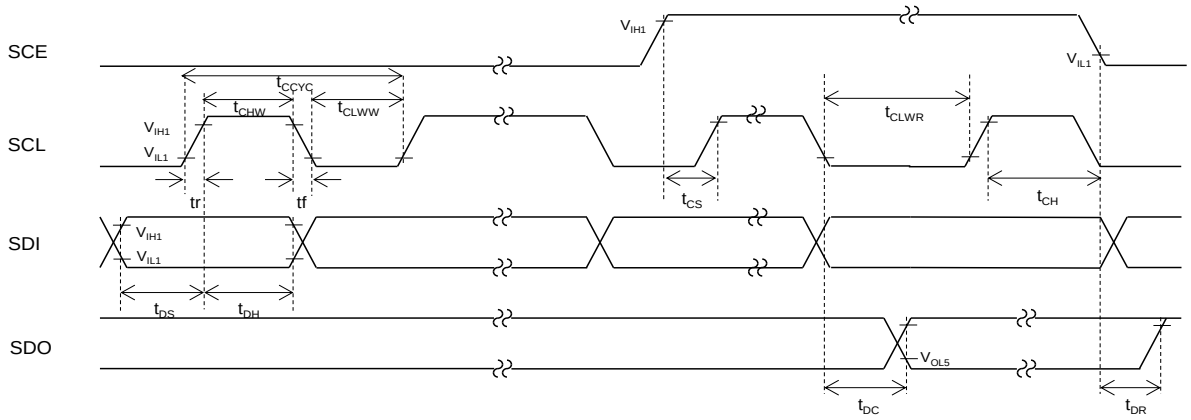


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MPU Interface Characteristics – continued

1. When SCL is stopped at the low level



2. When SCL is stopped at the high level

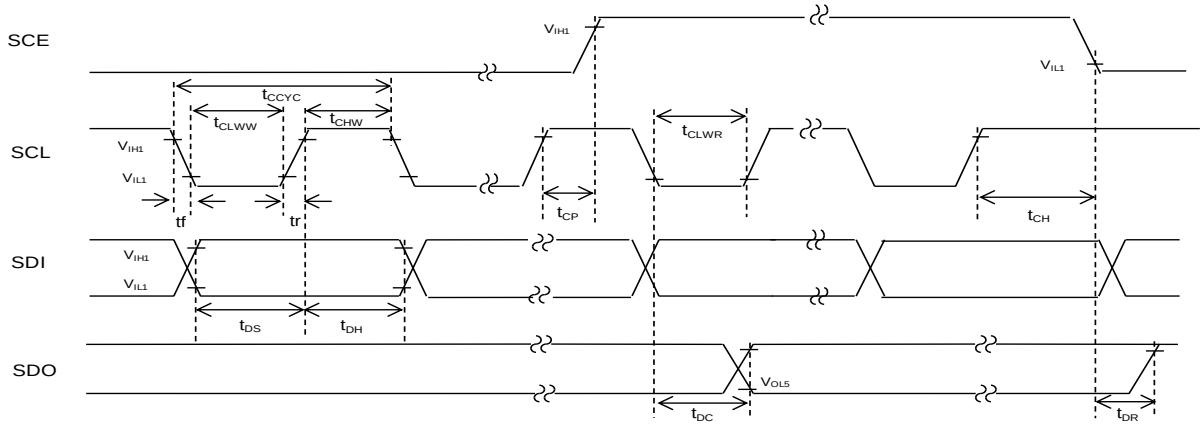


Figure 5. Serial Interface Timing

Pin Description

Pin	Pin No.	Function	Active	I/O	Handling when unused
S1/P1/G1 to S6/P6/G6	79,80, 1 to 4,	Segment output for displaying the display data transferred by serial data input. The S1/P1/G1 to S6/P6/G6 pins can also be used as General-purpose / PWM outputs when so set up by the control data.	-	O	OPEN
S7 to S55 S67,S68	5 to 53, 69,71	Segment output for displaying the display data transferred by serial data input.	-	O	OPEN
KS1/S56 to KS6/S61	54 to 59	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S56 to KS6/S61 pins can be used as segment outputs when so specified by the control data.	-	O	OPEN
KI1/S62 to KI5/S66	60 to 64	Key scan inputs These pins have built-in pull-down resistors. The KI1/S62 to KI5/S66 pins can be used as segment outputs when so specified by the control data.	-	I O	VSS OPEN
COM1 to COM4	65 to 68	Common driver output pins. The frame frequency is fo[Hz].	-	O	OPEN
OSC/S69	74	Segment output for displaying the display data transferred by serial data input. The pin OSC/S69 can be used as external clock input pin when set up by the control data.	-	I O	VSS OPEN
SCE SCL SDI	76 77 78	Serial data transfer inputs. Must be connected to the controller. SCE: Chip enable SCL: Clock for serial data transfer. SDI: Transfer data	H ↑ -	I I I	VSS VSS VSS
SDO	72	Output data	-	O	OPEN

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Pin Description – continued

Pin	Pin No.	Function	Active	I/O	Handling when unused
INHb*(Note)*	75	Display off control input. When INHb = low (VSS), Display forced off S1/P1/G1 to S6/P6/G6 = low (VSS) S7 to S69 = low (VSS) COM1 to COM4 = low (VSS) Stop the LCD drive bias voltage generation divider resistors. Stop the internal oscillation circuit. When INHb = high (VDD), Display on However, serial data transfer is possible when the display is forced off.	L	I	VDD
VDD	70	Power supply pin. A supply voltage of 2.7V to 6.0V must be applied to this pin.	-	-	-
VSS	73	Power supply pin. Must be connected to Ground.	-	-	-

(Note) Regarding the details of the INHb pin and the control of each output, refer to "INHb Pin and Display Control".

IO Equivalence Circuit

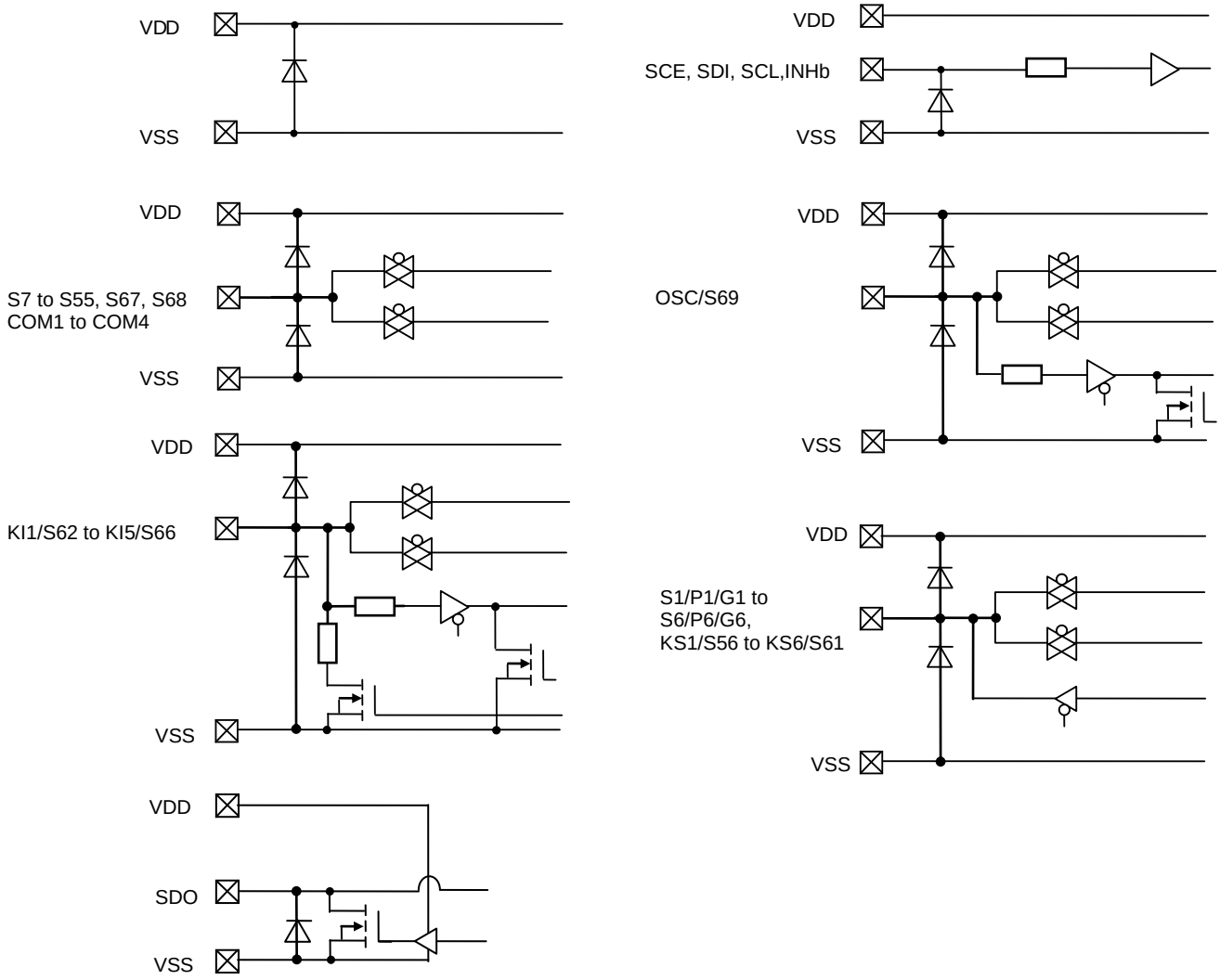


Figure 6. I/O Equivalence Circuit

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Serial Data Transfer Formats

1. 1/4 Duty

(1) When SCL is stopped at the low level

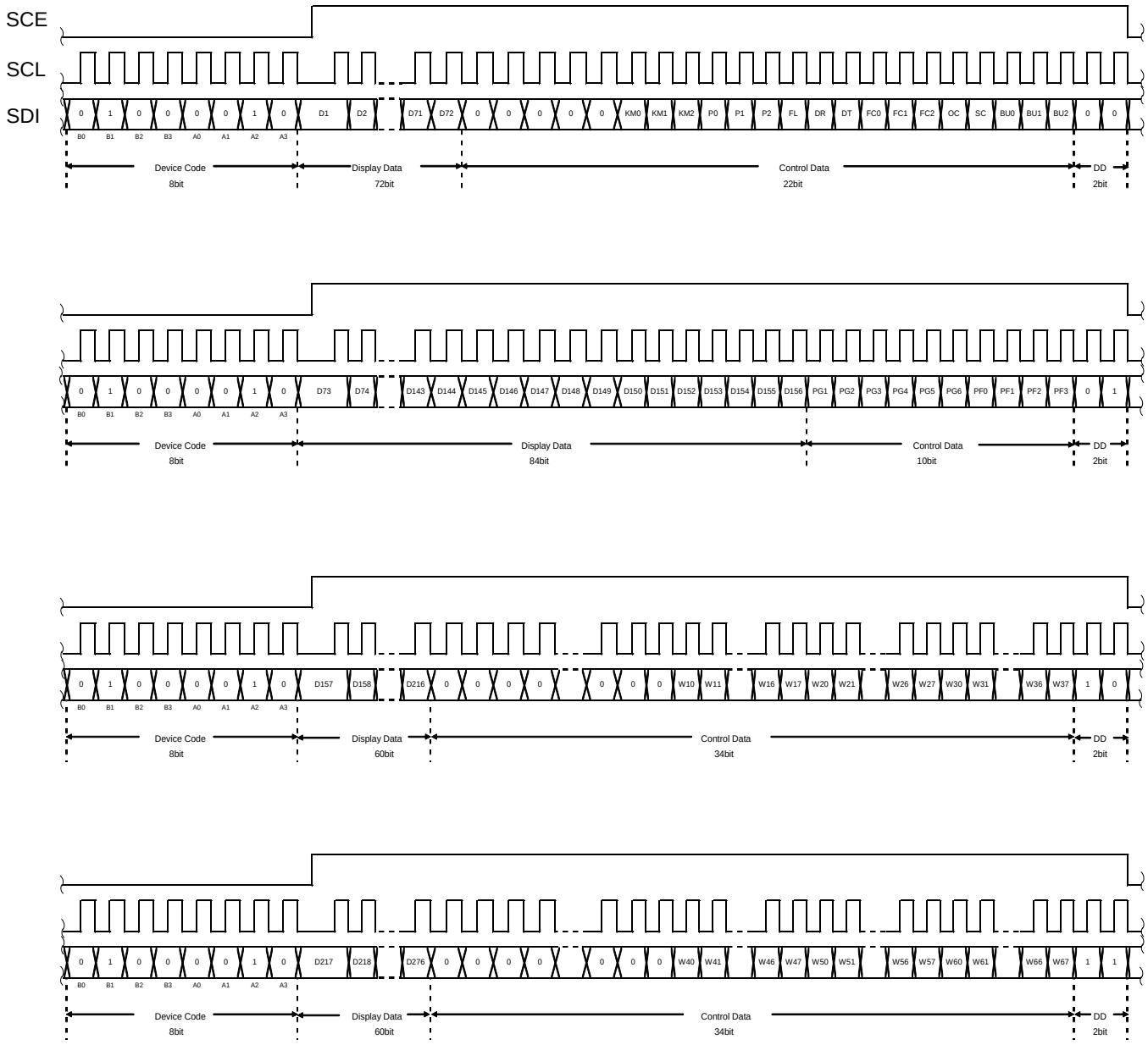


Figure 7. 3-SPI Data Transfer Format

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Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level

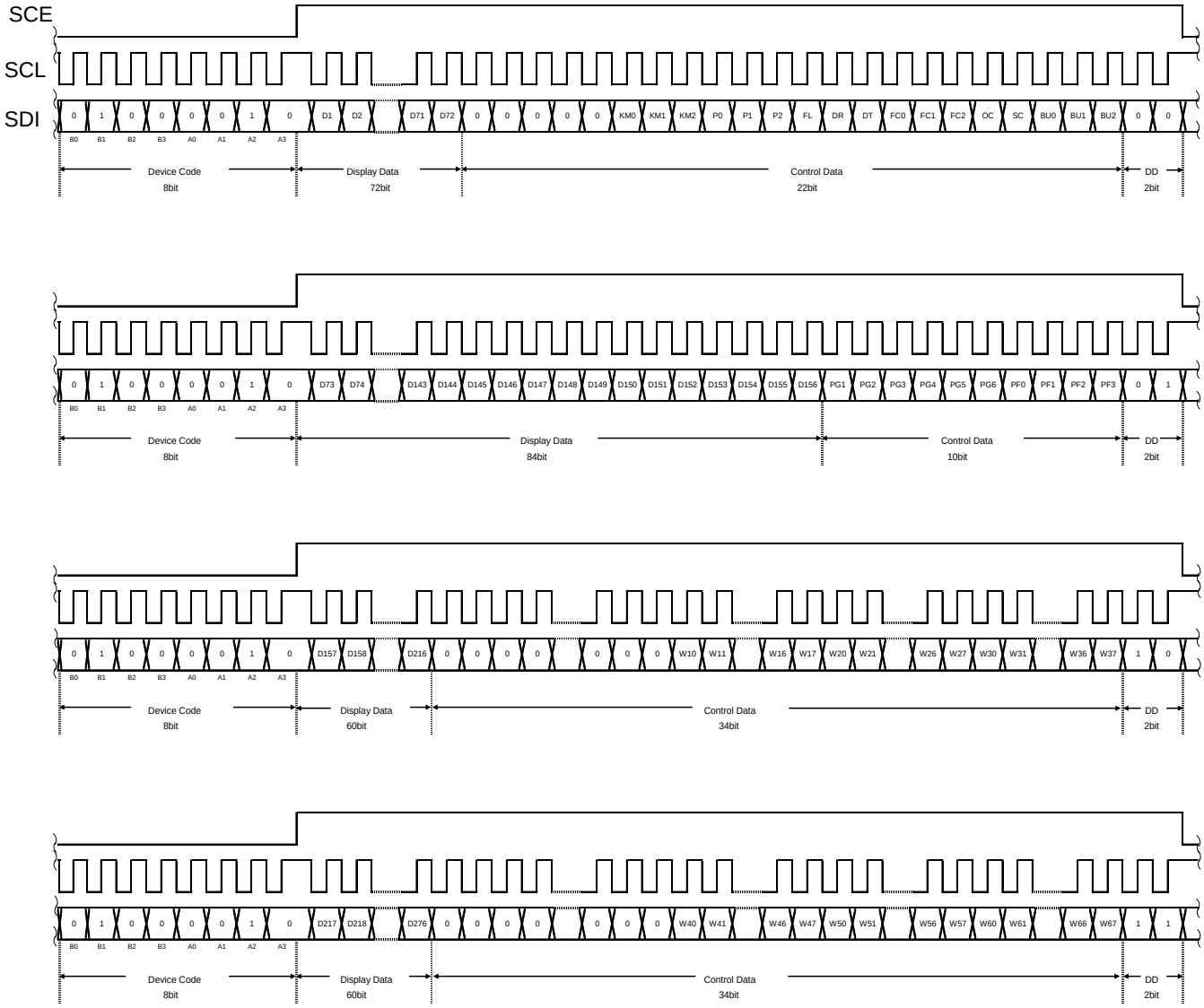


Figure 8. 3-SPI Data Transfer Format

Device code ---------- “42H”
D1 to D276 ---------- Display data
KM0 to KM2 ---------- Key Scan output pin / Segment output pin switching control data
P0 to P2 ---------- Segment / PWM / General-purpose output pin switching control data
FL ---------- Line Inversion or Frame Inversion switching control data
DR ---------- 1/3 Bias drive or 1/2 Bias drive switching control data
DT ---------- 1/4 Duty drive or 1/3 Duty drive switching control data
FC0 to FC2 ---------- Common / Segment output waveform frame frequency switching control data
OC ---------- Internal oscillator operating mode / External clock operating mode switching control data
SC ---------- Segment on/off control data
BU0 to BU2 ---------- Normal mode / power-saving mode control data
PG1 to PG6 ---------- PWM / General-purpose output control data
PF0 to PF3 ---------- PWM output waveform frame frequency control data
Wn0 to Wn7 (n=1 to 6) ---------- PWM output waveform duty control data
DD---------- Direction data

When it is coincident with device code, BU97520AKV-M capture display data and control data at falling edge of SCE.
So, please transfer the bit number of send display data and control data as specified number in the above figure.
Specified number of bits is 104bit (Device code: 8bit, Display data and Control data: 94bit, DD: 2bit).

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Serial Data Transfer Formats – continued

2. 1/3 Duty

(1) When SCL is stopped at the low level

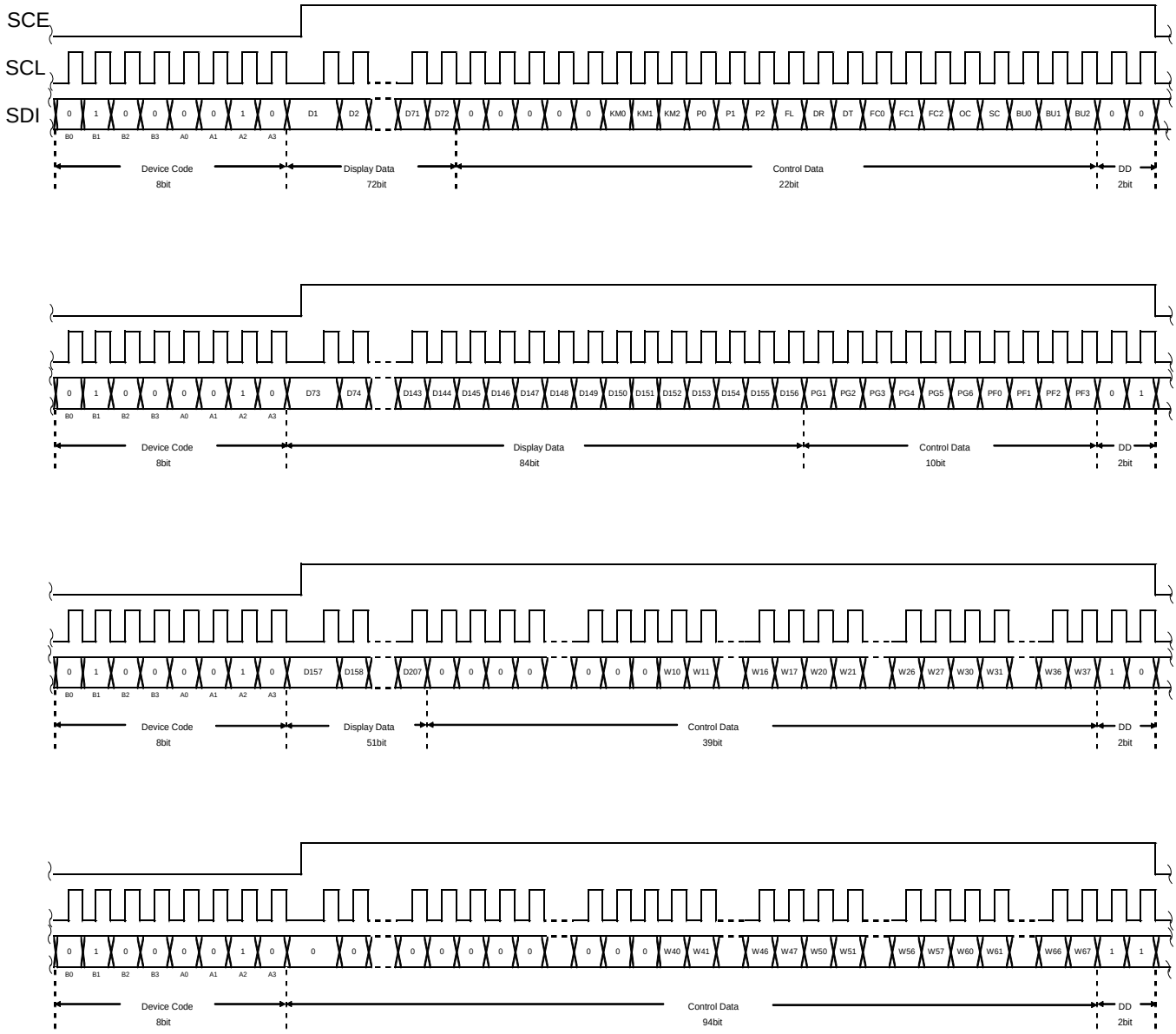


Figure 9. 3-SPI Data Transfer Format

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Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level

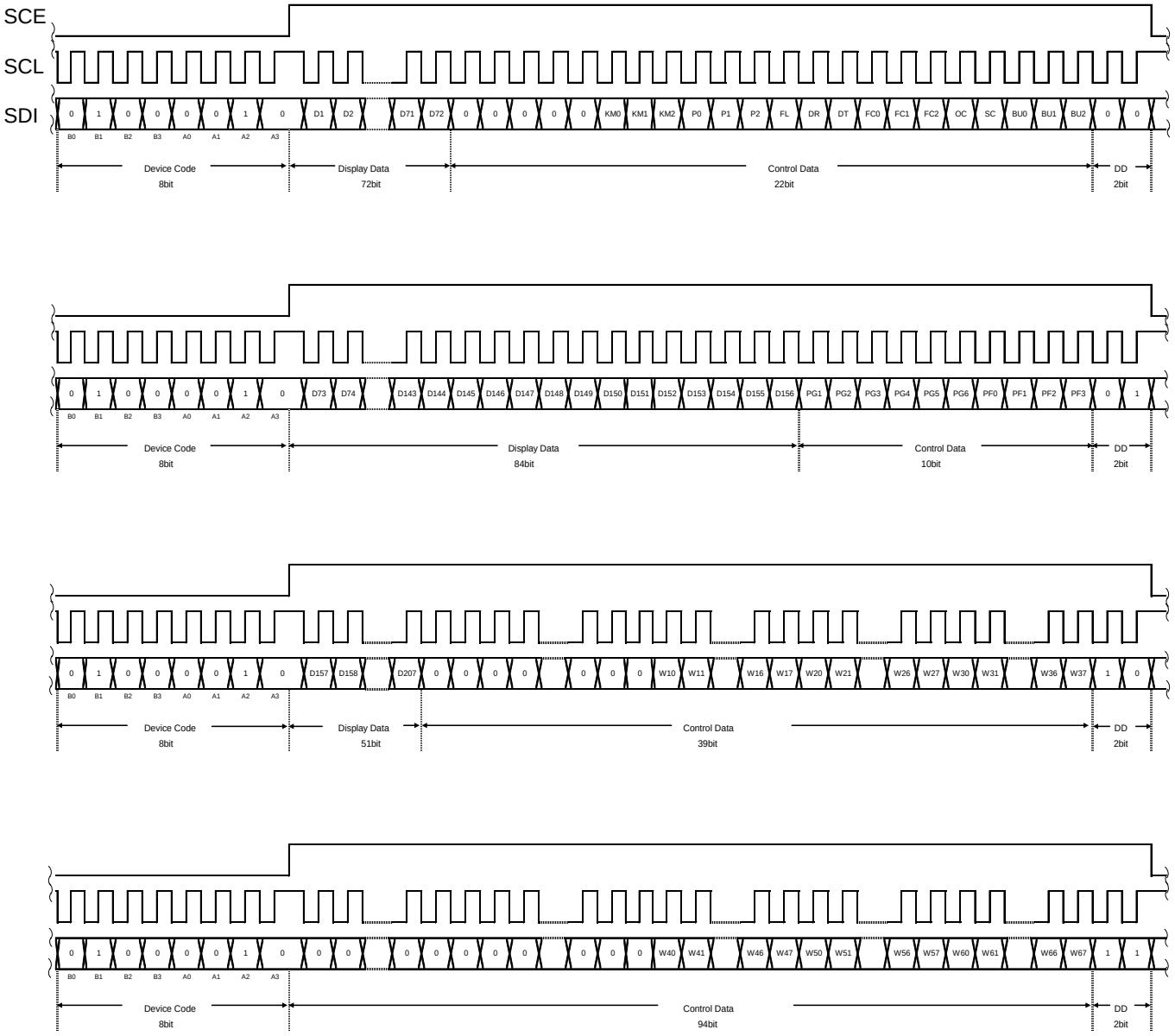


Figure 10. 3-SPI Data Transfer Format

Device code ---------- “42H”
D1 to D276 ---------- Display data
KM0 to KM2 ---------- Key Scan output pin / Segment output pin switching control data
P0 to P2 ---------- Segment / PWM / General-purpose output pin switching control data
FL ---------- Line Inversion or Frame Inversion switching control data
DR ---------- 1/3 Bias drive or 1/2 Bias drive switching control data
DT ---------- 1/4 Duty drive or 1/3 Duty drive switching control data
FC0 to FC2 ---------- Common / Segment output waveform frame frequency switching control data
OC ---------- Internal oscillator operating mode / External clock operating mode switching control data
SC ---------- Segment on/off control data
BU0 to BU2 ---------- Normal mode / power-saving mode control data
PG1 to PG6 ---------- PWM / General-purpose output control data
PF0 to PF3 ---------- PWM output waveform frame frequency control data
Wn0 to Wn7 (n=1 to 6) ---------- PWM output waveform duty control data
DD---------- Direction data

When it is coincident with device code, BU97520AKV-M capture display data and control data at falling edge of SCE.
So, please transfer the bit number of send display data and control data as specified number in the above figure.
Specified number of bits is 104bit (Device code: 8bit, Display data and Control data: 94bit, DD: 2bit).

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Control Data Functions

1. KM0, KM1 and KM2: Key Scan output pin / Segment output pin switching control data

These control data bits switch the functions of the KS1/S56 to KS6/S61 output pins between key scan output and segment output.

KM0	KM1	KM2	Output Pin State						Maximum Number of Input keys	Reset Condition
			KS1/S56	KS2/S57	KS3/S58	KS4/S59	KS5/S60	KS6/S61		
0	0	0	KS1	KS2	KS3	KS4	KS5	KS6	30	-
0	0	1	S56	KS2	KS3	KS4	KS5	KS6	25	-
0	1	0	S56	S57	KS3	KS4	KS5	KS6	20	-
0	1	1	S56	S57	S58	KS4	KS5	KS6	15	-
1	0	0	S56	S57	S58	S59	KS5	KS6	10	-
1	0	1	S56	S57	S58	S59	S60	KS6	5	-
1	1	0	S56	S57	S58	S59	S60	S61	0	-
1	1	1	S56	S57	S58	S59	S60	S61	0	○

2. P0, P1 and P2: Segment / PWM / General-purpose output pin switching control data

These control data bits are used to select the function of the S1/P1/G1 to S6/P6/G6 output pins (Segment Output Pins or PWM Output Pins or General-purpose Output Pins).

P0	P1	P2	S1/P1/G1	S2/P2/G2	S3/P3/G3	S4/P4/G4	S5/P5/G5	S6/P6/G6	Reset Condition
0	0	0	S1	S2	S3	S4	S5	S6	○
0	0	1	P1/G1	S2	S3	S4	S5	S6	-
0	1	0	P1/G1	P2/G2	S3	S4	S5	S6	-
0	1	1	P1/G1	P2/G2	P3/G3	S4	S5	S6	-
1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	S5	S6	-
1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	S6	-
1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	-
1	1	1	S1	S2	S3	S4	S5	S6	-

PWM output or General-purpose output pin is selected by PGx (x=1 to 6) control data bit.

When the General-purpose Output Pin Function is selected, the correspondence between the output pins and the respective display data is given in the table below.

Output Pins	Corresponding Display Data	
	1/4 Duty Mode	1/3 Duty Mode
S1/P1/G1	D1	D1
S2/P2/G2	D5	D4
S3/P3/G3	D9	D7
S4/P4/G4	D13	D10
S5/P5/G5	D17	D13
S6/P6/G6	D21	D16

When the General-purpose Output Pin Function is selected, the respective output pin outputs a “HIGH” level when its corresponding display data is set to “1”. Likewise, it will output a “LOW” level, if its corresponding display data is set to “0”. For example, S4/P4/G4 is used as a General-purpose Output Pin in case of 1/4 Duty, if its corresponding display data D13 is set to “1”, then S4/P4/G4 will output “HIGH(VDD)” level. Likewise, if D13 is set to “0”, then S4/P4/G4 will output “LOW(VSS)” level.

3. DR: 1/3 Bias drive or 1/2 Bias drive switching control data

This control data bit selects either 1/3 Bias drive or 1/2 Bias drive.

DR	Bias Drive Scheme	Reset Condition
0	1/3 Bias drive	○
1	1/2 Bias drive	-

4. FL: Line Inversion or Frame Inversion switching control data

This control data bit selects either Line Inversion or Frame Inversion.

FL	Inversion Setting	Reset Condition
0	Line	○
1	Frame	-

Typically, when driving large capacitance LCD, Line inversion will increase the influence of crosstalk.
Regarding driving waveform, refer to LCD Driving waveform.

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Control Data Functions – continued

5. DT: 1/4 Duty drive or 1/3 Duty drive switching control data

This control data bit selects either 1/4 Duty drive or 1/3 Duty drive.

DT	Duty Drive Scheme	Reset Condition
0	1/4 Duty drive	○
1	1/3 Duty drive	-

6. FC0, FC1 and FC2: Common / Segment output waveform frame frequency switching control data

These control data bits set the display frame frequency.

FC0	FC1	FC2	Display Frame Frequency fo(Hz)	Reset Condition
0	0	0	f_{OSC}*(Note)*/12288	○
0	0	1	f_{OSC}/10752	-
0	1	0	f_{OSC}/9216	-
0	1	1	f_{OSC}/7680	-
1	0	0	f_{OSC}/6144	-
1	0	1	f_{OSC}/4608	-
1	1	0	f_{OSC}/3840	-
1	1	1	f_{OSC}/3072	-

(Note) f_{OSC}: Internal oscillation frequency (600kHz Typ)

7. OC: Internal oscillator operating mode / External clock operating mode switching control data

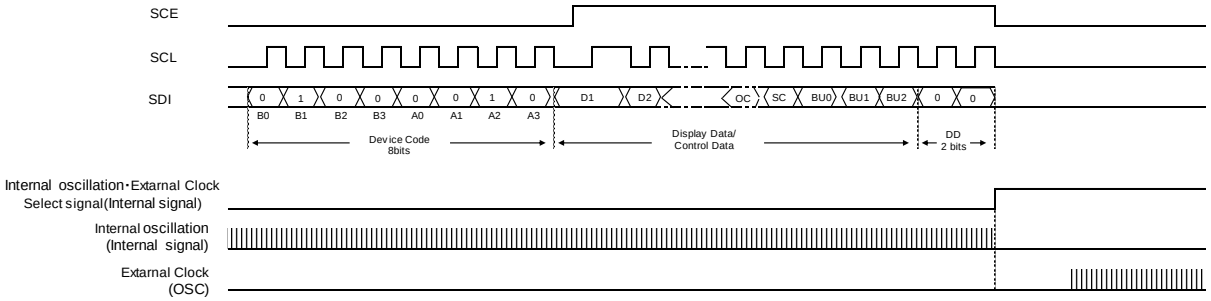
This control data bit selects the oscillation mode.

OC	Operating Mode	In/Out Pin(OSC/S69) Status	Reset Condition
0	Internal oscillator	S69 (segment output)	○
1	External Clock	OSC (clock input)	-

<External Clock input timing function>

Internal oscillation / external clock select signal behavior is below.

Please input external clock after serial data sending.



8. SC: Segment on/off control data

This control data bit controls the on/off state of the segments.

SC	Display State	Reset Condition
0	On	-
1	Off	○

Note that when the segments are turned off by setting SC to “1”, the segments are turned off by outputting segment off waveforms from the segment output pins.

9. BU, BU1 and BU2: Normal mode / power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

BU0	BU1	BU2	Mode	OSC Oscillator	Segment Outputs Common Outputs	Output Pin States During Key Scan Standby						Reset Condition
						KS1	KS2	KS3	KS4	KS5	KS6	
0	0	0	Normal	Operating	Operating	H	H	H	H	H	H	-
0	0	1	Power-saving	Stopped	Low(VSS)	L	L	L	L	L	H	-
0	1	0				L	L	L	L	H	H	-
0	1	1				L	L	L	H	H	H	-
1	0	0				L	L	H	H	H	H	-
1	0	1				L	H	H	H	H	H	-
1	1	0				H	H	H	H	H	H	-
1	1	1				H	H	H	H	H	H	○

Power-saving mode status: S1/P1/G1 to S6/P6/G6 = active only General-purpose output
S7 to S69 = low(VSS)
COM1 to COM4 = low(VSS)
Stop the LCD drive bias voltage generation circuit
Stop the Internal oscillation circuit
However, serial data transfer is possible.

Regarding the details of the INHb pin and the control of each output, refer to “INHb Pin and Display Control”.

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Control Data Functions – continued

10. PG1, PG2, PG3, PG4, PG5 and PG6: PWM / General-purpose output control data

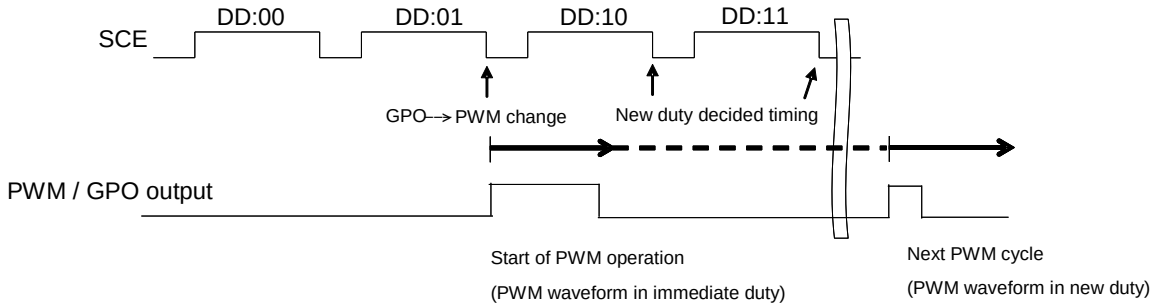
This control data bit select either PWM output or General-purpose output of Sx/Px/Gx pins.(x=1 to 6)

PGx(x=1 to 6)	Mode	Reset Condition
0	PWM output	○
1	General-purpose output	-

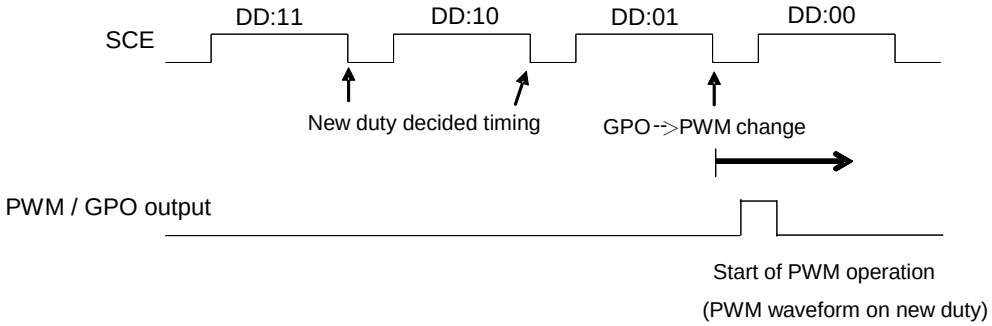
<PWM<->GPO Changing function>

Normal behavior of changing GPO to PWM is below.

- PWM operation is started by command import timing of DD:01 during GPO → PWM change.
- Please take care of reflect timing of new duty setting of DD:10 and DD:11 is from the next PWM.



In order to avoid this operation, please input commands in reverse as below.



11. PF0, PF1, PF2 and PF3: PWM output waveform frame frequency control data

These control data bits set the frame frequency for PWM output waveforms.

PF0	PF1	PF2	PF3	PWM output Frame Frequency fp(Hz)	Reset Condition
0	0	0	0	$f_{osc}/4096$	○
0	0	0	1	$f_{osc}/3840$	-
0	0	1	0	$f_{osc}/3584$	-
0	0	1	1	$f_{osc}/3328$	-
0	1	0	0	$f_{osc}/3072$	-
0	1	0	1	$f_{osc}/2816$	-
0	1	1	0	$f_{osc}/2560$	-
0	1	1	1	$f_{osc}/2304$	-
1	0	0	0	$f_{osc}/2048$	-
1	0	0	1	$f_{osc}/1792$	-
1	0	1	0	$f_{osc}/1536$	-
1	0	1	1	$f_{osc}/1280$	-
1	1	0	0	$f_{osc}/1024$	-
1	1	0	1	$f_{osc}/768$	-
1	1	1	0	$f_{osc}/512$	-
1	1	1	1	$f_{osc}/256$	-

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Control Data Functions – continued

12. W10 to W17[(Note)], W20 to W27, W30 to W37, W40 to W47, W50 to W57 and W60 to W67: PWM output waveform duty control data.
These control data bits set the high level pulse width for PWM output waveforms.

N = 1 to 6, Tp = 1/fp

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Wn6	Wn7	PWM Duty	Reset Condition
0	0	0	0	0	0	0	0	(1/256) x Tp	○
0	0	0	0	0	0	0	1	(2/256) x Tp	-
0	0	0	0	0	0	1	0	(3/256) x Tp	-
0	0	0	0	0	0	1	1	(4/256) x Tp	-
0	0	0	0	0	1	0	0	(5/256) x Tp	-
0	0	0	0	0	1	0	1	(6/256) x Tp	-
0	0	0	0	0	1	1	0	(7/256) x Tp	-
0	0	0	0	0	1	1	1	(8/256) x Tp	-
0	0	0	0	1	0	0	0	(9/256) x Tp	-
0	0	0	0	1	0	0	1	(10/256) x Tp	-
0	0	0	0	1	0	1	0	(11/256) x Tp	-
0	0	0	0	1	0	1	1	(12/256) x Tp	-
0	0	0	0	1	1	0	0	(13/256) x Tp	-
0	0	0	0	1	1	0	1	(14/256) x Tp	-
0	0	0	0	1	1	1	0	(15/256) x Tp	-
0	0	0	0	1	1	1	1	(16/256) x Tp	-
0	0	0	1	0	0	0	0	(17/256) x Tp	-
0	0	0	1	0	0	0	1	(18/256) x Tp	-
0	0	0	1	0	0	1	0	(19/256) x Tp	-
0	0	0	1	0	0	1	1	(20/256) x Tp	-
0	0	0	1	0	1	0	0	(21/256) x Tp	-
0	0	0	1	0	1	0	1	(22/256) x Tp	-
0	0	0	1	0	1	1	0	(23/256) x Tp	-
0	0	0	1	0	1	1	1	(24/256) x Tp	-
0	0	0	1	1	0	0	0	(25/256) x Tp	-
0	0	0	1	1	0	0	1	(26/256) x Tp	-
0	0	0	1	1	0	1	0	(27/256) x Tp	-
1	1	1	0	0	1	0	1	(230/256) x Tp	-
1	1	1	0	0	1	1	0	(231/256) x Tp	-
1	1	1	0	0	1	1	1	(232/256) x Tp	-
1	1	1	0	1	0	0	0	(233/256) x Tp	-
1	1	1	0	1	0	0	1	(234/256) x Tp	-
1	1	1	0	1	0	1	0	(235/256) x Tp	-
1	1	1	0	1	0	1	1	(236/256) x Tp	-
1	1	1	0	1	1	0	0	(237/256) x Tp	-
1	1	1	0	1	1	0	1	(238/256) x Tp	-
1	1	1	0	1	1	1	0	(239/256) x Tp	-
1	1	1	0	1	1	1	1	(240/256) x Tp	-
1	1	1	1	0	0	0	0	(241/256) x Tp	-
1	1	1	1	0	0	0	1	(242/256) x Tp	-
1	1	1	1	0	0	1	0	(243/256) x Tp	-
1	1	1	1	0	0	1	1	(244/256) x Tp	-
1	1	1	1	0	1	0	0	(245/256) x Tp	-
1	1	1	1	0	1	0	1	(246/256) x Tp	-
1	1	1	1	0	1	1	0	(247/256) x Tp	-
1	1	1	1	0	1	1	1	(248/256) x Tp	-
1	1	1	1	1	0	0	0	(249/256) x Tp	-
1	1	1	1	1	0	0	1	(250/256) x Tp	-
1	1	1	1	1	0	1	0	(251/256) x Tp	-
1	1	1	1	1	0	1	1	(252/256) x Tp	-
1	1	1	1	1	1	0	0	(253/256) x Tp	-
1	1	1	1	1	1	0	1	(254/256) x Tp	-
1	1	1	1	1	1	1	0	(255/256) x Tp	-
1	1	1	1	1	1	1	1	(256/256) x Tp	-

(Note): W10 to W17:S1/P1/G1 PWM duty data
W20 to W27:S2/P2/G2 PWM duty data
W30 to W37:S3/P3/G3 PWM duty data
W40 to W47:S4/P4/G4 PWM duty data
W50 to W57:S5/P5/G5 PWM duty data
W60 to W67:S6/P6/G6 PWM duty data.

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Display Data and Output Pin Correspondence

1. 1/4 Duty

Output Pin(Note)	COM1	COM2	COM3	COM4
S1/P1/G1	D1	D2	D3	D4
S2/P2/G2	D5	D6	D7	D8
S3/P3/G3	D9	D10	D11	D12
S4/P4/G4	D13	D14	D15	D16
S5/P5/G5	D17	D18	D19	D20
S6/P6/G6	D21	D22	D23	D24
S7	D25	D26	D27	D28
S8	D29	D30	D31	D32
S9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204
S52	D205	D206	D207	D208
S53	D209	D210	D211	D212
S54	D213	D214	D215	D216
S55	D217	D218	D219	D220
S56	D221	D222	D223	D224
S57	D225	D226	D227	D228
S58	D229	D230	D231	D232
S59	D233	D234	D235	D236
S60	D237	D238	D239	D240
S61	D241	D242	D243	D244
S62	D245	D246	D247	D248
S63	D249	D250	D251	D252

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Display Data and Output Pin Correspondence – continued

Output Pin*(Note)*	COM1	COM2	COM3	COM4
S64	D253	D254	D255	D256
S65	D257	D258	D259	D260
S66	D261	D262	D263	D264
S67	D265	D266	D267	D268
S68	D269	D270	D271	D272
S69	D273	D274	D275	D276

(Note) The Segment Output Pin function is assumed to be selected for the output pins – S1/P1/G1 to S6/P6/G6.

To illustrate further, the states of the S21 output pin is given in the table below.

Display Data				State of S21 Output Pin
D81	D82	D83	D84	
0	0	0	0	LCD Segments corresponding to COM1 to COM4 are OFF.
0	0	0	1	LCD Segment corresponding to COM4 is ON.
0	0	1	0	LCD Segment corresponding to COM3 is ON.
0	0	1	1	LCD Segments corresponding to COM3 and COM4 are ON.
0	1	0	0	LCD Segment corresponding to COM2 is ON.
0	1	0	1	LCD Segments corresponding to COM2 and COM4 are ON.
0	1	1	0	LCD Segments corresponding to COM2 and COM3 are ON.
0	1	1	1	LCD Segments corresponding to COM2, COM3 and COM4 are ON.
1	0	0	0	LCD Segment corresponding to COM1 is ON.
1	0	0	1	LCD Segments corresponding to COM1 and COM4 are ON.
1	0	1	0	LCD Segments corresponding to COM1 and COM3 are ON.
1	0	1	1	LCD Segments corresponding to COM1, COM3 and COM4 are ON.
1	1	0	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	0	1	LCD Segments corresponding to COM1, COM2, and COM4 are ON.
1	1	1	0	LCD Segments corresponding to COM1, COM2, and COM3 are ON.
1	1	1	1	LCD Segments corresponding to COM1 to COM4 are ON.

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Display Data and Output Pin Correspondence – continued

2. 1/3 Duty

Output Pin(Note)	COM1	COM2	COM3
S1/P1/G1	D1	D2	D3
S2/P2/G2	D4	D5	D6
S3/P3/G3	D7	D8	D9
S4/P4/G4	D10	D11	D12
S5/P5/G5	D13	D14	D15
S6/P6/G6	D16	D17	D18
S7	D19	D20	D21
S8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D85	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156
S53	D157	D158	D159
S54	D160	D161	D162
S55	D163	D164	D165
S56	D166	D167	D168
S57	D169	D170	D171
S58	D172	D173	D174
S59	D175	D176	D177
S60	D178	D179	D180
S61	D181	D182	D183
S62	D184	D185	D186
S63	D187	D188	D189

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Display Data and Output Pin Correspondence – continued

Output Pin*(Note)*	COM1	COM2	COM3
S64	D190	D191	D192
S65	D193	D194	D195
S66	D196	D197	D198
S67	D199	D200	D201
S68	D202	D203	D204
S69	D205	D206	D207

(Note) The Segment Output Pin function is assumed to be selected for the output pins – S1/P1/G1 to S6/P6/G6.

To illustrate further, the states of the S21 output pin is given in the table below.

Display Data			State of S21 Output Pin
D61	D62	D63	
0	0	0	LCD Segments corresponding to COM1, COM2 and COM3 are OFF.
0	0	1	LCD Segment corresponding to COM3 is ON.
0	1	0	LCD Segment corresponding to COM2 is ON.
0	1	1	LCD Segments corresponding to COM2 and COM3 are ON.
1	0	0	LCD Segment corresponding to COM1 is ON.
1	0	1	LCD Segments corresponding to COM1 and COM3 are ON.
1	1	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	1	LCD Segments corresponding to COM1, COM2 and COM3 are ON.

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Serial Data Output

1. When SCL is stopped at the low level*(Note 1)*

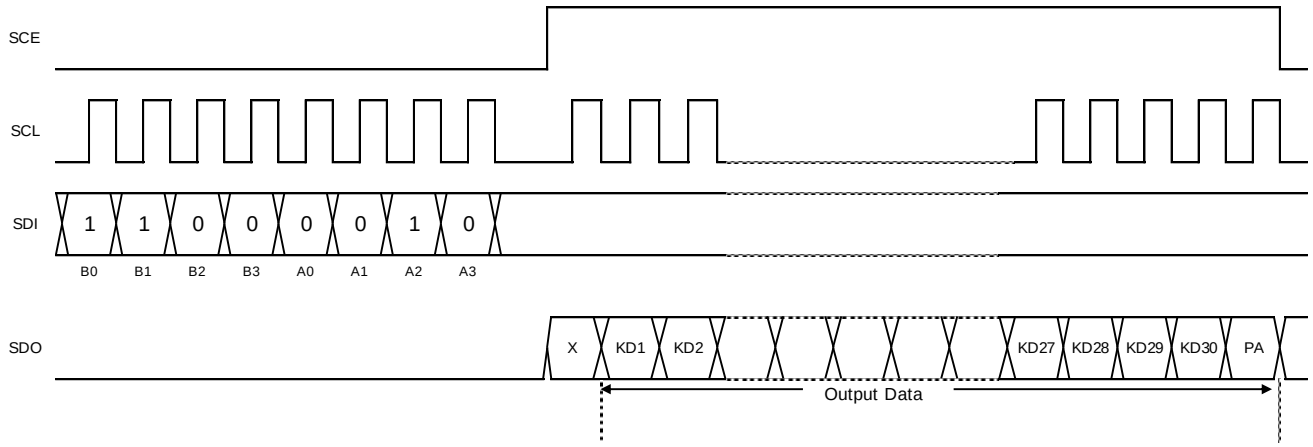


Figure 11. Serial data output format

(Note 1)
1. X=Don't care
2. B0 to B3, A0 to A3: Serial Interface address
3. Serial Interface address: 43H
4. KD1 to KD30: Key data
5. PA: Power-saving acknowledge data
6. If a key data read operation is executed when SDO is high, the read key data (KD1 to KD30) and power-saving acknowledge data (PA) will be invalid.

2. When SCL is stopped at the high level*(Note 2)*

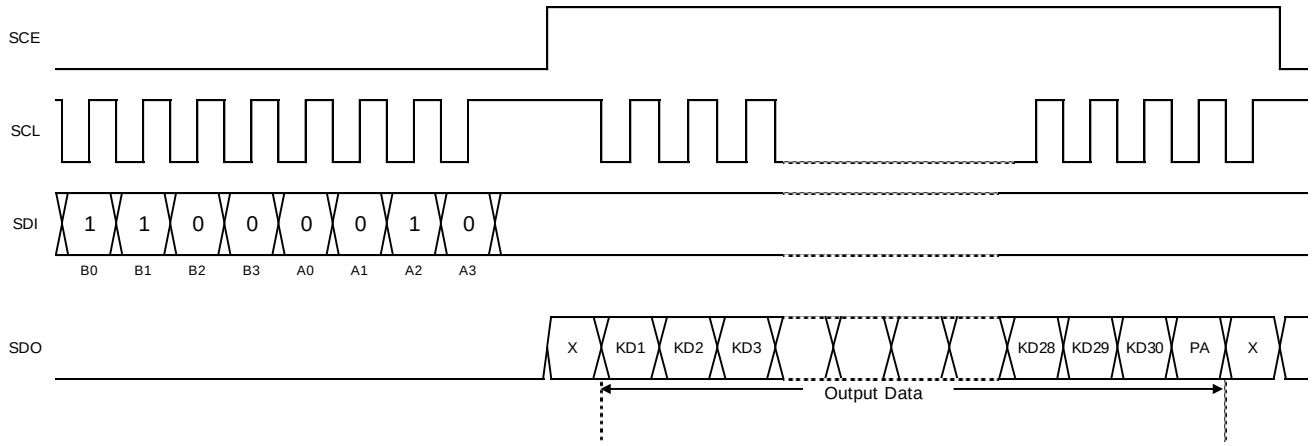


Figure 12. Serial Data Output Format

(Note 2)
1. X=Don't care
2. B0 to B3, A0 to A3: Serial Interface address
3. Serial Interface address: 43H
4. KD1 to KD30: Key data
5. PA: Power-saving acknowledge data
6. If a key data read operation is executed when SDO is high, the read key data (KD1 to KD30) and power-saving acknowledge data (PA) will be invalid.

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Output Data

1. KD1 to KD30: Key Data
   When a key matrix of up to 30 keys is formed from the KS1 to KS6 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

Item	KI1	KI2	KI3	KI4	KI5
KS1	KD1	KD2	KD3	KD4	KD5
KS2	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

2. PA: Power-saving Acknowledge Data
   This output data is set to the state when the key was pressed. In that case SDO will go to the low level. If serial data is input during this period and the mode is set (normal mode or power-saving mode), the IC will be set to that mode. PA is set to 1 in the power-saving mode and to 0 in the normal mode.

Power-saving Mode

Power-saving mode is activated when least one of control data BU0 or BU1 or BU2 is set to 1. All segment and common outputs will go low. The oscillation circuit will stop (It can be restarted by a key press), thus reducing power consumption. This mode can be disabled when control data bits BU0, BU1 and BU2 are all set to 0. However, note that the S1/P1/G1 to S6/P6/G6 outputs can still be used as General-purpose output pins according to the state of the P0 to P2 control data bits, even in power-saving mode. (See Control Data Functions.)

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Key Scan Operation Function

1. Key Scan Timing

The key scan period is 4608T(s). To reliably determine the on/off state of the keys, the BU97520AKV-M scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on SDO) 9840T(s) after starting a key scan. If the key data does not agree and a key was pressed at that point, it scans the keys again. Thus the BU97520AKV-M cannot detect a key press shorter than 9840T(s).

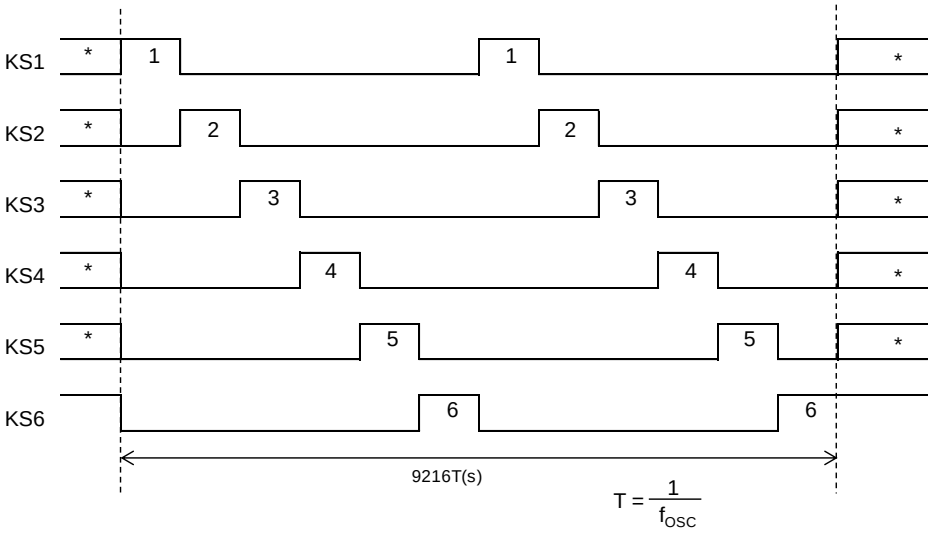


Figure 13. Key Scan Timing*(Note)*

(Note) In power-saving mode the high/low state of these pins is determined by the BU0 to BU2 bits in the control data. Key scan output signals are not output from pins that are set “L”.

2. In Normal Mode

The pins KS1 to KS6 are set “H”.

When a key is pressed a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.

If a key is pressed for longer than 9840T(s) (Where $T=1/f_{OSC}$) the BU97520AKV-M outputs a key data read request (a low level on SDO) to the controller. The controller acknowledges this request and reads the key data. However, if SCE is high during a serial data transfer, SDO will be set “H”.

After the controller reads the key data, the key data read request is cleared (SDO is set high) and the BU97520AKV-M performs another key scan. Also note that SDO, being an open-drain output, requires a pull-up resistor (between 1kΩ and 10kΩ).

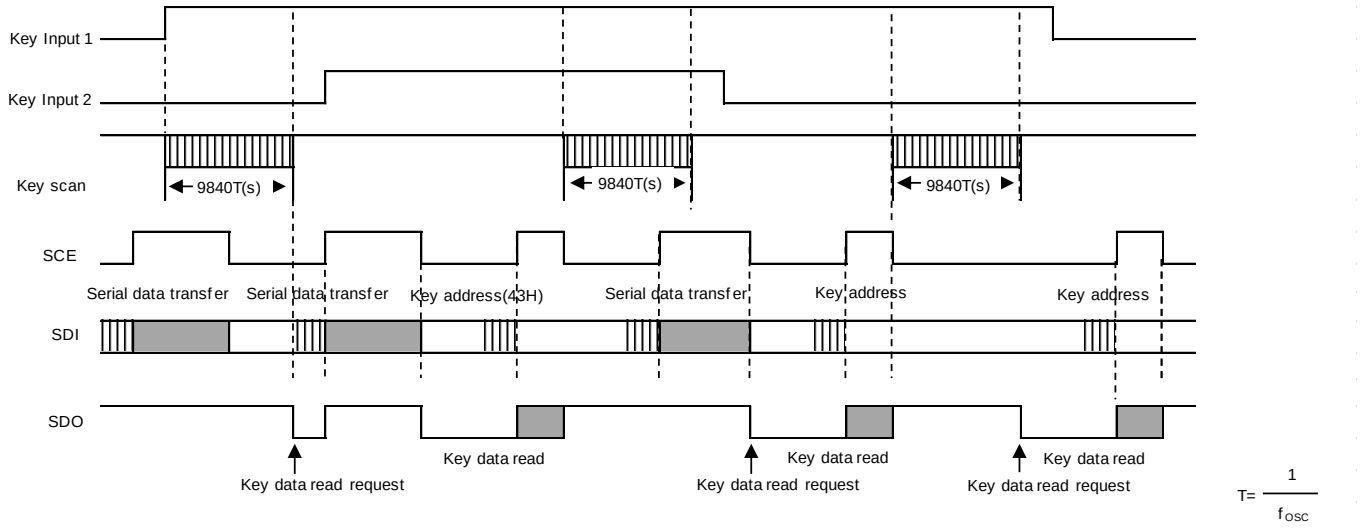


Figure 14. Key Scan Operation In Normal Mode

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Key Scan Operation Function – continued

3. In Power-saving Mode

The pins KS1 to KS6 are set to high or low by the BU0 to BU2 bits in the control data. (See the Control Data Functions for details.)

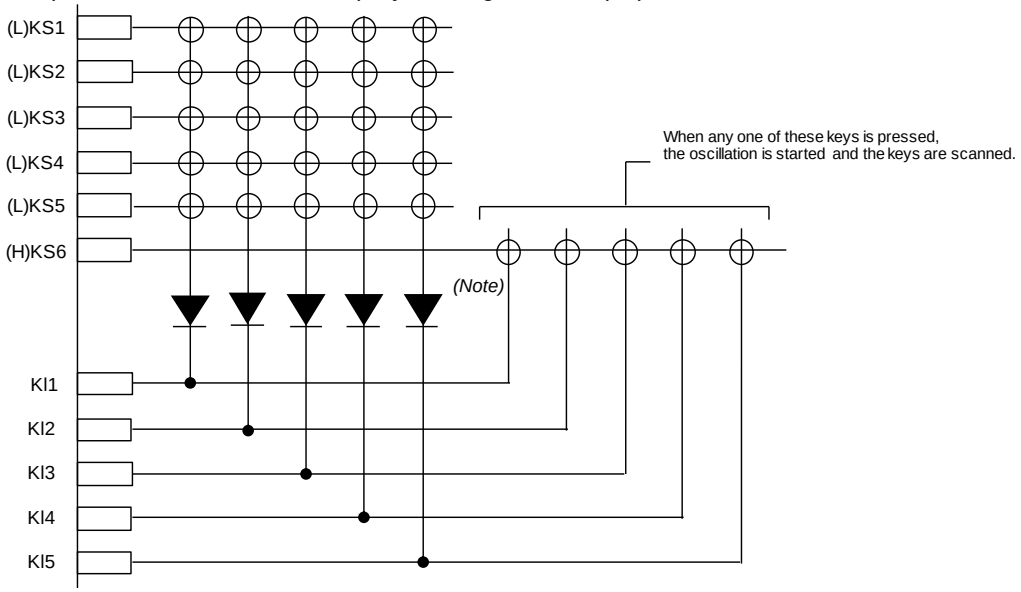
If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, the oscillation is started and a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.

If a key is pressed for longer than 9840T(s)(Where T=1/f_{OSC}) the BU97520AKV-M outputs a key data read request (a low level on SDO) to the controller. The controller acknowledges this request and reads the key data. However, if SCE is high during a serial data transfer, SDO will be set high.

After the controller reads the key data, the key data read request is cleared (SDO is set high) and the BU97520AKV-M performs another key scan. However, this does not clear power-saving mode. Also note that SDO, being an open-drain output, requires a pull-up resistor (between 1kΩ and 10kΩ).

Power-saving mode key scan example

Example: BU0=0, BU1=0, BU2=1 (only KS6 high level output)



(Note)

These diodes are required to reliable recognize multiple key presses on the KS6 line when power-saving mode state with only KS6 high, as in the above example. That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.

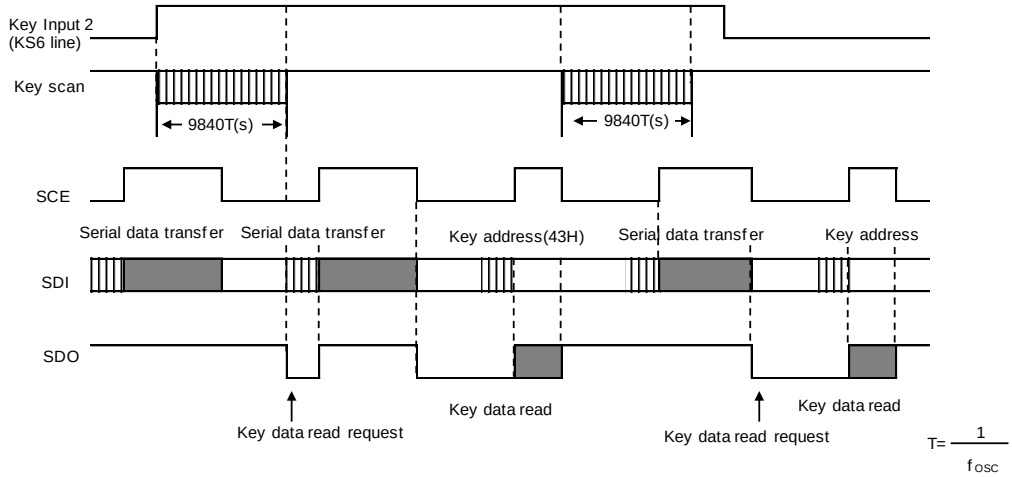


Figure 15. Key Scan Operation In Power-saving Mode

Multiple Key Press

Although the BU97520AKV-M is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines or multiple key presses on the KS1 to KS6 output pin lines, multiple key presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should ignore the key data if the key data contains three or more bits that has a value of “1”.

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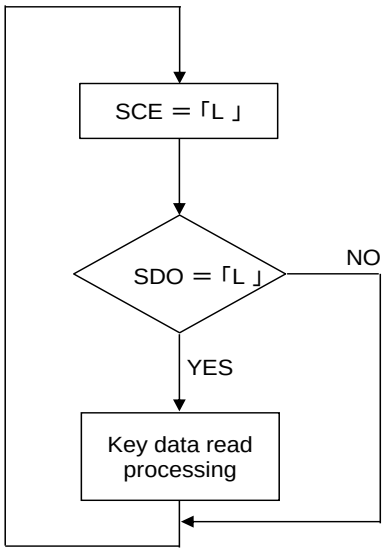
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Controller Key Data Read Technique

When the controller receives a key data read request from BU97520AKV-M, it performs a key data read acquisition operation using either the Timer Based Key Data Acquisition or the Interrupt Based Key Data Acquisition.

1. Timer Based Key Data Acquisition Technique

Under the Timer Based Key Data Acquisition Technique, the controller uses a timer to determine the states of the keys (on or off) and read the key data. Please refer to the flow chart below.



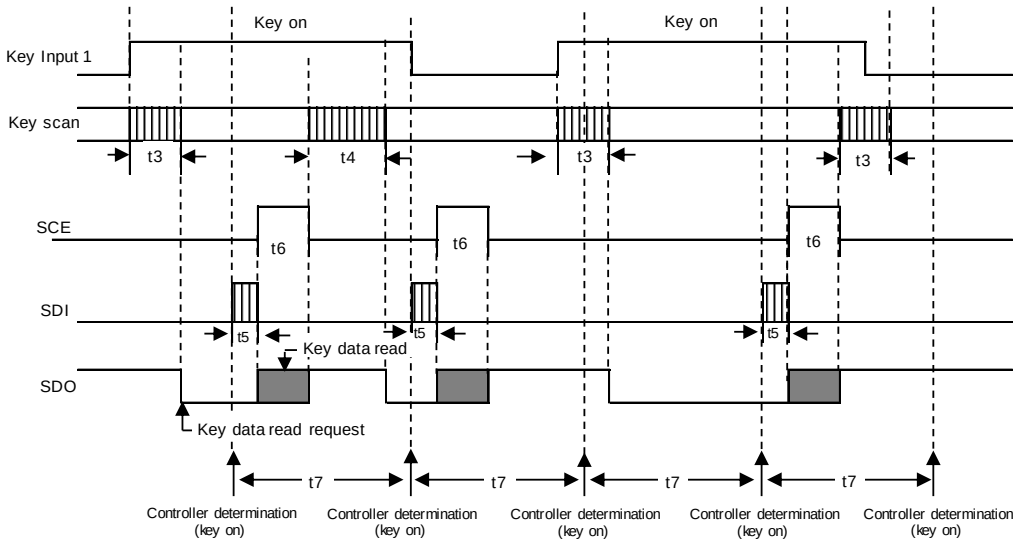
Key data read processing: Refer to "Serial Data Output"

Figure 16. Flowchart

In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the SDO state when SCE is low every t7 period without fail. If SDO is low, the controller recognizes that a key has been pressed and executes the key data read operation.

The period t7 in this technique must satisfy the following condition.
t7>t4+t5+t6

If a key data read operation is executed when SDO is high, the read key data (KD1 to KD30) and power-saving acknowledge data (PA) will be invalid.



t3: Key scan execution time when the key data agreed for two key scans. 9840T(s)
t4: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. 19680T(s) (T = 1 / f_{OSC})
t5: Key address (43H) transfer time
t6: Key data read time

Figure 17. Timer Based Key Data Read Operation

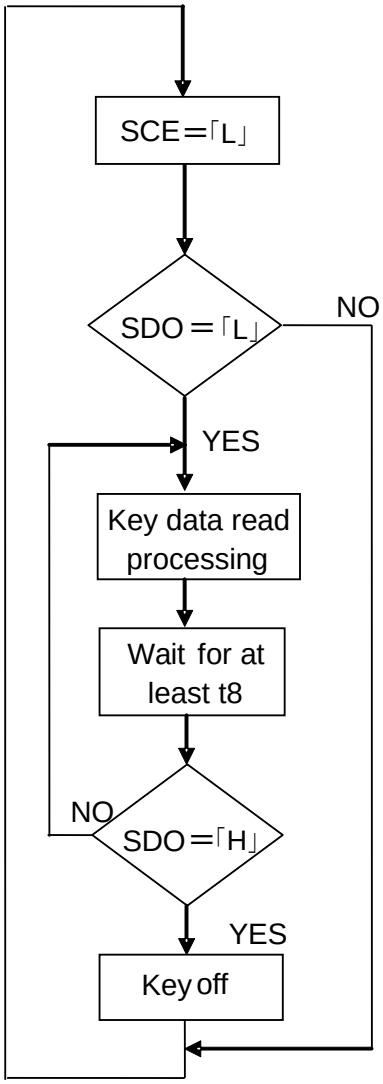
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Controller Key Data Read Technique – continued

2. Interrupt Based Key Data Acquisition Technique

Under the Interrupt Based Key Data Acquisition Technique, the controller uses interrupts to determine the state of the keys (on or off) and read the key data. Please refer to the flow chart diagram below.



Key data read processing: Refer to "Serial Data Output"

Figure 18. Flowchart

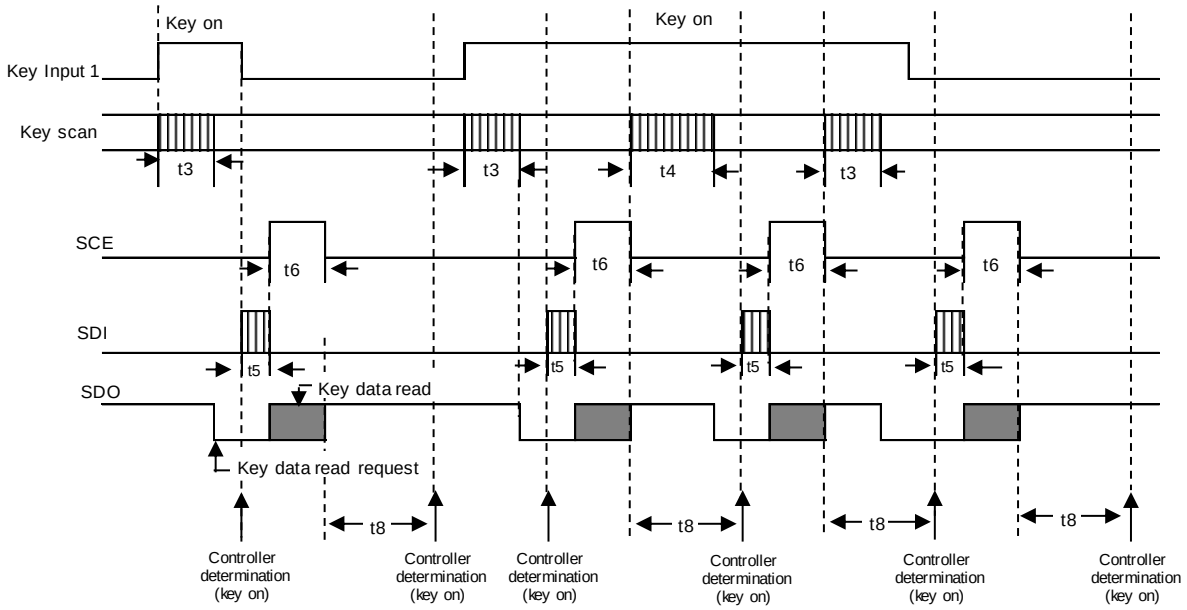
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Controller Key Data Read Technique – continued

In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the SDO state when SCE is low. If SDO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t8 has elapsed by checking the SDO state when SCE is low and reading the key data. The period t8 in this technique must satisfy t8 > t4.

If a key data read operation is executed when SDO is high, the read key data (KD1 to KD30) and power-saving acknowledge data (PA) will be invalid.



t3: Key scan execution time when the key data agreed for two key scans. 9840T(s)
t4: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. 19680T(s) (T = 1 / f_{OSC})
t5: Key address (43H) transfer time
t6: Key data read time

Figure 19. Interrupt Based Key Data Read Operation

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LCD Driving Waveform

1. Line Inversion 1/4 Duty 1/3Bias Drive Scheme

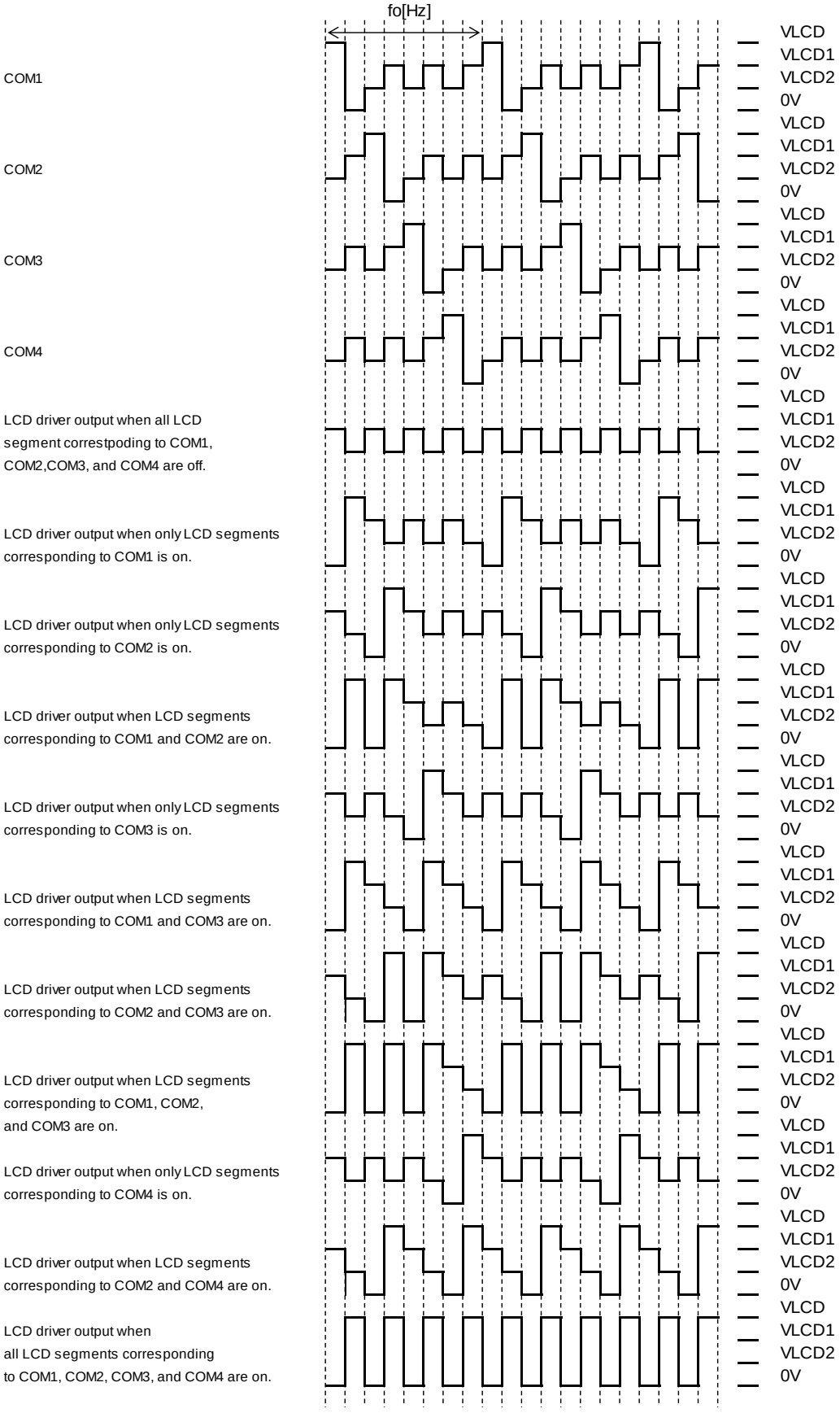


Figure 20. LCD Waveform (1/4 Duty, 1/3 Bias, Line Inversion)

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LCD Driving Waveform – continued

2. Line Inversion 1/4 Duty 1/2 Bias Drive Scheme

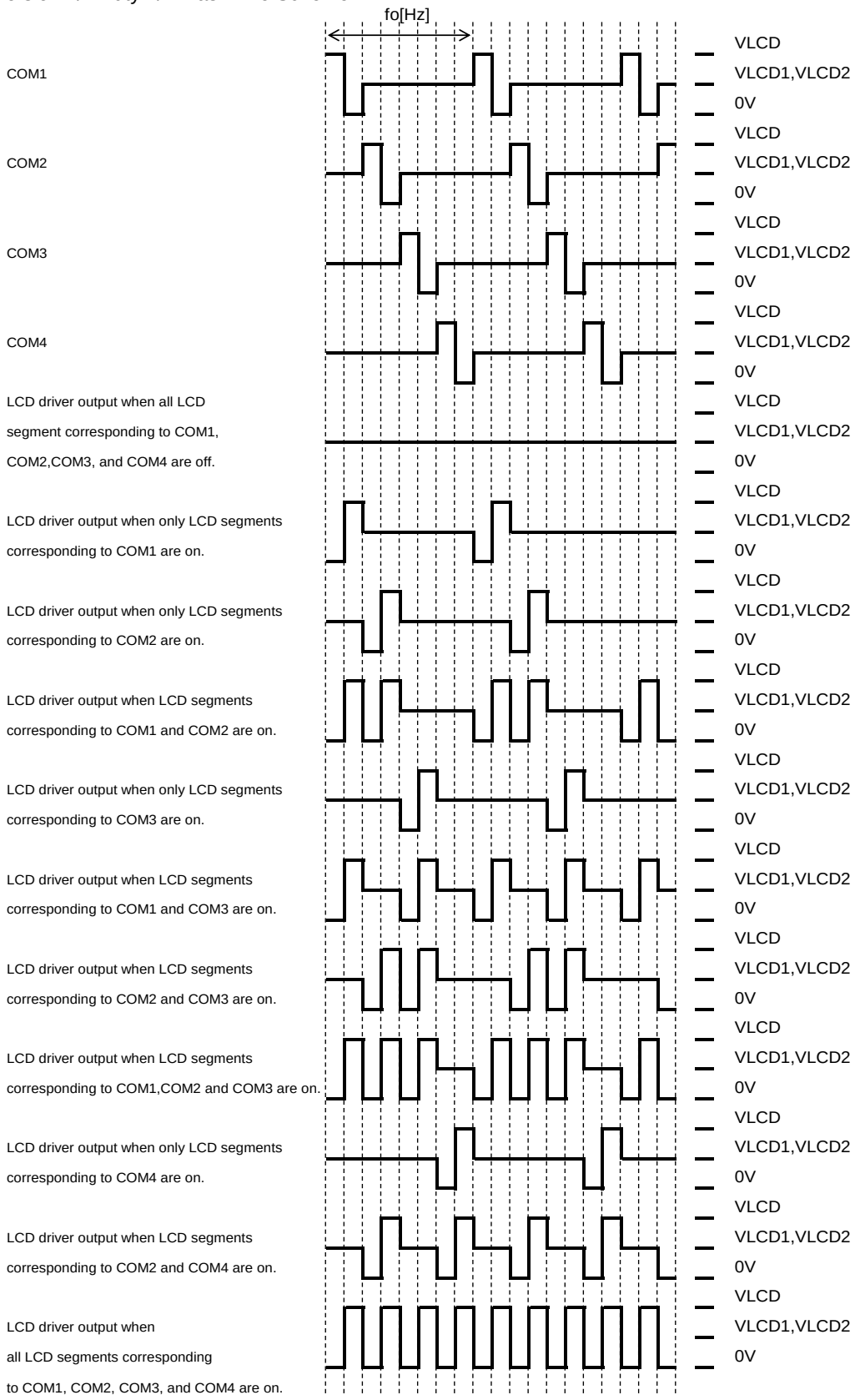


Figure 21. LCD Waveform (1/4 Duty, 1/2 Bias, Line Inversion)

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LCD Driving Waveform – continued

3. Line Inversion 1/3 Duty 1/3 Bias Drive Scheme

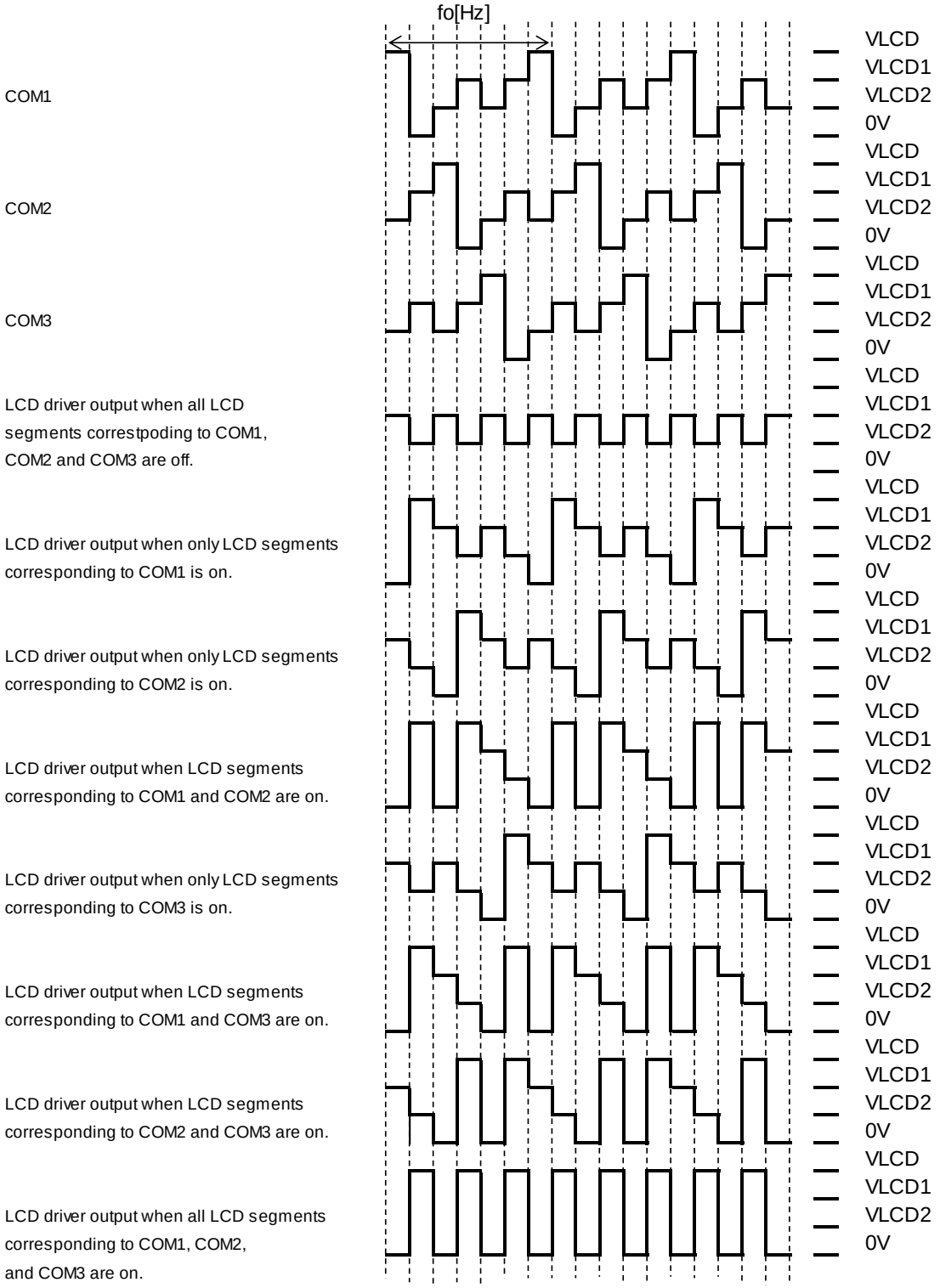


Figure 22. LCD Waveform (1/3 Duty, 1/3 Bias, Line Inversion)*(Note)*

(*Note)* COM4 function is same as COM1 at 1/3 Duty.

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LCD Driving Waveform – continued

4. Line Inversion 1/3 Duty 1/2 Bias Drive Scheme

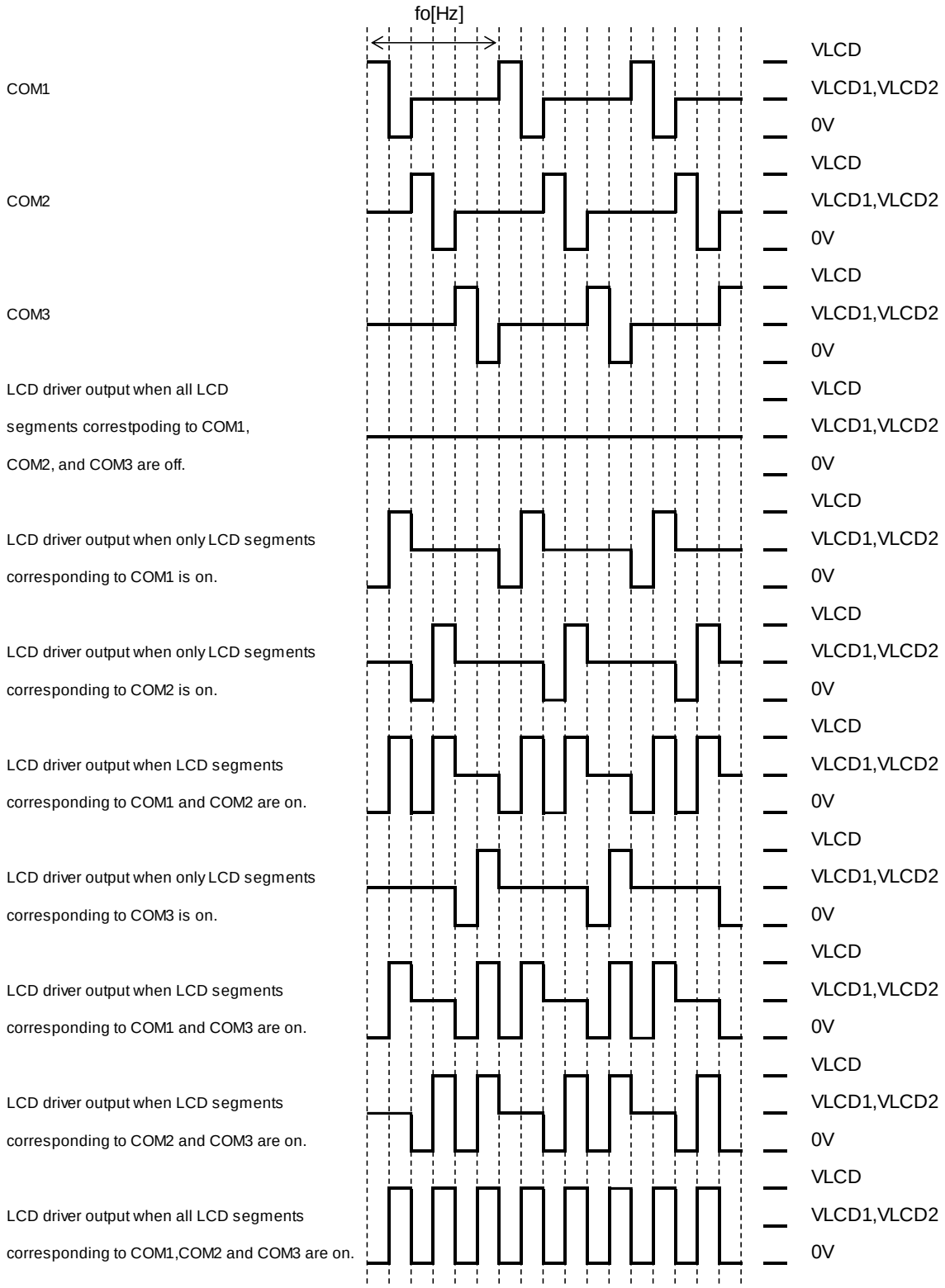


Figure 23. LCD Waveform (1/3 Duty, 1/2 Bias, Line Inversion)*(Note)*

(Note) COM4 function is same as COM1 at 1/3 Duty.

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LCD Driving Waveform – continued

5. Frame Inversion 1/4 Duty 1/3 Bias Drive Scheme

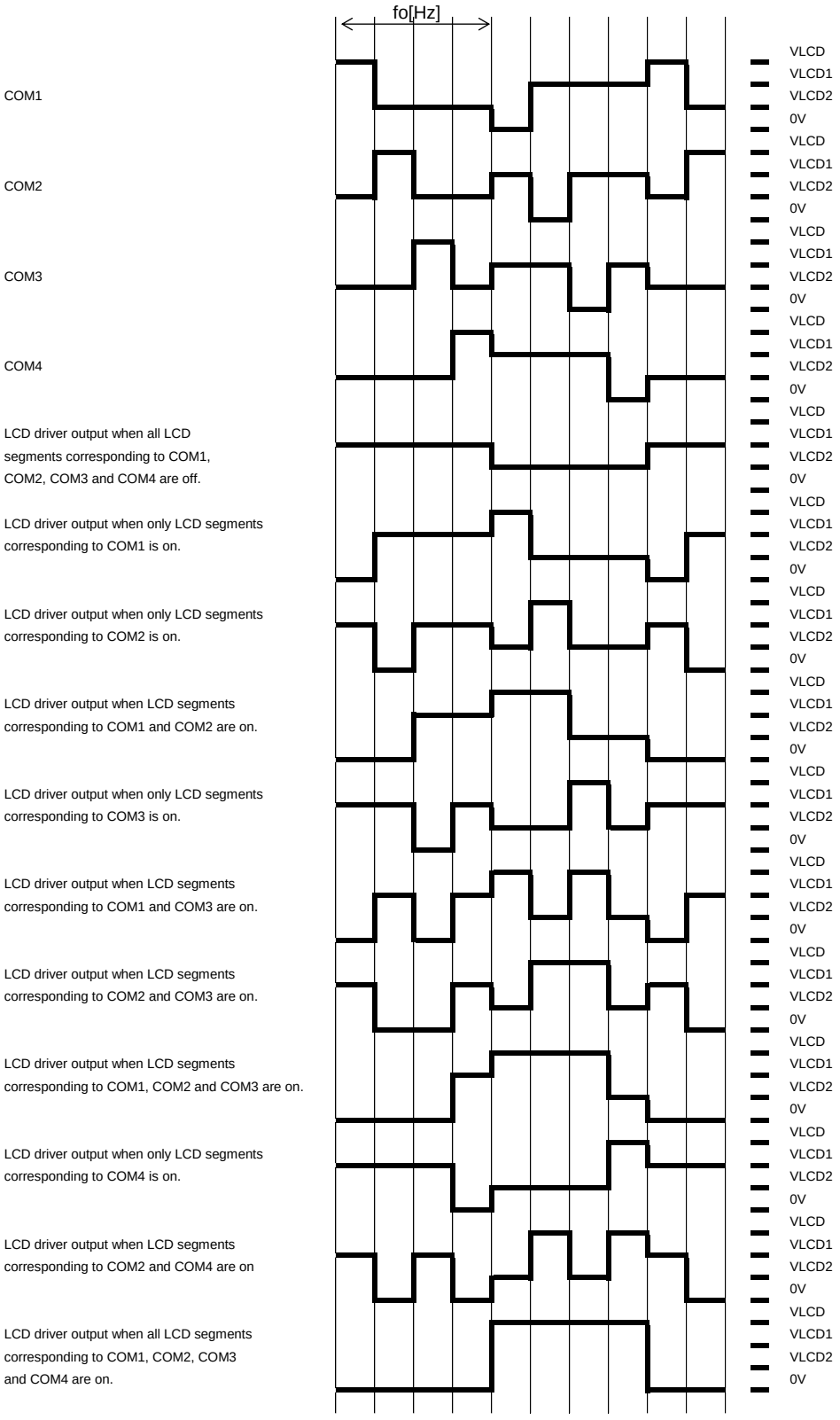


Figure 24. LCD Waveform (1/4 Duty, 1/3 Bias, Frame Inversion)

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LCD Driving Waveform – continued

6. Frame Inversion 1/4 Duty 1/2 Bias Drive Scheme

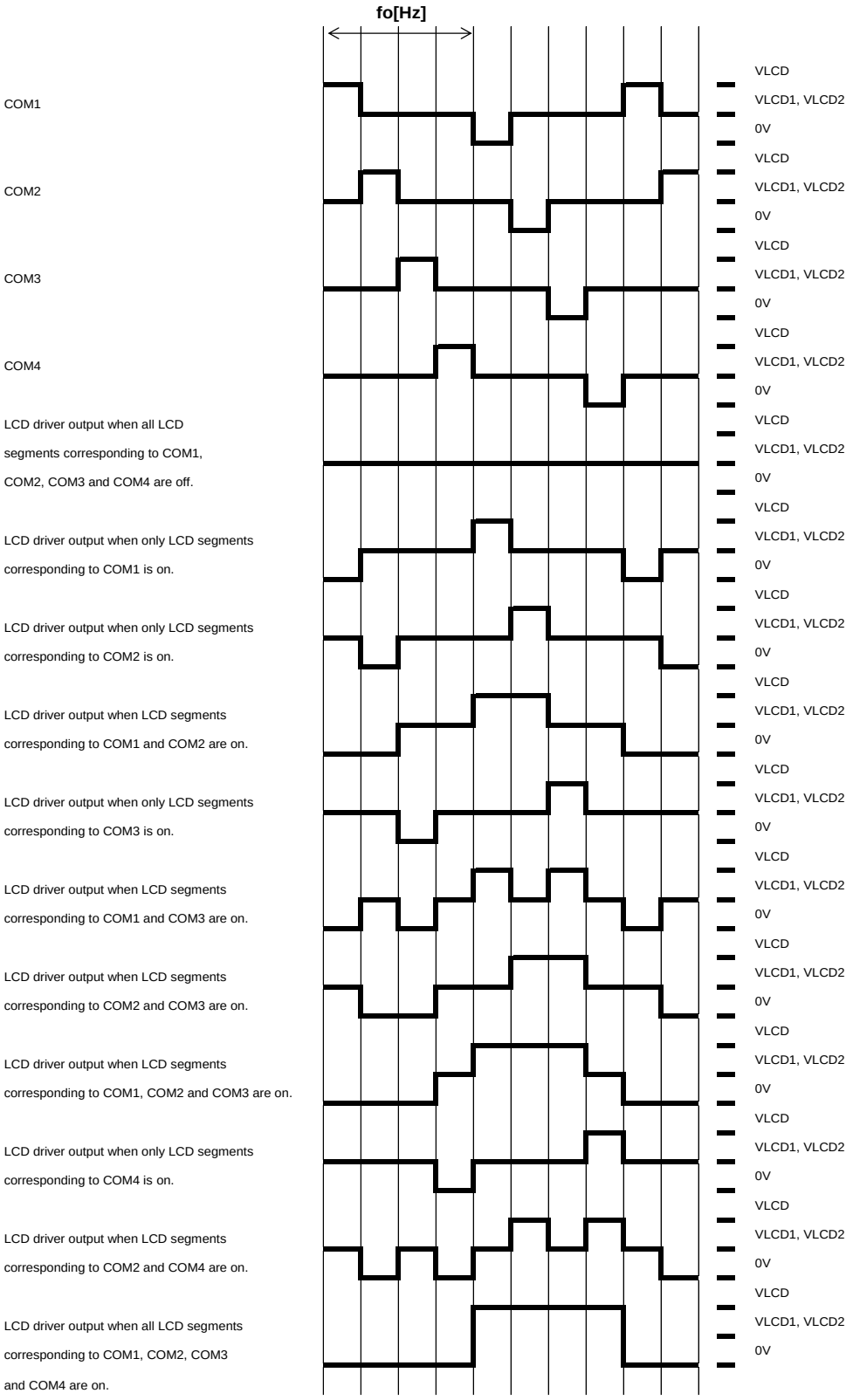


Figure 25. LCD Waveform (1/4 Duty, 1/2 Bias, Frame Inversion)

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LCD Driving Waveform – continued

7. Frame Inversion 1/3 Duty 1/3 Bias Drive Scheme

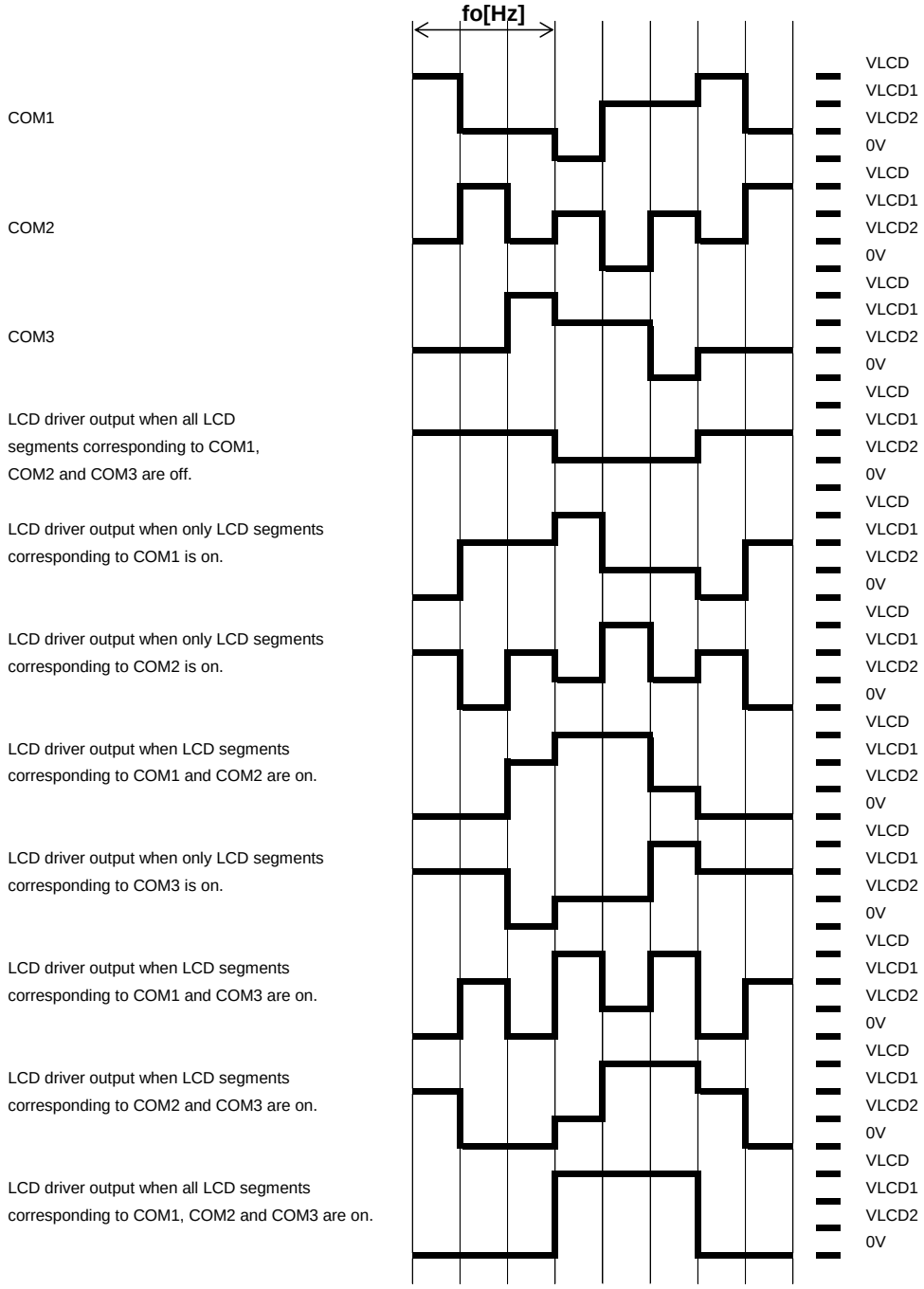


Figure 26. LCD Waveform (1/3 Duty, 1/3 Bias, Frame Inversion)*(Note)*

(Note) COM4 function is same as COM1 at 1/3 Duty.

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LCD Driving Waveform – continued

8. Frame Inversion 1/3 Duty 1/2 Bias Drive Scheme

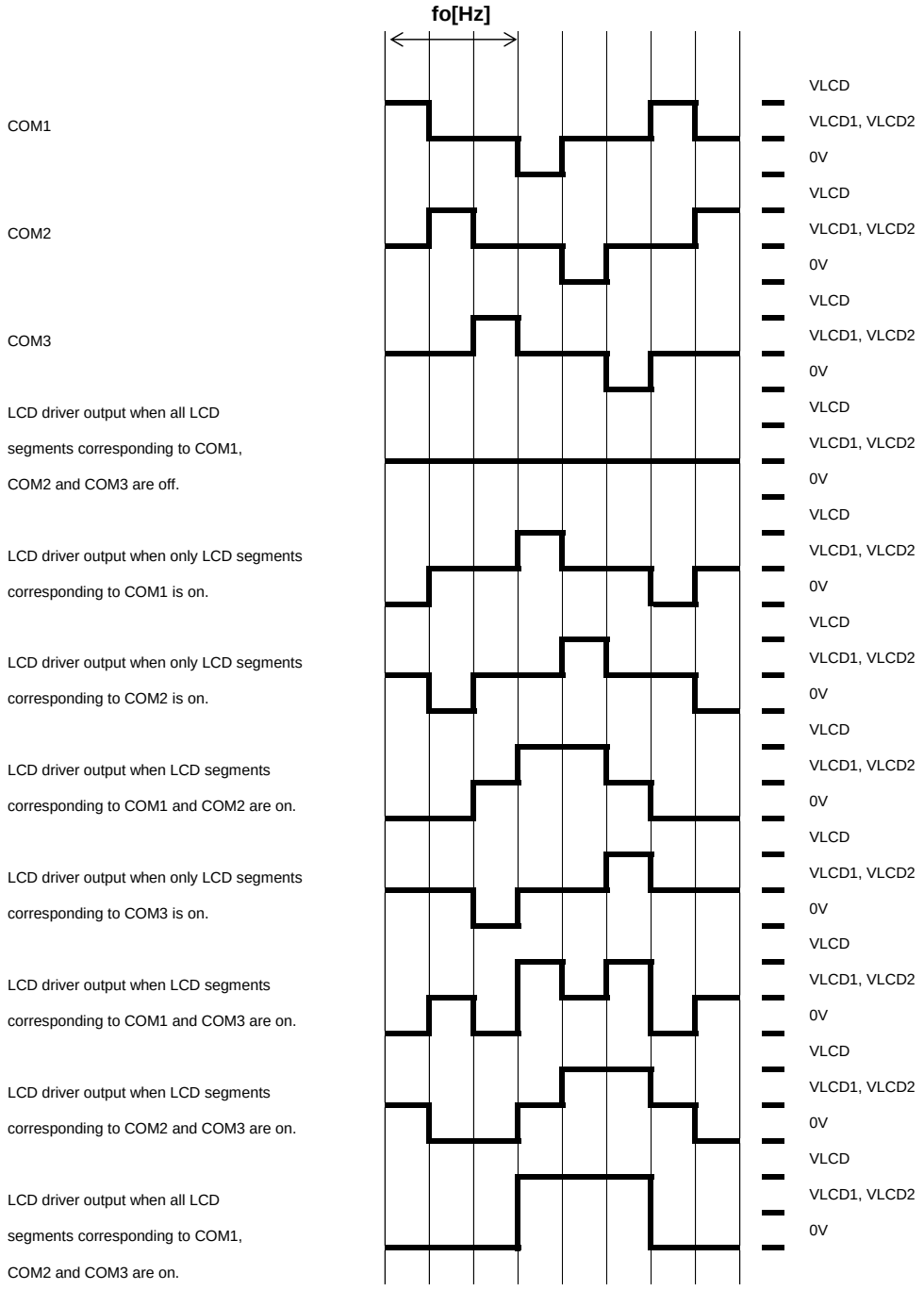


Figure 27. LCD Waveform (1/3 Duty, 1/2 Bias, Frame Inversion)*(Note)*

(Note) COM4 function is same as COM1 at 1/3 Duty.

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INHb Pin and Display Control

The INHb pin operates Display off of LCD.
INHb control depends on set pin function.

Below table shows pin function and control by the INHb pin.

Pin Function	Control	
	INHb = L	INHb = H
SEG/COM	Display forced off	Display on
PWM/GPO	Operation Stop	Operation Available
Key Scan	Available regardless of INHb	
External Clock Input	Available regardless of INHb	

Below table shows pin name and pin state of INHb = L.
Each output state are decided by Control data(P0 to P2, KM0 to KM2, OC)
For the details, please refer to "Control Data Functions".

Pin Name	Pin Function(*Note*) (In case of INHb = L)					
	SEG	COM	PWM	GPO	Keyscan	External Clock Input
S1/P1/G1 to S6/P6/G6	Stop (VSS)	-	Stop (VSS)	Stop (VSS)	-	-
S7 to S55, S67, S68	Stop (VSS)	-	-	-	-	-
KS1/S56 to KS6/S61	Stop (VSS)	-	-	-	Keyscan Output Operation	-
KI1/S62 to KI5/S66	Stop (VSS)	-	-	-	Keyscan Input Operation	-
OSC/S69	Stop (VSS)	-	-	-	-	Clock Input Operation
COM1 to COM4	-	Stop (VSS)	-	-	-	-

(Note) "-" means the pin does not have the function.
For example, S1/P1/G1 to S6/P6/G6 are not set COM, Keyscan and External Clock Input.

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INHb Pin and Display Control- continued

Since the IC internal data (the display data D1 to D276 and the control data) is undefined when power is first applied, applications should set the INHb pin low at the same time as power is applied to turn off the display (This sets the S1/P1/G1 to S6/P6/G6, S7 to S69, COM1 to COM4 to the VSS level.) and during this period send serial data from the controller. The controller should then set the INHb pin high after the data transfer has completed. This procedure prevents meaningless displays at power on.

1. 1/4 Duty

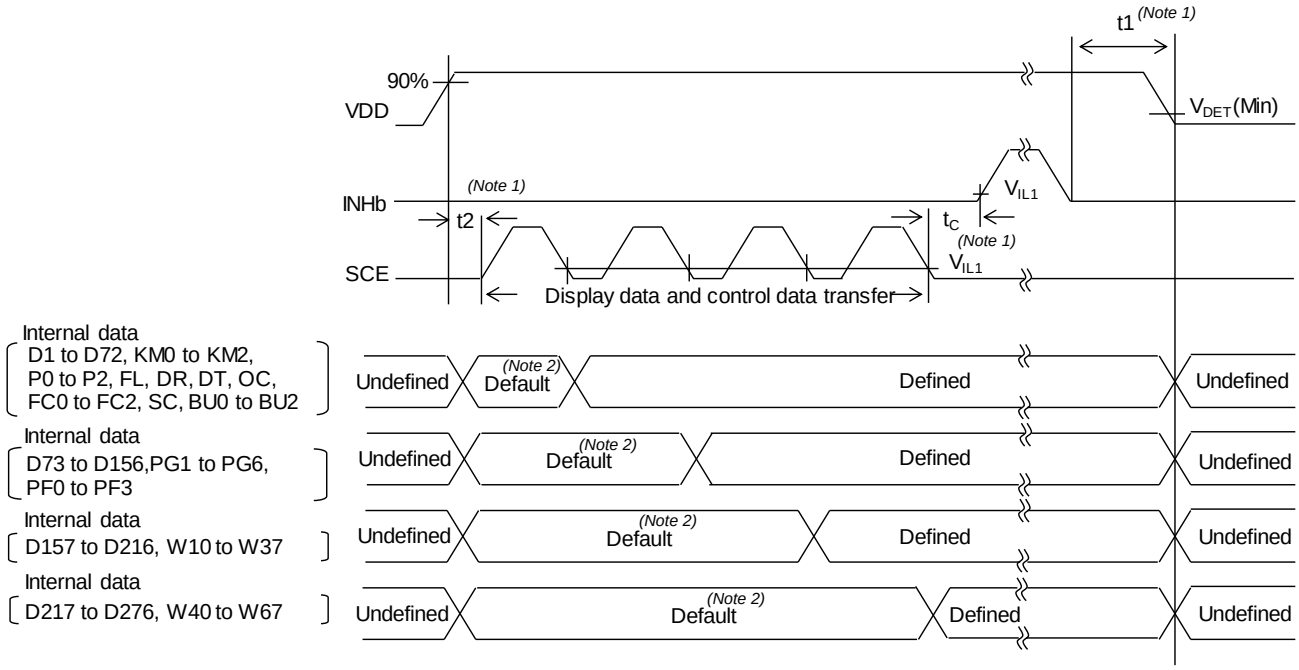


Figure 28. Power on/off and INHb Control Sequence (1/4 Duty)

(Note 1) t1≥0, t2≥0, t_C: 10µs (Min)
When VDD level is over 90%, there may be cases where command is not received correctly in unstable VDD.
(Note 2) Display data are undefined. Regarding default value, refer to Reset Condition.

2. 1/3 Duty

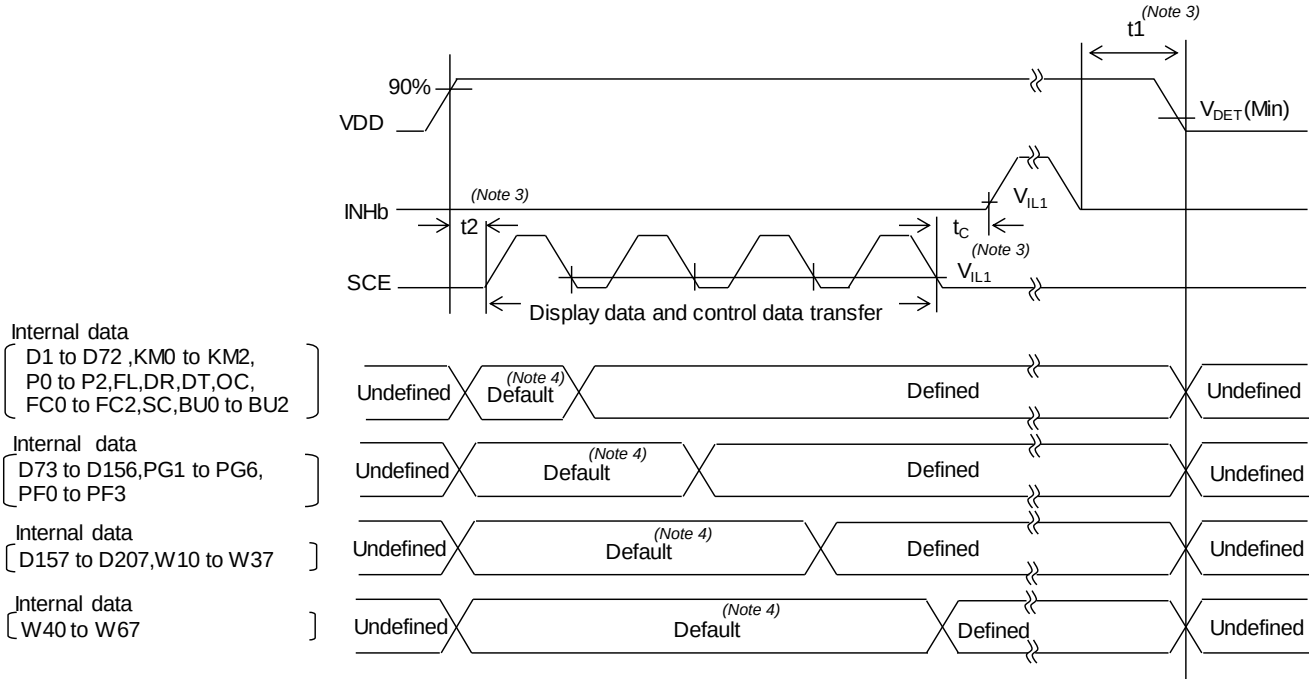


Figure 29. Power ON/OFF and INHb Control Sequence (1/3 Duty)

(Note 3) t1≥0, t2≥0, t_C: 10µs (Min)
When VDD level is over 90%, there may be cases where command is not received correctly in unstable VDD.
(Note 4) Display data are undefined. Regarding default value, refer to Reset Condition.

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Oscillation Stabilization Time

It must be noted that the oscillation of the internal oscillation circuit is unstable for a maximum of 100µs (oscillation stabilization time) after oscillation has started.

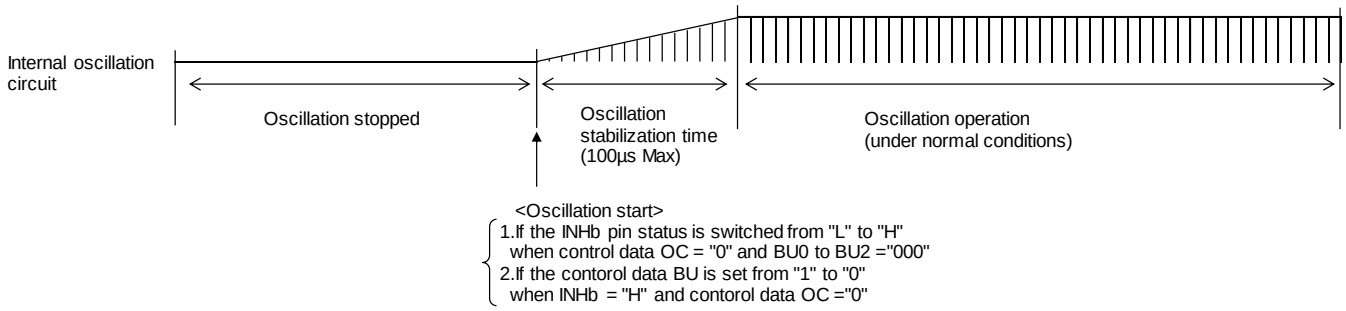


Figure 30. Oscillation Stabilization Time

Power-saving Mode Operation in External Clock Mode

After receiving [BU0,BU1,BU2]=[1,1,1], BU97520AKV-M enter to power saving mode synchronized with frame then Segment and Common pins output VSS level.

Therefore, in external clock mode, it is necessary to input the external clock based on each frame frequency setting after sending [BU0,BU1,BU2]=[1,1,1].
For the required number of clock, refer to "6. FC0, FC1 and FC2: Common / Segment output waveform frame frequency switching control data".

For example, please input the external clock as below.
[FC0,FC1,FC2]=[0,0,0]: In case of f_{OSC}/12288 setting, it needs over 12288clk,
[FC0,FC1,FC2]=[0,1,0]: In case of f_{OSC}/9216 setting, it needs over 9216clk,
[FC0,FC1,FC2]=[1,1,1]: In case of f_{OSC}/3072 setting, it needs over 3072clk

Please refer to the timing chart below.

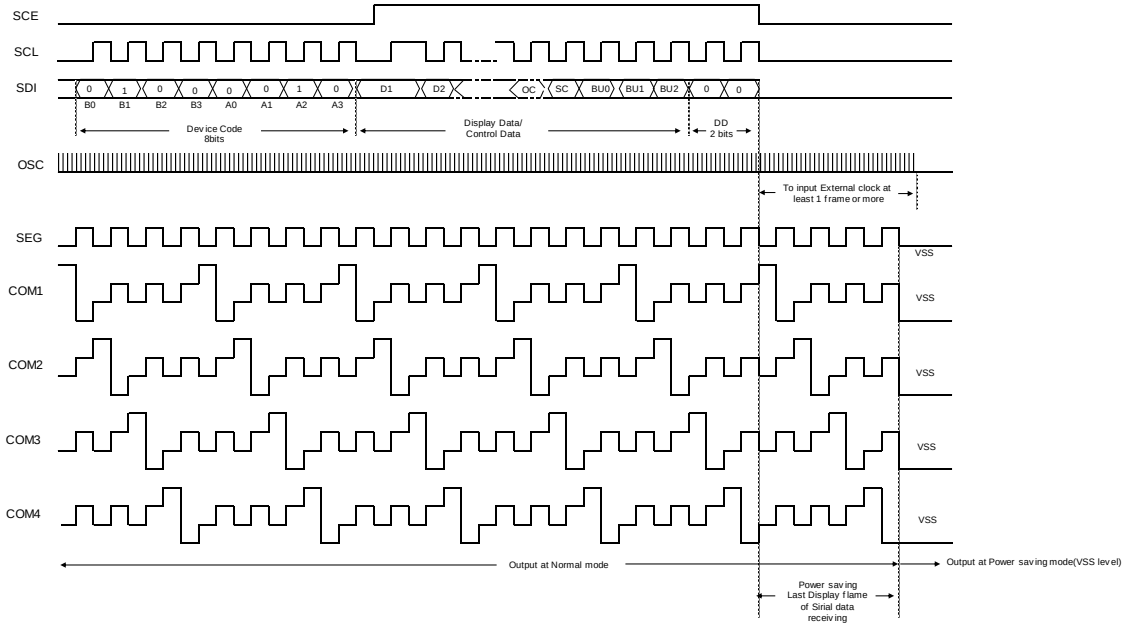


Figure 31. External Clock Stop Timing(1/4 Duty)

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Voltage Detection Type Reset Circuit (VDET)

The Voltage Detection Type Reset Circuit generates an output signal that resets the system when power is applied for the first time and when the power supply voltage drops (that is, for example, the power supply voltage is less than or equal to the power down detection voltage V_{DET} = 1.8V Typ.). To ensure that this reset function works properly, it is recommended that a capacitor be connected to the power supply line so that both the power supply voltage (VDD) rise time when power is first applied and the power supply voltage (VDD) fall time when the voltage drops are at least 1ms.

To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.

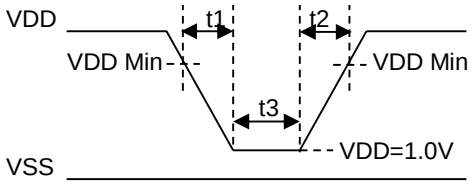


Figure 32. VDET Detection Timing

Power supply voltage VDD fall time: t1 > 1ms
Power supply voltage VDD rise time: t2 > 1ms
Internal reset power supply retain time: t3 > 1ms

When it is difficult to keep above conditions, it is possibility to cause meaningless display due to no IC initialization.
Please execute the IC initialization as quickly as possible after Power-on to reduce such an affect.
See the IC initialization flow as below.
But since commands are not received when the power is OFF, the IC initialization flow is not the same function as POR.

Set [BU0,BU1,BU2]=[1,1,1](power-saving mode) and SC=1(Display Off) as quickly as possible after Power-on.
BU97520AKV-M can receive commands in 0ns after Power-on(VDD level is 90%).
Please refer to the timing chart of "INHb Pin and Display Control".

Reset Condition

When BU97520AKV-M is initialized, the internal status after power supply has been reset as the following table.

Instruction	At Reset Condition
Key Scan Mode	[KM0,KM1,KM2]=[1,1,1]: Key scan no use
S1/P1/G1 to S6/P6/G6 Pin	[P0,P1,P2]=[0,0,0]:all segment output
LCD Bias	DR=0:1/3 Bias
LCD Duty	DT=0:1/4 Duty
Line / Frame Inversion Mode	FL=0:Line Inversion
Display Frame Frequency	[FC0,FC1,FC2]=[0,0,0]:f_{OSC}/12288
Display Clock Mode	OC=0:Internal oscillator
LCD Display	SC=1:OFF
Power Mode	[BU0,BU1,BU2] =[1,1,1]:Power saving mode
PWM/GPO Output	PGx=0:PWM output(x=1 to 6)
PWM Frequency	[PF0,PF1,PF2,PF3]=[0,0,0,0]: f_{OSC} /4096
PWM Duty	[Wn0 to Wn7]=[0,0,0,0,0,0,0,0] 1/256xTp(n=1 to 6,Tp=1/fp)

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

10. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

11. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

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Ordering Information

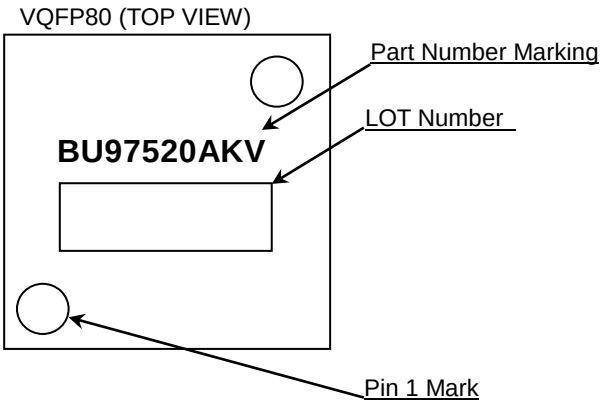
B U 9 7 5 2 0 A K V - M E 2

Part Number

Package
KV : VQFP80

Product Rank
M: for Automotive
Packaging Specification
E2: Embossed tape and reel
(VQFP80)

Marking Diagram

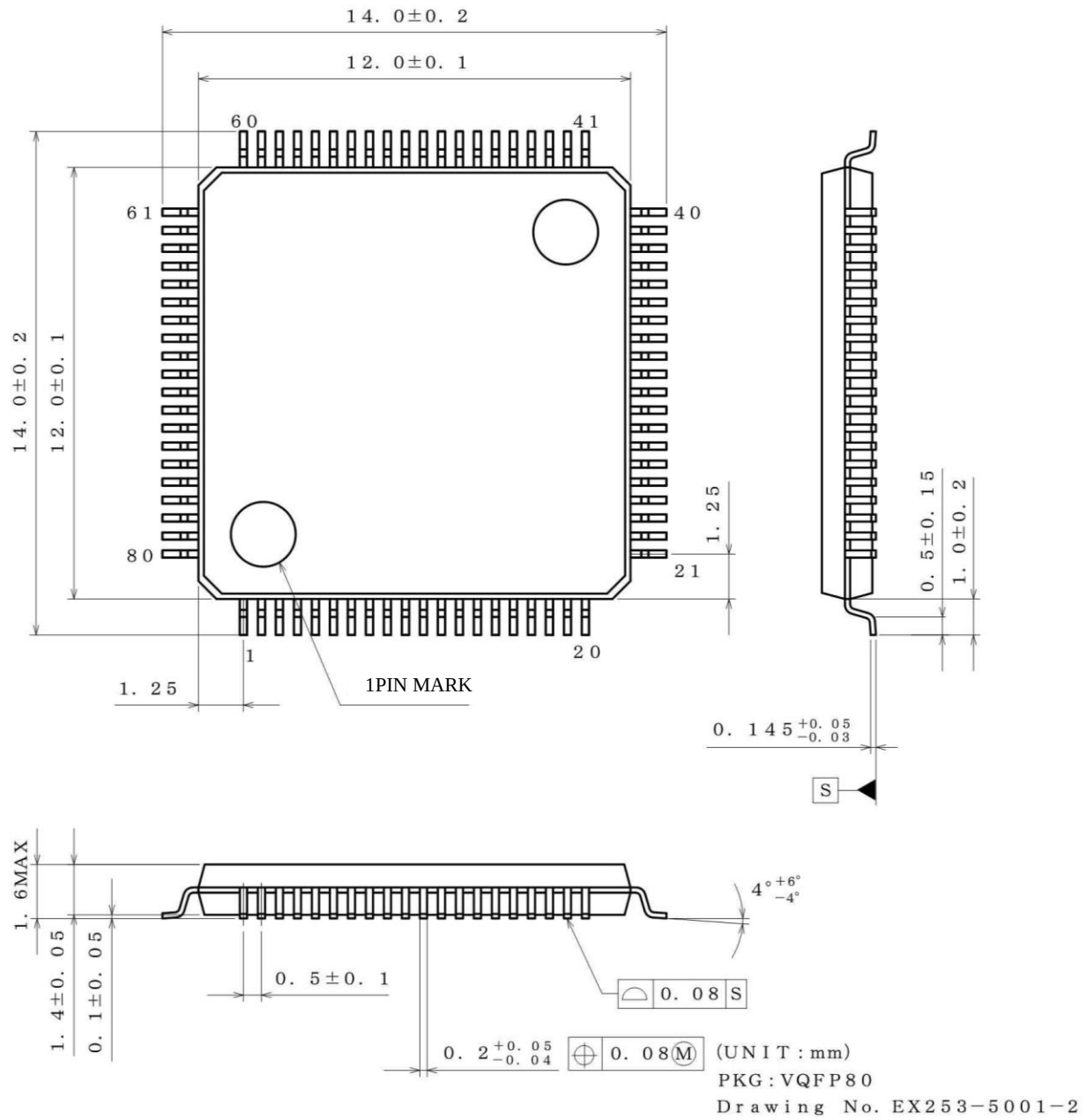


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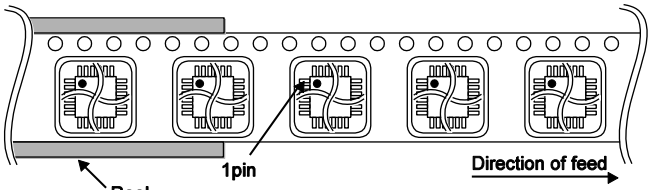
Physical Dimension, Tape and Reel Information

Package Name	VQFP80



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Version	Date	Description
001	14.Feb.2014	New Release
002	26.Feb.2014	Correction of erroneous descriptions in Figure 8 and Figure10.
003	24.Mar.2014	Change the condition of VIH1 and VIH2 in page 3
004	17.Apr.2014	Correction of erroneous descriptions in Figure 3. Correction of erroneous chapter number.
005	17.Feb.2015	Modify Note number. Add Note on AEC-Q100 Qualified in page 1. Add External Clock Duty Min limit in page 4. Modify Data Setup Time Min limit in page 4. Modify Data Hold Time Min limit in page 4. Modify SCE Wait Time Min limit in page 4. Modify SCE Setup Time Min limit in page 4. Modify SCE Hold Time Min limit in page 4. Modify High-level Clock Pulse Width Min limit in page 4. Modify Low-level Clock Pulse Width (Write) Min limit in page 4. Modify SDO Output Delay Time CL description in page 4. Modify SDO Rise Time CL description in page 4. Add Clock Cycle Time in page 4. Add Low-Level Clock Pulse Width (Read) in page 4. Add RPU and CL explanation in page 4. Add SDO signal, tccyc and tclwr on Figure5 Serial Interface Timing in page 5. Modify tclww from tclw on Figure5 Serial Interface Timing in page 5. Modify reference level of tchw to VIH1 from 50% on Figure5 Serial Interface Timing in page 5. Modify reference level of tclww t to VIL1 from 50% on Figure5 Serial Interface Timing in page 5. Delete tcp on Figure5 Serial Interface Timing(1.When SCL is stopped at the low level) in page 5. Delete tcs on Figure5 Serial Interface Timing(2.When SCL is stopped at the high level) in page 5. Add packing specification for tray in page 39 and page 40.
006	19.Mar.2015	Modify INHb Handling when unused of Pin Description in page 6.
007	27.Dec.2017	Page 3. Modify Temparature condition in Absolute Maximum Ratings.Ta=25˚C → Removed Page 3. Modify Maximum Supply Voltage in Absolute Maximum Ratings. -0.3 to +6.5 → -0.3 to +7.0. Page 3. Modify Input Voltage in Absolute Maximum Ratings. -0.3 to +6.5 → -0.3 to +7.0. Page 3. Add OSC in Absolute Maximum Ratings Input Voltage. Page 3. Add Caution2 in Absolute Maximum Ratings condition. (Moved from Operational Notes) Page.3. Add OSC pin in Electrical Characteristics table. Page 4. Add External Clock Rise Time and External Clock Fall Time in Oscillation Characteristics. Page 5. Add KI1/S62 to KI5/S66 in Pin Description I/O and Handling when unused Input terminal description. Page 5. Add OSC/S69 in Pin Description I/O and Handling when unused Input terminal description. Page 11 to 14. Add Reset condition in Control Data Functions. Page 11. Add 4. FL: Line Inversion or Frame Inversion control data explanation. Page 12. Add External Clock input timing function in 7. OC: Internal oscillator operating mode / External clock operating mode control data. Page 34. Modify Figure 28. Power on/off and INHb Control Sequence (1/4 Duty). Page 34. Modify Figure 29. Power on/off and INHb Control Sequence (1/3 Duty). Page 35. Add Power-saving mode operation in external clock mode. Page 36. Add Voltage Detection Type Reset Circuit (VDET) explanation. Correction of errors. Minor translation to have more conformity between Japanese and English version.
008	02.Aug.2019	Page.6 Add Pin Description Note Page.8,10,and 12 Add Description Page.34 Add INHb Pin and Display Control description

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Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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